



US 20190250467A1

(19) **United States**

(12) **Patent Application Publication**

KIM et al.

(10) **Pub. No.: US 2019/0250467 A1**

(43) **Pub. Date: Aug. 15, 2019**

(54) **LIQUID CRYSTAL DISPLAY AND MANUFACTURING METHOD THEREOF**

Publication Classification

(71) Applicant: **Samsung Display Co., Ltd.**, Yongin-si (KR)

(51) **Int. Cl.**
G02F 1/1337 (2006.01)

(72) Inventors: **Su Jeong KIM**, Seoul (KR); **Oh Jeong KWON**, Hwaseong-si (KR); **Ki Chul SHIN**, Seongnam-si (KR)

(52) **U.S. Cl.**
CPC .. *G02F 1/133753* (2013.01); *G02F 1/133788* (2013.01); *G02F 2001/133726* (2013.01); *G02F 2001/133773* (2013.01); *G02F 2001/133761* (2013.01)

(21) Appl. No.: **16/392,583**

(57) **ABSTRACT**

(22) Filed: **Apr. 23, 2019**

Related U.S. Application Data

(62) Division of application No. 14/303,843, filed on Jun. 13, 2014, now Pat. No. 10,317,734.

A liquid crystal display includes a thin film transistor panel including a first alignment layer, an opposing panel including a second alignment layer, and opposite to the thin film transistor panel, and a liquid crystal layer between the thin film transistor panel and the opposing panel, and including liquid crystal molecules, wherein a difference between a pretilt angle provided by the first alignment layer and a pretilt angle provided by the second alignment layer is equal to or greater than about 0.8 degree.

Foreign Application Priority Data

Jul. 24, 2013 (KR) 10-2013-0087491

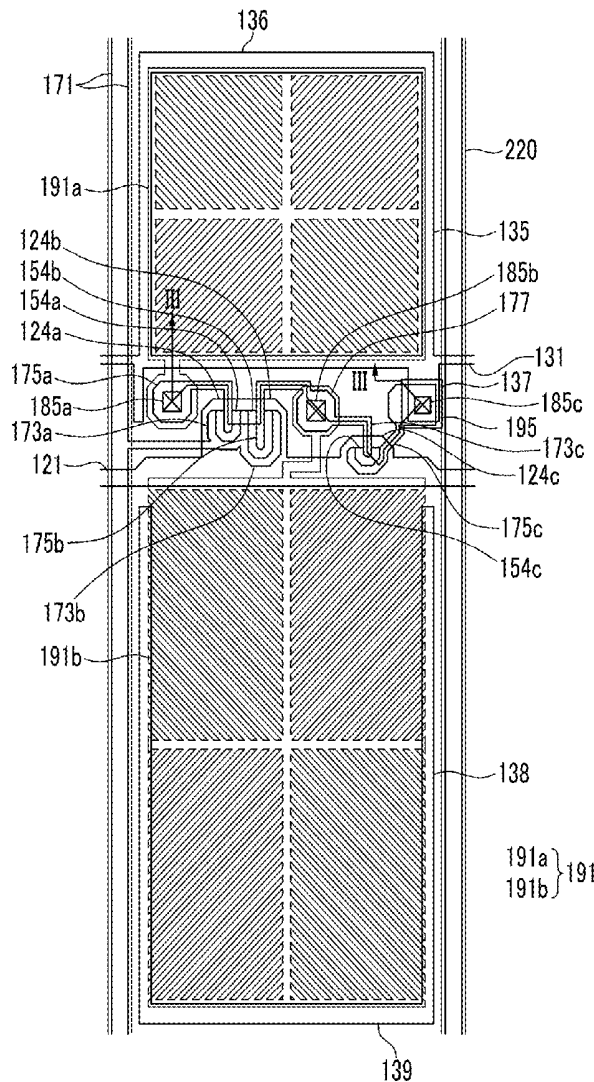


FIG. 1

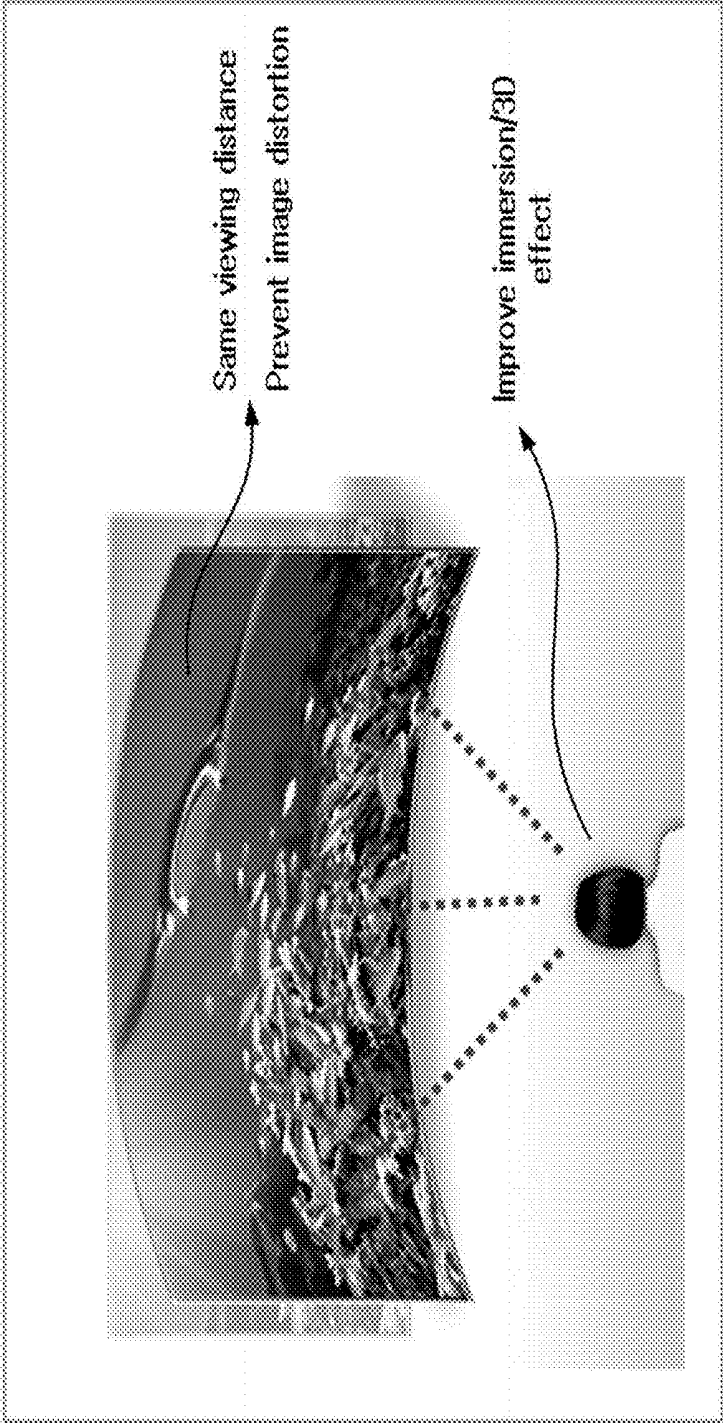


FIG.2

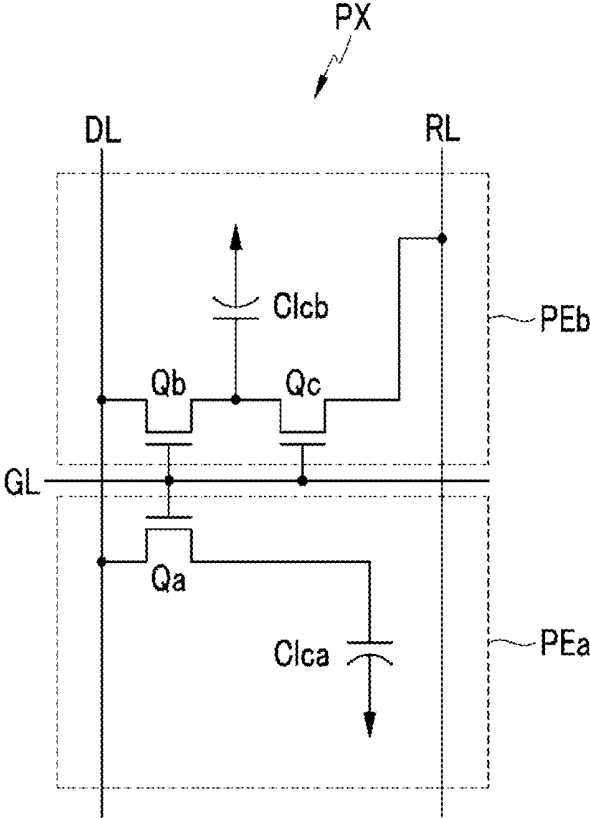


FIG.3

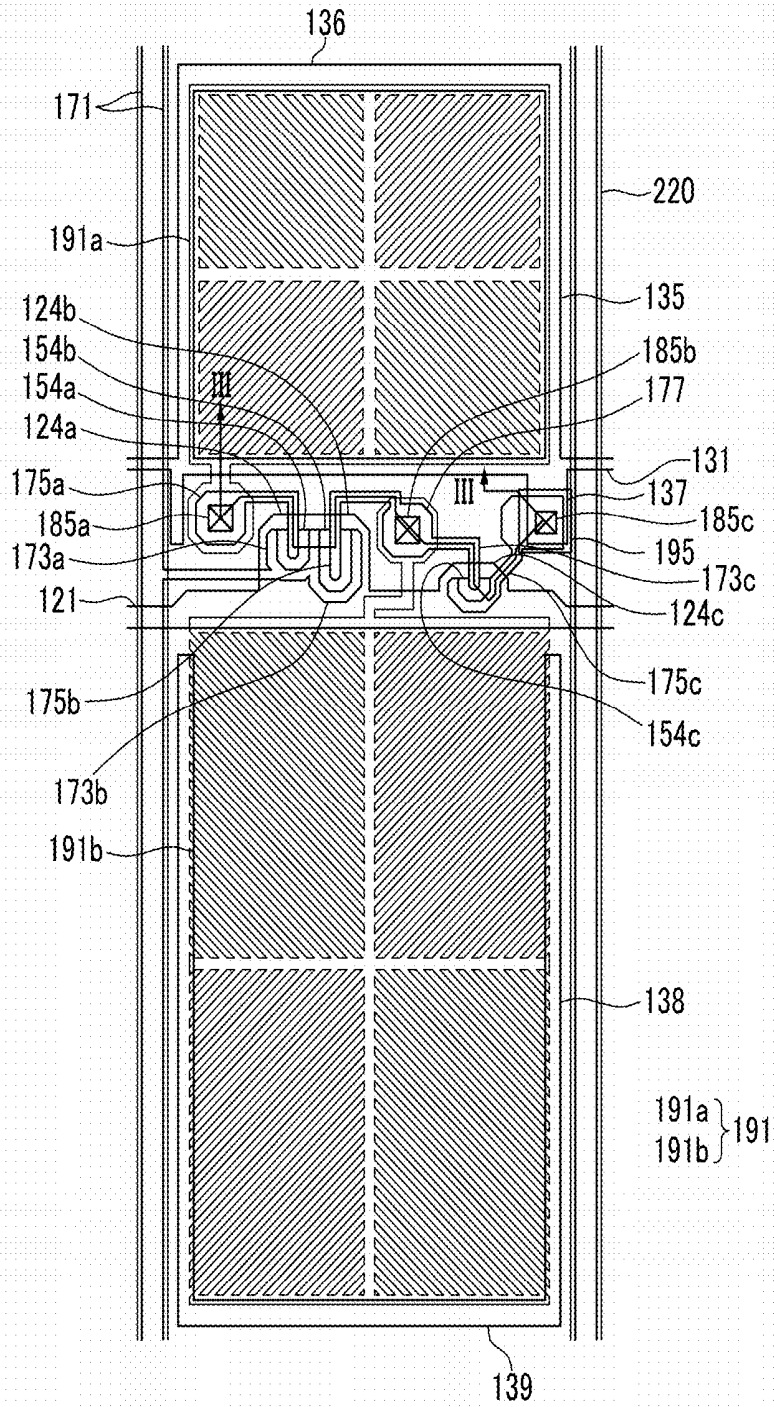


FIG. 4

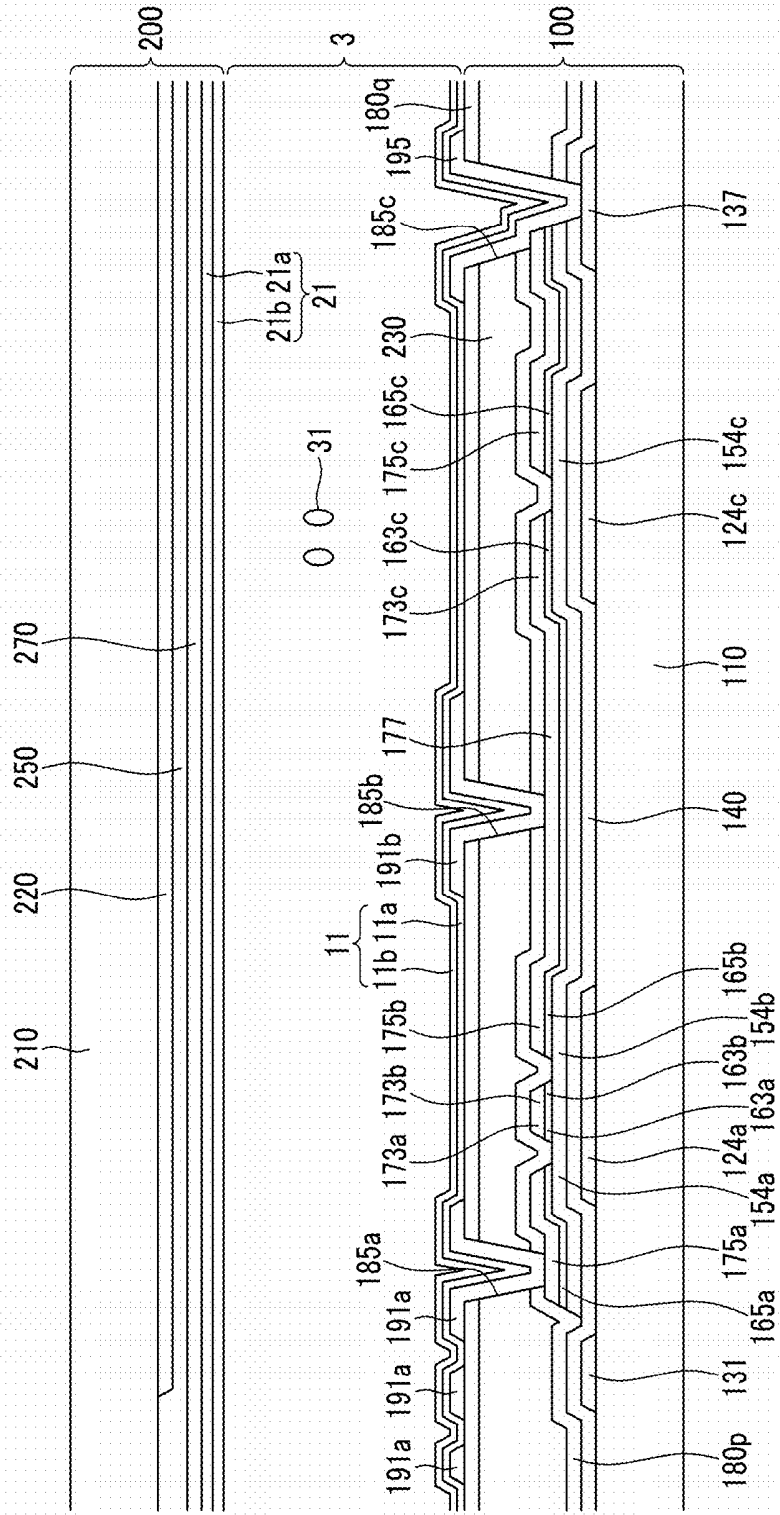


FIG.5

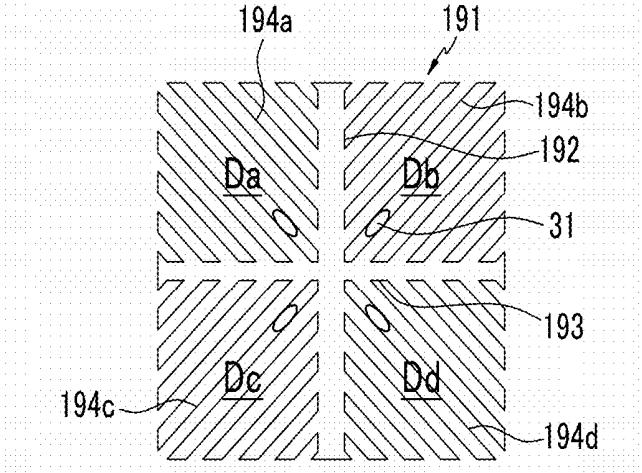


FIG.6

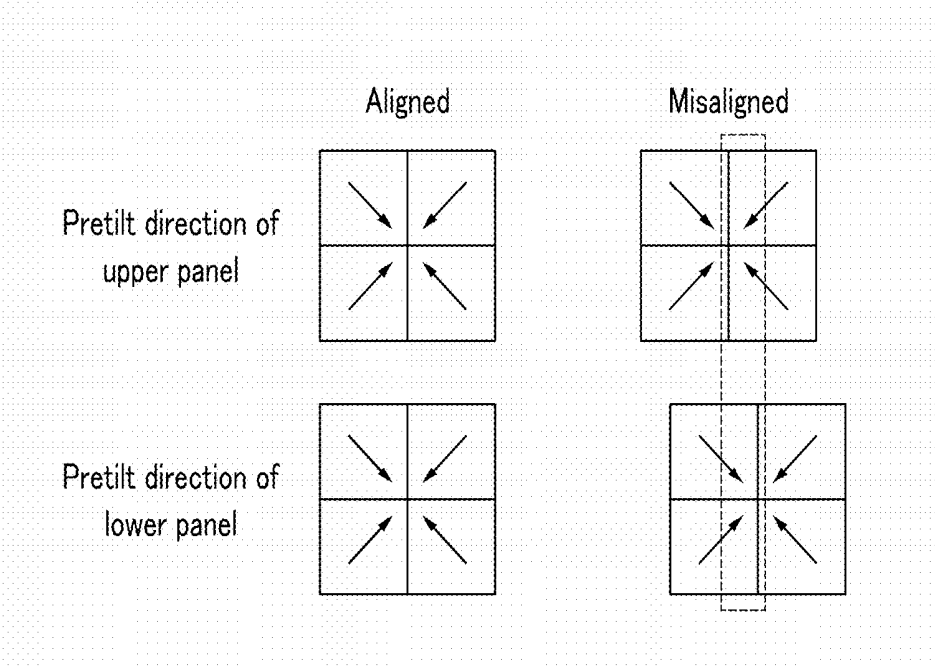


FIG.7

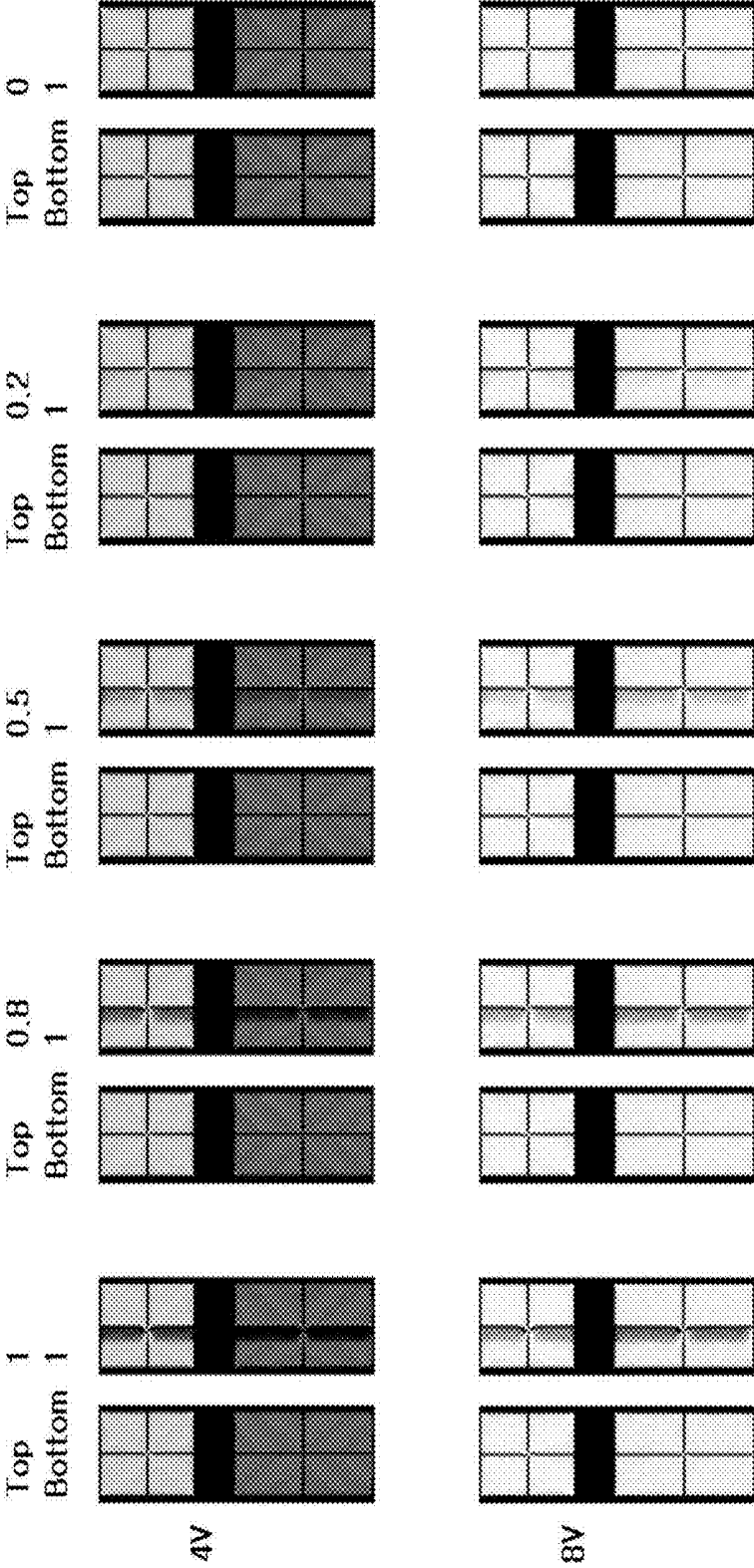


FIG.8

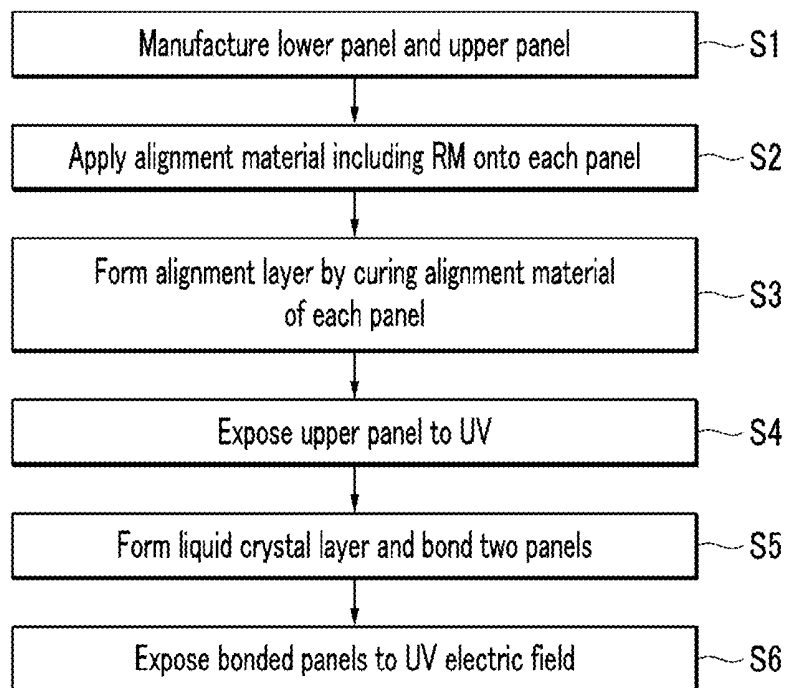


FIG.9

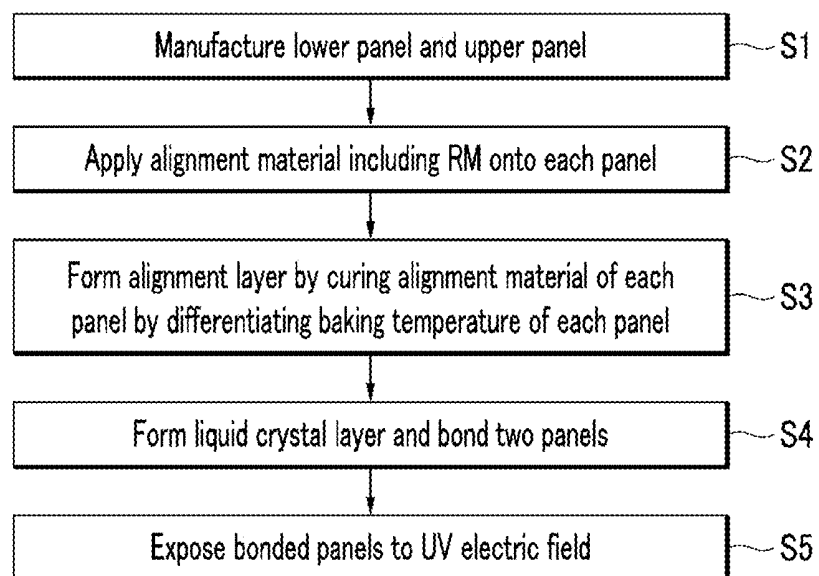
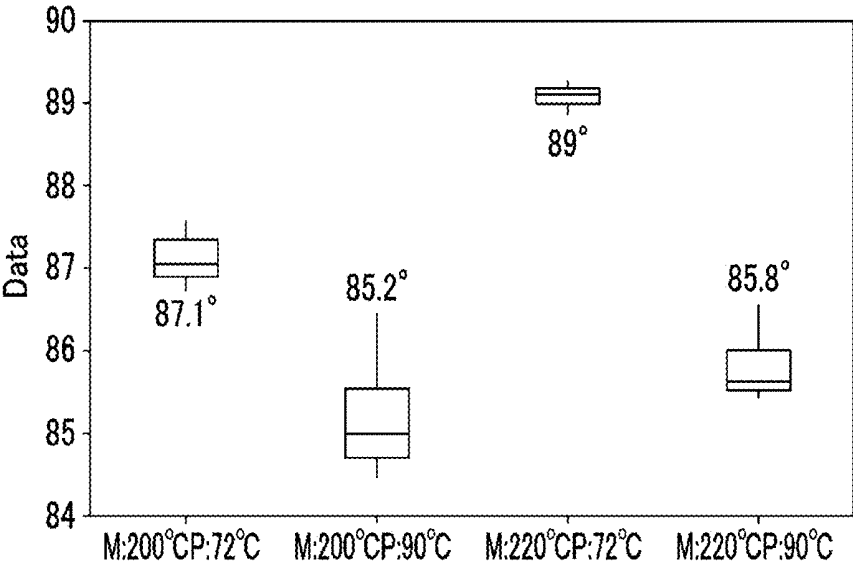


FIG. 10



LIQUID CRYSTAL DISPLAY AND MANUFACTURING METHOD THEREOF

[0001] This application is a divisional of U.S. patent application Ser. No. 14/303,843, filed on Jun. 13, 2014, which claims priority to Korean Patent Application No. 10-2013-0087491 filed on Jul. 24, 2013, and all the benefits accruing therefrom under 35 U.S.C. § 119, the entire contents of which are incorporated herein by reference.

BACKGROUND

(a) Field

[0002] The invention relates to a liquid crystal display and a manufacturing method thereof.

(b) Description of the Related Art

[0003] A liquid crystal display (“LCD”), which is one of the flat panel displays widely used presently, includes two panels on which electrodes are formed, and a liquid crystal layer interposed therebetween, generates an electric field by applying a voltage to the electrodes, rearranges liquid crystal molecules of the liquid crystal layer, and adjusts transmittance of light through the rearranged liquid crystal molecules to display an image.

[0004] The LCD uses an alignment layer in order to arrange the liquid crystal molecules of the liquid crystal layer in a desired direction. Further, in a case where the electric field is applied to the liquid crystal layer, in order to predetermine a direction of a movement of the liquid crystal molecules, the liquid crystal molecules are arranged to have a pretilt. In order to achieve the pretilt of the liquid crystal molecule, a method of mixing and photopolymerizing reactive mesogen in the liquid crystal layer is known.

[0005] Recently, a size of the LCD has been increased, and in order to improve immersion and realism for viewers, a curved display panel has been developed as illustrated in FIG. 1.

SUMMARY

[0006] Since a boundary of a display panel is fixed by a sealant, when the display panel is bent, buckling is generated at a center portion of a panel, and thus two panels of the display panel are misaligned. The misalignment of the panels causes a partial deviation in the directions of pretilts formed in the two panels in a plurality of same directions, so that a dark portion, such as texture, is generated in a pixel, thereby degrading a display quality.

[0007] The invention has been made in an effort to provide a liquid crystal display (“LCD”) having an excellent display quality, and a manufacturing method thereof.

[0008] Further, the invention has been made in an effort to provide an LCD effectively preventing a quality of an image from deteriorating due to a distortion of an alignment between the two panels in a curved display panel, and a manufacturing method thereof.

[0009] An exemplary embodiment of the invention provides a liquid crystal display including a thin film transistor (“TFT”) panel including a first alignment layer, an opposing panel including a second alignment layer, and opposite to the TFT panel, and a liquid crystal layer including liquid crystal molecules between the TFT panel and the opposing panel, in which a difference between a pretilt angle provided by the

first alignment layer and a pretilt angle provided by the second alignment layer is equal to or greater than about 0.8 degree.

[0010] In the invention, a pretilt may include a direction and an angle, and a pretilt direction may refer to an angle at which a long axis of a liquid crystal molecule projected on a substrate surface is inclined based on a gate line or a data line, and a pretilt angle may also refer to an angle at which the long axis of the liquid crystal molecule is inclined based on a line vertical to a horizontal surface of the substrate.

[0011] In an exemplary embodiment, the first alignment layer and the second alignment layer may include a same alignment material.

[0012] In an exemplary embodiment, the first alignment layer may include a first alignment adjusting layer and a first pretilt adjusting layer, and the second alignment layer may include a second alignment adjusting layer and a second pretilt adjusting layer, in which the first pretilt adjusting layer defines a thin film transistor panel-side pretilt angle of the liquid crystal molecules, and the second pretilt adjusting layer defines an opposing panel-side pretilt angle of the liquid crystal molecules.

[0013] In an exemplary embodiment, the opposing panel-side pretilt angle by the second pretilt adjusting layer may be smaller than the thin film transistor panel-side pretilt angle by the first pretilt adjusting layer.

[0014] In an exemplary embodiment, the first and second alignment adjusting layers may include a polymer including a vertical alignment material, and the first and second pretilt adjusting layers include polymers including reactive mesogen.

[0015] In an exemplary embodiment, the TFT panel may further include a pixel electrode including a plurality of fine branch portions, and the polymers including the reactive mesogen of the first and second pretilt adjusting layer may be arranged in a direction of the plurality of fine branch portions.

[0016] In an exemplary embodiment, the LCD may include a curved display panel including the TFT panel and the opposing panel.

[0017] Another exemplary embodiment of the invention provides a method of manufacturing a liquid crystal display including manufacturing a TFT panel and an opposing panel opposite to the TFT panel, applying an alignment material onto each of the thin film transistor panel and the opposing panel, forming alignment layers by curing the alignment material of each of the thin film transistor panel and the opposing panel, exposing only one of the thin film transistor panel and the opposing panel to ultraviolet rays (“UV”), forming a liquid crystal layer and bonding the thin film transistor panel and the opposing panel, and exposing the bonded panels to UV electric field.

[0018] In an exemplary embodiment, a difference between a pretilt angle provided by the alignment layer on the TFT panel and a pretilt angle provided by the alignment layer formed the opposing panel may be equal to or greater than about 0.8 degree.

[0019] In an exemplary embodiment, the applying an alignment material may include applying a same alignment material including reactive mesogen onto each of the TFT panel and the opposing panel.

[0020] In an exemplary embodiment, the opposing panel may be exposed to the UV.

[0021] In an exemplary embodiment, the alignment layers may include an alignment adjusting layer and a pretilt adjusting layer.

[0022] In an exemplary embodiment, the exposing only one of the two panels to UV may include exposing only one of the two panels to UV with an intensity of approximately 5 joules per square centimeter (J/cm^2) to approximately 30 J/cm^2 for about 20 minutes to about 1 hour.

[0023] In an exemplary embodiment, the method may include baking the TFT panel and the opposing panel at different temperatures, respectively, before the forming of the liquid crystal layer and the bonding of the two panels.

[0024] Another exemplary embodiment of the invention is to provide a method of manufacturing a liquid crystal display including manufacturing a TFT panel and an opposing panel opposite to the TFT panel, applying an alignment material onto each of the thin film transistor panel and an opposing panel, forming alignment layers by curing the alignment material of each of the thin film transistor panel and an opposing panel, in which the thin film transistor panel and an opposing panel are baked at different temperatures, respectively, forming a liquid crystal layer and bonding the thin film transistor panel and an opposing panel, and exposing the bonded panels to an UV electric field.

[0025] In an exemplary embodiment, a difference between a pretilt angle provided by the alignment layer on the TFT panel and a pretilt angle provided by the alignment layer formed the opposing panel may be equal to or greater than about 0.8 degree.

[0026] In an exemplary embodiment, the applying a alignment material may include applying a same alignment material including reactive mesogen onto each of the TFT panel and the opposing panel.

[0027] In an exemplary embodiment, the forming the alignment layers may include differentiating pre-curing temperatures and/or main-curing temperatures for the alignment materials of the respective panels.

[0028] In an exemplary embodiment, the alignment material applied onto the opposing panel may be subjected to pre-curing at a lower temperature than that of the alignment material applied onto the TFT panel. In this case, the former may be subjected to main-curing at a higher temperature than or the same temperature as that of the latter.

[0029] In an exemplary embodiment, the alignment material applied onto the opposing panel may be subjected to main-curing at a higher temperature than that of the alignment material applied onto the TFT panel. In this case, the former may be subjected to pre-curing at a lower temperature than or the same temperature as that of the latter.

[0030] In an exemplary embodiment, the alignment layers may include an alignment adjusting layer and a pretilt adjusting layer.

[0031] In an exemplary embodiment, the method may further include exposing only one of the two panels to UV before the forming of the liquid crystal layer and the bonding of the two panels.

[0032] According to the exemplary embodiments of the invention, even though an LCD is implemented with a curved LCD panel, it is possible to decrease or effectively prevent a dark portion, such as a texture, on a screen.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The above and other exemplary embodiments, advantages and features of this disclosure will become more apparent by describing in further detail exemplary embodiments thereof with reference to the accompanying drawings, in which:

[0034] FIG. 1 is a diagram illustrating an exemplary embodiment of a curved liquid crystal display (“LCD”) according to the invention.

[0035] FIG. 2 is an equivalent circuit diagram for the exemplary embodiment of one pixel of the LCD according to the invention.

[0036] FIG. 3 is a plan view for the exemplary embodiment of one pixel of the LCD according to the invention.

[0037] FIG. 4 is a cross-sectional view taken along line III-III of the LCD of FIG. 3.

[0038] FIG. 5 is a top plan view illustrating to the exemplary embodiment of a basic region of a pixel electrode of the LCD according to the invention.

[0039] FIG. 6 is a diagram illustrating an exemplary embodiment of a misalignment of a pretilt direction due to the misalignment between upper and lower panels generated in the curved display panel.

[0040] FIG. 7 is a diagram illustrating a display quality according to a difference between a lower panel-side pretilt angle and an upper panel-side pretilt angle as a simulation image.

[0041] FIG. 8 is a flowchart of the exemplary embodiment of a manufacturing method of the LCD according to the invention.

[0042] FIG. 9 is a flowchart of another exemplary embodiment of a manufacturing method of the LCD according to the invention.

[0043] FIG. 10 is a graph illustrating a pretilt angle varying according to a curing temperature of an alignment material.

DETAILED DESCRIPTION

[0044] The invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described exemplary embodiments may be modified in various different ways, all without departing from the spirit or scope of the invention.

[0045] In the drawings, the thickness of layers, films, panels, regions, etc., are exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being “on” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” another element, there are no intervening elements present.

[0046] It will be understood that, although the terms “first,” “second,” “third” etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, “a first element,” “component,” “region,” “layer” or “section” discussed below could be

termed a second element, component, region, layer or section without departing from the teachings herein.

[0047] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms, including “at least one,” unless the content clearly indicates otherwise. “Or” means “and/or.” As used herein, the term “and/or” includes any and all combinations of one or more of the associated listed items. It will be further understood that the terms “comprises” and/or “comprising,” or “includes” and/or “including” when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0048] Furthermore, relative terms, such as “lower” or “bottom” and “upper” or “top,” may be used herein to describe one element’s relationship to another element as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in one of the figures is turned over, elements described as being on the “lower” side of other elements would then be oriented on “upper” sides of the other elements. The exemplary term “lower,” can therefore, encompass both an orientation of “lower” and “upper,” depending on the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as “below” or “beneath” other elements would then be oriented “above” the other elements. The exemplary terms “below” or “beneath” can, therefore, encompass both an orientation of above and below.

[0049] “About” or “approximately” as used herein is inclusive of the stated value and means within an acceptable range of deviation for the particular value as determined by one of ordinary skill in the art, considering the measurement in question and the error associated with measurement of the particular quantity (i.e., the limitations of the measurement system). For example, “about” can mean within one or more standard deviations, or within $\pm 30\%$, 20% , 10% , 5% of the stated value.

[0050] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0051] Exemplary embodiments are described herein with reference to cross section illustrations that are schematic illustrations of idealized exemplary embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, exemplary embodiments described herein should not be construed as limited to the particular shapes of regions as illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features.

Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present claims.

[0052] Now, a liquid crystal display (“LCD”) according to an exemplary embodiment of the invention will be described in detail with reference to the accompanying drawings.

[0053] FIG. 2 is an equivalent circuit diagram for one pixel of an LCD according to an exemplary embodiment of the invention. A disposition of signal lines and pixels of the LCD according to the exemplary embodiment of the invention, and a driving method thereof will be described with reference to FIG. 2.

[0054] A pixel PX of the LCD may include a plurality of signal lines including a gate line GL transferring a gate signal, a data line DL transferring a data signal, and a voltage dividing reference voltage line RL transferring a voltage dividing reference voltage, first, second, and third switching elements Qa, Qb, and Qc connected to the signal lines, and first and second liquid crystal capacitors Clca and Clcb.

[0055] The first and second switching elements Qa and Qb are connected to the gate line GL and the data line DL, respectively, and the third switching element Qc is connected to an output terminal of the second switching element Qb and the voltage dividing reference voltage line RL. The first switching element Qa and the second switching element Qb are three terminal elements, such as a thin film transistor (“TFT”), and control terminals thereof are connected with the gate line GL, and input terminals thereof are connected with the data line DL. An output terminal of the first switching element Qa is connected to the first liquid crystal capacitor Clca, and an output terminal of the second switching element Qb is connected to input terminals of the second liquid crystal capacitor Clcb and the third switching element Qc. The third switching element Qc is also a three terminal element, such as a TFT, and a control terminal thereof is connected with the gate line GL, an input terminal thereof is connected with the second liquid crystal capacitor Clcb, and an output terminal thereof is connected with the voltage dividing reference voltage line RL.

[0056] When a gate-on signal is applied to the gate line GL, the first switching element Qa, the second switching element Qb and the third switching element Qc connected to the gate line GL are turned on. As a result, a data voltage applied to the data line is applied to a first subpixel electrode PEa and a second subpixel electrode PEb through the turned-on first switching element Qa and second switching element Qb. Since the data voltages applied to the first subpixel electrode PEa and the second subpixel electrode PEb are the same as each other, the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb are charged with the same voltage value as a difference value between a common voltage and the data voltage, but simultaneously, the voltage charged in the second liquid crystal capacitor Clcb is divided through the turned-on third switching element Qc. Accordingly, the voltage charged in the second liquid crystal capacitor Clcb is decreased by a difference between the common voltage and the voltage dividing reference voltage.

[0057] The voltage charged in the first liquid crystal capacitor Clca and the voltage charged in the second liquid crystal capacitor Clcb are changed, so that inclined angles of liquid crystal molecules in the first subpixel and the second

subpixels are different, and thus luminance between the two subpixels is different. When the voltage of the first liquid crystal capacitor Clca and the voltage of the second liquid crystal capacitor Clcb are appropriately adjusted, an image viewed from a side can be maximally close to an image viewed from a front side, thereby improves side visibility.

[0058] In the illustrated exemplary embodiment, the pixel PX includes the second liquid crystal capacitor Clcb and the third switching element Qc connected to the voltage dividing reference voltage line RL in order to make the voltage charged in the first liquid crystal capacitor Clca and the voltage charged in the second liquid crystal capacitor Clcb be different from each other, but may be differently configured depending on an exemplary embodiment. In an exemplary embodiment, the second liquid crystal capacitor Clcb may be connected to a step-down capacitor, for example. Particularly, the pixel PX may include the third switching element Qc including a first terminal connected to a step-down gate line, a second terminal connected to the second liquid crystal capacitor Clcb, and a third terminal connected to the step-down capacitor, so that some of an amount of charges charged in the second liquid crystal capacitor Clcb is charged in the step-down capacitor and thus the charged voltages of the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb may be differently set from each other. In another exemplary embodiment, the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb may be connected to different data lines, so as to receive different data voltages, respectively, so that the charged voltages of the first liquid crystal capacitor Clca and the second liquid crystal capacitor Clcb may be differently set from each other.

[0059] A structure of the LCD according to the exemplary embodiment illustrated in FIG. 2 will be described with reference to FIGS. 3 to 5. FIG. 3 is a plan view illustrating an exemplary embodiment of one pixel of the LCD according to the exemplary embodiment of the invention, and FIG. 4 is a cross-sectional view taken along line III-III of the LCD of FIG. 3. FIG. 5 is a top plan view illustrating a basic region of a pixel electrode of the LCD according to the exemplary embodiment of the invention.

[0060] First, referring to FIGS. 3 and 4, the LCD according to the exemplary embodiment includes a lower panel 100 and an upper panel 200 facing each other, a liquid crystal layer 3 interposed between the lower and upper panels 100 and 200, and a pair of polarizers (not illustrated) attached to external surfaces of the lower and upper panels 100 and 200.

[0061] First, the lower panel 100 will be described.

[0062] A gate conductor including a gate line 121 and a voltage dividing reference voltage line 131 is disposed on an insulation substrate 110 including transparent glass or plastic. The gate line 121 includes a first gate electrode 124a, a second gate electrode 124b, a third gate electrode 124c and a wide end portion (not illustrated) for connecting with another layer or an external driving circuit. The voltage dividing reference voltage line 131 includes first storage electrodes 135 and 136 and a reference electrode 137. Further, second storage electrodes 138 and 139, which are not connected with the voltage dividing reference voltage line 131 but overlap the second subpixel electrode 191b, are also provided.

[0063] A gate insulation layer 140 is disposed on the gate line 121 and the voltage dividing reference voltage line 131,

and a first semiconductor 154a, a second semiconductor 154b and a third semiconductor 154c are disposed on the gate insulation layer 140. A plurality of ohmic contacts 163a, 165a, 163b, 165b, 163c, and 165c is disposed on the semiconductors 154a, 154b and 154c.

[0064] A data conductor including a plurality of data lines 171 including a first source electrode 173a and a second source electrode 173b, a first drain electrode 175a, a second drain electrode 175b, a third source electrode 173c and a third drain electrode 175c is disposed on the ohmic contacts 163a, 165a, 163b, 165b, 163c and 165c and the gate insulation layer 140. The data conductor and the semiconductors and the ohmic contacts disposed under the data conductor may be simultaneously provided by using one mask. The data line 171 includes a wide end portion (not illustrated) for connecting with another layer or an external driving circuit.

[0065] The first gate electrode 124a, the first source electrode 173a, and the first drain electrode 175a provide the first TFT Qa together with a first semiconductor 154a, and a channel of the TFT is disposed on the semiconductor 154a between the first source electrode 173a and the first drain electrode 175a. Similarly, the second gate electrode 124b, the second source electrode 173b and the second drain electrode 175b provide the second TFT Qb together with a second semiconductor 154b, and a channel thereof is disposed on the semiconductor 154b between the second source electrode 173b and the second drain electrode 175b. The third gate electrode 124c, the third source electrode 173c and the third drain electrode 175c provide the third TFT Qc together with a third semiconductor 154c, and a channel is disposed on the semiconductor 154c between the third source electrode 173c and the third drain electrode 175c. The second drain electrode 175b is connected with the third source electrode 173c, and includes a widely expanded portion 177.

[0066] A first passivation layer 180p is disposed on the data conductors 171, 173c, 175a, 175b, and 175c, and exposed portions of the semiconductors 154a, 154b, and 154c. In an exemplary embodiment, the first passivation layer 180p may include an inorganic insulation layer, such as silicon nitride or silicon oxide. The first passivation layer 180p may effectively prevent a pigment of a color filter 230 from flowing in the exposed portions of the semiconductors 154a, 154b and 154c.

[0067] The color filter 230 is disposed on the first passivation layer 180p. The color filter 230 is extended in a vertical direction along adjacent two data lines.

[0068] A second passivation layer 180q is disposed on the color filter 230. In an exemplary embodiment, the second passivation layer 180q may include an inorganic insulation layer, such as silicon nitride or silicon oxide. The second passivation layer 180q effectively prevents the color filter 230 from being lifted up and suppresses a contamination of the liquid crystal layer 3 due to an organic material, such as a solvent, flowing in from the color filter 230, thereby effectively preventing a defect, such as an afterimage, which may be caused during the driving of a screen.

[0069] The first passivation layer 180p and the second passivation layer 180q are provided with a first contact hole 185a and a second contact hole 185b, through which the first drain electrode 175a and the second drain electrode 175b are exposed. The first passivation layer 180p, the second passivation layer 180q, and the gate insulation layer 140 are

provided with a third contact hole **185c**, through which a part of the reference electrode **137** and a part of the third drain electrode **175c** are exposed, and a connection member **195** covers the third contact hole **185c**. The connecting member **195** electrically connects the reference electrode **137** and the third drain electrode **175c** exposed through the third contact hole **185c**.

[0070] A plurality of pixel electrodes **191** is disposed on the second passivation layer **180q**. The respective pixel electrodes **191** are separated from each other with the gate line **121** interposed therebetween, and include first subpixel electrode **191a** and second subpixel electrode **191b** adjacent in a column direction based on the gate line **121**. In exemplary embodiments, the pixel electrode **191** may include a transparent conductive material, such as indium tin oxide (“ITO”) and indium zinc oxide (“IZO”), or may include a reflective metal, such as aluminum, silver, chromium, and an alloy thereof.

[0071] Each of the first subpixel electrode **191a** and the second subpixel electrode **191b** include one or more basic electrodes illustrated in FIG. **5** or modifications of the basic electrode.

[0072] The first subpixel electrode **191a** and the second subpixel electrode **191b** are physically and electrically connected with the first drain electrode **175a** and the second drain electrode **175b** through the first contact hole **185a** and the second contact hole **185b**, respectively, and receives the data voltage from the first drain electrode **175a** and the second drain electrode **175b**. Some of the data voltage applied to the second drain electrode **175b** is divided through the third source electrode **173c**, so that a magnitude of the voltage applied to the first subpixel electrode **191a** is larger than a magnitude of the voltage applied to the second subpixel electrode **191b**.

[0073] The first subpixel electrode **191a** and the second subpixel electrode **191b**, to which the data voltage is applied, generate an electric field together with a common electrode **270** of the upper panel **200** to be described below so as to determine a direction of the liquid crystal molecule of the liquid crystal layer **3** between the two electrodes **191** and **270**. Luminance of light passing through the liquid crystal layer **3** is changed according to the determined direction of the liquid crystal molecule as described above.

[0074] A lower alignment layer **11** is disposed on the pixel electrode **191**. The lower alignment layer **11** includes an alignment adjusting layer **11a** and a pretilt adjusting layer **11b**.

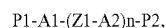
[0075] The alignment adjusting layer **11a** includes a polymer including a vertical alignment material. In an exemplary embodiment, the alignment adjusting layer **11a** may be a polymer including a dianhydride-based monomer, such as an alicyclic dianhydride-based monomer, for example, a diamine-based monomer, such as an aromatic diamine-based monomer and an aliphatic ring substituted aromatic diamine-based monomer, for example, and an aromatic epoxide-based monomer that is a crosslinker. In an exemplary embodiment, the alignment adjusting layer **11a** may include at least one of polymer-based materials, such as polyamide, polyamic acid, polysiloxane, nylon, polyvinyl-alcohol (“PVA”), and polyvinyl chloride (“PVC”), for example.

[0076] The pretilt adjusting layer **11b** includes a polymer in which the vertical alignment material and a monomer including reactive mesogen (“RM”) are chemically bonded

to each other. In exemplary embodiments, the polymer included in the pretilt adjusting layer **11b** may include a dianhydride-based monomer, such as an alicyclic dianhydride-based monomer, for example, and a diamine-based monomer, such as a photoactive diamine-based monomer, an alkylated aromatic diamine-based monomer and an aromatic diamine-based monomer, for example.

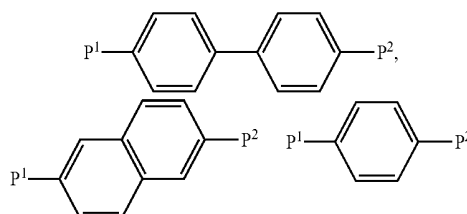
[0077] The photoactive diamine-based monomer of the polymer is a monomer including reactive mesogen, and serves to determine a direction of the pretilt of the pretilt adjusting layer **11b** of the lower alignment layer **11**. In an exemplary embodiment, the polymer of the alignment adjusting layer **11** and the polymer including the RM of the pretilt adjusting layer **11b** may be chemically bonded to each other.

[0078] The RM is a material which is photo-cured by light such as ultraviolet rays (“UV”), for example, to limit the pretilt to one direction. In an exemplary embodiment, the RM may be a compound expressed by a formula below.



[0079] where P1 and P2 are independently selected from acrylate, methacrylate, vinyl, vinyloxy and epoxy groups, A1 and A2 are independently selected from 1,4-phenylene and naphthalene-2,6-diyl groups, Z1 is one of COO—, OCO— and a single bond, and n is one of 0, 1 and 2.

[0080] In further detail, a compound expressed as one of the next equations can be exemplified.



[0081] Here, P1 and P2 are independently selected from acrylate, methacrylate, vinyl, vinyloxy, or epoxy groups, for example.

[0082] Now, the upper panel **200** will be described.

[0083] A light blocking member **220** is disposed on an insulation substrate **210**. The light blocking member **220** is also referred to as a black matrix, and effectively prevents a leakage of light. A plurality of openings (not illustrated) facing the pixel electrodes **191** is defined in the light blocking member **220** having almost the same shape as that of the pixel electrode **191**. The light blocking member **220** effectively prevents a leakage of light between the pixel electrodes **191**. The light blocking member **220** may include a portion corresponding to the gate line **121** and the data line **171**, and a portion corresponding to the TFT. Depending on an exemplary embodiment, the light blocking member **220** may be disposed only on the lower panel **100**, or may be disposed on both the upper and lower panels **100** and **200**.

[0084] An overcoat **250** is disposed on the light blocking member. The overcoat **250** may include an organic insulating material, and provides a flat surface. Depending on an exemplary embodiment, the overcoat **250** may be omitted.

[0085] The common electrode **270** is disposed on the overcoat **250**. The common electrode **270** may include a transparent conductor, such as ITO and IZO.

[0086] An upper alignment layer **21** is disposed on the common electrode **270**. Similar to the lower alignment layer **11**, the upper alignment layer **21** includes an alignment adjusting layer **21a** and a pretilt adjusting layer **21b**. Detailed configurations of the alignment adjusting layer **21a** and the pretilt adjusting layer **21** and a relationship therebetween may be the same as those described in the lower alignment layer **11**. The upper alignment layer **21** may include the same material as that of the lower alignment layer **11**. In a case where the upper and lower alignment layers **21** and **11** include different materials each other, many problems, such as an afterimage, for example, may be caused. However, even though the upper alignment layer **21** and the lower alignment layer **11** include the same material, the angles of the pretilts provided by the alignment adjusting layer **21a** of the upper alignment layer **21** and the alignment adjusting layer **11a** of the lower alignment layer **11** may be different from each other.

[0087] The liquid crystal layer **3** includes a plurality of liquid crystal molecules **31**, and the liquid crystal molecule **31** are aligned to be vertical to the surfaces of the two substrates **110** and **210** in a state where a voltage is not applied to the two electric field generating electrodes **191** and **270**, and are aligned to have a pretilt inclined in the same direction as a longitudinal direction of a cutout pattern of the pixel electrode **191**. The liquid crystal molecules **31** may be vertically aligned by the vertical alignment materials within the lower alignment layer **11** and the upper alignment layer **21**, and the pretilts of the liquid crystal molecules **31** may be adjusted by the pretilt adjusting layer **11b** of the lower alignment layer **11** and the pretilt adjusting layer **21b** of the upper alignment layer **21**.

[0088] The pretilt angles of the liquid crystal molecules **31** may be divided into a lower panel-side pretilt angle by the pretilt adjusting layer **11b** of the lower alignment layer **11**, and an upper panel-side pretilt angle by the pretilt adjusting layer **21b** of the upper alignment layer **21**, and the lower panel-side pretilt angle and the upper panel-side pretilt angle are different from each other. In an exemplary embodiment, the difference in the angle may be approximately 0.8 degrees or more, and the upper panel-side pretilt angle may be smaller than the lower panel-side pretilt angle.

[0089] A basic electrode of the pixel electrode **191** will be described with reference to FIG. 5.

[0090] As shown in FIG. 5, an entire shape of the basic electrode is a quadrangle, and includes a cross-shaped stem portion including a horizontal stem portion **193** and a vertical stem portion **192** orthogonal to the horizontal stem portion **193**. Further, the basic electrode is divided into a first sub region Da, a second sub region Db, a third sub region Dc and a fourth sub region Dd by the horizontal stem portion **193** and the vertical stem portion **192**, and the first to fourth sub regions Da, Db, Dc, and Dd include a plurality of first fine branch portions **194a**, a plurality of second fine branch portions **194b**, a plurality of third fine branch portions **194c** and a plurality of fourth fine branch portions **194d**, respectively.

[0091] The first fine branch portion **194a** is obliquely extended in a left upper direction from the horizontal stem portion **193** or the vertical stem portion **192**, and the second fine branch portion **194b** is obliquely extended in a right upper direction from the horizontal stem portion **193** or the vertical stem portion **192**. The third fine branch portion **194c** is obliquely extended in a left lower direction from the

horizontal stem portion **193** or the vertical stem portion **192**, and the fourth fine branch portion **194d** is obliquely extended in a right lower direction from the horizontal stem portion **193** or the vertical stem portion **192**.

[0092] The first to fourth fine branch portions **194a**, **194b**, **194c**, and **194d** form approximately 45 degrees or 135 degrees with respect to the gate lines **121a** and **121b** or the horizontal stem portion **193**. Further, the fine branch portions **194a**, **194b**, **194c**, and **194d** of adjacent two sub regions of the first to fourth sub regions Da, Db, Dc, and Dd may be orthogonal to each other.

[0093] Widths of the fine branch portions **194a**, **194b**, **194c**, and **194d** may be about 2.5 micrometers (μm) to about 5.0 μm , and an interval between the fine branch portions **194a**, **194b**, **194c**, and **194d** adjacent within one sub region Da, Db, Dc, or Dd may be about 2.5 μm to about 5.0 μm . The widths and the intervals may be taken in a direction substantially perpendicular to a direction in which the branch portion extends (e.g., longitudinal direction).

[0094] According to the exemplary embodiment of the invention, the widths of the fine branch portions **194a**, **194b**, **194c** and **194d** may increase as being close to the horizontal stem portion **193** or the vertical stem portion **192**, and a difference between a portion having the largest width and a portion having the smallest width in one fine branch portion **194a**, **194b**, **194c**, or **194d** may be about 0.2 μm to about 1.5 μm .

[0095] The first subpixel electrode **191a** and the second subpixel electrode **191b** are connected with the first drain electrode **175a** or the second drain electrode **175b** through the first contact hole **185a** and the second contact hole **185b**, and receives a data voltage from the first drain electrode **175a** and the second drain electrode **175b**. In this case, sides of the first to fourth fine branch portions **194a**, **194b**, **194c**, and **194d** distort the electric field to create horizontal components determining a direction of the inclination of the liquid crystal molecules **31**. The horizontal components of the electric field are almost horizontal to the sides of the first to fourth fine branch portions **194a**, **194b**, **194c**, and **194d**. Accordingly, as illustrated in FIG. 5, the liquid crystal molecules **31** are inclined in a direction parallel to the longitudinal direction of the fine branch portions **194a**, **194b**, **194c**, and **194d**. The pixel electrode **191** includes the four sub regions Da to Dd in which the longitudinal directions of the fine branch portions **194a**, **194b**, **194c**, and **194d** are different from each other, so that the directions, in which the liquid crystal molecules **31** are inclined, are approximately four directions, and four domains in which the alignment directions of the liquid crystal molecules **31** are different from each other are disposed on the liquid crystal layer **3**. As described above, when varying the directions in which the liquid crystal molecules are inclined, a reference viewing angle of the LCD is increased.

[0096] Now, deterioration in display quality generable in the curved LCD will be described with reference to FIG. 6. FIG. 6 is a diagram illustrating an exemplary embodiment of a misalignment of a pretilt direction due to the misalignment between the upper and lower panels generated in the curved display panel.

[0097] Referring to FIGS. 4 and 5 together, the liquid crystal molecule **31** of the liquid crystal layer **3** are aligned to have a pretilt inclined in the same direction as the longitudinal direction of a cutout pattern of the pixel electrode **191** in a state where an electric field is not applied, and

for the pretilt of the liquid crystal molecules **31**, the pretilt adjusting layers **11b** and **21b** disposed on the alignment layers **11** and **21** of the lower and upper panels **100** and **200** have the pretilt inclined in the same direction as the cutout pattern of the pixel electrode **191**.

[0098] The pretilts of the pretilt adjusting layers **11b** and **21b** are provided in the same direction at a position at which the lower panel **100** and the upper panel **200** face each other, which may be expressed with an alignment state illustrated in a left drawing of FIG. 6. However, when the display panel is bent in order to provide the curved display panel, the alignment between the lower panel and the upper panel is distorted, and as a result, like a portion indicated with a dotted-line quadrangle of a right drawing of FIG. 6, there occurs a region in which the direction of the pretilt of the pretilt adjusting layer **11b** of the lower panel **100** is misaligned with the direction of the pretilt of the pretilt adjusting layer **21b** of the upper panel **200**. A problem in the direction in which the liquid crystal molecules **31** are inclined is generated in the region, so that a texture is generated in the screen. According to the invention, in a case where the pretilt angle by the lower pretilt adjusting layer **11b** and the pretilt angle by the upper pretilt adjusting layer **21b** are differently provided from each other, it is possible to decrease or effectively prevent a generation of the texture generated on the screen.

[0099] FIG. 7 is a diagram illustrating a display quality according to a difference between the lower panel-side pretilt angle and the upper panel-side pretilt angle as a simulation image.

[0100] In FIG. 7, a voltage of 4 V is applied to five pairs of pixels positioned in an upper line, and a voltage of 8 V is applied to five pairs of pixels positioned in a lower line. In one pair of pixels in each line, a left side is a state in which an upper panel-side pretilt direction and a lower panel-side pretilt direction are aligned, and a right side is a state in which the upper panel-side pretilt direction and the lower panel-side pretilt direction are misaligned by 30 μm . A display state was simulated while gradually decreasing the upper panel-side pretilt angle from 1 degree to 0 degree in a state where the lower panel-side pretilt angle is fixed at 1 degree.

[0101] It can be seen that in both the upper and lower lines, as the upper panel-side pretilt angle is decreased, the generation of the texture is gradually weak, and when the pretilt angle is 0.2 degree, the texture is rarely generated, and when the pretilt angle is 0 degree, the texture completely disappears. A result of the simulation in the curved display panel for transmittance and luminance variation is represented in Table 1 below.

TABLE 1

Pretilt (degree)		Transmittance Simulation (a.u.)		Luminance	
Lower panel	Upper panel	Delta	30 μm Aligned	30 μm Misaligned	variation (%)
1.0	0	1.0	0.17072	0.17072	0.0
	0.2	0.8	0.17191	0.16988	-1.2
	0.5	0.5	0.17339	0.16651	-4.0
	0.8	0.2	0.17459	0.1625	-6.9
	1	0.0	0.17527	0.15955	-9.0

[0102] Referring to Table 1, the delta represents a difference between the upper panel-side pretilt angle and the

lower panel-side pretilt angle, and the transmittance simulation is measured in absorbance unit (a.u.). As represented in Table 1, when the lower panel and the upper panel are misaligned under a condition that both the lower panel-side pretilt angle and the upper panel-side pretilt angle are 1 degree, luminance is approximately decreased by 9 percent (%). When a difference between the pretilt angles is 0.8 degree or more, even though the alignment is distorted, luminance deviation is decreased to a level under approximately 1.2%, and when a difference between the pretilt angles is approximately 1 degree, the luminance deviation is 0.

[0103] Now, exemplary embodiments in which the alignment layer is provided so as to have a difference between the lower panel-side pretilt angle and the upper panel-side pretilt angle will be described with reference to FIGS. 8 to 10.

[0104] FIG. 8 is a flowchart of a manufacturing method of the LCD according to the exemplary embodiment of the invention.

[0105] As illustrated in FIG. 8, first, a lower panel and an upper panel are manufactured (S1). Here, the manufacturing of the lower panel means manufacturing a TFT panel, except for a lower alignment layer. In an exemplary embodiment, the lower panel is manufactured by providing the gate conductor, the data conductor, the TFT, the color filter, the pixel electrode, and the like, which are disposed on the insulating substrate as described with reference to FIGS. 2 to 5. The manufacturing of the upper panel means manufacturing an opposing panel, except for an upper alignment layer, as an opposing panel of the TFT panel. In an exemplary embodiment, the upper panel is provided by providing a light blocking member, a common electrode, and the like on the insulating substrate. Depending on an exemplary embodiment, the light blocking member may be disposed only on the lower panel, or may be disposed on both the upper and lower panels.

[0106] Next, an alignment material including RM is applied onto the lower panel and the upper panel manufactured as described above (S2). The application of the alignment material may be performed by a method, such as inkjet printing and roll printing. In an exemplary embodiment, the alignment material applied onto the lower panel and the upper panel may be the same as each other. In an exemplary embodiment, the alignment layer is the same as that of the description given in relation to the alignment layer.

[0107] Next, an alignment layer including an alignment adjusting layer and a pretilt adjusting layer is provided by curing the alignment material applied onto each panel (S3). The curing of the alignment material may include pre-curing at a low temperature and main-curing at a high temperature.

[0108] The pre-curing is to heat the alignment material at, for example, approximately 70 degrees Celsius ($^{\circ}\text{C}$.) to approximately 100 $^{\circ}\text{C}$., and a solvent of the alignment material is evaporated, and a combination within the alignment material is phase-separated by the pre-curing. The phase-separation is generated by a difference in a polarity of components within the alignment material, and a material having a relatively large polarity moves to a surrounding area of the electrode, and a material having a relatively small polarity moves above the surrounding area.

[0109] The main-curing is heating the alignment material at, for example, approximately 200 $^{\circ}\text{C}$. to approximately 250 $^{\circ}\text{C}$., and stacks the alignment layer, in which a material having a relatively large polarity, for example, a polymer

layer providing the alignment adjusting layer, is disposed at a lower side, and a material having a relatively small polarity, for example, a polymer layer providing the pretilt adjusting layer, is disposed at an upper side. As described above, the polymer providing the pretilt adjusting layer is a polymer in which a monomer including RM is bonded to another monomer.

[0110] Next, only the upper panel is exposed to UV (S4). Accordingly, a part or the entirety of RM of the alignment layer disposed on the upper panel is photo-cured in a state where the pretilt is not provided. Accordingly, in the alignment layer of the upper panel, the amount of reactive mesogen, which is not photo-cured, arranged in the same direction as those of the liquid crystal molecules to form the pretilt during the exposure to a UV electric field later is decreased. The UV exposure may be continued for about 20 minutes to about 1 hour with an intensity of approximately 5 joules per square centimeter (J/cm^2) to approximately 30 J/cm^2 , but is not limited thereto. Depending on an exemplary embodiment of the invention, the UV exposure may be performed only on the lower panel, not the upper panel.

[0111] Next, a liquid crystal layer is provided and the two panels are bonded to each other (S5). The forming of the liquid crystal layer may be performed before or after the bonding of the two panels. That is, liquid crystals are dropped onto any one panel by a method, such as inkjet printing, and then the other panel may be bonded to the one panel, and the two panels are bonded to each other and then liquid crystal may be injected through an injection opening between the two panels.

[0112] Next, the bonded panels are exposed to an ultraviolet ray electric field (S6). Here, as well known to those skilled in the art, the exposure to the UV electric field means changing an alignment so that the liquid crystal molecules have pretilts in a desired direction and angle by applying an electric field to the liquid crystal, and irradiating UV in a state where compounds including RM are arranged in the same direction as those of the liquid crystal molecules. When the UV are irradiated onto the compounds including RM arranged in the same direction as those of the liquid crystal molecules, RM is photo-cured. Accordingly, the compounds including RM of the pretilt adjusting layer is cured in a state of being arranged in the same direction as those of the liquid crystal molecules in a surrounding area.

[0113] However, the upper panel is already exposed to the UV in an operation S4, so that at least some of the RM of the upper panel is photo-cured. Accordingly, even though the panels are bonded and then are exposed to the UV electric field, the reactive mesogen, which is arranged in the same direction as those of the liquid crystal molecules to be photo-cured, may be less than that of the lower panel or may rarely exist. Accordingly, the pretilt by the pretilt adjusting layer of the upper panel is smaller than the pretilt by the pretilt adjusting layer of the lower panel, so that a difference between the pretilt angles of the upper panel and the lower panel may be created.

[0114] FIG. 9 is a flowchart of a manufacturing method of the LCD according to another exemplary embodiment of the invention, and FIG. 10 is a graph illustrating a pretilt angle varying according to a curing temperature of an alignment material.

[0115] The exemplary embodiment of FIG. 9 is similar to the exemplary embodiment of FIG. 8, but is different from the exemplary embodiment of FIG. 8 in terms of an opera-

tion of forming the alignment layer by curing the alignment material, and does not include an operation of exposing only the upper panel to UV.

[0116] Particularly, first, a lower panel and an upper panel are manufactured (S1), and then an alignment material including RM is applied onto the lower panel and the upper panel (S2).

[0117] Next, an alignment layer including an alignment adjusting layer and a pretilt adjusting layer is provided by curing the alignment material applied onto each panel by differentiating a baking temperature of each panel (S3). In the applied alignment material, the amount of remaining RM which may be involved in forming the pretilt during the exposure to an UV electric field later, is changed according to the baking temperature for curing the alignment material. Accordingly, liquid crystal molecules of the liquid crystal layer disposed between the panels baked at the different temperature conditions may be arranged to have different panel-side pretilt angles. A difference in the backing temperature of each panel may mean a difference in a pre-curing temperature and/or a difference in a main-curing temperature for the alignment material of each panel.

[0118] Although it is not theoretically limited, in a case where the pre-curing temperature is relatively high, the RM may be better phase-separated, and in a case where the main-curing temperature is relatively high, RM may be decomposed by thermal reaction. The former case means an increase in the amount of RM involved in the pretilt, and the latter case means an opposite case.

[0119] The graph of FIG. 10 represents the pretilt angle of the liquid crystal molecules in a case where the alignment layer is provided while varying the pre-curing temperature and the main-curing temperature, and then the exposure to the UV electric field is performed on the alignment layer under the same condition. In the graph, a horizontal axis represents curing temperatures (M: main-curing temperature, P: pre-curing temperature), and a vertical axis represents a pretilt angle (however, herein, values marked on the vertical axis are angles inclined based on a horizontal surface of the substrate, accordingly, the pre-tilt angle is represented by subtracting the angle indicated in the graph from 90 degrees, i.e., 90° minus the angle indicated in the graph). In the graph, boxes and vertical lines connected to a top line and a bottom line of each of the boxes represent quartiles. The bottom line, a middle line, and the top line of each of the boxes indicate first, second, and third quartiles of data set, respectively. The values above or below the boxes indicate the second quartile, which is the median of the data. End points of the vertical lines connected to the top line and the bottom line of each of the boxes indicate the highest and lowest values of the data set, respectively.

[0120] It can be seen that in a case where the pre-curing temperature is relatively higher, and the main-curing temperature is relatively lower (e.g., a second data from a left side of the horizontal axis), the pretilt angle is larger. Even though the alignment material is subjected to the pre-curing at the same temperature, in a case where the main-curing temperature is lower, the pretilt angle is larger. Similarly, even though the alignment material is subjected to the main-curing at the same temperature, in a case where the pre-curing temperature is higher, the pretilt angle is larger. As described above, the alignment layer is provided by

differentiating the baking temperature of each panel, so that each panel-side pretilt angle of the liquid crystal molecules may be differently set later.

[0121] Next, a liquid crystal layer is provided and the two panels are bonded to each other (S4). The liquid crystal layer may be provided by dropping liquid crystals before the bonding of the panels or injecting liquid crystals after the bonding of the panels.

[0122] Next, the bonded panels are exposed to an UV electric field (S5), and RM is photo-cured in a state where compounds including the RM of the alignment layer are arranged in the same direction as those of the liquid crystal molecules. As described above, since the amount of reactive mesogen, which is photo-curable in the direction in which the liquid crystal molecules are arranged by the exposure to the UV electric field in the alignment layer of each panel may be different due to a difference in the baking temperature, a lower panel-side pretilt angle and an upper panel-side pretilt angle may be differently provided from each other.

[0123] The exemplary embodiment of FIG. 8 and the exemplary embodiment of FIG. 9 may be combined and performed. In an exemplary embodiment, after the alignment layer is provided by differentiating the backing temperature of each panel, UV may be irradiated to only one panel before the bonding of the two panels (or before the forming of the liquid crystal layer depending on a case).

[0124] While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A method of manufacturing a liquid crystal display, the method comprising:

manufacturing a thin film transistor panel, and an opposing panel opposite to the thin film transistor panel;

applying an alignment material onto each of the thin film transistor panel and the opposing panel;

forming alignment layers by curing the alignment material of each of the thin film transistor panel and the opposing panel;

exposing only one of the thin film transistor panel and the opposing panel to ultraviolet rays;

forming a liquid crystal layer and bonding the thin film transistor panel and the opposing panel; and

exposing the bonded panels to an ultraviolet ray electric field.

2. The method of claim 1, wherein:

a difference between a pretilt angle provided by the alignment layer on the thin film transistor panel and a pretilt angle provided by the alignment layer on the opposing panel is equal to or greater than about 0.8 degree.

3. The method of claim 2, wherein:

the applying the alignment material includes applying a same alignment material including reactive mesogen onto each of the thin film transistor panel and the opposing panel.

4. The method of claim 3, wherein:

the opposing panel is exposed to the ultraviolet rays.

5. The method of claim 3, wherein:

the alignment layers include an alignment adjusting layer and a pretilt adjusting layer.

6. The method of claim 3, wherein:

the exposing only one of the thin film transistor panel and the opposing panel to ultraviolet rays includes exposing only one of the thin film transistor panel and the opposing panel to ultraviolet rays with an intensity of approximately 5 joules per square centimeter to approximately 30 joules per square centimeter for about 20 minutes to about 1 hour.

7. The method of claim 3, further comprising:

baking the thin film transistor panel and the opposing panel at different temperatures, respectively, before the forming the liquid crystal layer and the bonding of the thin film transistor panel and the opposing panel.

8. A method of manufacturing a liquid crystal display, the method comprising:

manufacturing a thin film transistor panel, and an opposing panel opposite to the thin film transistor panel;

applying an alignment material onto each of the thin film transistor panel and the opposing panel;

forming alignment layers by curing the alignment material of each of the thin film transistor panel and the opposing panel, in which the thin film transistor panel and the opposing panel are baked at different temperatures, respectively;

forming a liquid crystal layer and bonding the thin film transistor panel and the opposing panel; and

exposing the bonded panels to an ultraviolet ray electric field.

9. The method of claim 8, wherein:

a difference between a pretilt angle provided by the alignment layer on the thin film transistor panel and a pretilt angle provided by the alignment layer on the opposing panel is equal to or greater than about 0.8 degree.

10. The method of claim 9, wherein:

the applying the alignment material includes applying a same alignment material including reactive mesogen onto each of the thin film transistor panel and the opposing panel.

11. The method of claim 10, wherein:

the forming the alignment layers includes differentiating pre-curing temperatures for the alignment materials of the thin film transistor panel and the opposing panel, respectively.

12. The method of claim 10, wherein:

the forming the alignment layers includes differentiating main-curing temperatures for the alignment materials of the thin film transistor panel and the opposing panel, respectively.

13. The method of claim 10, wherein:

the forming the alignment layers includes differentiating pre-curing temperatures and main-curing temperatures for the alignment materials of the thin film transistor panel and the opposing panel, respectively.

14. The method of claim 10, wherein:

the alignment material applied onto the opposing panel is subjected to pre-curing at a lower temperature than that of the alignment material applied onto the thin film transistor panel.

15. The method of claim 10, wherein:
the alignment material applied onto the opposing panel is
subjected to main-curing at a higher temperature than
that of the alignment material applied onto the thin film
transistor panel.

16. The method of claim 8, wherein:
the alignment layers include an alignment adjusting layer
and a pretilt adjusting layer.

17. The method of claim 8, further comprising:
exposing only one panel among the thin film transistor
and opposing panels to ultraviolet rays before the
forming the liquid crystal layer and the bonding the thin
film transistor panel and an opposing panel.

* * * * *

专利名称(译)	液晶显示器及其制造方法		
公开(公告)号	US20190250467A1	公开(公告)日	2019-08-15
申请号	US16/392583	申请日	2019-04-23
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO. , LTD.		
[标]发明人	KIM SU JEONG KWON OH JEONG SHIN KI CHUL		
发明人	KIM, SU JEONG KWON, OH JEONG SHIN, KI CHUL		
IPC分类号	G02F1/1337		
CPC分类号	G02F1/133753 G02F1/133788 G02F2001/133761 G02F2001/133773 G02F2001/133726 G02F1/1333 G02F1/133711 G02F1/133723		
优先权	1020130087491 2013-07-24 KR		
外部链接	Espacenet USPTO		

摘要(译)

液晶显示器包括：薄膜晶体管面板，包括第一取向层；相对面板，包括第二取向层，与薄膜晶体管面板相对；以及液晶层，位于薄膜晶体管面板和相对面板之间，包括液晶分子，其中由第一取向层提供的预倾角与由第二取向层提供的预倾角之间的差值等于或大于约0.8度。

