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METHOD OF MANUFACTURING THE SAME****Publication Classification**(71) Applicant: **MITSUBISHI ELECTRIC
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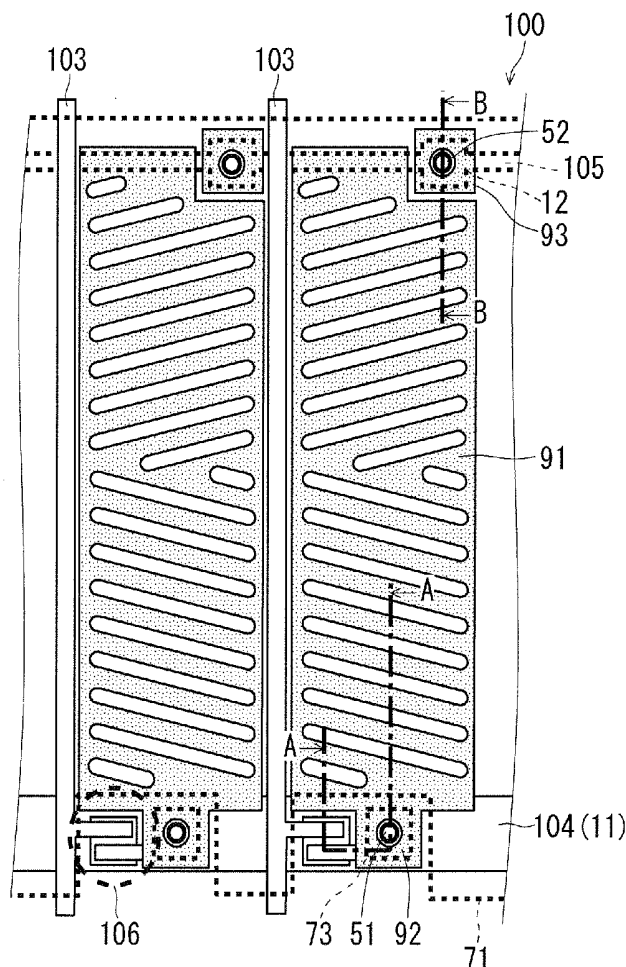
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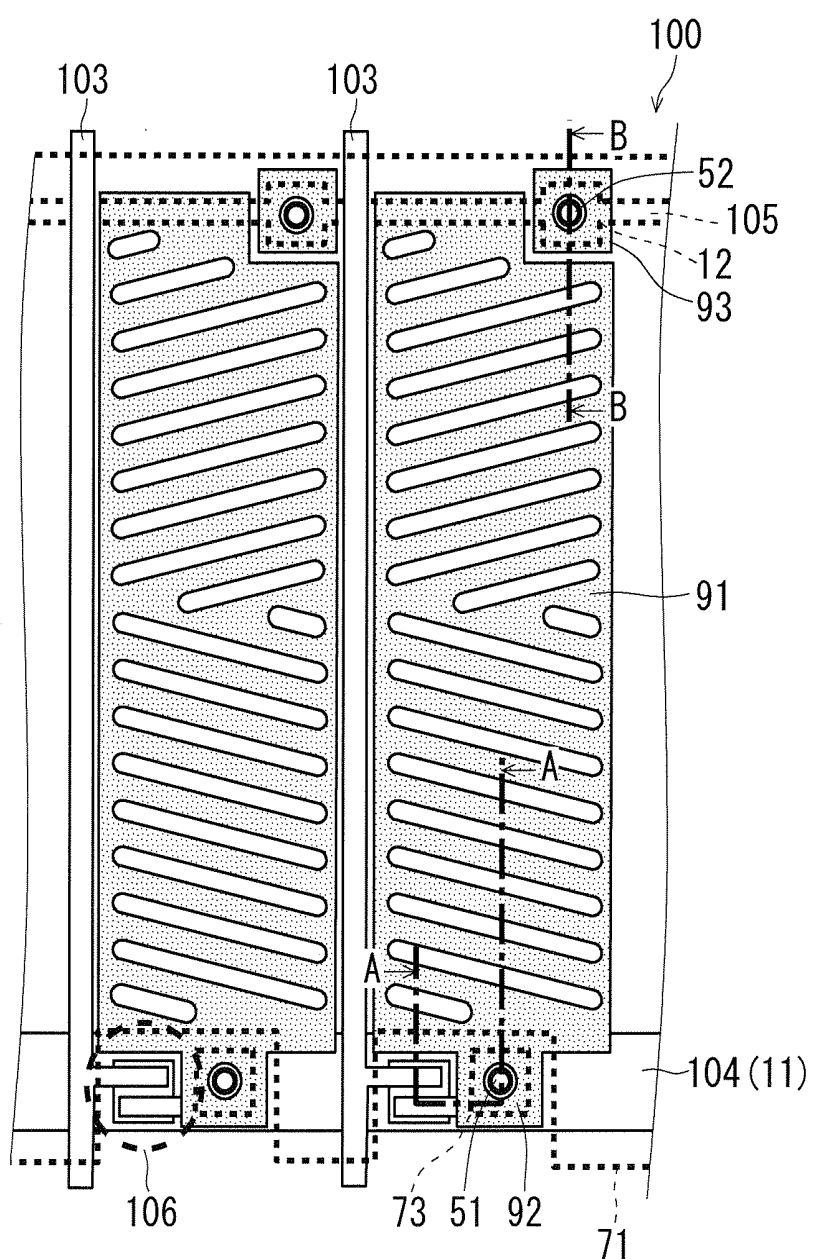
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ABSTRACT

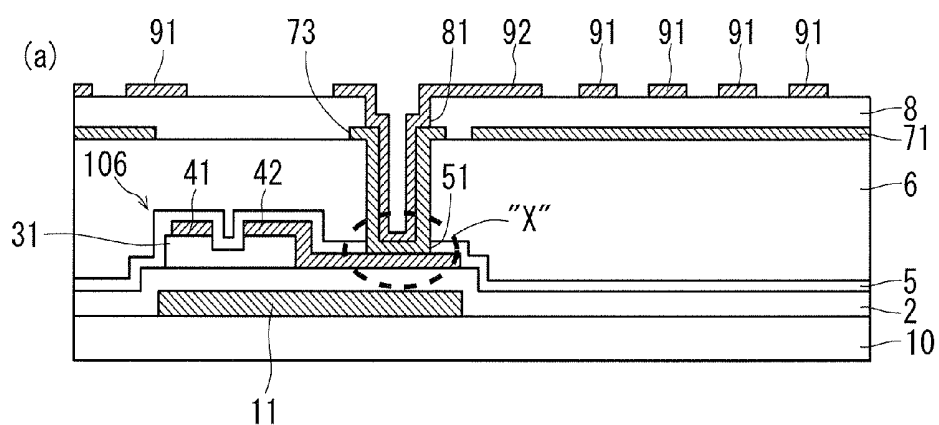
A liquid crystal display panel includes: a transparent insulating substrate; a signal line and a scanning line arranged in a display region on the transparent insulating substrate and crossing each other in a matrix; a protective insulating film arranged so as to cover at least the signal line and the scanning line from above; a first insulating film that covers the protective insulating film from above; and a first contact hole that penetrates at least the first insulating film and the protective insulating film to reach a surface of a common interconnect. The first contact hole has a bottom and an inner side surface covered with a first stacked film composed of a first transparent conductive film made of the same material as the lower electrode and a second transparent conductive film made of the same material as the upper electrode.



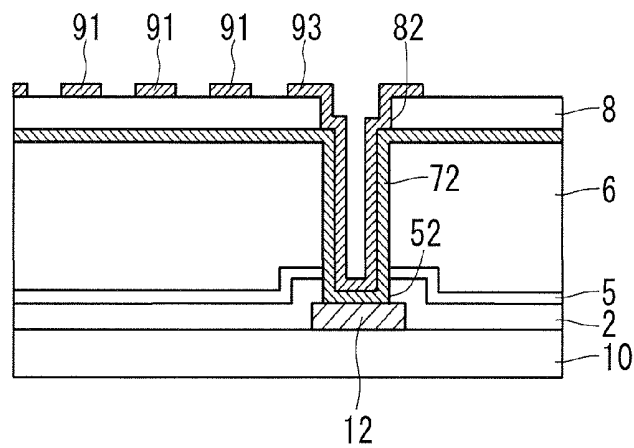
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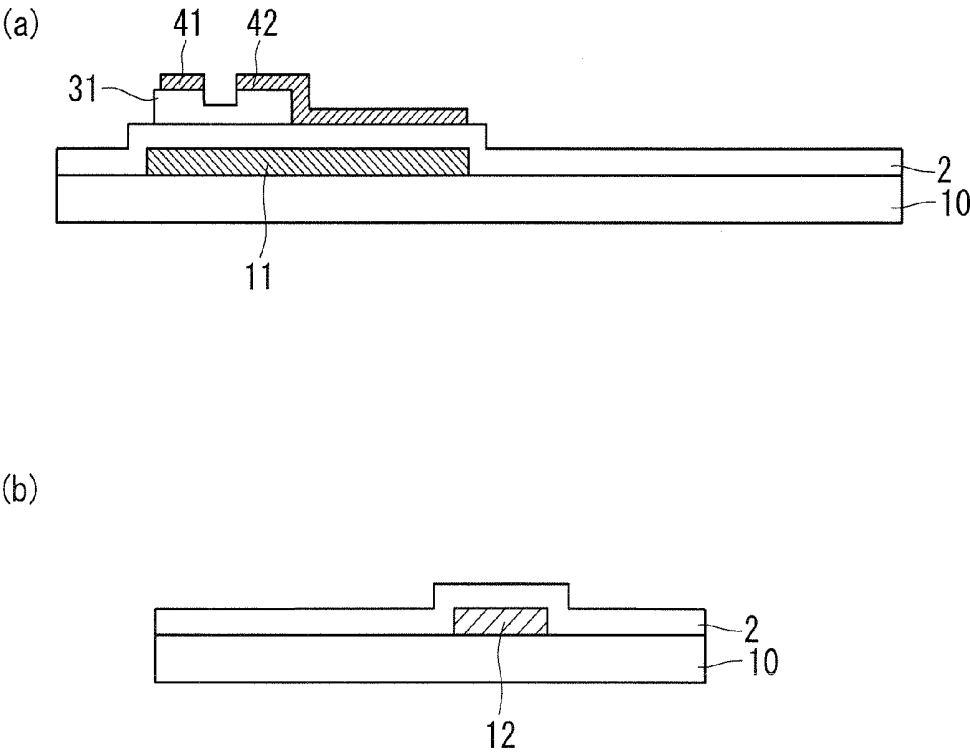
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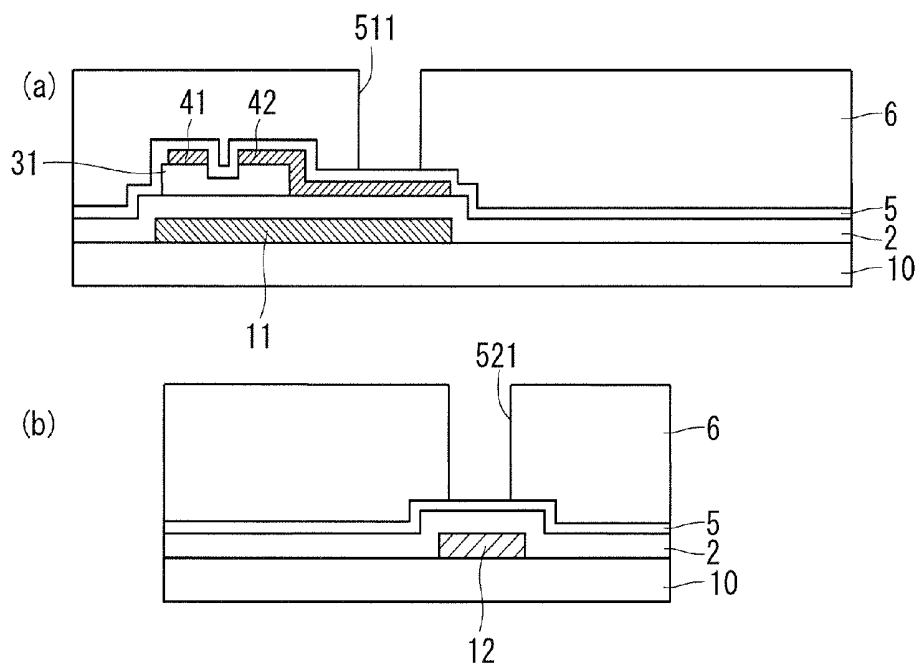
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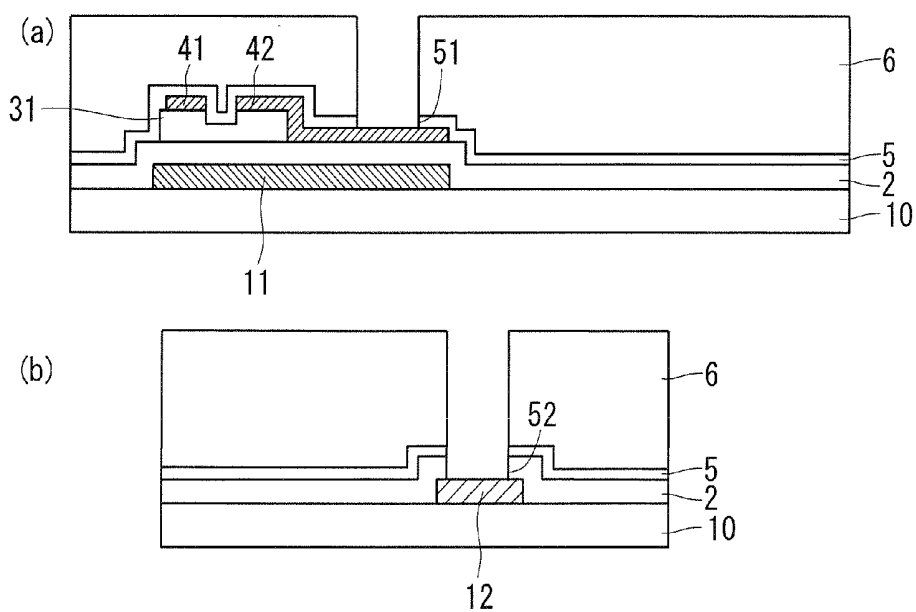
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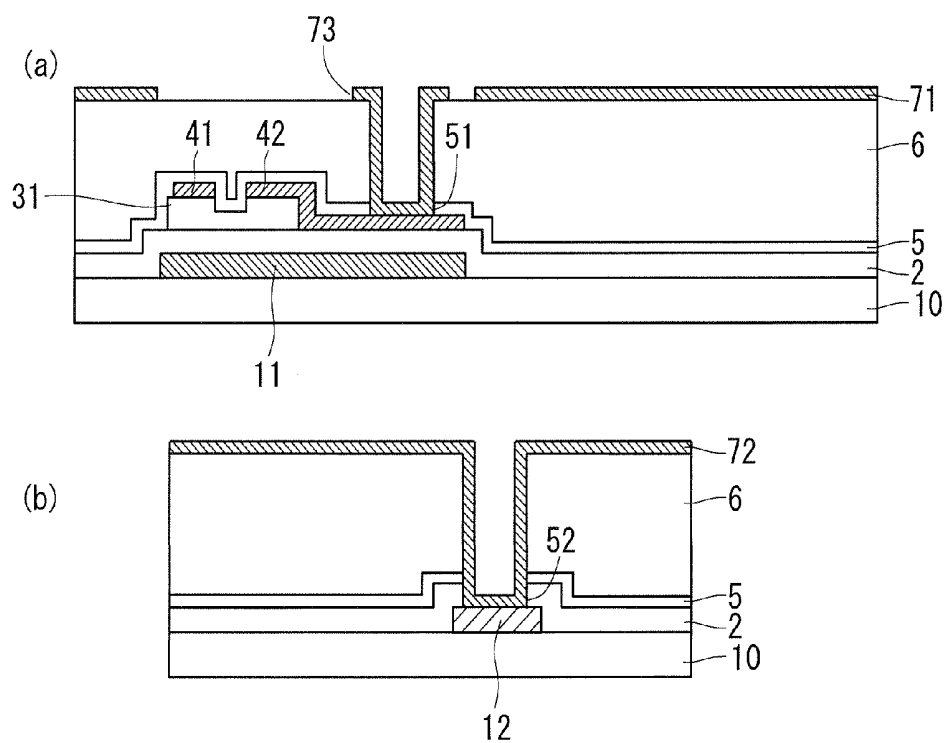
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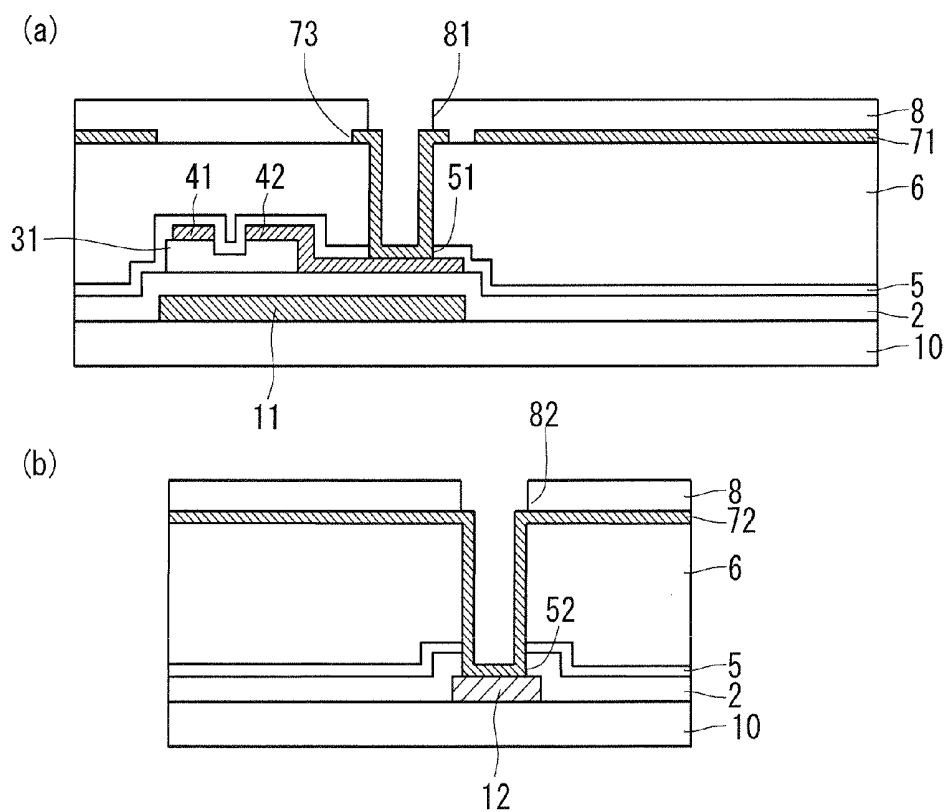
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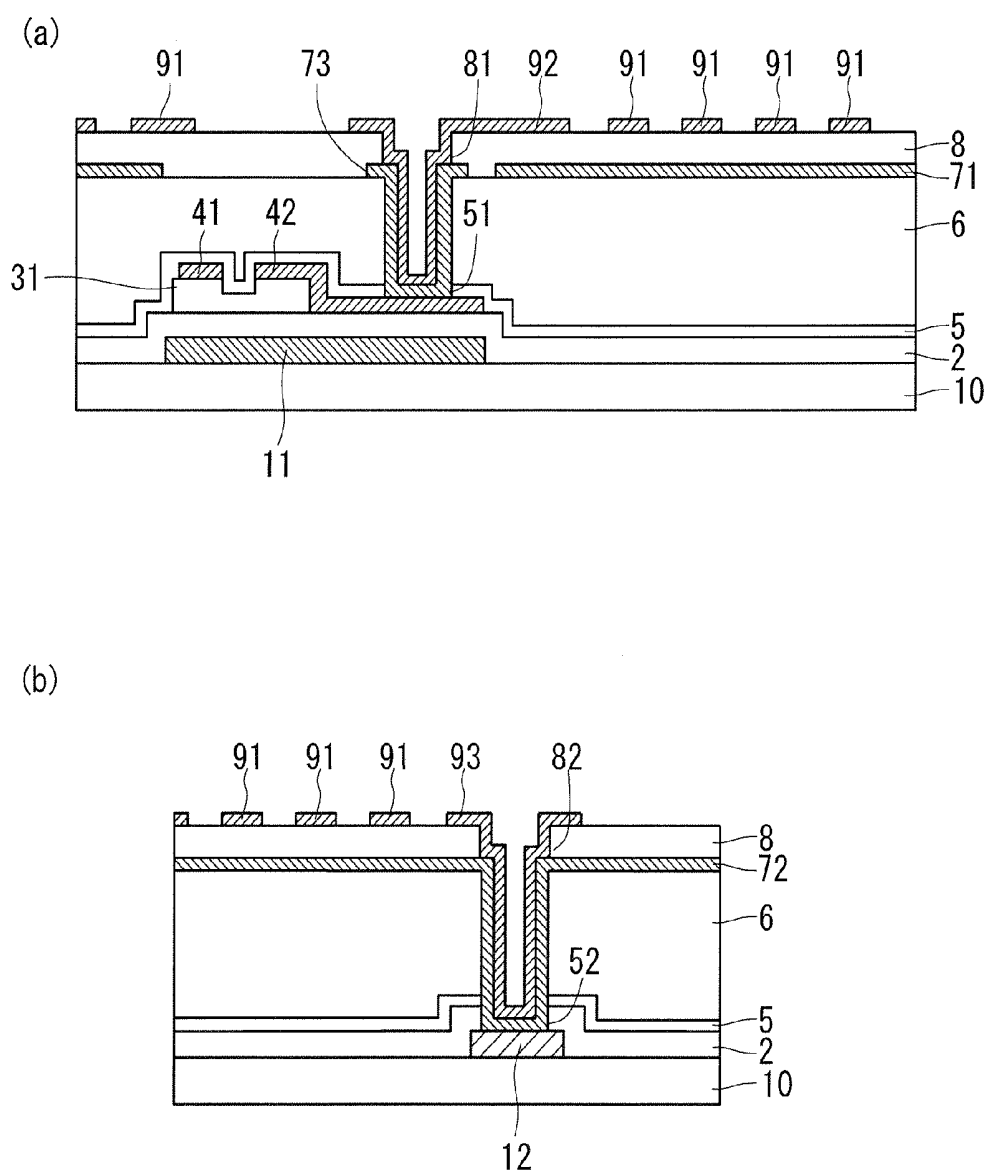
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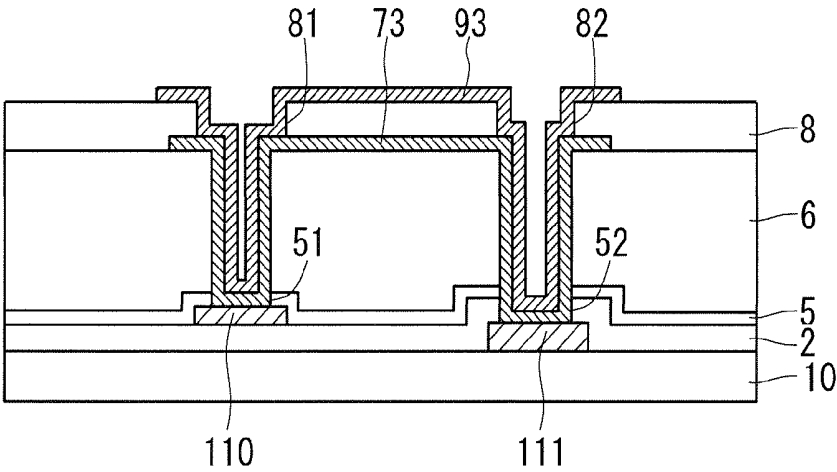
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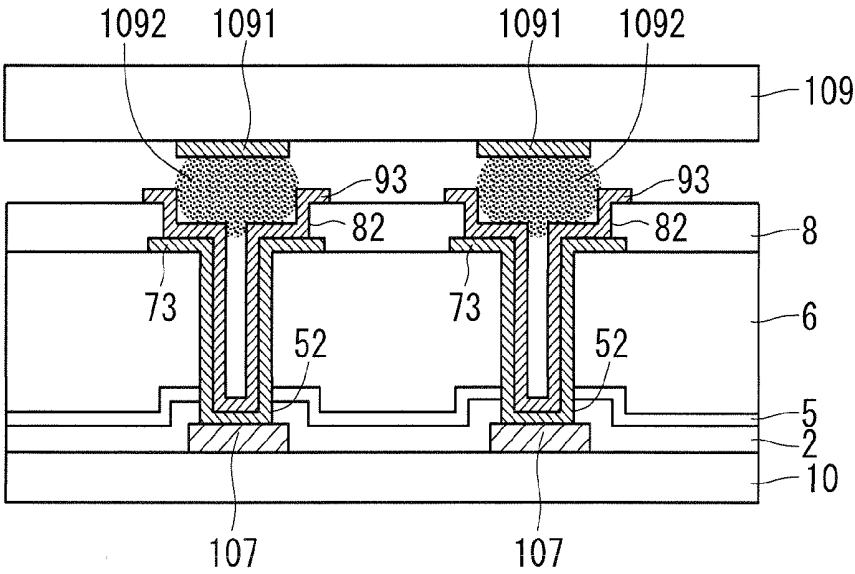
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LIQUID CRYSTAL DISPLAY PANEL AND METHOD OF MANUFACTURING THE SAME

FIELD OF THE INVENTION

[0001] The present invention relates to a liquid crystal display panel forming a liquid crystal display and a method of manufacturing the liquid crystal display panel.

BACKGROUND ART

[0002] A TN (twisted nematic) mode has widely been used as one of display systems for a liquid crystal display. However, the TN mode has been replaced by a lateral electric field system in recent years that applies a voltage between a pixel electrode and an opposed electrode to generate an electric field in a direction substantially horizontal to a panel, thereby driving liquid crystal molecules in a horizontal direction.

[0003] The lateral electric field system works advantageously for wider viewing angles, higher resolution and higher brightness, and is considered to become the mainstream of medium and small sized panels represented by smartphones and tablets, for example.

[0004] The lateral electric field system includes known modes such as an IPS (in-plane switching) mode and an FFS (fringe field switching) mode. In the FFS mode, a lower electrode and an upper electrode with a slit are arranged while an insulating film is placed therebetween. One of the upper and lower electrodes functions as a pixel electrode and the other electrode functions as an opposed electrode. An electric field is generated in a direction from the slit of the upper electrode toward a liquid crystal above the upper electrode. The electric field thereby generated drives the liquid crystal.

[0005] In a display region of an active-matrix liquid crystal display, a thin-film transistor is formed below a lower electrode while a protective insulating film is provided between the lower electrode and the thin-film transistor. Regarding application of a voltage, an arbitrary control signal (voltage) is applied to the thin-film transistor from outside via a signal line to turn on the thin-film transistor. In response, a predetermined voltage is applied to the lower or upper electrode via a contact hole formed in the protective insulating film. Japanese Patent No. 4487318 describes an example of such a liquid crystal display panel.

[0006] In the aforementioned structure, if a conductive layer formed inside the contact hole in the protective insulating film and an electrode of the thin-film transistor are not connected stably, an electric field is not generated normally between the lower and upper electrodes, leading to display failure in some cases.

[0007] Hence, the lower and upper electrode are each composed of a transparent conductive film of a thickness of 100 nm or less in order to increase the transparency of the transparent conductive film.

[0008] This forms an interconnect inside the contact hole composed of the thin transparent conductive film, and this transparent conductive film is further formed on an electrode surface of the thin-film transistor at the bottom of the contact hole.

[0009] The contact hole is small in width so the coating performance of the transparent conductive film is reduced at the inner side wall of the contact hole. Hence, with the intention of preventing cut of the transparent conductive film at a stepped part (step cut), extreme care should be taken so as to

maintain a sufficient thickness of the transparent conductive film on a part hard to cover with the transparent conductive film.

[0010] In the liquid crystal display panel disclosed in Japanese Patent No. 4487318, a contact hole to be formed in the protective insulating film (passivation film) (contact hole in the protective insulating film), and a contact hole to be formed in a planarized film composed of an organic film and covering the protective insulating film (contact hole in the planarized film), are provided separately.

[0011] As a result, the contact hole in the planarized film is formed inwardly of the contact hole in the protective insulating film, and the transparent conductive film is formed on the side wall of the contact hole in the planarized film and on the electrode surface, as shown in FIG. 5.

[0012] According to a method of manufacturing the liquid crystal display panel disclosed in Japanese Patent No. 4487318, the contact hole in the planarized film is formed by dry etching. More specifically, a resist mask is formed, and selectivity between the resist and the planarized film (ratio between the respective etching amounts) is adjusted under conditions for the dry etching. This can form the contact hole in the planarized film into a tapered shape (shape where an opening part is larger in area than the bottom) relatively easily. This shape achieves favorable coating performance of the transparent conductive film. The aforementioned method can also form a contact hole in a planarized film made of a photosensitive material into the same shape.

[0013] In the liquid crystal display panel disclosed in Japanese Patent No. 4487318, however, a metal film as an electrode of the thin-film transistor and the planarized film directly contact each other, as shown for example in FIG. 10. The planarized film composed of an organic film and the like contains a slight amount of water and this water may generate corrosion of the metal film. Additionally, the planarized film on the metal film generally does not have strong adhesive force so it may become separated in some cases. Separation of the planarized film may generate a step cut of the transparent conductive film.

[0014] A material for the metal film and that for the planarized film should be limited in order to avoid the aforementioned problems. Thus, it is preferable that the protective insulating film cover the metal film from above to prevent contact between the metal film and the planarized film. To be specific, the protective insulating film is provided with the intention of shielding water and enhancing the adhesive force of the planarized film. Thus, a silicon nitride (SiN) film is suitable as the protective insulating film.

[0015] Preferably, a contact hole is formed in the planarized film on the protective insulating film in order to prevent contact between the metal film and the planarized film.

[0016] An SiN film is etched at a high etching rate. Hence, if the protective insulating film is composed of the SiN film for the aforementioned reason, the contact hole in the protective insulating film is formed into an upright shape and cannot be formed into a tapered shape easily, unlike the contact hole in the planarized film.

[0017] Additionally, a surface of the metal film at the bottom of the contact hole may be roughened to generate a gap (notch) in the outer circumference of the bottom of the contact hole. In this case, the coating performance of the transparent conductive film may be degraded at the gap to generate a step cut of the transparent conductive film, leading to the probability of display failure.

SUMMARY OF THE INVENTION

[0018] It is an object of the present invention to provide a liquid crystal display panel and a method of manufacturing the same capable of preventing a step cut of a transparent conductive film inside a contact hole.

[0019] According to the present invention, a liquid crystal display panel includes: a transparent insulating substrate; a signal line and a scanning line arranged in a display region on the transparent insulating substrate and crossing each other in a matrix; a common interconnect arranged so as to extend in parallel with the signal line or the scanning line; a protective insulating film arranged so as to cover at least the signal line and the scanning line from above; a first insulating film that covers the protective insulating film from above; a lower electrode and an upper electrode arranged one above the other to be opposed to each other above the first insulating film; and a first contact hole that penetrates at least the first insulating film and the protective insulating film to reach a surface of the common interconnect. The first contact hole has a bottom and an inner side surface covered with a first stacked film composed of a first transparent conductive film made of the same material as the lower electrode and a second transparent conductive film made of the same material as the upper electrode.

[0020] In this liquid crystal display panel, the first contact hole has a bottom and an inner side surface covered with the first stacked film composed of the first transparent conductive film made of the same material as the lower electrode and the second transparent conductive film made of the same material as the upper electrode. This can prevent a step cut of a transparent conductive film inside the first contact hole.

[0021] These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] FIG. 1 is a plan view showing a planar structure of a liquid crystal display panel of a preferred embodiment of the present invention;

[0023] FIG. 2 is a plan view showing the structure of a pixel part in a display region;

[0024] FIGS. 3 and 4 are sectional views each showing a partial structure of the pixel part;

[0025] FIGS. 5 to 10 are sectional views each showing a step of manufacturing the liquid crystal display panel of the preferred embodiment of the present invention; and

[0026] FIGS. 11 and 12 each show an example of a different way of application of the present invention.

EMBODIMENT FOR CARRYING OUT THE INVENTION

[0027] In a first preferred embodiment of the present invention described below, the present invention is applied to a liquid crystal display panel of an FFS (fringe field switching) mode.

<Device Structure>

[0028] FIG. 1 is a plan view showing a planar structure of a liquid crystal display panel 100 of a preferred embodiment of the present invention. FIG. 1 is a schematic view, so that it does not reflect an actual size and the like of a component

shown therein. To prevent complication, a part except for those relevant to the present invention is omitted, and some of these relevant parts are simplified in FIG. 1.

[0029] As shown in FIG. 1, the liquid crystal display panel 100 is broadly divided into a display region 101 in which an image is displayed and a frame region 102 surrounding the display region 101.

[0030] The display region 101 includes a plurality of signal lines 103 and a plurality of scanning lines 104. The signal lines 103 and the scanning lines 104 extend to be perpendicular to each other. A plurality of common interconnects 105 is provided in parallel with the scanning lines 104. A region surrounded by adjacent signal lines 103 and the scanning line 104 form one pixel part. Accordingly, the display region 101 includes a plurality of pixel parts arranged in a matrix.

[0031] A thin-film transistor 106 is arranged at an intersection between the signal line 103 and the scanning line 104. One thin-film transistor 106 is provided in one pixel.

[0032] The frame region 102 includes a plurality of mount terminals 107 to which pulled-out interconnects 110 extending from the signal lines 103 in the display region 101 and pulled-out interconnects 111 extending from the scanning lines 104 in the display region 101 are connected, and a plurality of external connection terminals 1071 connected to the corresponding mount terminals 107. The common interconnects 105 are tied in the frame region 102 and receive a common potential.

[0033] An IC (integrated circuit) chip 109 for signal control is connected to the corresponding mount terminals 107. Interconnect substrates 108 such as FPCs (flexible printed circuits) are connected to the corresponding external connection terminals 1071.

[0034] FIG. 2 is a plan view showing the structure of the pixel parts in the display region 101. The present invention relates to the structure of what is called a TFT substrate, so that a color filter substrate arranged to be opposed to the TFT substrate will not be described and will not be shown in the drawings.

[0035] As shown in FIG. 2, the pixel parts each include a pixel electrode 91 and an opposed electrode 71 arranged one above the other. A voltage is applied between the pixel electrode 91 and the opposed electrode 71 to generate an electric field in a direction substantially horizontal to the liquid crystal display panel 100. This drives liquid crystal molecules in a horizontal direction to realize display of an image.

[0036] In order to apply a display voltage to the pixel electrode 91 based on signal data input from outside, the thin-film transistor 106 is arranged on a transparent insulating substrate (not shown in FIG. 2) on the lower side of the pixel electrode 91 and the opposed electrode 71.

[0037] The thin-film transistor 106 has a gate electrode connected to the scanning line 104, and a source electrode connected to the signal line 103. A protective insulating film (not shown in FIG. 2) is provided on the transparent insulating substrate. The pixel electrode 91 is electrically connected to a drain electrode (not shown in FIG. 2) via a contact hole 51 formed in the protective insulating film. The opposed electrode 71 is electrically connected to the common interconnect 105 via a contact hole 52 formed in the protective insulating film.

[0038] If a control signal is supplied via the scanning line 104 in the aforementioned structure, a current starts to flow from the source electrode into the drain electrode of the thin-film transistor 106. To be specific, a voltage determined

based on signal data supplied via the signal line **103** is applied to the pixel electrode **91**. The pixel electrode **91** has a plurality of slits in order for an electric field generated in response to the voltage determined based on the signal data to go up.

[0039] The signal data supplied via the signal line **103** is given from the IC chip **109** connected to the mount terminal **107** in the frame region **102** or from the interconnect substrate **108** connected to the external connection terminal **1071**. A voltage responsive to display data is applied to the pixel electrode **91**.

[0040] Next, the structure in cross section of the pixel part is described by using FIGS. **3** and **4**. In (a) portion of FIG. **3** is a sectional view along line A-A taken from arrows of FIG. **2**. FIG. **4** is a sectional view along line B-B taken from arrows of FIG. **2**.

[0041] As shown in (a) portion of FIG. **3**, a gate electrode **11** is formed in a region on a transparent insulating substrate **10** in the display region **101** and where the thin-film transistor **106** is formed. The scanning line **104** extending from the gate electrode **11** and a common interconnect pad **12** extending from the common interconnect **105** arranged in parallel with the scanning line **104** are further formed on the transparent insulating substrate **10** in the display region **101**.

[0042] A gate insulating film **2** is formed so as to cover the gate electrode **11**, the scanning line **104**, the common interconnect **105**, and the common interconnect pad **12**. An SiN film may be used as the gate insulating film **2**, for example.

[0043] An insular semiconductor film **31** is provided in a region above the gate electrode **11** so as to contact the gate insulating film **2**.

[0044] The semiconductor film **31** is composed of any one of amorphous silicon, microcrystalline silicon and polycrystalline silicon, or of a silicon semiconductor film including a combination of stacked layers made of two or more of these materials, or of an oxide semiconductor film.

[0045] The semiconductor film **31** is divided into a source region and a drain region while a channel region is defined therebetween. A source electrode **41** and a drain electrode **42** are formed on the source and drain regions respectively.

[0046] As a result, the thin-film transistor **106** is composed of the gate electrode **11**, the semiconductor film **31**, and the source and drain electrodes **41** and **42**.

[0047] The signal line **103** (FIG. **2**) composed of a metal film made of the same material as the source and drain electrodes **41** and **42** is formed on the gate insulating film **2**. A protective insulating film **5** is formed so as to entirely cover the thin-film transistor **106** and the signal line **103** from above.

[0048] The protective insulating film **5** is an inorganic insulating film that may either be a single-layered film composed of an SiN film or a multi-layered film (composed of an SiO film and an SiN film).

[0049] A planarized film **6** is formed on the protective insulating film **5**. The SiN film prevents degradation of the characteristics of the thin-film transistor **106** due to water entering from the planarized film **6**, for example. The planarized film **6** may be omitted, and only the protective insulating film **5** composed of the SiN film may be provided.

[0050] The planarized film **6** is composed of an organic resin film mainly containing acrylic or an SOG (spin-on-glass) film. The reason is as follows. Noise from the signal line **103** may affect the pixel electrode **91** to reduce display quality. An acrylic resin film or an SOG film has a dielectric constant ϵ of from about three to four lower than that of an SiN

film of from six to seven. In this way, the acrylic resin film or the SOG film reduces a parasitic resistance, thereby allowing suppression of the influence by the noise.

[0051] An acrylic resin has high transparency, can be obtained at low cost, is easy to handle as it becomes applicable as a coating film by dissolving in an organic solvent, and can be sintered at a relatively low temperature.

[0052] An SiO₂ film formed by process such as CVD process or sputtering process has a dielectric constant ϵ similar to that of an SOG film. However, the SiO₂ film cannot be planarized as easy as the SiN film.

[0053] The opposed electrode **71** composed of a first transparent conductive film made of ITO (indium tin oxide) or IZO (indium zinc oxide) is formed on a planar surface of the planarized film **6**. An interlayer insulating film **8** is formed on the planarized film **6** so as to cover the opposed electrode **71**. The pixel electrode **91** composed of a second transparent conductive film made of ITO or IZO is formed on the interlayer insulating film **8**.

[0054] The contact hole **51** is formed so as to penetrate the protective insulating film **5** on the drain electrode **42** to reach the drain electrode **42**. Further, as shown in FIG. **4**, the contact hole **52** is formed so as to penetrate the gate insulating film **2** and the protective insulating film **5** above the common interconnect pad **12**.

[0055] As shown in (a) portion of FIGS. **3** and **4** respectively, the contact holes **51** and **52** are formed in the planarized film **6** on the protective insulating film **5** in order for metal films such as the drain electrode **42** and the common interconnect pad **12** not to contact the planarized film **6** directly. This can prevent corrosion of metal films forming the drain electrode **42** and the common interconnect pad **12** due to water in the planarized film **6**. The protective insulating film **5** is exposed at respective inner side surfaces of the contact holes **51** and **52** near the bottom surfaces thereof. The planarized film **6** is exposed at these inner side surfaces above the protective insulating film **5**.

[0056] As shown in FIG. **4**, the opposed electrode **71** is electrically connected to the common interconnect pad **12** via the transparent conductive film **72** extending from the opposed electrode **71** and the contact hole **52**. To be specific, the transparent conductive film **72** extending from the opposed electrode **71** covers the inner side surface of the contact hole **52** and a surface of the common interconnect pad **12** exposed at the bottom surface of the contact hole **52**, thereby electrically connecting the common interconnect pad **12** and the opposed electrode **71**.

[0057] The opposed electrode **71** is further electrically connected via a contact hole **82** in the interlayer insulating film **8** formed above the contact hole **52** to a transparent conductive film **93** made of the same material as the pixel electrode **91** and formed in the same layer as the pixel electrode **91**. To be specific, the transparent conductive film **93** covers the transparent conductive film **72** from above that covers the inner surface of the contact hole **52**, so that the inner side surface and the bottom of the contact hole **52** are covered with a stacked film composed of the transparent conductive films **72** and **93**.

[0058] The transparent conductive film **93** and the pixel electrode **91** are electrically independent so that they are not electrically connected to each other.

[0059] As shown in (b) portion of FIG. **3**, a transparent conductive film **73** made of the same material as the opposed electrode **71** and formed in the same layer as the opposed

electrode **71** is formed so as to cover the inner side surface of the contact hole **51** and a surface of the drain electrode **42** exposed at the bottom of the contact hole **51**.

[0060] The transparent conductive film **73** and the opposed electrode **71** are electrically independent so that they are not electrically connected to each other.

[0061] The pixel electrode **91** is electrically connected via a contact hole **82** in the interlayer insulating film **8** formed above the contact hole **51** to the transparent conductive film **73** that covers the inner surface of the contact hole **51**, thereby electrically connecting the pixel electrode **91** and the drain electrode **42**. To be specific, a transparent conductive film **92** extending from the pixel electrode **91** covers the inner side surface of the contact hole **81** and further covers the transparent conductive film **73** from above that covers the inner surface of the contact hole **51**. As a result, the inner side surface and the bottom of the contact hole **51** are covered with a stacked film composed of the transparent conductive films **73** and **92**.

[0062] The contact holes **81** and **82** in the interlayer insulating film **8** are formed to have openings larger than those of the contact holes **51** and **52** in the protective insulating film **5** respectively.

[0063] As a result, the inner surface of the contact hole **52** can be covered with a stacked film composed of the transparent conductive films **72** and **93**, and the inner surface of the contact hole **51** can be covered with a stacked film composed of the transparent conductive films **73** and **92**.

[0064] A transparent conductive film is formed as a thin film of a thickness of 100 nm or less in terms of the need of increasing the transparency thereof. Thus, it is preferable that a contact hole have a tapered shape in cross section in order to enhance the coating performance of the transparent conductive film. The contact holes **51** and **52** are generally formed by dry etching. The contact holes **51** and **52** are formed simultaneously by etching through different film thicknesses. Hence, etching time should be controlled for the contact hole **52** to be formed by etching through a greater thickness. This makes it difficult to form the contact holes **51** and **52** into a tapered shape.

[0065] The respective surfaces of the drain electrode **42** and the common interconnect pad **12** should be exposed at the respective bottoms of the contact hole **51** and **52**. It is likely that the dry etching will etch the respective surfaces of these metal films excessively in a thickness direction, so that the surfaces of these metal films become rough compared to the conditions thereof at the time of their deposition.

[0066] A surface of a metal film forming an interface with the protective insulating film **5** composed of an SiN film may be given a gap (notch) generated in the outer circumference of a contact hole directly below the protective insulating film **5**. This reduces the coating performance of a transparent conductive film to be formed in a subsequent step. In this case, a resultant transparent conductive film may become a very thin film, leading to the probability of a step cut of the transparent conductive film.

[0067] In (b) portion of FIG. 3 shows a region "X" in an enlarged manner including the bottom surface of the contact hole **51** and its vicinity shown in (a) portion of FIG. 3. As shown in (b) portion of FIG. 3, the inner side surface of the protective insulating film **5** projects slightly further toward the inside of the contact hole **51** than the inner side surface of the planarized film **6**. This is for the reason that, when the protective insulating film **5** is dry etched by using a contact

hole formed in the planarized film **6** as an etching mask, the inner side surface of the planarized film **6** is etched slightly to be recessed, thereby making the protective insulating film **5** project toward the inside of the contact hole.

[0068] The surface of the drain electrode **42** is roughened as a result of the dry etching with the contact hole. This dry etching etches the protective insulating film **5** deeper to generate notches (indicated by arrows), forming the bottom into a "reverse" tapered shape.

[0069] If only one of the transparent conductive films **73** and **92** is formed, a film thickness becomes thin at the notched parts of the bottom. In this case, a step cut may be generated easily. In this preferred embodiment, the stacked film composed of the transparent conductive films **73** and **92** is formed. Thus, a large film thickness can be maintained at the notched parts, making it possible to prevent a step cut.

<Manufacturing Method>

[0070] A method of manufacturing the liquid crystal display panel **100** of this preferred embodiment of the present invention is described next by using FIGS. 5 to 9 while referring to FIGS. 1 and 2. In the manufacturing method of the liquid crystal display panel, the display and frame regions are formed simultaneously. Meanwhile, the manufacturing method described below is directed to formation of the display region.

[0071] First, a first metal film is deposited by sputtering process on one main surface (front surface) of the transparent insulating substrate **10** composed for example of a glass substrate. Examples of a material for the first metal film include aluminum (Al), an alloy containing aluminum, molybdenum (Mo), and chrome (Cr).

[0072] Then, a photoresist made of a photosensitive resin is applied on the first metal film for example by spin coating. The applied photoresist is subjected to a first photolithography step including exposure and development, thereby patterning the photoresist into a desirable shape. Then, by using this photoresist as an etching mask, the first metal film is etched into a desirable pattern. Next, the photoresist pattern is removed, thereby forming the gate electrode **11** of (a) portion of FIG. 5 and the common interconnect pad **12** of (b) portion of FIG. 5, and at the same time, forming the scanning line **104** (FIG. 2) and the common interconnect **105** (FIG. 2). Further, in the frame region **102** (FIG. 1), the pulled-out interconnects **111** extending from the scanning lines **104**, a bundle of the common interconnects **105**, and the mount terminals **107** (FIG. 1) connected to the pulled-out interconnects **111** are formed.

[0073] Next, the gate insulating film **2** and a semiconductor film are deposited successively in this order by plasma CVD process so as to cover the transparent insulating substrate **10** entirely on which the gate electrode **11** and the common interconnect pad **12** are formed. The gate insulating film **2** is composed of an SiN film, and the semiconductor film is composed of any one of amorphous silicon, microcrystalline silicon and polycrystalline silicon, or of a silicon semiconductor film made of two or more of these materials, or of an oxide semiconductor film.

[0074] A photoresist made of a photosensitive resin is applied on the semiconductor film for example by spin coating. The applied photoresist is subjected to a second photolithography step including exposure and development, thereby patterning the photoresist into a desirable shape. Next, by using this photoresist as an etching mask, the semiconductor

film is etched to form the insular semiconductor film **31** including the source, channel, and drain regions as shown in (a) portion of FIG. **5**.

[0075] Then, a second metal film is deposited by sputtering process so as to cover the entire gate insulating film **2** from above including the semiconductor film **31**. Examples of a material for the second metal film include aluminum (Al), an alloy containing aluminum, molybdenum (Mo), and chrome (Cr).

[0076] Then, a photoresist made of a photosensitive resin is applied on the second metal film for example by spin coating. The applied photoresist is subjected to a third photolithography step including exposure and development, thereby patterning the photoresist into a desirable shape. Next, by using this photoresist as an etching mask, the second metal film is etched into a desirable pattern. Then, the photoresist pattern is removed, thereby forming the source electrode **41** on the source region of the semiconductor film **31** as shown in (a) portion of FIG. **5**, and at the same time, forming the signal line **103** extending from the source electrode **41** and forming the drain electrode **42** on the drain region. Further, in the frame region **102** (FIG. **1**), the pulled-out interconnects **110** extending from the signal lines **103**, the mount terminals **107** (FIG. **1**) connected to the pulled-out interconnects **110**, and the external connection terminals **1071** (FIG. **1**) are formed.

[0077] Next, as shown in (a) portion of FIG. **6** and (b) portion of FIG. **6**, an SiN film is deposited by plasma CVD process so as to cover the entire transparent insulating substrate **10** on which the aforementioned structures are formed, thereby forming the protective insulating film **5**.

[0078] Then, an organic resin mainly containing acrylic and the like is applied as a photosensitive resin on the protective insulating film **5** for example by spin coating to form the planarized film **6**. The planarized film **6** is subjected to a fourth photolithography step including exposure and development, thereby patterning a contact hole **511** and a contact hole **512** in the planarized film **6** as shown in (a) portion of FIG. **6** and (b) portion of FIG. **6** respectively.

[0079] More specifically, the contact hole **511** is formed so as to reach a position above the drain electrode **42** on the semiconductor film **31** and away from the semiconductor film **31**. The contact hole **521** is formed so as to reach a position above the common interconnect pad **12**. Although not shown in the drawings, contact holes are also formed so as to reach at respective positions above the pulled-out interconnects **110** and the pulled-out interconnects **111** in the frame region **102**.

[0080] Next, the protective insulating film **5** is dry etched via the contact hole **511** by using the planarized film **6** as an etching mask, thereby forming the contact hole **51** reaching the surface of the drain electrode **42** as shown in (a) portion of FIG. **7**. The protective insulating film **5** and the gate insulating film **2** are dry etched via the contact hole **52**, thereby forming the contact hole **52** reaching the surface of the common interconnect pad **12** as shown in (b) portion of FIG. **7**. Although not shown in the drawings, contact holes are also formed to reach respective positions above the pulled-out interconnects **110** and the pulled-out interconnects **111** in the frame region **102**.

[0081] The contact holes **51** and **52** are formed simultaneously by etching through different film thicknesses. Hence, etching time is controlled for the contact hole **52** to be formed by etching through a greater thickness, so that etching for the contact hole **52** is finished within the same time as the contact

hole **51**. The contact holes **51** and **52** are formed into an upright shape and preferably, into a tapered shape in cross section.

[0082] Etching time is controlled such that the respective surfaces of the drain electrode **42** and the common interconnect pad **12** are exposed at the bottoms of the contact holes **51** and **52** respectively. Generally, etching time is determined with a margin in consideration of variations in etching speed or variations in film thickness. Specifically, etching proceeds so far as to reach a level of over-etching. Thus, it is likely that dry etching will etch a surface of a metal film more than necessary in a thickness direction to roughen the surface of the metal film, compared to the condition thereof at the time of its deposition. At the same time, the surface of the metal film forming an interface with an SiN film may be given a gap (notch) generated in the outer circumference of a contact hole directly below the SiN film.

[0083] After the contact holes **51** and **52** are formed, the planarized film **6** is not removed but it remains as part of the protective insulating film **5** as shown in (a) portion of FIG. **8** and (b) portion of FIG. **8**.

[0084] Next, the first transparent conductive film is deposited by sputtering process so as to cover the entire planarized film **6** from above. The first transparent conductive film can be made of ITO or IZO.

[0085] The first transparent conductive film is deposited so as to cover a planar region in the surface of the planarized film **6** and the respective inner surfaces of the contact holes **51** and **52**.

[0086] Then, a photoresist made of a photosensitive resin is applied on the planarized film **6** for example by spin coating. The applied photoresist is subjected to a fifth photolithography step including exposure and development, thereby patterning the photoresist into a desirable shape. Next, by using this photoresist as an etching mask, the first transparent conductive film is etched. Then, the photoresist pattern is removed, thereby patterning the opposed electrode **71** in the planar region in the surface of the planarized film **6** and forming the transparent conductive film **73** on the inner surface of the contact hole **51** and a surrounding of this inner surface, as shown in (a) portion of FIG. **8**. The transparent conductive film **73** is electrically independent of the opposed electrode **71**. Further, the transparent conductive film **72** extending from the opposed electrode **71** is formed so as to cover the inner surface of the contact hole **52**, as shown in (b) portion of FIG. **8**.

[0087] Next, an SiN film is deposited by plasma CVD process so as to cover the entire planarized film **6** from above on which the opposed electrode **71** is formed, thereby forming the interlayer insulating film **8**.

[0088] At this time, the SiN film is deposited at a temperature not exceeding the heatproof temperature of the planarized film **6**. More specifically, if the planarized film **6** is made of an acrylic resin, the SiN film is deposited at a temperature of about 220° C. or less.

[0089] Then, a photoresist made of a photosensitive resin is applied on the interlayer insulating film **8** for example by spin coating. The applied photoresist is subjected to a sixth photolithography step including exposure and development, thereby patterning the photoresist into a desirable shape. Next, by using this photoresist as an etching mask, the interlayer insulating film **8** is dry etched. Then, the photoresist pattern is removed, thereby forming the contact hole **81** continuous with upper part of the contact hole **51** as shown in (a)

portion of FIG. 9 and forming the contact hole 82 continuous with upper part of the contact hole 52 as shown in (b) portion of FIG. 9.

[0090] The contact holes 81 and 82 are formed to have openings larger than those of the contact holes 51 and 52 under the contact holes 81 and 82 respectively. The interlayer insulating film 8 has a uniform thickness. Thus, it is desirable that the contact holes 81 and 82 be formed into a tapered shape by controlling etching conditions.

[0091] The transparent conductive films 73 and 72 exist below the contact holes 81 and 82 respectively. Thus, the transparent conductive films 73 and 72 function as stopper layers during the dry etching, thereby preventing damage on the planarized film 6 to be generated during the etching.

[0092] Next, the second transparent conductive film is deposited by sputtering process so as to cover the entire interlayer insulating film 8 from above. The second transparent conductive film can be made of ITO or IZO.

[0093] The second transparent conductive film is deposited so as to cover the planar region in the surface of the interlayer insulating film 8, on the respective inner surfaces of the contact holes 81 and 51 continuous with each other, and on the respective inner surfaces of the contact holes 82 and 52 continuous with each other.

[0094] Then, a photoresist made of a photosensitive resin is applied on the interlayer insulating film 8 for example by spin coating. The applied photoresist is subjected to a seventh photolithography step including exposure and development, thereby patterning the photoresist into a desirable shape. Next, by using this photoresist as an etching mask, the second transparent conductive film is etched. Then, the photoresist pattern is removed, thereby forming the pixel electrode 91 with slits above the opposed electrode 71. Further, the transparent conductive film 92 extending from the pixel electrode 91 covers the inner side surface of the contact hole 81. The transparent conductive film 92 further covers the transparent conductive film 73 from above that covers the inner surface of the contact hole 51. As a result, the inner side surface and the bottom of the contact hole 51 are covered with the stacked film composed of the transparent conductive films 73 and 92, as shown in (a) portion of FIG. 10.

[0095] Further, as shown in (b) portion of FIG. 10, the transparent conductive film 93 electrically independent of the pixel electrode 91 covers the inner side surface of the contact hole 82. The transparent conductive film 93 further covers the transparent conductive film 72 from above that covers the inner surface of the contact hole 52. As a result, the inner side surface and the bottom of the contact hole 52 are covered with the stacked film composed of the transparent conductive films 72 and 93.

[0096] As described above, in the liquid crystal display panel 100 of this preferred embodiment, in order for the drain electrode 42 and the common interconnect pad 12 not to contact the planarized film 6, the respective inner surfaces of the contact holes 51 and 52 formed in the planarized film 6 on the protective insulating film 5 are each covered with a stacked film composed of transparent conductive films. This can prevent corrosion of the metal films of the drain electrode 42 and the common interconnect pad 12 due to water in the planarized film 6.

[0097] Metal films such as the drain electrode 42 and the common interconnect pad 12 do not contact the planarized film 6 directly. Thus, the planarized film 6 can be made of an acrylic resin not having strong force to contact a metal film.

[0098] An acrylic resin becomes applicable as a coating film by dissolving in an organic solvent and can be sintered at a relatively low temperature, so that the contact holes 51 and 52 can be formed simultaneously by using a contact hole pattern in the planarized film 6. This allows reduction of manufacturing steps.

[0099] The contact holes 51 and 52 are formed by dry etching the protective insulating film 5 via the contact holes 511 and 512 respectively by using the planarized film 6 as an etching mask. This allows reduction of a required alignment margin, compared to that required for forming contact holes separately. As a result, the contact holes can be formed in smaller regions. This can reduce an area occupied by the contact holes in a display region to increase an aperture ratio, thereby achieving enhanced display characteristics.

[0100] The respective inner surfaces of the contact holes 51 and 52 are each covered with a stacked film composed of transparent conductive films. Thus, even if the protective insulating film 5 projects at the inner side surfaces of the contact holes 51 and 52 in the planarized film 6 to generate a gap (notch) in the outer circumference of a contact hole directly below the protective insulating film 5, generation of a step cut is suppressed so that the electrical characteristics of a transparent conductive film can be stabilized, thereby achieving high-quality display.

<First Example of Different Way of Application>

[0101] In the aforementioned example, the present invention is applied to a contact hole formed in the display region 101 of a liquid crystal display panel. The present invention is also applicable to a contact hole formed in the frame region 102.

[0102] The pulled-out interconnects 110 and 111 extending from the signal line 103 and the scanning line 104 respectively in the display region 101 are formed in the frame region 102. Contact holes may be formed to reach parts of the pulled-out interconnects 110 and 111, and interconnects made of the same material as the first or second transparent conductive film and formed in the same layer as the first or second transparent conductive film may be connected via these contact holes. The present invention is applicable to such contact holes.

[0103] A first example of a different way of application of the present invention is described next by using FIG. 11. FIG. 11 is a sectional view showing a connection structure between interconnects. In the frame region 102, the pulled-out interconnects 110 and 111 extending from the signal line 103 and the scanning line 104 respectively in the display region 101 may cross each other or may be electrically connected to each other, for example. This electrical connection can be established via the contact holes 51 and 52 formed in the planarized film 6.

[0104] FIG. 11 shows an exemplary structure where the pulled-out interconnects 110 and 111 extending from the signal line 103 and the scanning line 104 respectively are electrically connected via the transparent conductive films 73 and 93.

[0105] By referring to FIG. 11, the contact holes 51 and 52 are formed so as to reach upper parts of the pulled-out interconnects 110 and 111 respectively. The contact holes 81 and 82 penetrating the interlayer insulating film 8 are formed above the contact holes 51 and 52 respectively.

[0106] The respective inner surfaces of the contact holes 81 and 51 continuous with each other are covered with a stacked

film composed of the transparent conductive films 73 and 93, and the respective inner surfaces of the contact holes 82 and 52 continuous with each other are covered with a stacked film composed of the transparent conductive films 73 and 93. Further, the transparent conductive film 73 in the continuous contact holes 81 and 51 and the transparent conductive film 73 in the continuous contact holes 82 and 52 are connected via the transparent conductive film 73 on the planarized film 6.

[0107] The transparent conductive film 93 in the continuous contact holes 81 and 51 and the transparent conductive film 93 in the continuous contact holes 82 and 52 are connected via the transparent conductive film 93 on the interlayer insulating film 8.

[0108] The aforementioned parallel connection between the interconnects composed of the transparent conductive films can reduce an interconnect resistance. Further, the interconnects in the frame region 102 can be connected in the same steps as the step of manufacturing the contact holes and the step of manufacturing the transparent conductive films in the display region 101. This can reduce manufacturing steps, compared to the case where the interconnects in the frame region 102 are connected in a different manufacturing step.

<Second Example of Different Way of Application>

[0109] The mount terminals 107 are formed at respective ends of the pulled-out interconnects 110 and 111, and the external connection terminals 1071 are connected to the mount terminals 107. The present invention is also applicable to contact holes reaching the mount terminals 107 and the external connection terminals 1071.

[0110] By forming the contact holes in the frame region 102 into the same shape as that of the contact holes in the display region 101, the yield and reliability of an entire liquid crystal display panel can be enhanced.

[0111] A second example of a different way of application of the present invention is described next by using FIG. 12. In the frame region 102, the mount terminals 107 are formed at respective end portions of the pulled-out interconnects 110 and 111 extending from the signal line 103 and the scanning line 104 respectively in the display region 101. The IC chip 109 for signal control is connected to the mount terminals 107.

[0112] FIG. 12 shows a connection structure between the mount terminals 107 and the IC chip 109. The mount terminals 107 and the electrode terminals 1091 of the IC chip 109 are electrically connected via the transparent conductive films 73 and 93.

[0113] By referring to FIG. 12, the contact holes 52 are formed so as to reach upper parts of the mount terminals 107. The contact holes 82 penetrating the interlayer insulating film 8 are formed above the corresponding contact holes 52.

[0114] The respective inner surfaces of the contact holes 82 and 52 continuous with each other are covered with a stacked film composed of the transparent conductive films 73 and 93.

[0115] Bumps 1092 composed of resin containing conductive particles are provided to be connected to the electrode terminals 1091 of the IC chip 109. The IC chip 109 is placed such that the bumps 1092 contact the inner sides of the contact holes 82 the inner surfaces of which are covered with the transparent conductive film 93. The IC chip 109 is bonded under pressure to flattened out the bumps 1092, thereby mounting the IC chip 109 on the liquid crystal display panel 100.

[0116] In this way, the mount terminals 107 and the electrode terminals 1091 of the IC chip 109 are electrically connected via the contact holes same as those in the display region 101. This increases the mechanical strength of the contact holes to achieve higher strength during pressure bonding of the IC chip 109.

[0117] The mount terminals 107 are composed of the same metal film as the signal line 103 or the scanning line 104 and are covered with a transparent conductive film to suppress corrosion thereof due to moisture (water) in ambient air. The mount terminals 107 are covered with a stacked film composed of the transparent conductive films 73 and 93, so that corrosion of the mount terminals 107 can be suppressed more effectively. This suppresses generation of a defective at a later stage to maintain a quality, thereby realizing cost reduction.

[0118] The pixel electrode has been described as an upper electrode and the opposed electrode has been described as a lower electrode. Alternatively, the pixel electrode may be a lower electrode and the opposed electrode may be an upper electrode. The upper electrode of this case is given a slit in order to generate an electric field in an upward direction (direction of a liquid crystal layer).

[0119] The opposed electrode is described as having an integral structure extending through the display region as described in the preferred embodiment. The opposed electrode can be divided per pixel into sections, and these sections may be electrically connected via a contact hole.

[0120] The preferred embodiment of the present invention can be modified or omitted where appropriate without departing from the scope of the invention.

[0121] While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.

What is claimed is:

1. A liquid crystal display panel, comprising:

- a transparent insulating substrate;
 - a signal line and a scanning line arranged in a display region on said transparent insulating substrate and crossing each other in a matrix;
 - a common interconnect arranged so as to extend in parallel with said signal line or said scanning line;
 - a protective insulating film arranged so as to cover at least said signal line and said scanning line from above;
 - a first insulating film that covers said protective insulating film from above;
 - a lower electrode and an upper electrode arranged to be opposed to each other above said first insulating film, said lower and upper electrodes being arranged one above the other; and
 - a first contact hole that penetrates at least said first insulating film and said protective insulating film to reach a surface of said common interconnect,
- wherein said first contact hole has a bottom and an inner side surface covered with a first stacked film composed of a first transparent conductive film made of the same material as said lower electrode and a second transparent conductive film made of the same material as said upper electrode.

2. The liquid crystal display panel according to claim 1, comprising a thin-film transistor formed at an intersection between said signal line and said scanning line, wherein said thin-film transistor includes:

a gate electrode arranged on said transparent insulating substrate;

a gate insulating film arranged so as to cover said transparent insulating substrate from above including said gate electrode;

a semiconductor film arranged on said gate insulating film and at a position opposed to said gate electrode; and

a source electrode and a drain electrode arranged on a source region and a drain region of said semiconductor film so as to contact said source and drain regions respectively, and

said protective insulating film covers said thin-film transistor from above,

said liquid crystal display panel comprising a second contact hole that penetrates said first insulating film and said protective insulating film to reach a surface of said drain electrode,

wherein said second contact hole has a bottom and an inner side surface covered with a second stacked film composed of said first and second transparent conductive films.

3. The liquid crystal display panel according to claim 2, wherein

said first transparent conductive film of said first stacked film is a film extending from said lower electrode,

said second transparent conductive film of said first stacked film is a film electrically independent of said upper electrode,

said first transparent conductive film of said second stacked film is a film electrically independent of said lower electrode, and

said second transparent conductive film of said second stacked film is a film extending from said upper electrode.

4. The liquid crystal display panel according to claim 2, comprising an interlayer insulating film arranged between said upper and lower electrodes, wherein

said interlayer insulating film includes

a third contact hole formed at a position corresponding to upper part of said first contact hole, said third contact hole penetrating said interlayer insulating film to be continuous with said first contact hole, and

a fourth contact hole formed at a position corresponding to upper part of said second contact hole, said fourth contact hole penetrating said interlayer insulating film to be continuous with said second contact hole,

said second transparent conductive film of said first stacked film extends into said first contact hole via said third contact hole,

said second transparent conductive film of said second stacked film extends into said second contact hole via said fourth contact hole, and

said third and fourth contact holes have openings larger in a plane than those of said first and second contact holes respectively.

5. The liquid crystal display panel according to claim 1, wherein

said first insulating film includes an organic resin film, and said protective insulating film includes an SiN film.

6. The liquid crystal display panel according to claim 2, wherein

said gate electrode and said common interconnect are made of the same material and arranged in the same layer,

said gate insulating film covers said common interconnect, and

said first contact hole penetrates said gate insulating film to reach a surface of said common interconnect.

7. The liquid crystal display panel according to claim 6, wherein

said signal line is made of the same material as said source electrode, arranged in the same layer as said source electrode, and connected to said source electrode, and

said scanning line is made of the same material as said gate electrode, arranged in the same layer as said gate electrode, and connected to said gate electrode,

said liquid crystal display panel further comprising:

a first pulled-out interconnect and a second pulled-out interconnect arranged in an outer peripheral region of said display region, said first and second pulled-out interconnects extending from said signal line and said scanning line respectively;

a fifth contact hole that penetrates said first insulating film, said protective insulating film and said gate insulating film to reach a surface of said second pulled-out interconnect; and

a sixth contact hole that penetrates said first insulating film and said protective insulating film to reach a surface of said first pulled-out interconnect, wherein

said fifth contact hole has a bottom and an inner side surface covered with said first stacked film composed of said first and second transparent conductive films,

said sixth contact hole has a bottom and an inner side surface covered with said second stacked film composed of said first and second transparent conductive films, and

said first and second pulled-out interconnects are electrically connected to each other via said first and second stacked films.

8. The liquid crystal display panel according to claim 6, wherein

said signal line is made of the same material as said source electrode, arranged in the same layer as said source electrode, and connected to said source electrode, and

said scanning line is made of the same material as said gate electrode, arranged in the same layer as said gate electrode, and connected to said gate electrode,

said liquid crystal display panel further comprising:

a first pulled-out interconnect and a second pulled-out interconnect arranged in an outer peripheral region of said display region, said first and second pulled-out interconnects extending from said signal line and said scanning line respectively;

a first terminal electrode and a second terminal electrode connected to said first and second pulled-out interconnects respectively; and

at least one of a fifth contact hole and a sixth contact hole, said fifth contact hole penetrating said first insulating film, said protective insulating film and said gate insulating film to reach a surface of said second terminal electrode, said sixth contact hole penetrating said first insulating film and said protective insulating film to reach a surface of first terminal electrode, wherein

said fifth contact hole has a bottom and an inner side surface covered with said first stacked film composed of said first and second transparent conductive films, and

said sixth contact hole has a bottom and an inner side surface covered with said second stacked film composed of said first and second transparent conductive films.

9. A method of manufacturing the liquid crystal display panel as recited in claim 2, comprising the steps of:

- (a) forming said first contact hole and said second contact hole simultaneously, said first contact hole being formed so as to penetrate at least said first insulating film and said protective insulating film to reach a surface of said common interconnect, said second contact hole being formed so as to penetrate said first insulating film and said protective insulating film to reach a surface of said drain electrode;
- (b) covering said bottom and said inner side surface of said first contact hole and covering said bottom and said inner side surface of said second contact hole simultaneously with said first transparent conductive film made of the same material as said lower electrode; and
- (c) covering an inner surface of said first contact hole and covering an inner surface of said second contact hole simultaneously with said second transparent conductive film made of the same material as said upper electrode, said respective inner surfaces of said first and second contact holes being covered with said first transparent conductive film.

10. The method according to claim 9, further comprising:

- (d) after said step (a), forming said lower electrode on said first insulating film;

- (e) after said step (d), forming an interlayer insulating film so as to cover said lower electrode from above;

- (f) forming a third contact hole and a fourth contact hole simultaneously, said third contact hole being formed at a position corresponding to upper part of said first contact hole so as to penetrate said interlayer insulating film to be continuous with said first contact hole, said fourth contact hole being formed at a position corresponding to upper part of said second contact hole so as to penetrate said interlayer insulating film to be continuous with said second contact hole; and

- (g) after said step (f), forming said upper electrode on said interlayer insulating film, wherein

performing said step (d) realizes said step (b) simultaneously,

performing said step (g) realizes said step (c) simultaneously, thereby making said second transparent conductive film extend into said first contact hole via said third contact hole and extend into said second contact hole via said fourth contact hole, and

said step (f) includes a step of making said third and fourth contact holes have openings larger in a plane than those of said first and second contact holes respectively.

* * * * *

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摘要(译)

液晶显示面板包括：透明绝缘基板；信号线和扫描线，设置在透明绝缘基板上的显示区域中并以矩阵形式彼此交叉；保护绝缘膜，其布置成至少从上方覆盖信号线和扫描线；从上方覆盖保护绝缘膜的第一绝缘膜；第一接触孔，其至少穿透第一绝缘膜和保护绝缘膜以到达公共互连的表面。第一接触孔具有底部和内侧表面，第一堆叠膜覆盖有由与下电极相同的材料制成的第一透明导电膜和由与上电极相同的材料制成的第二透明导电膜。

