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(54) **METHOD FOR DRIVING LIQUID CRYSTAL DISPLAY DEVICE**

(71) Applicant: **Semiconductor Energy Laboratory Co., Ltd.**, Atsugi-shi (JP)

(72) Inventor: **Hiroyuki MIYAKE**, Atsugi (JP)

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(30) **Foreign Application Priority Data**

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(57) **ABSTRACT**

An object is to suppress deterioration of a displayed image even when a refresh rate is reduced in displaying a still image. A liquid crystal display device includes a pixel transistor electrically connected to a pixel electrode, and a capacitor having one electrode electrically connected to the pixel electrode and the other electrode electrically connected to a capacitor line. The pixel transistor is turned on and a voltage based on an image signal is supplied to the pixel electrode, and then, the pixel transistor is turned off so that a holding period during which the pixel electrode holds the voltage based on the image signal starts. A holding signal corresponding to change of the voltage based on the image signal in the pixel electrode in the holding period is supplied to the capacitor line so that a potential of the pixel electrode is constant.

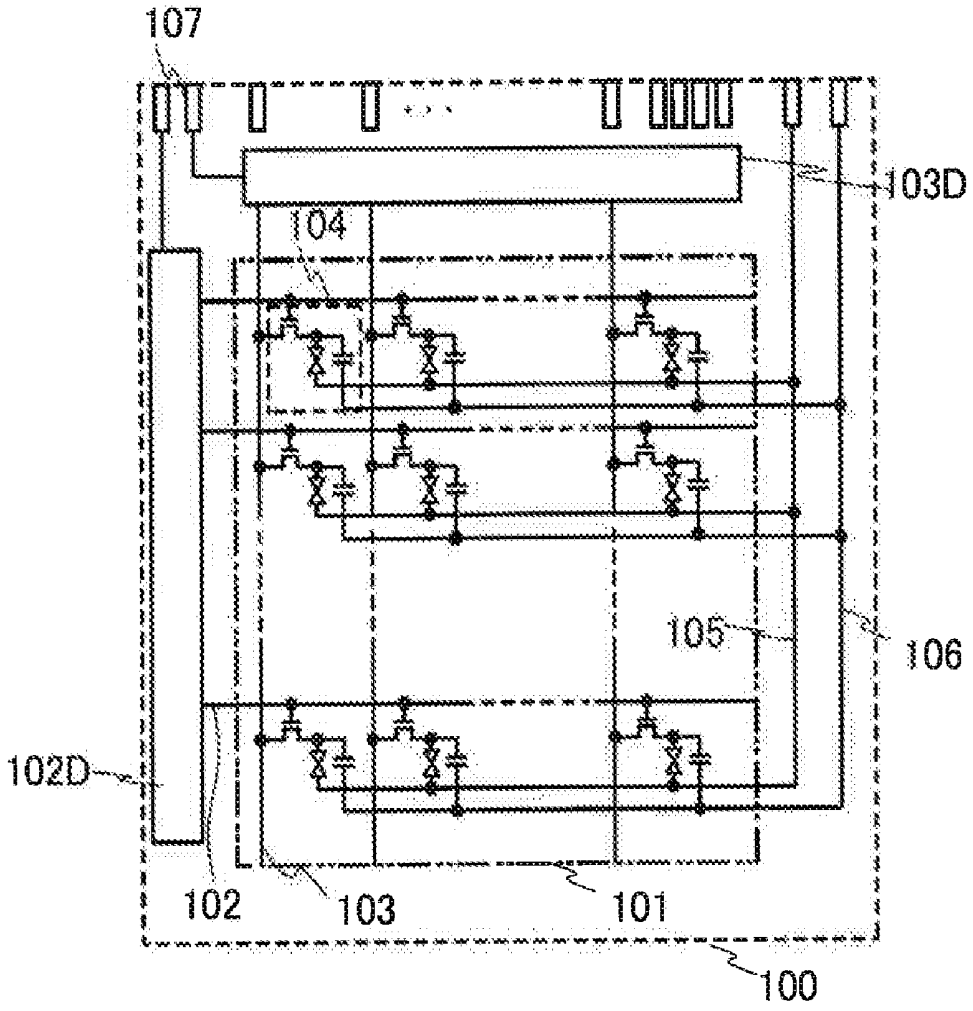


FIG. 1A

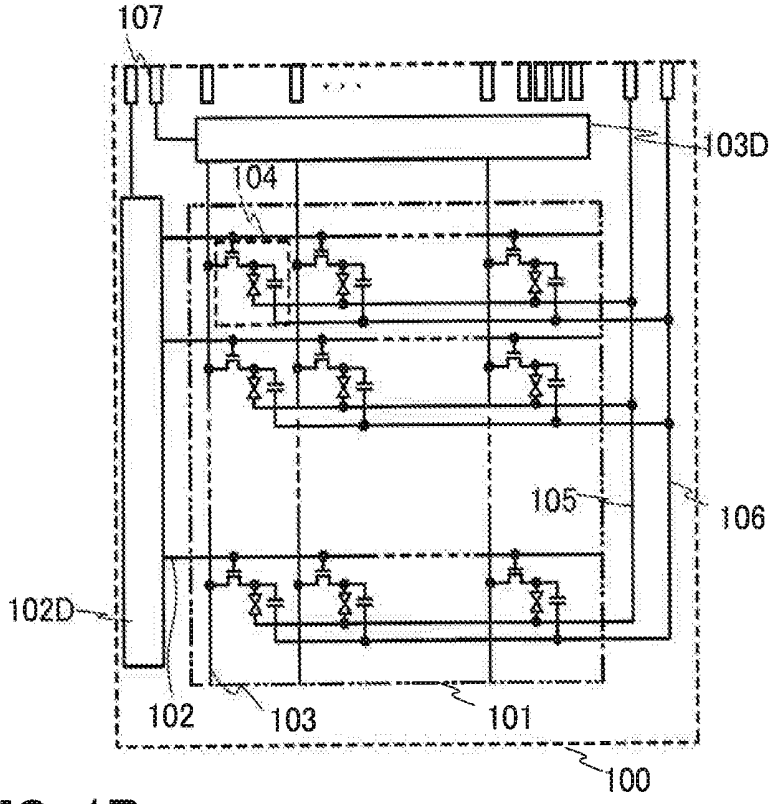


FIG. 1B

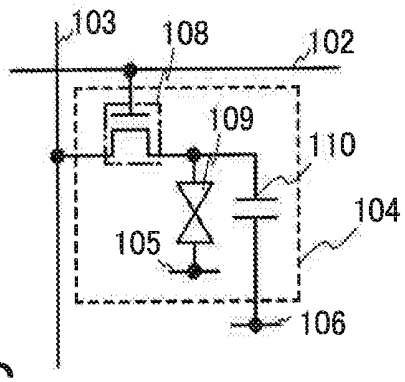


FIG. 1C

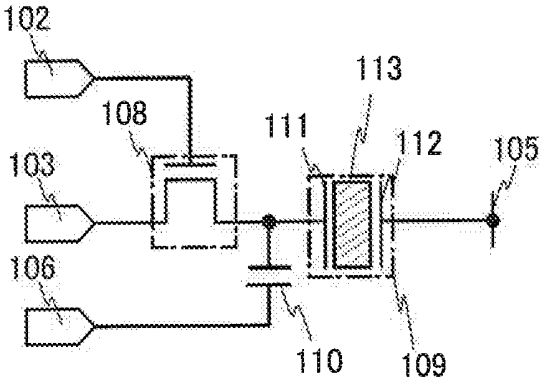


FIG. 2A

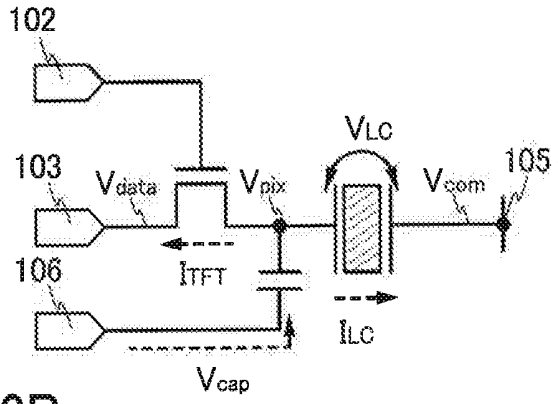

102
103
106
Vdata
Vpix
VLC
Vcom
105
ITFT
ILC
Vcap

FIG. 2B

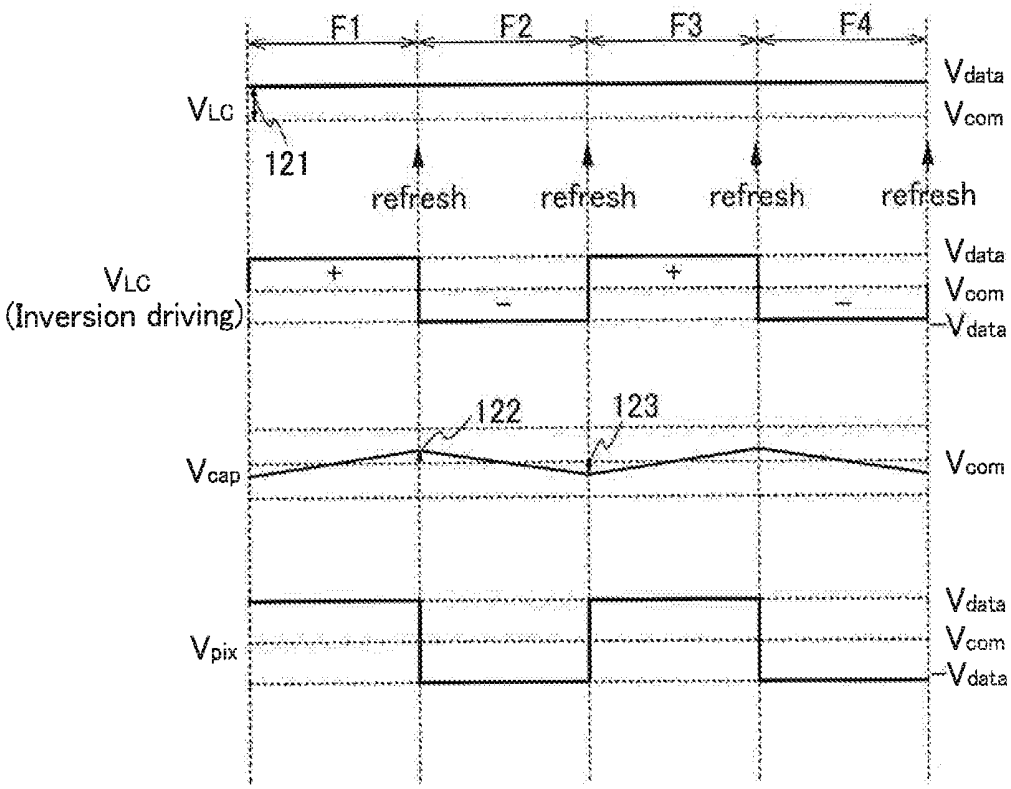

F1
F2
F3
F4
Vdata
VLC
Vcom
121
refresh
refresh
refresh
refresh
VLC
(Inversion driving)
+
−
+
−
Vdata
Vcom
Vdata
122
123
Vcap
Vcom
Vdata
Vpix
Vcom
Vdata

FIG. 3

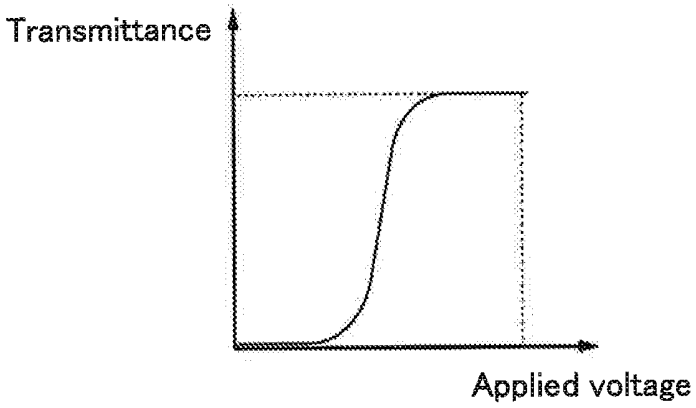


FIG. 4

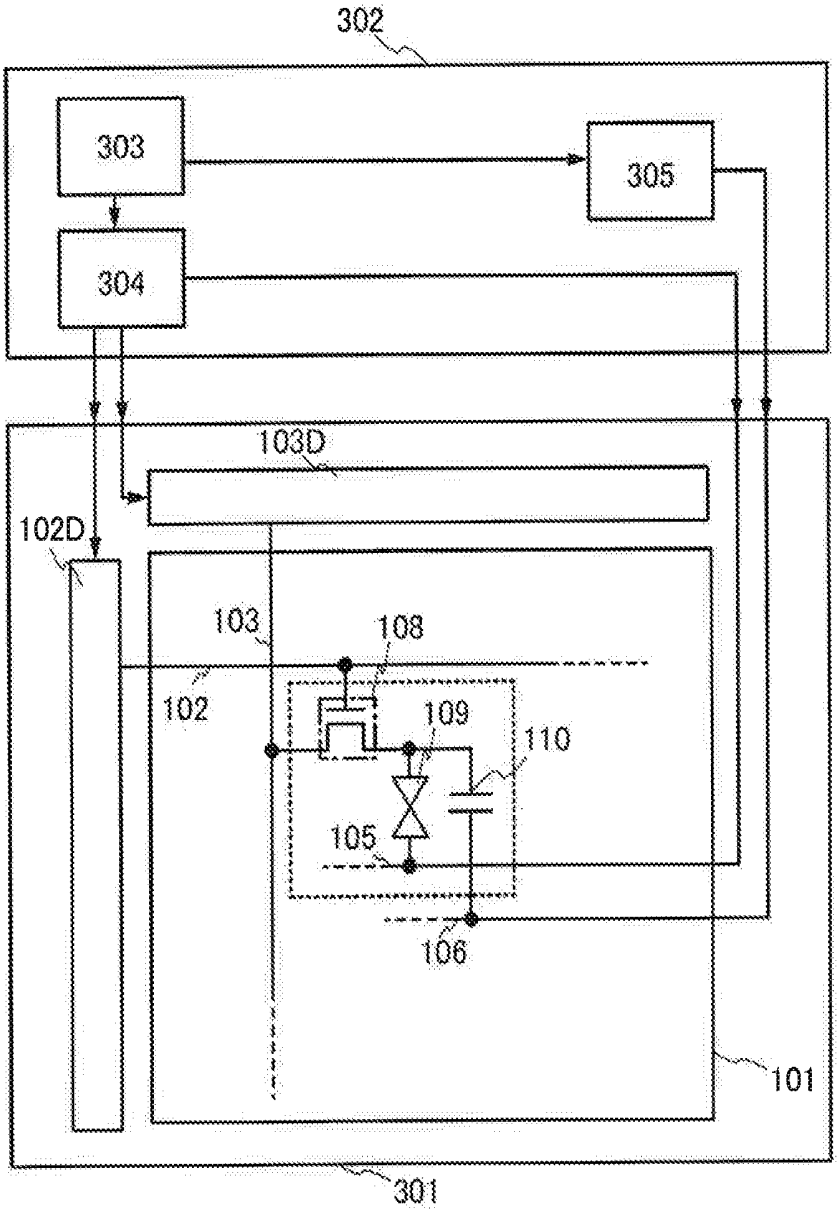


FIG. 5

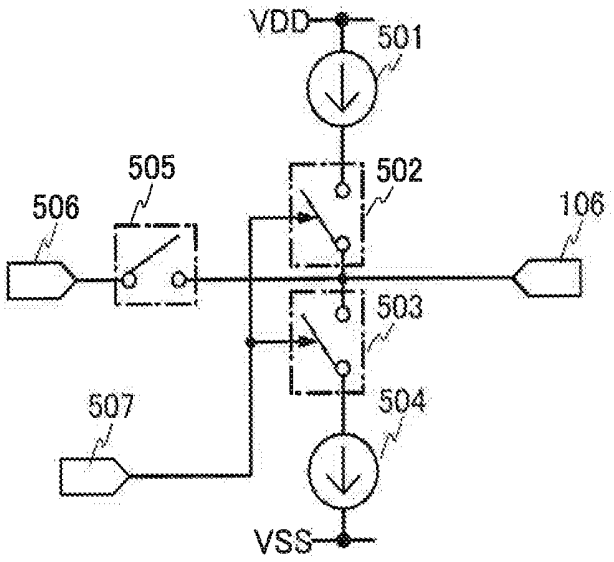


FIG. 6A

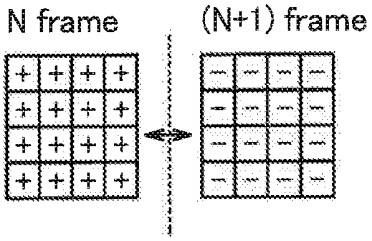


FIG. 6B

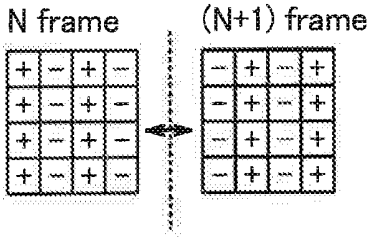


FIG. 6C

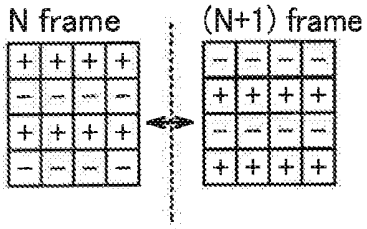


FIG. 6D

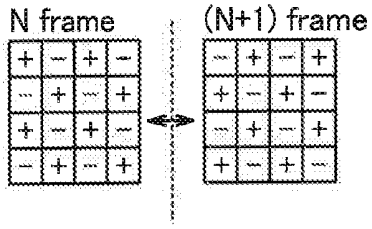


FIG. 7A

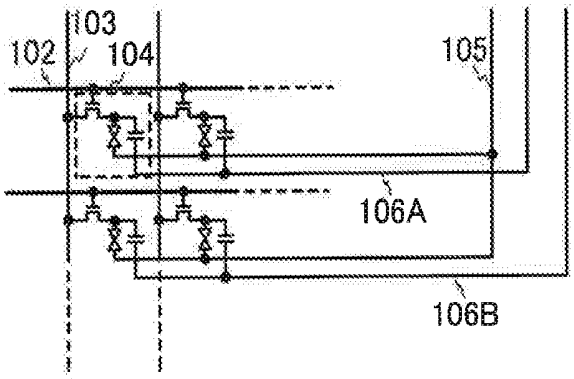


FIG. 7B

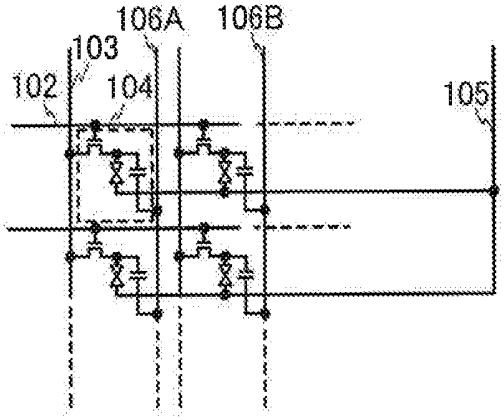


FIG. 7C

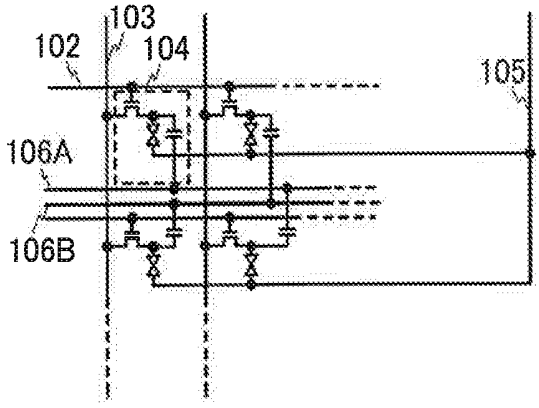


FIG. 8A

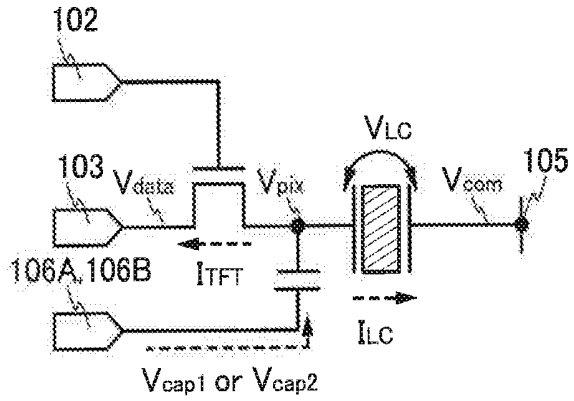

102
103
Vdata
Vpix
VLC
Vcom
105
106A,106B
ITFT
ILC
Vcap1 or Vcap2

FIG. 8B

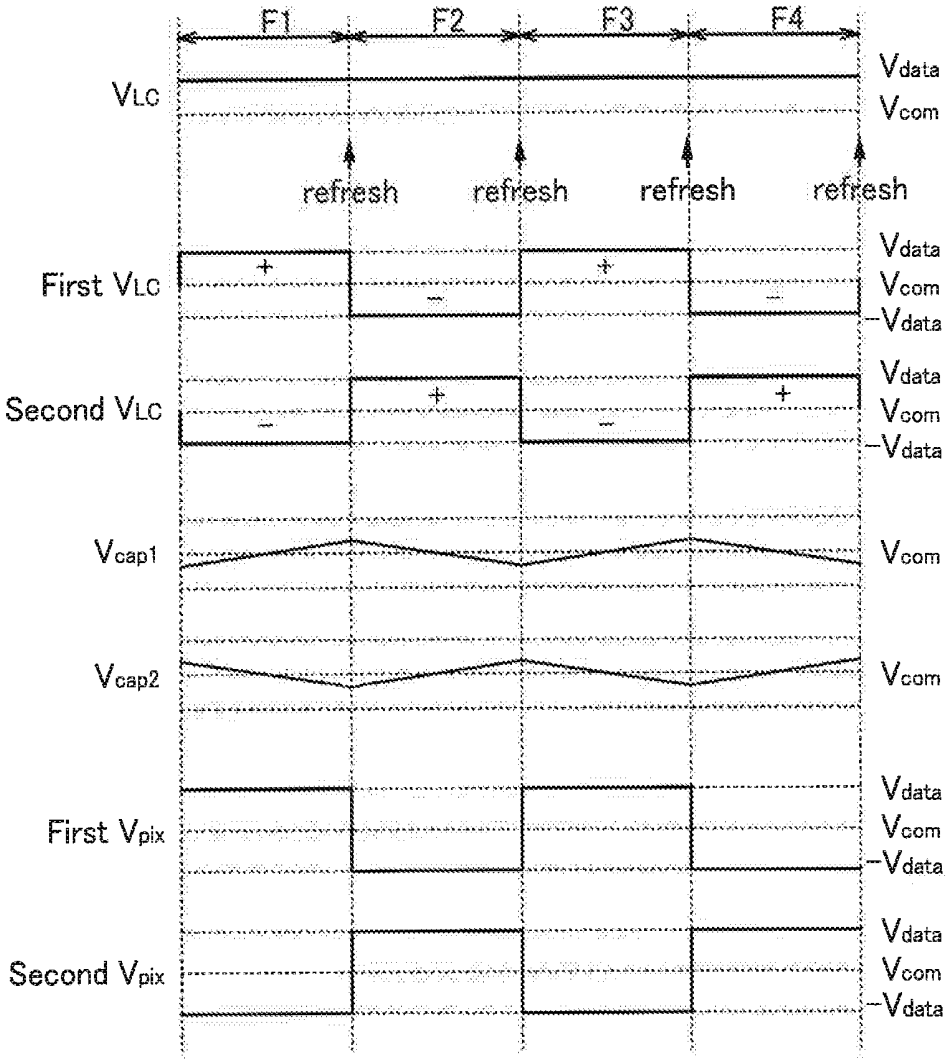

F1
F2
F3
F4
VLC
Vdata
Vcom
refresh
refresh
refresh
refresh
First VLC
Second VLC
Vcap1
Vcap2
First Vpix
Second Vpix
+
−
−Vdata

FIG. 9A

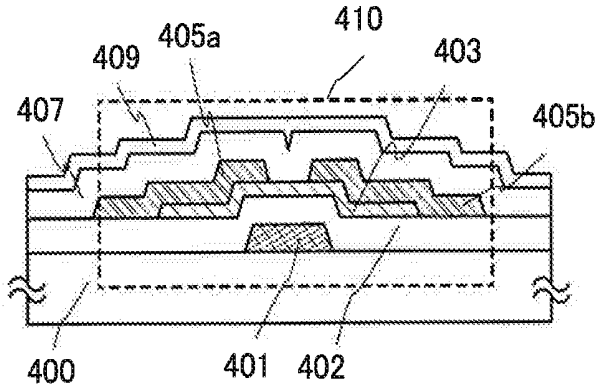


FIG. 9B

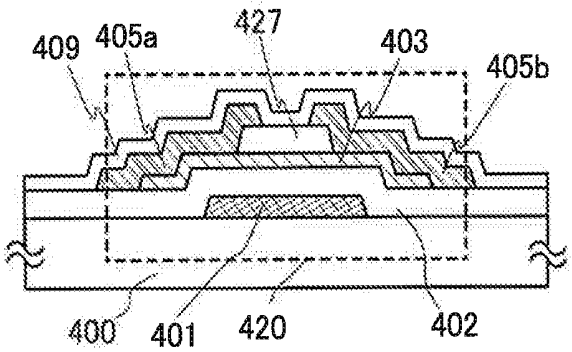


FIG. 9C

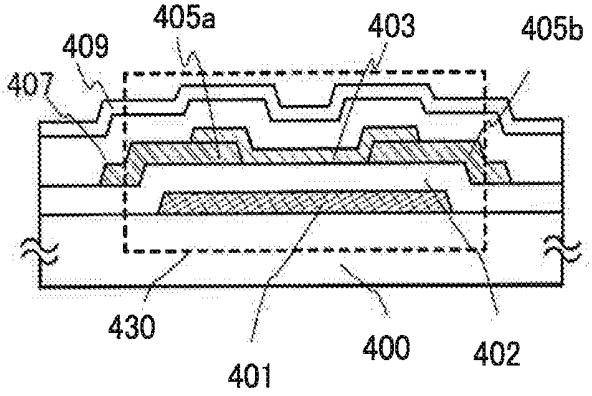
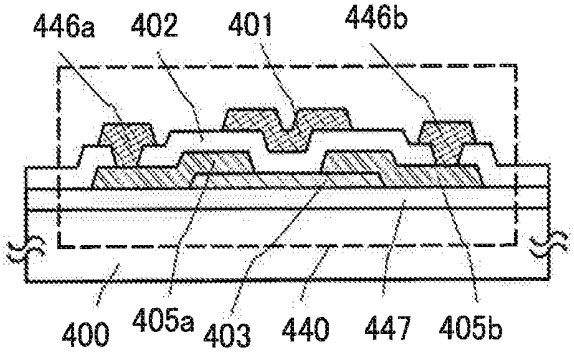


FIG. 9D



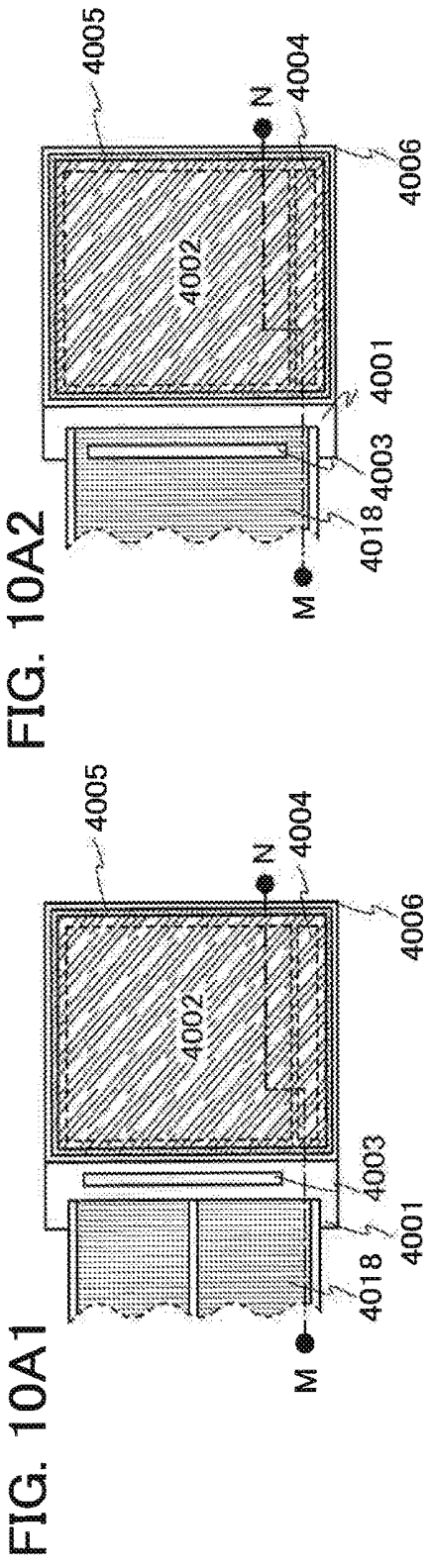


FIG. 10A1

FIG. 10A2

FIG. 10B

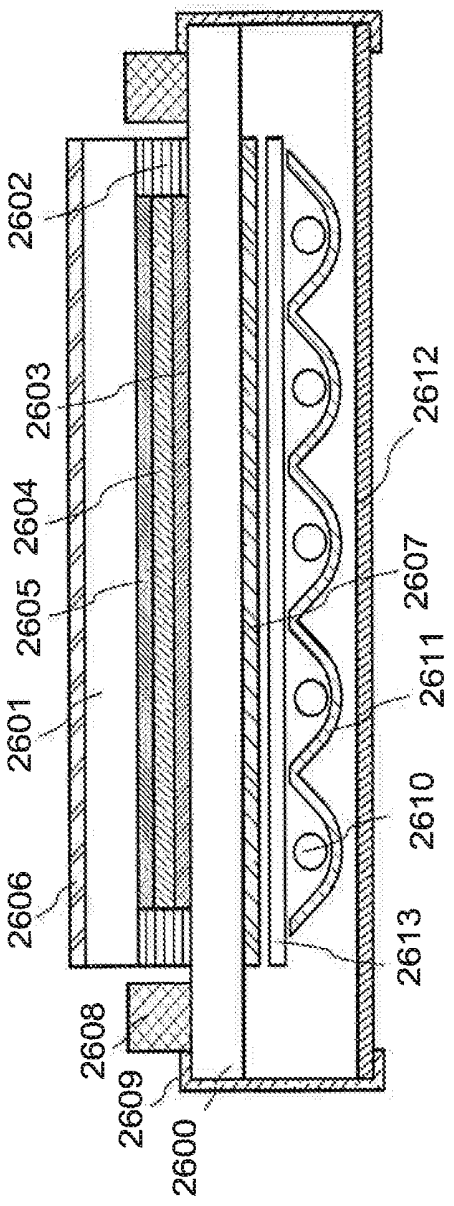

2602
2603
2604
2605
2601
2606
2608
2609
2600
2612
2607
2611
2610
2613

FIG. 11

FIG. 12A

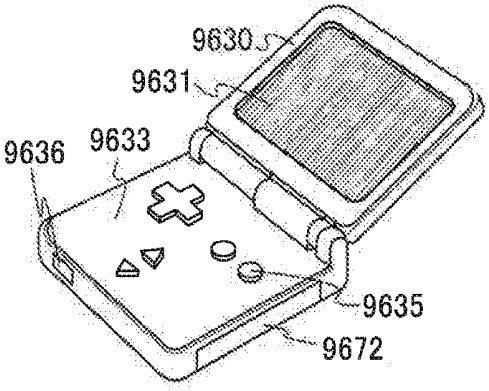


FIG. 12B

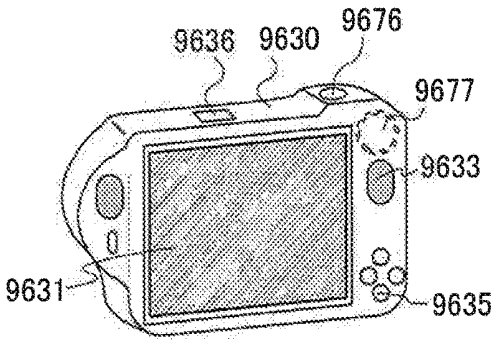


FIG. 12C

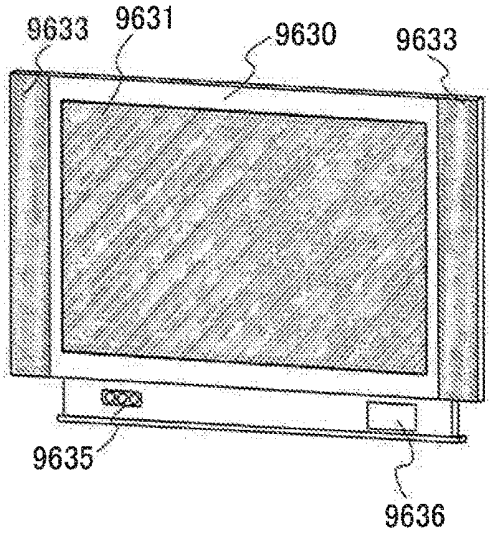


FIG. 12D

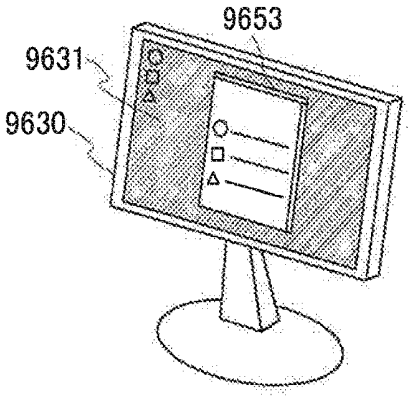


FIG. 13A

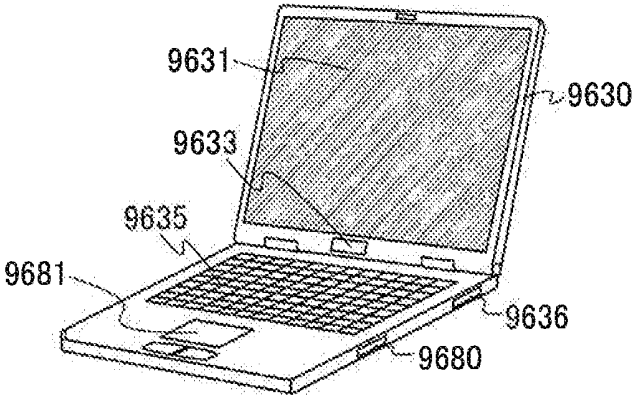


FIG. 13B

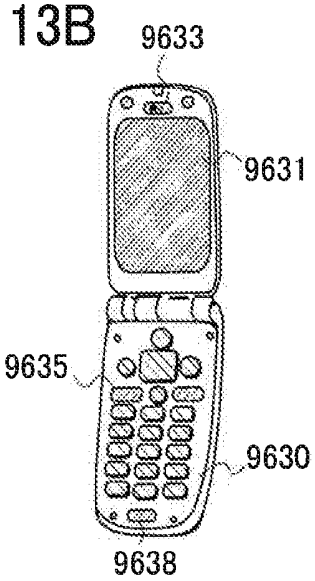


FIG. 13C

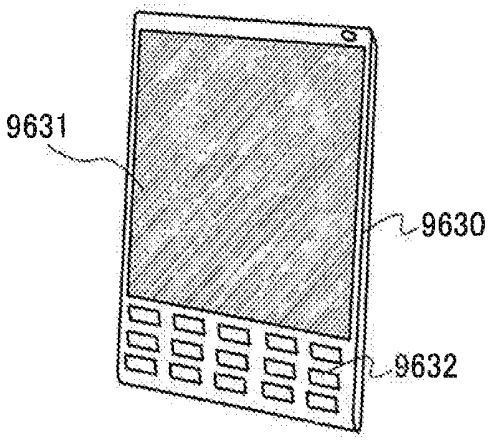


FIG. 13D

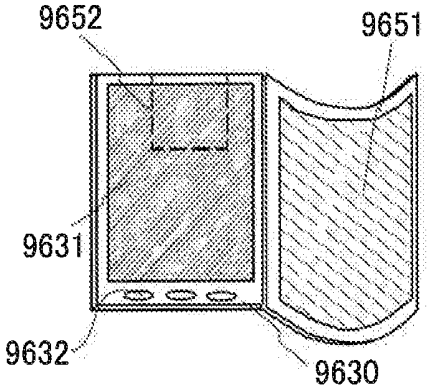


FIG. 14A

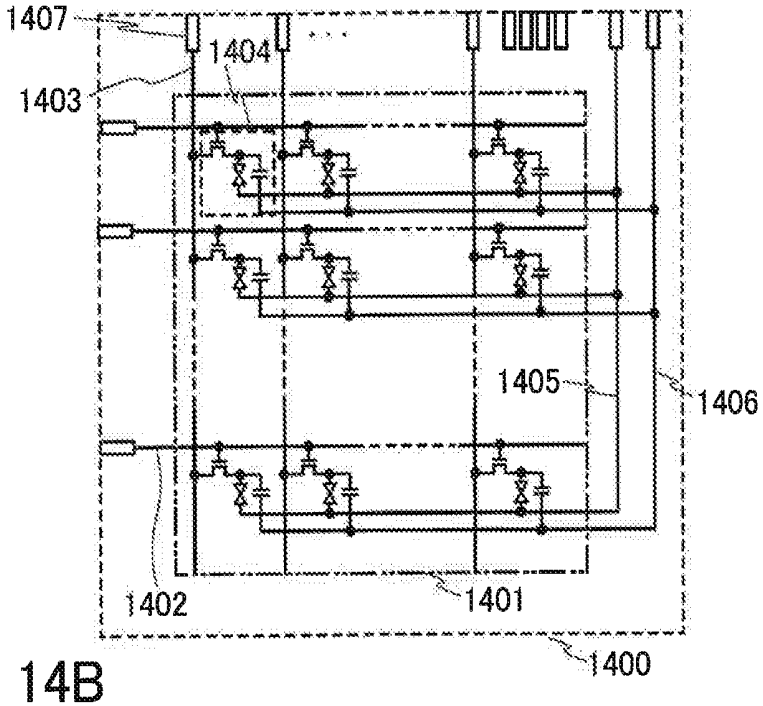


FIG. 14B

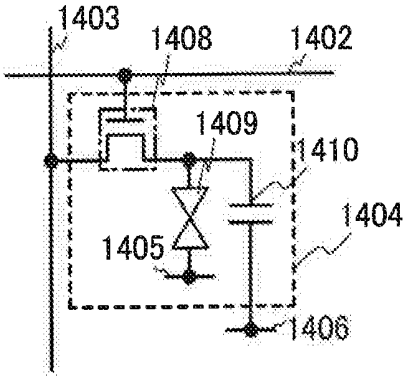


FIG. 14C

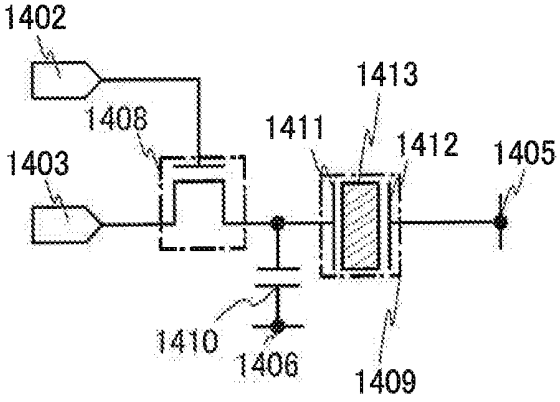


FIG. 15A

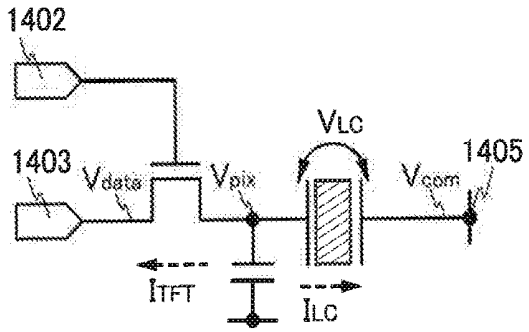
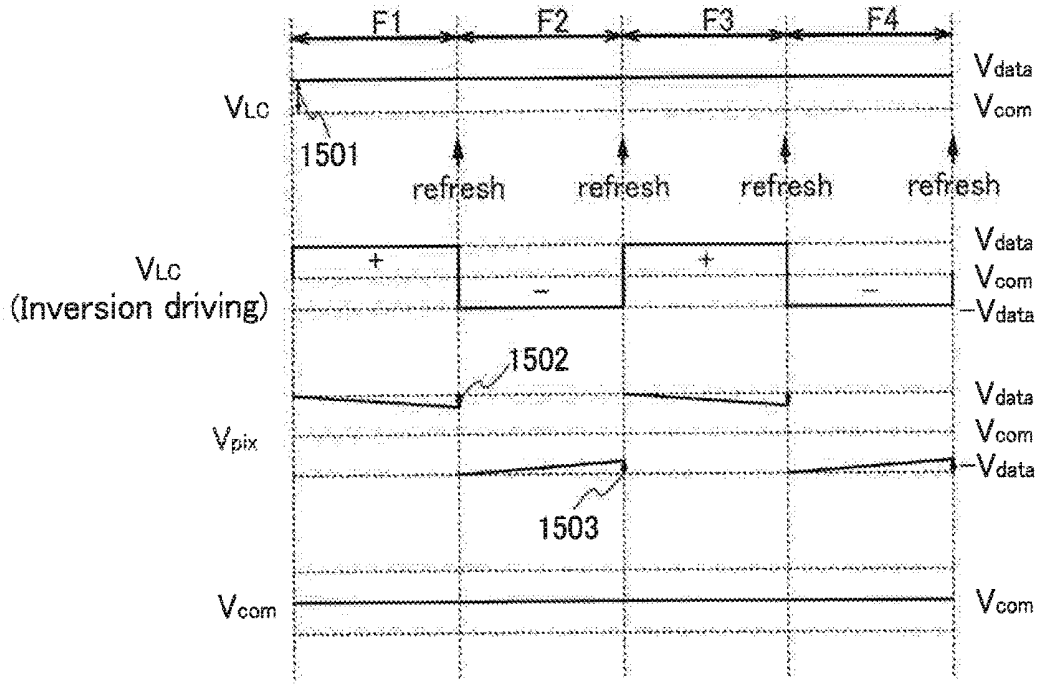


FIG. 15B



METHOD FOR DRIVING LIQUID CRYSTAL DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 12/976,431, filed Dec. 22, 2010, now allowed, which claims the benefit of a foreign priority application filed in Japan as Serial No. 2009-295608 on Dec. 25, 2009, both of which are incorporated by reference.

TECHNICAL FIELD

[0002] The present invention relates to a method for driving a liquid crystal display device, a liquid crystal display device, or an electronic device including a liquid crystal display device.

BACKGROUND ART

[0003] Liquid crystal display devices are widely used in large display devices such as television sets and small display devices such as mobile phones. Higher value-added devices have been demanded and the development has progressed. In recent years, attention is attracted to the development of low power consumption liquid crystal display devices, in terms of the increase in interest in global environment and improvement in convenience of mobile devices.

[0004] Non-Patent Document 1 discloses a structure in which the refresh rate in the case of displaying a moving image and that in the case of displaying a still image are different from each other in order to reduce power consumption of a liquid crystal display device. Moreover, Non-Patent Document 1 discloses a structure in which, in order to prevent flickers from being perceived with change in drain-common voltage due to switching of signals in a break period and a scanning period when a still image is displayed, alternating-current signals with the same phase are applied to a signal line and a common electrode also in a break period so that the drain-common voltage does not change.

REFERENCE

[0005] Non-Patent Document 1: Kazuhiko Tsuda, et al., "Ultra low power consumption technologies for mobile TFT-LCDs", IDW'02, pp. 295-298 (2002)

DISCLOSURE OF INVENTION

[0006] As in Non-Patent Document 1, lower power consumption can be realized by a reduction in refresh rate. However, a voltage between a pixel electrode and a common electrode cannot be kept constant in some cases because the potential of the pixel electrode is changed by the off-state current of a pixel transistor and/or leakage current from liquid crystals. Therefore, a displayed image deteriorates because a voltage applied to the liquid crystals is changed.

[0007] An object is described in detail, using a specific example shown in drawings. FIG. **14**A is a schematic diagram of a display panel in a liquid crystal display device. A display panel **1400** in FIG. **14**A includes a pixel portion **1401**, a gate line (also referred to as a scan line) **1402**, a signal line (also referred to as a data line) **1403**, a pixel **1404**, a common electrode **1405**, a capacitor line **1406**, and a terminal portion **1407**.

[0008] FIG. **14**B illustrates the pixel **1404** in FIG. **14**A. The pixel **1404** includes a pixel transistor **1408**, a liquid crystal element **1409**, and a capacitor **1410**. A gate of the pixel transistor **1408** is connected to the gate line **1402**. A first terminal serving as one of a source and a drain of the pixel transistor **1408** is connected to the signal line **1403**. A second terminal serving as the other of the source and the drain of the pixel transistor **1408** is connected to one electrode of the liquid crystal element **1409** and a first electrode of the capacitor **1410**. The other electrode of the liquid crystal element **1409** is connected to the common electrode **1405**. A second electrode of the capacitor **1410** is connected to the capacitor line **1406**. Note that the pixel transistor **1408** is a thin film transistor (TFT) including a thin semiconductor layer.

[0009] FIG. **14**C illustrates the pixel **1404** in a manner different from FIG. **14**B in order to focus on each of the wirings and the elements. The reference numerals of the wirings and the elements are the same as those in FIG. **14**B. Note that for description of the liquid crystal element **1409**, FIG. **14**C illustrates a pixel electrode **1411** as the electrode on the pixel transistor **1408** side, a counter electrode **1412** as the electrode on the common electrode **1405** side, and a liquid crystal **1413** placed between the pixel electrode **1411** and the counter electrode **1412**.

[0010] FIG. **15**A illustrates the same diagram as FIG. **14**C and focuses on a potential of each wiring, a voltage between electrodes, and a current flowing through each element. An image signal supplied to the signal line **1403** is a voltage V_{data}. A voltage held in the pixel electrode **1411** is V_{pix}. A voltage of the counter electrode **1412** is V_{com}. A voltage applied to the liquid crystal **1413** is V_{LC}. FIG. **15**A also illustrates an off-state current I_{TFT} of the pixel transistor and a current I_{LC} flowing through the liquid crystal.

[0011] FIG. **15**B is a general timing chart showing the potential of each wiring and the voltage between electrodes illustrated in FIG. **15**A. In the timing chart in FIG. **15**B, a period is divided into periods F**1** to F**4**. The following description is made on the assumption that the same image, that is, a still image is displayed in the periods F**1** to F**4**. That is, in the periods F**1** to F**4**, the voltage V_{LC} applied to the liquid crystal **1413** is a constant voltage V_{data} (indicated by an arrow **1501** in FIG. **15**B). It is known that the liquid crystal element **1409** deteriorates by application of voltage in one direction to the liquid crystal **1413**, and that inversion driving is commonly used in which the polarity of voltage applied to the liquid crystal element **1409** is inverted per predetermined period. For example, when inversion driving is performed in the periods F**1** to F**4**, a voltage whose polarity is changed per predetermined period, such as V_{LC} (inversion driving) in FIG. **15**B, is applied to the liquid crystal element **1409** even when the same image is displayed.

[0012] When the refresh rate is reduced in order to decrease power consumption in displaying a still image, each of the periods F**1** to F**4** is extended. As the period is extended, the voltage (V_{pix}) held in the pixel electrode **1411** is changed to rise or fall from V_{data} (indicated by an arrow **1502** or an arrow **1503** in FIG. **15**B) due to the off-state current I_{TFT} and/or the current I_{LC} flowing through the liquid crystal. On the other hand, the voltage V_{com} of the counter electrode **1412** is fixed. The voltage V_{LC} that is actually applied to the liquid crystal **1413** is significantly changed at the boundary between the periods F**1** to F**4** (denoted by

"refresh" in FIG. **15**B), which contributes to image deterioration when a still image is displayed.

[0013] In view of the above, an object of one embodiment of the present invention is to suppress deterioration of a displayed image even when a refresh rate is reduced in displaying a still image.

[0014] One embodiment of the present invention is a method for driving a liquid crystal display device. The liquid crystal display device includes a pixel transistor electrically connected to a pixel electrode, and a capacitor having one of electrodes electrically connected to the pixel electrode and the other of the electrodes electrically connected to a capacitor line. The pixel transistor is turned on and a voltage based on an image signal is supplied to the pixel electrode, and then, the pixel transistor is turned off so that a holding period during which the pixel electrode holds the voltage based on the image signal starts. A holding signal corresponding to change of the voltage based on the image signal in the pixel electrode in the holding period is supplied to the capacitor line so that a potential of the pixel electrode is constant.

[0015] One embodiment of the present invention is a method for driving a liquid crystal display device. The liquid crystal display device includes a pixel transistor electrically connected to a pixel electrode, and a capacitor having one of electrodes electrically connected to the pixel electrode and the other of the electrodes electrically connected to a capacitor line. The pixel transistor is turned on and a voltage based on an image signal is supplied to the pixel electrode, and then, the pixel transistor is turned off so that a holding period during which the pixel electrode holds the voltage based on the image signal starts. When the voltage based on the image signal in the pixel electrode rises in the holding period, a holding signal for controlling so as to lower the voltage based on the image signal is supplied to the capacitor line so that a potential of the pixel electrode is constant.

[0016] One embodiment of the present invention is a method for driving a liquid crystal display device. The liquid crystal display device includes a pixel transistor electrically connected to a pixel electrode, and a capacitor having one of electrodes electrically connected to the pixel electrode and the other of the electrodes electrically connected to a capacitor line. The pixel transistor is turned on and a voltage based on an image signal is supplied to the pixel electrode, and then, the pixel transistor is turned off so that a holding period during which the pixel electrode holds the voltage based on the image signal starts. When the voltage based on the image signal in the pixel electrode falls in the holding period, a holding signal for controlling so as to raise the voltage based on the image signal is supplied to the capacitor line so that a potential of the pixel electrode is constant.

[0017] In the method for driving a liquid crystal display device according to one embodiment of the present invention, a semiconductor layer of the pixel transistor may be an oxide semiconductor.

[0018] In the method for driving a liquid crystal display device according to one embodiment of the present invention, the holding period may be 60 seconds or longer.

[0019] In the method for driving a liquid crystal display device according to one embodiment of the present invention, the liquid crystal display device may be driven with frame inversion driving, common inversion driving, source line inversion driving, gate line inversion driving, or dot inversion driving per frame period.

[0020] According to one embodiment of the present invention, deterioration of a displayed image can be suppressed even when the refresh rate is reduced in displaying a still image.

BRIEF DESCRIPTION OF DRAWINGS

[0021] In the accompanying drawings:

[0022] FIGS. **1**A to **1**C each illustrate a diagram for explaining a circuit diagram of one embodiment of the present invention;

[0023] FIGS. **2**A and **2**B are diagrams for explaining a timing chart of one embodiment of the present invention;

[0024] FIG. **3** illustrates a diagram for explaining an example of properties of a liquid crystal in one embodiment of the present invention;

[0025] FIG. **4** illustrates a diagram for explaining a block diagram of one embodiment of the present invention;

[0026] FIG. **5** illustrates a diagram for explaining a circuit diagram of one embodiment of the present invention;

[0027] FIGS. **6**A to **6**D each illustrate a diagram for explaining a schematic diagram of one embodiment of the present invention;

[0028] FIGS. **7**A to **7**C each illustrate a diagram for explaining a circuit diagram of one embodiment of the present invention;

[0029] FIGS. **8**A and **8**B are diagrams for explaining a timing chart of one embodiment of the present invention;

[0030] FIGS. **9**A to **9**D each illustrate a diagram for explaining a transistor of one embodiment of the present invention;

[0031] FIGS. **10**A**1**, **10**A**2**, and **10**B each illustrate a diagram for explaining a liquid crystal display device of one embodiment of the present invention;

[0032] FIG. **11** illustrates a diagram for explaining a liquid crystal display device of one embodiment of the present invention;

[0033] FIGS. **12**A to **12**D each illustrate a diagram for explaining an electronic device of one embodiment of the present invention;

[0034] FIGS. **13**A to **13**D each illustrate a diagram for explaining an electronic device of one embodiment of the present invention;

[0035] FIGS. **14**A to **14**C are diagrams for explaining an object; and

[0036] FIGS. **15**A and **15**B are diagrams for explaining an object.

BEST MODE FOR CARRYING OUT THE INVENTION

[0037] Embodiments of the present invention will be described below with reference to the accompanying drawings. Note that the present invention can be carried out in many different modes, and it is easily understood by those skilled in the art that modes and details of the present invention can be modified in various ways without departing from the spirit and the scope of the present invention. Therefore, the present invention is not construed as being limited to the following description of the embodiments. Note that in structures of the present invention described below, reference numerals denoting the same portions are used in common in different drawings.

[0038] Note that the size of a component, the thickness of a layer, a region, or distortion of signal waveform illustrated

in drawings in embodiments is exaggerated for simplicity in some cases. Therefore, embodiments of the present invention are not limited to such scales.

[0039] Note that terms "first", "second", "third" to "Nth" (N is a natural number) employed in this specification are used in order to avoid confusion between components and do not set a limitation on number.

Embodiment 1

[0040] For explaining this embodiment, FIG. **1**A illustrates a schematic diagram of a display panel in a liquid crystal display device. A display panel **100** in FIG. **1**A includes a pixel portion **101**, a gate line (also referred to as a scan line) **102**, a signal line (also referred to as a data line) **103**, a pixel **104**, a common electrode **105**, a capacitor line **106**, a terminal portion **107**, a gate line driver circuit **102**D, and a signal line driver circuit **103**D.

[0041] Note that FIG. **1**A illustrates the structure in which the gate line driver circuit **102**D and the signal line driver circuit **103**D are provided over the display panel **100**; as in FIG. **14**A, the gate line driver circuit **102**D and the signal line driver circuit **103**D are not necessarily provided over the display panel **100**. When the gate line driver circuit **102**D and the signal line driver circuit **103**D are provided over the display panel **100**, the number of terminals in the terminal portion **107** can be reduced and the size of the liquid crystal display device can be reduced.

[0042] The pixels **104** are arranged (placed) in matrix. Here, the expression "pixels are arranged (placed) in matrix" includes the case where the pixels are arranged in a straight line and the case where the pixels are arranged in a jagged line, in a longitudinal direction or a lateral direction. Accordingly, in the case of performing full color display with three color elements (e.g., RGB), the expression "pixels are arranged (placed) in matrix" also includes the case where pixels are arranged in stripes and the case where dots of the three color elements are arranged in a delta pattern.

[0043] FIG. **1**B illustrates the pixel **104** in FIG. **1**A. The pixel **104** includes a pixel transistor **108**, a liquid crystal element **109**, and a capacitor **110**. A gate of the pixel transistor **108** is connected to the gate line **102**. A first terminal serving as one of a source and a drain of the pixel transistor **108** is connected to the signal line **103**. A second terminal serving as the other of the source and the drain of the pixel transistor **108** is connected to one electrode of the liquid crystal element **109** and a first electrode of the capacitor **110**. The other electrode of the liquid crystal element **109** is connected to the common electrode **105**. A second electrode of the capacitor **110** is connected to the capacitor line **106**. Note that the pixel transistor **108** is a thin film transistor (TFT) including a thin semiconductor layer.

[0044] Note that when it is explicitly described that "A and B are connected," the case where A and B are electrically connected, the case where A and B are functionally connected, and the case where A and B are directly connected are included therein.

[0045] Note that as the pixel transistor **108**, a thin film transistor (TFT) including amorphous silicon, polycrystalline silicon, microcrystalline (also referred to as microcrystal or semi-amorphous) silicon, or single crystal silicon can be used. A transistor including a compound semiconductor or an oxide semiconductor such as ZnO, a-InGaZnO, SiGe, or GaAs; a thin film transistor obtained by thinning such a compound semiconductor or oxide semiconductor; or the like can be used. Accordingly, the manufacturing temperature can be lowered and for example, such a transistor can be formed at room temperature.

[0046] Note that one pixel corresponds to one element whose brightness can be controlled. Therefore, for example, one pixel corresponds to one color element and brightness is expressed with one color element. Accordingly, in the case of a color display device having color elements of R (Red), G (Green), and B (Blue), a minimum unit of an image is composed of three pixels of an R pixel, a G pixel, and a B pixel. Note that a color that is different from R, G, and B may be used for a color element. For example, three pixels of yellow, cyan, and magenta may be used.

[0047] Note that a thin film transistor is an element having at least three terminals of gate, drain, and source. The thin film transistor includes a channel region between a drain region and a source region, and a current can flow through the drain region, the channel region, and the source region. Here, since the source and the drain of the transistor may change depending on the structure, the operating condition, and the like of the transistor, it is difficult to define which is a source or a drain. Therefore, in this document (the specification, the claims, the drawings, and the like), a region functioning as a source or a drain is not called a source or a drain in some cases. In such a case, for example, one of the source and the drain is referred to as a first terminal, a first electrode, or a source region and the other of the source and the drain is referred to as a second terminal, a second electrode, or a drain region in some cases.

[0048] FIG. **1**C illustrates the pixel **104** in a manner different from FIG. **1**B in order to focus on each of the wirings and the elements. The reference numerals of the wirings and the elements are the same as those in FIG. **1**B. Note that for description of the liquid crystal element **109**, FIG. **1**C illustrates a pixel electrode **111** as the electrode on the pixel transistor **108** side, a counter electrode **112** as the electrode on the common electrode **105** side, and a liquid crystal **113** placed between the pixel electrode **111** and the counter electrode **112**. FIG. **1**C differs from FIG. **14**C in that instead of supplying a fixed voltage to the capacitor line **106** connected to the second electrode of the capacitor **110**, a signal whose voltage is changed per predetermined period is supplied to the second electrode of the capacitor **110**.

[0049] FIG. **2**A illustrates the same diagram as FIG. **1**C, and focuses on a potential of each wiring, a voltage between electrodes, and a current flowing through each element as in FIG. **15**A. An image signal supplied to the signal line **103** is a voltage V_{data}. A signal supplied to the capacitor line **106** (a holding signal) is a voltage V_{cap}. A voltage held in the pixel electrode **111** is V_{pix}. A voltage of the counter electrode **112** is V_{com}. A voltage applied to the liquid crystal **113** is V_{LC}. FIG. **2**A also illustrates an off-state current I_{TFT} of the pixel transistor and a current I_{LC} flowing through the liquid crystal **113**.

[0050] Specifically, there is a period during which the pixel transistor is turned on and the voltage V_{data} based on an image signal is supplied to the pixel electrode **111** in order to write an image signal into a pixel (the period is hereinafter referred to as a writing period), and a voltage held in the pixel electrode **111** is V_{pix}. The voltage V_{pix} is held by turning off the pixel transistor. Note that in a period for holding V_{pix} (hereinafter referred to as a holding period), V_{pix} is changed to rise or fall because of the off-state current I_{TFT} and/or the current I_{LC}; thus, it is necessary to regularly

perform refresh operation. Note that a writing period and a holding period can be collectively referred to as one frame period.

[0051] Note that in this specification, a writing period is extremely shorter than a holding period. For that reason, in some cases, a writing period is not shown in a timing chart and a holding period is described as one frame period.

[0052] When a thin film transistor in which an oxide semiconductor is used for a semiconductor layer is used as the pixel transistor, the off-state current I_{TFT} can be extremely reduced. Thus, it is possible to obtain a structure in which only the current I_{LC} flowing through the liquid crystal **113** is largely contributed to change in voltage V_{pix}. As a result, the holding period can be drastically extended to 60 seconds or more, and the refresh rate can be significantly reduced.

[0053] Note that voltage often refers to a potential difference between a given potential and a reference potential (e.g., a ground potential). Accordingly, voltage, potential, and potential difference can be referred to as potential, voltage, and voltage difference, respectively.

[0054] Like FIG. **15**B, FIG. **2**B illustrates a general timing chart showing the potential of each wiring and the voltage between electrodes illustrated in FIG. **2**A. In the timing chart in FIG. **2**B, a period is divided into periods F**1** to F**4**. The following description is made on the assumption that the same image, that is, a still image is displayed in the periods F**1** to F**4**. That is, in the periods F**1** to F**4**, the voltage V_{LC} applied to the liquid crystal **113** is a constant voltage V_{data}, (indicated by an arrow **121** in FIG. **2**B). It is known that the liquid crystal element **109** deteriorates by application of voltage in one direction to the liquid crystal **113**, and that inversion driving is commonly used in which the polarity of voltage applied to the liquid crystal element is inverted per predetermined period. For example, frame inversion driving is realized when each of the periods F**1** to F**4** is regarded as one frame period and inversion driving is performed per frame period; a voltage whose polarity is changed per predetermined period, such as V_{LC} (inversion driving) in FIG. **2**B, is applied to the liquid crystal element even when the same image is displayed.

[0055] When the refresh rate is reduced in order to decrease power consumption in displaying a still image, each of the periods F**1** to F**4** is extended. As the period is extended, the voltage V_{pix} held in the pixel electrode **111** rises or falls because of the off-state current I_{TFT} and/or the current I_{LC} flowing through the liquid crystal, as described in FIG. **15**B.

[0056] In the structure in this embodiment, image deterioration in displaying a still image is reduced in such a manner that the holding signal V_{cap} compensates a voltage corresponding to the amount of rise or fall from V_{data} of the voltage (V_{pix}) held in the pixel electrode **111** due to the off-state current I_{TFT} and/or the current I_{LC} flowing through the liquid crystal. Specifically, in the periods F**1** to F**4** each of which is one frame period, the voltage of the holding signal V_{cap} is raised or lowered by the amount of change in voltage V_{pix}. (indicated by an arrow **122** or an arrow **123** in FIG. **2**B). In other words, the voltage of the holding signal V_{cap} is lowered when the voltage V_{pix} is changed to rise, whereas the voltage of the holding signal V_{cap} is raised when the voltage V_{pix} is changed to fall. The voltage V_{LC} applied between the voltage V_{pix} and the voltage V_{com} of the counter electrode **112** which is a fixed voltage is not much changed at the boundary between the periods F**1** to F**4** (denoted by "refresh" in FIG. **2**B), and image deterioration in displaying a still image can be reduced. Note that V_{LC} (inversion driving) is a voltage that is inverted in each of the periods F**1** to F**4**, so that V_{cap} is a signal that alternately repeats rise and fall. Note that the reduction in change of V_{pix}, that is, V_{LC} by control of the voltage of the holding signal V_{cap} as described above can be referred to as "making the voltage V_{pix}, that is, the voltage V_{LC} constant"; it is to be noted that "constant" in this case includes minute change in voltage which hardly affects actual display.

[0057] Note that the amount indicated by the arrow **122** or the arrow **123** that corresponds to the amount of change in voltage is changed in accordance with an image signal. In particular, when an image signal is hardly supplied to the pixel electrode, the voltage rarely changes. FIG. **3** illustrates the relation between a transmittance and voltage applied to the liquid crystal **113**. As seen from FIG. **3**, there is no problem in the case where an image signal is hardly supplied to the pixel electrode, that is, in the case where an applied voltage is low, where the transmittance corresponding to the applied voltage is hardly changed when the applied voltage is changed a little.

[0058] FIG. **4** is a block diagram of a liquid crystal display device including a circuit that outputs the holding signal V_{cap}. The liquid crystal display device in FIG. **4** includes a display panel portion **301** and a peripheral circuit portion **302**. The display panel portion **301** has a structure similar to that of the display panel **100** in FIG. **1**A; therefore, the description is not repeated. The peripheral circuit portion **302** includes a circuit **303** for switching between a moving image and a still image (hereinafter referred to as an image switching circuit **303**), a display control circuit **304**, and a holding signal generation circuit **305**. Note that the display panel portion **301** and the peripheral circuit portion **302** are preferably formed over different substrates; they may be formed over the same substrate.

[0059] The image switching circuit **303** judges whether image signals supplied from the outside are for a moving image or a still image and switches an image between a moving image and a still image. The image switching circuit **303** may automatically judge whether image signals supplied from the outside are for a moving image or a still image by comparing the image signals for subsequent frame periods, or may switch an image between a moving image and a still image in accordance with a signal from the outside.

[0060] The display control circuit **304** supplies a signal for displaying a moving image, for example, an image signal, a clock signal, and the like to the display panel portion **301** when the image switching circuit **303** judges that the image signals are for a moving image. On the other hand, when the image switching circuit **303** judges that the image signals are for a still image, the display control circuit **304** supplies a signal for displaying a still image, for example, an image signal, a clock signal, and the like to the display panel portion **301** at predetermined timing while reducing the refresh rate.

[0061] The holding signal generation circuit **305** generates the holding signal V_{cap} supplied to the capacitor line **106** when the image switching circuit **303** judges that the image signals are for a still image. When the image switching circuit **303** judges that the image signals are for a moving image, the holding signal generation circuit **305** supplies a

given constant voltage, for example, a signal same as the common voltage V_{com} to the display panel portion **301**.

[0062] Note that a high power supply potential VDD refers to a potential that is higher than a reference potential, and a low power supply potential VSS refers to a potential that is lower than or equal to the reference potential. Both the high power supply potential and the low power supply potential are preferably potentials with which a thin film transistor can operate. Note that the high power supply potential VDD and the low power supply potential VSS are collectively referred to as a power supply voltage in some cases.

[0063] An example of the structure of the holding signal generation circuit **305** is described with reference to FIG. **5**. As an example, the holding signal generation circuit **305** illustrated in FIG. **5** includes a first current source circuit **501**, a first switch **502**, a second switch **503**, a second current source circuit **504**, and a third switch **505**. The holding signal generation circuit **305** in FIG. **5** controls rise or fall in voltage of the capacitor line **106** by the first current source circuit **501** and the second current source circuit **504** in such a manner that on/off of the first switch **502** and the second switch **503** is alternately switched by control of a switching terminal **507** in a period during which a still image is displayed. Note that when the voltage of the capacitor line **106** is a given constant voltage, the third switch **505** is turned on so that the capacitor line **106** is connected to a terminal **506** to which the common voltage Vm is supplied.

[0064] Note that it is preferable that the first switch **502**, the second switch **503**, and the third switch **505** be transistors, and the first switch **502** and the second switch **503** be transistors with opposite polarities.

[0065] As described above, the structure shown in this embodiment can suppress deterioration of a displayed image even when the refresh rate is reduced in displaying a still image.

[0066] This embodiment can be implemented in appropriate combination with any of the components described in the other embodiments.

Embodiment 2

[0067] In this embodiment, a structure different from the structure described in Embodiment 1 will be described.

[0068] Embodiment 1 describes the structure for frame inversion driving illustrated in FIG. **6**A; this embodiment explains source line inversion driving in which inversion driving with the polarity inverted per signal line is performed as illustrated in FIG. **6**B, gate line inversion driving in which inversion driving with the polarity inverted per gate line is performed as illustrated in FIG. **6**C, and dot inversion driving in which inversion driving with inverted polarity is performed between adjacent pixels as illustrated in FIG. **6**D, by using a circuit configuration of a pixel, and the like. Note that the part of the same description as that in Embodiment 1 is not repeated. Operation for common inversion driving is the same as that for frame inversion driving; therefore, description of common inversion driving is omitted. Note that FIGS. **6**A to **6**D illustrate examples in which image signals with polarities inverted between an Nth frame (N is a natural number) and a (N+1)th frame are supplied (the polarity is denoted by a plus sign or a minus sign in FIGS. **6**A to **6**D); alternatively, another driving method may be employed.

[0069] The methods for inversion driving in FIGS. **6**B to **6**D are different from the method in FIG. **6**A, which is the inversion driving in Embodiment 1, in that image signals of different polarities are supplied in one frame period; accordingly, a voltage supplied to a capacitor line is changed depending on the polarity of an image signal.

[0070] Specific description is made using simple circuit configurations. FIG. **7**A illustrates a circuit configuration of a pixel for source line inversion driving, corresponding to FIG. **6**B. FIG. **7**A illustrates a gate line **102**, a signal line **103**, a pixel **104**, a common electrode **105**, a first capacitor line **106**A, and a second capacitor line **106**B. The first capacitor line **106**A is connected to pixels to which image signals of one polarity are supplied, and the second capacitor line **106**B is connected to other pixels to which image signals of a different polarity are supplied as illustrated in FIG. **6**B. FIG. **7**B illustrates a circuit configuration of a pixel for gate line inversion driving, corresponding to FIG. **6**C. FIG. **7**B illustrates a gate line **102**, a signal line **103**, a pixel **104**, a common electrode **105**, a first capacitor line **106**A, and a second capacitor line **106**B. The first capacitor line **106**A is connected to pixels to which image signals of one polarity are supplied, and the second capacitor line **106**B is connected to other pixels to which image signals of a different polarity are supplied as illustrated in FIG. **6**C. FIG. **7**C illustrates a circuit configuration of a pixel for dot inversion driving, corresponding to FIG. **6**D. FIG. **7**C illustrates a gate line **102**, a signal line **103**, a pixel **104**, a common electrode **105**, a first capacitor line **106**A, and a second capacitor line **106**B. The first capacitor line **106**A is connected to pixels to which image signals of one polarity are supplied, and the second capacitor line **106**B is connected to other pixels to which image signals of the different polarity are supplied as illustrated in FIG. **6**D. The above-described first capacitor line **106**A and second capacitor line **106**B in FIGS. **7**A to **7**C are supplied with a first holding signal V_{cap1} and a second holding signal V_{cap2} which are different holding signals.

[0071] FIG. **8**A illustrates the same diagram as FIG. **2**A and focuses on a potential of each wiring, a voltage between electrodes, and a current flowing through each element. The difference from FIG. **2**A is that FIG. **8**A illustrates the first holding signal V_{cap1} and the second holding signal V_{cap2} described with reference to FIGS. **7**A to **7**C.

[0072] Like FIG. **2**B, FIG. **8**B illustrates a general timing chart showing the potential of each wiring and the voltage between electrodes illustrated in FIG. **8**A. Image signals of different polarities are supplied to the liquid crystal element **109**, and the liquid crystal **113** is supplied with a first voltage V_{LC} and a second voltage V_{LC} that are inverted per frame period. Then, the first holding signal V_{cap1} or the second holding signal V_{cap2} that compensates the amount of rise or fall in the voltage (V_{pix}) held in the pixel electrode **111** from V_{data} due to the off-state current I_{TFT} and/or the current I_{LC} flowing through the liquid crystal is supplied. The first V_{pix} and the second V_{pix} in a pixel to which image signals of different polarities are supplied in the periods F**1** to F**4** each of which is one frame period are not much changed at the boundary between the periods F**1** to F**4** (denoted by "refresh" in FIG. **8**B); thus, image deterioration in displaying a still image can be reduced.

[0073] As described above, the structure shown in this embodiment can suppress deterioration of a displayed image even when the refresh rate is reduced in displaying a still image.

[0074] This embodiment can be implemented in appropriate combination with any of the components described in the other embodiments.

Embodiment 3

[0075] In this embodiment, an example of a transistor that can be applied to a liquid crystal display device disclosed in this specification will be described.

[0076] FIGS. **9**A to **9**D each illustrate an example of a cross-sectional structure of a transistor.

[0077] A transistor **410** illustrated in FIG. **9**A is a kind of bottom-gate structure thin film transistor and is also called an inverted staggered thin film transistor.

[0078] The transistor **410** includes, over a substrate **400** having an insulating surface, a gate electrode layer **401**, a gate insulating layer **402**, an oxide semiconductor layer **403**, a source electrode layer **405***a*, and a drain electrode layer **405***b*. An insulating layer **407** is provided to cover the transistor **410** and be stacked over the oxide semiconductor layer **403**. A protective insulating layer **409** is provided over the insulating layer **407**.

[0079] A transistor **420** illustrated in FIG. **9**B has a kind of bottom-gate structure called a channel-protective type (channel-stop type) and is also referred to as an inverted staggered thin film transistor.

[0080] The transistor **420** includes, over a substrate **400** having an insulating surface, a gate electrode layer **401**, a gate insulating layer **402**, an oxide semiconductor layer **403**, an insulating layer **427** that is provided over a channel formation region in the oxide semiconductor layer **403** and functions as a channel protective layer, a source electrode layer **405***a*, and a drain electrode layer **405***b*. A protective insulating layer **409** is provided to cover the transistor **420**.

[0081] A transistor **430** illustrated in FIG. **9**C is a bottom-gate type thin film transistor and includes, over a substrate **400** which is a substrate having an insulating surface, a gate electrode layer **401**, a gate insulating layer **402**, a source electrode layer **405***a*, a drain electrode layer **405***b*, and an oxide semiconductor layer **403**. An insulating layer **407** is provided to cover the transistor **430** and be in contact with the oxide semiconductor layer **403**. A protective insulating layer **409** is provided over the insulating layer **407**.

[0082] In the transistor **430**, the gate insulating layer **402** is provided in contact with the substrate **400** and the gate electrode layer **401**. The source electrode layer **405***a* and the drain electrode layer **405***b* are provided in contact with the gate insulating layer **402**. The oxide semiconductor layer **403** is provided over the gate insulating layer **402**, the source electrode layer **405***a*, and the drain electrode layer **405***b*.

[0083] A transistor **440** illustrated in FIG. **9**D is a kind of top-gate structure thin film transistor. The transistor **440** includes, over a substrate **400** having an insulating surface, an insulating layer **447**, an oxide semiconductor layer **403**, a source electrode layer **405***a* and a drain electrode layer **405***b*, a gate insulating layer **402**, and a gate electrode layer **401**. A wiring layer **446***a* and a wiring layer **446***b* are provided in contact with the source electrode layer **405***a* and the drain electrode layer **405***b*, respectively, to be electrically connected to the source electrode layer **405***a* and the drain electrode layer **405***b*, respectively.

[0084] In this embodiment, the oxide semiconductor layer **403** is used as a semiconductor layer.

[0085] As the oxide semiconductor layer **403**, any of the following oxide semiconductor layers can be used: a quaternary metal oxide film such as an In—Sn—Ga—Zn—O film; a ternary metal oxide film such as an In—Ga—Zn—O film, an In—Sn—Zn—O film, an In—Al—Zn—O film, a Sn—Ga—Zn—O film, an Al—Ga—Zn—O film, or a Sn—Al—Zn—O film; a binary metal oxide film such as an In—Zn—O film, a Sn—Zn—O film, an Al—Zn—O film, a Zn—Mg—O film, a Sn—Mg—O film, or an In—Mg—O film; an In—O film, a Sn—O film, or a Zn—O film. Further, the above-described oxide semiconductor layer may contain SiO_2.

[0086] As the oxide semiconductor layer **403**, a thin film expressed by $InMO_3(ZnO)_m$ (m>0) can be used. Here, M represents one or more metal elements selected from Ga, Al, Mn, and Co. For example, M can be Ga, Ga and Al, Ga and Mn, or Ga and Co. An oxide semiconductor film whose composition formula is represented by $InMO_3(ZnO)_m$ (m>0) where at least Ga is contained as M is referred to as an In—Ga—Zn—O oxide semiconductor, and a thin film thereof is also referred to as an In—Ga—Zn—O film.

[0087] Note that in the structure in this embodiment, the oxide semiconductor is an intrinsic (i-type) or substantially intrinsic semiconductor obtained by removal of hydrogen, which is an n-type impurity, from the oxide semiconductor for high purification so that the oxide semiconductor contains an impurity other than the main component as little as possible. In other words, the oxide semiconductor in this embodiment is a highly purified i-type (intrinsic) semiconductor or a substantially intrinsic semiconductor obtained by removing impurities such as hydrogen and water as much as possible, not by adding an impurity element. Therefore, the oxide semiconductor layer included in the thin film transistor is a highly purified and electrically i-type (intrinsic) oxide semiconductor layer.

[0088] The number of carriers in the highly purified oxide semiconductor is very small (close to zero), and the carrier concentration is less than $1\times10^{14}/cm^3$, preferably less than $1\times10^{12}/cm^3$, further preferably less than $1\times10^{11}/cm^3$.

[0089] The number of carriers in the oxide semiconductor is so small that the off-state current of the transistor can be reduced. Specifically, the off-state current of the thin film transistor including the oxide semiconductor layer (per channel width of 1 μm) can be reduced to 10 aA/μm (1×10^{-17} A/μm) or lower, further reduced to 1 aA/μm (1×10^{-18} A/μm) or lower, and still further reduced to 10 zA/μm (1×10^{-20} A/μm). In other words, in circuit design, the oxide semiconductor can be regarded as an insulator when the transistor is off. Moreover, when the thin film transistor is on, the current supply capability of the oxide semiconductor layer is expected to be higher than that of a semiconductor layer formed of amorphous silicon.

[0090] In each of the transistors **410**, **420**, **430**, and **440** including the oxide semiconductor layer **403**, the current in an off state (the off-state current) can be small. Thus, the retention time for an electric signal such as image data can be extended, and an interval between writings can be extended. As a result, the frequency of refresh can be reduced, so that power consumption can be further reduced.

[0091] Furthermore, the transistors **410**, **420**, **430**, and **440** including the oxide semiconductor layer **403** can have relatively high field-effect mobility as the ones formed using

an amorphous semiconductor, thus, the transistors can operate at high speed. As a result, high functionality and high-speed response of a display device can be realized.

[0092] Although there is no particular limitation on a substrate that can be used as the substrate **400** having an insulating surface, the substrate needs to have heat resistance at least high enough to withstand heat treatment to be performed later. A glass substrate made of barium borosilicate glass, aluminoborosilicate glass, or the like can be used.

[0093] In the case where the temperature of heat treatment to be performed later is high, a glass substrate whose strain point is greater than or equal to 730° C. is preferably used. For a glass substrate, a glass material such as aluminosilicate glass, aluminoborosilicate glass, or barium borosilicate glass is used, for example. Note that a glass substrate containing a larger amount of barium oxide (BaO) than boron oxide (B_2O_3), which is practical heat-resistant glass, may be used.

[0094] Note that a substrate formed of an insulator, such as a ceramic substrate, a quartz substrate, or a sapphire substrate, may be used instead of the glass substrate. Alternatively, crystallized glass or the like may be used. A plastic substrate or the like can be used as appropriate.

[0095] In the bottom-gate structure transistors **410**, **420**, and **430**, an insulating film serving as a base film may be provided between the substrate and the gate electrode layer. The base film has a function of preventing diffusion of an impurity element from the substrate, and can be formed with a single-layer structure or a layered structure including a silicon nitride film, a silicon oxide film, a silicon nitride oxide film, and/or a silicon oxynitride film.

[0096] The gate electrode layer **401** can be formed with a single-layer structure or a layered structure using a metal material such as molybdenum, titanium, chromium, tantalum, tungsten, aluminum, copper, neodymium, or scandium or an alloy material containing any of these materials as its main component.

[0097] As a two-layer structure of the gate electrode layer **401**, any of the following layered structures is preferably employed, for example: a two-layer structure in which a molybdenum layer is stacked over an aluminum layer, a two-layer structure in which a molybdenum layer is stacked over a copper layer, a two-layer structure in which a titanium nitride layer or a tantalum nitride layer is stacked over a copper layer, or a two-layer structure in which a titanium nitride layer and a molybdenum layer are stacked. As a three-layer structure of the gate electrode layer **401**, it is preferable to employ a stack of a tungsten layer or a tungsten nitride layer, a layer of an alloy of aluminum and silicon or an alloy of aluminum and titanium, and a titanium nitride layer or a titanium layer. Note that the gate electrode layer can be formed using a light-transmitting conductive film. An example of a material for the light-transmitting conductive film is a light-transmitting conductive oxide.

[0098] The gate insulating layer **402** can be formed with a single-layer structure or a layered structure using any of a silicon oxide layer, a silicon nitride layer, a silicon oxynitride layer, a silicon nitride oxide layer, an aluminum oxide layer, an aluminum nitride layer, an aluminum oxynitride layer, an aluminum nitride oxide layer, and a hafnium oxide layer by a plasma CVD method, a sputtering method, or the like.

[0099] The gate insulating layer **402** can have a structure in which a silicon nitride layer and a silicon oxide layer are stacked from the gate electrode layer side. For example, a 100-nm-thick gate insulating layer is formed in such a manner that a silicon nitride layer (SiN_y (y>0)) having a thickness of 50 nm to 200 nm is formed as a first gate insulating layer by a sputtering method and then a silicon oxide layer (SiO_x (x>0)) having a thickness of 5 nm to 300 nm is stacked as a second gate insulating layer over the first gate insulating layer. The thickness of the gate insulating layer **402** may be set as appropriate depending on characteristics needed for a thin film transistor, and may be approximately 350 nm to 400 nm.

[0100] For a conductive film used for the source electrode layer **405***a* and the drain electrode layer **405***b*, an element selected from Al, Cr, Cu, Ta, Ti, Mo, and W, an alloy containing any of these elements, or an alloy film containing a combination of any of these elements can be used, for example. A structure may be employed in which a high-melting-point metal layer of Cr, Ta, Ti, Mo, W, or the like is stacked on one or both of a top surface and a bottom surface of a metal layer of Al, Cu, or the like. By using an aluminum material to which an element preventing generation of hillocks and whiskers in an aluminum film, such as Si, Ti, Ta, W, Mo, Cr, Nd, Sc, or Y, is added, heat resistance can be increased.

[0101] A conductive film serving as the wiring layers **446***a* and **446***b* connected to the source electrode layer **405***a* and the drain electrode layer **405***b* can be formed using a material similar to that of the source and drain electrode layers **405***a* and **405***b*.

[0102] The source electrode layer **405***a* and the drain electrode layer **405***b* may have a single-layer structure or a layered structure of two or more layers. For example, the source electrode layer **405***a* and the drain electrode layer **405***b* can have a single-layer structure of an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, or a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order.

[0103] The conductive film to be the source electrode layer **405***a* and the drain electrode layer **405***b* (including a wiring layer formed using the same layer as the source and drain electrode layers) may be formed using a conductive metal oxide. As the conductive metal oxide, indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), an alloy of indium oxide and tin oxide (In_2O_3—SnO_2, referred to as ITO), an alloy of indium oxide and zinc oxide (In_2O_3—ZnO), or any of the metal oxide materials containing silicon or silicon oxide can be used.

[0104] As the insulating layers **407**, **427**, and **447** and the protective insulating layer **409**, an inorganic insulating film such as an oxide insulating layer or a nitride insulating layer is preferably used.

[0105] As the insulating layers **407**, **427**, and **447**, an inorganic insulating film such as a silicon oxide film, a silicon oxynitride film, an aluminum oxide film, or an aluminum oxynitride film can be typically used.

[0106] As the protective insulating layer **409**, an inorganic insulating film such as a silicon nitride film, an aluminum nitride film, a silicon nitride oxide film, or an aluminum nitride oxide film can be used.

[0107] A planarization insulating film may be formed over the protective insulating layer **409** in order to reduce surface roughness due to the transistor. The planarization insulating film can be formed using a heat-resistant organic material such as polyimide, acrylic, benzocyclobutene, polyamide, or

epoxy. Other than such organic materials, it is possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that the planarization insulating film may be formed by stacking a plurality of insulating films formed from these materials.

[0108] By using the transistor including the oxide semiconductor layer in this embodiment, it is possible to provide a highly functional liquid crystal display device with lower power consumption.

[0109] This embodiment can be implemented in appropriate combination with any of the components described in the other embodiments.

Embodiment 4

[0110] When thin film transistors are manufactured and used for a pixel portion and a driver circuit, a liquid crystal display device having a display function can be manufactured. Further, part of or the entire driver circuit can be formed over a substrate where a pixel portion is formed, using a thin film transistor; thus, a system-on-panel can be obtained.

[0111] Note that the liquid crystal display device includes any of the following modules in its category: a module provided with a connector, for example, a flexible printed circuit (FPC), a tape automated bonding (TAB) tape, or a tape carrier package (TCP); a module provided with a printed wiring board at the end of a TAB tape or a TCP; and a module where an integrated circuit (IC) is directly mounted on a display element by a chip-on-glass (COG) method.

[0112] The appearance and a cross section of a liquid crystal display device will be described with reference to FIGS. **10**A**1**, **10**A**2**, and **10**B. FIGS. **10**A**1** and **10**A**2** are plan views of panels in which thin film transistors **4010** and **4011** and a liquid crystal element **4013** are sealed between a first substrate **4001** and a second substrate **4006** with a sealant **4005**. FIG. **10**B is a cross-sectional view along M-N in FIGS. **10**A**1** and **10**A**2**.

[0113] The sealant **4005** is provided so as to surround a pixel portion **4002** and a gate line driver circuit **4004** that are provided over the first substrate **4001**. The second substrate **4006** is provided over the pixel portion **4002** and the gate line driver circuit **4004**. Therefore, the pixel portion **4002** and the gate line driver circuit **4004** are sealed together with a liquid crystal layer **4008**, by the first substrate **4001**, the sealant **4005**, and the second substrate **4006**. A signal line driver circuit **4003** that is formed using a single crystal semiconductor film or a polycrystalline semiconductor film over a substrate separately prepared is mounted in a region that is different from the region surrounded by the sealant **4005** over the first substrate **4001**.

[0114] Note that there is no particular limitation on the connection method of a driver circuit that is separately formed, and a COG method, a wire bonding method, a TAB method, or the like can be used. FIG. **10**A**1** illustrates an example where the signal line driver circuit **4003** is mounted by a COG method. FIG. **10**A**2** illustrates an example where the signal line driver circuit **4003** is mounted by a TAB method.

[0115] The pixel portion **4002** and the gate line driver circuit **4004** provided over the first substrate **4001** include a plurality of thin film transistors. FIG. **10**B illustrates the thin film transistor **4010** included in the pixel portion **4002** and the thin film transistor **4011** included in the gate line driver circuit **4004**. Insulating layers **4041***a*, **4041***b*, **4042***a*, **4042***b*, **4020**, and **4021** are provided over the thin film transistors **4010** and **4011**.

[0116] A highly reliable thin film transistor including an oxide semiconductor layer can be used as the thin film transistors **4010** and **4011**. In this embodiment, the thin film transistors **4010** and **4011** are n-channel thin film transistors.

[0117] A conductive layer **4040** is provided over part of the insulating layer **4021**, which overlaps with a channel formation region of an oxide semiconductor layer in the thin film transistor **4011** for the driver circuit. The conductive layer **4040** is provided at the position overlapping with the channel formation region of the oxide semiconductor layer, so that the amount of change in threshold voltage of the thin film transistor **4011** before and after the BT (bias-temperature) test can be reduced. The potential of the conductive layer **4040** may be the same or different from that of a gate electrode layer of the thin film transistor **4011**. The conductive layer **4040** can also function as a second gate electrode layer. The potential of the conductive layer **4040** may be GND or 0 V, or the conductive layer **4040** may be in a floating state.

[0118] A pixel electrode layer **4030** included in the liquid crystal element **4013** is electrically connected to the thin film transistor **4010**. A counter electrode layer **4031** of the liquid crystal element **4013** is provided for the second substrate **4006**. A portion where the pixel electrode layer **4030**, the counter electrode layer **4031**, and the liquid crystal layer **4008** overlap with one another corresponds to the liquid crystal element **4013**. Note that the pixel electrode layer **4030** and the counter electrode layer **4031** are provided with an insulating layer **4032** and an insulating layer **4033** functioning as alignment films, respectively, and the liquid crystal layer **4008** is sandwiched between the pixel electrode layer **4030** and the counter electrode layer **4031** with the insulating layers **4032** and **4033** therebetween.

[0119] Note that a light-transmitting substrate can be used as the first substrate **4001** and the second substrate **4006**; glass, ceramics, or plastics can be used. As plastics, a fiberglass-reinforced plastics (FRP) plate, a polyvinyl fluoride (PVF) film, a polyester film, or an acrylic resin film can be used.

[0120] A spacer **4035** is a columnar spacer obtained by selective etching of an insulating film and is provided in order to control the distance (a cell gap) between the pixel electrode layer **4030** and the counter electrode layer **4031**. Note that a spherical spacer may be used. The counter electrode layer **4031** is electrically connected to a common potential line formed over the substrate where the thin film transistor **4010** is formed. With use of the common connection portion, the counter electrode layer **4031** and the common potential line can be electrically connected to each other by conductive particles arranged between a pair of substrates. Note that the conductive particles can be included in the sealant **4005**.

[0121] Alternatively, liquid crystal exhibiting a blue phase for which an alignment film is unnecessary may be used. A blue phase is one of liquid crystal phases, which is generated just before a cholesteric phase changes into an isotropic phase while temperature of cholesteric liquid crystal is increased. Since the blue phase is only generated within a narrow range of temperature, a liquid crystal composition containing a chiral agent at 5 wt % or more so as to improve

the temperature range is used for the liquid crystal layer **4008**. The liquid crystal composition that includes a liquid crystal exhibiting a blue phase and a chiral agent has a short response time of 1 msec or less, has optical isotropy, which makes the alignment process unneeded, and has a small viewing angle dependence.

[0122] Note that this embodiment can also be applied to a transflective liquid crystal display device in addition to a transmissive liquid crystal display device.

[0123] This embodiment shows the example of the liquid crystal display device in which a polarizing plate is provided on the outer side of the substrate (on the viewer side) and a coloring layer and an electrode layer used for a display element are provided in this order on the inner side of the substrate; alternatively, a polarizing plate may be provided on the inner side of the substrate. The layered structure of the polarizing plate and the coloring layer is not limited to that in this embodiment and may be set as appropriate depending on materials of the polarizing plate and the coloring layer or conditions of the manufacturing process. Further, a light-blocking film serving as a black matrix may be provided in a portion other than a display portion.

[0124] The insulating layer **4041***a* that serves as a channel protective layer and the insulating layer **4041***b* that covers an outer edge portion (including a side surface) of the stack of the oxide semiconductor layers are formed in the thin film transistor **4011**. In a similar manner, the insulating layer **4042***a* that serves as a channel protective layer and the insulating layer **4042***b* that covers an outer edge portion (including a side surface) of the stack of the oxide semiconductor layers are formed in the thin film transistor **4010**.

[0125] The insulating layers **4041***b* and **4042***b* that are oxide insulating layers covering the outer edge portion (including the side surface) of the stack of the oxide semiconductor layers can increase the distance between the gate electrode layer and a wiring layer (e.g., a source wiring layer or a capacitor wiring layer) formed over or around the gate electrode layer, so that the parasitic capacitance can be reduced. In order to reduce the surface roughness of the thin film transistors, the thin film transistors are covered with the insulating layer **4021** serving as a planarizing insulating film. Here, as the insulating layers **4041***a*, **4041***b*, **4042***a*, and **4042***b*, a silicon oxide film is formed by a sputtering method, for example.

[0126] Moreover, the insulating layer **4020** is formed over the insulating layers **4041***a*, **4041***b*, **4042***a*, and **4042***b*. As the insulating layer **4020**, a silicon nitride film is formed by an RF sputtering method, for example.

[0127] The insulating layer **4021** is formed as the planarizing insulating film. As the insulating layer **4021**, an organic material having heat resistance, such as polyimide, acrylic, benzocyclobutene, polyamide, or epoxy can be used. Other than such organic materials, it is also possible to use a low-dielectric constant material (a low-k material), a siloxane-based resin, PSG (phosphosilicate glass), BPSG (borophosphosilicate glass), or the like. Note that the insulating layer **4021** may be formed by stacking a plurality of insulating films formed of these materials.

[0128] In this embodiment, a plurality of thin film transistors in the pixel portion may be surrounded together by a nitride insulating film. It is possible to use a nitride insulating film as the insulating layer **4020** and the gate insulating layer and to provide a region where the insulating layer **4020** is in contact with the gate insulating layer so as to surround at least the periphery of the pixel portion in the active matrix substrate. In this manufacturing process, entry of moisture from the outside can be prevented. Further, even after the device is completed as a liquid crystal display device, entry of moisture from the outside can be prevented in the long term, and the long-term reliability of the device can be improved.

[0129] Note that a siloxane-based resin corresponds to a resin including a Si—O—Si bond formed using a siloxane-based material as a starting material. The siloxane-based resin may include an organic group (e.g., an alkyl group or an aryl group) or a fluoro group as a substituent. The organic group may include a fluoro group.

[0130] There is no particular limitation on the formation method of the insulating layer **4021**, and any of the following methods and tools can be employed, for example, depending on the material: a sputtering method, an SOG method, a spin coating method, a dipping method, a spray coating method, a droplet discharge method (e.g., an ink-jet method, screen printing, and offset printing), a doctor knife, a roll coater, a curtain coater, and a knife coater. The baking step of the insulating layer **4021** also serves as annealing of the semiconductor layer, so that a liquid crystal display device can be efficiently manufactured.

[0131] The pixel electrode layer **4030** and the counter electrode layer **4031** can be formed using a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (referred to as ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added.

[0132] Alternatively, the pixel electrode layer **4030** and the counter electrode layer **4031** can be formed using a conductive composition including a conductive high molecule (also referred to as a conductive polymer). The pixel electrode formed using the conductive composition preferably has a sheet resistance of less than or equal to 10000 ohms per square and a transmittance of greater than or equal to 70% at a wavelength of 550 nm. Further, the resistivity of the conductive high molecule included in the conductive composition is preferably less than or equal to 0.1 Ω·cm.

[0133] As the conductive high molecule, a so-called π-electron conjugated conductive high molecule can be used. Examples are polyaniline or a derivative thereof, polypyrrole or a derivative thereof, polythiophene or a derivative thereof, and a copolymer of two or more of these materials.

[0134] A variety of signals and potentials are supplied from an FPC **4018** to the signal line driver circuit **4003** which is formed separately, the gate line driver circuit **4004**, or the pixel portion **4002**.

[0135] A connection terminal electrode **4015** is formed from the same conductive film as the pixel electrode layer **4030** included in the liquid crystal element **4013**, and a terminal electrode **4016** is formed from the same conductive film as source and drain electrode layers of the thin film transistors **4010** and **4011**.

[0136] The connection terminal electrode **4015** is electrically connected to a terminal included in the FPC **4018** via an anisotropic conductive film **4019**.

[0137] Note that FIGS. **10**A1 and **10**A2 illustrate the example in which the signal line driver circuit **4003** is formed separately and mounted on the first substrate **4001**;

however, the this embodiment is not limited to this structure. The gate line driver circuit may be separately formed and then mounted, or only part of the signal line driver circuit or part of the gate line driver circuit may be separately formed and then mounted.

[0138] FIG. **11** illustrates an example of a structure of a liquid crystal display device.

[0139] FIG. **11** illustrates an example of a liquid crystal display device. A TFT substrate **2600** and a counter substrate **2601** are fixed to each other with a sealant **2602**. A pixel portion **2603** including a TFT and the like, a display element **2604** including a liquid crystal layer, and a coloring layer **2605** are provided between the substrates so that a display region is formed. The coloring layer **2605** is necessary to perform color display. In the RGB system, coloring layers corresponding to colors of red, green, and blue are provided for pixels. A polarizing plate **2606** is provided on the outer side of the counter substrate **2601**. A polarizing plate **2607** and a diffusion plate **2613** are provided on the outer side of the TFT substrate **2600**. A light source includes a cold cathode tube **2610** and a reflective plate **2611**. A circuit board **2612** is connected to a wiring circuit portion **2608** of the TFT substrate **2600** by a flexible wiring board **2609** and includes an external circuit such as a control circuit or a power source circuit. The polarizing plate and the liquid crystal layer may be stacked with a retardation plate therebetween.

[0140] For a method for driving the liquid crystal display device, a TN (twisted nematic) mode, an IPS (in-plane-switching) mode, an FFS (fringe field switching) mode, an MVA (multi-domain vertical alignment) mode, a PVA (patterned vertical alignment) mode, an ASM (axially symmetric aligned micro-cell) mode, an OCB (optically compensated birefringence) mode, an FLC (ferroelectric liquid crystal) mode, an AFLC (antiferroelectric liquid crystal) mode, or the like can be used.

[0141] Through the above-described process, it is possible to manufacture a liquid crystal display device in which deterioration of a displayed image can be reduced in displaying a still image.

[0142] This embodiment can be implemented in appropriate combination with any of the components described in the other embodiments.

Embodiment 5

[0143] In this embodiment, an example of an electronic device including the liquid crystal display device described in any of the above-described embodiments will be described.

[0144] FIG. **12**A illustrates a portable game machine that can include a housing **9630**, a display portion **9631**, a speaker **9633**, operation keys **9635**, a connection terminal **9636**, a recording medium reading portion **9672**, and the like. The portable game machine in FIG. **12**A can have a function of reading a program or data stored in the recording medium to display it on the display portion, a function of sharing information with another portable game machine by wireless communication, and the like. Note that the functions of the portable game machine in FIG. **12**A are not limited to those described above, and the portable game machine can have various functions.

[0145] FIG. **12**B illustrates a digital camera that can include a housing **9630**, a display portion **9631**, a speaker **9633**, operation keys **9635**, a connection terminal **9636**, a shutter button **9676**, an image receiving portion **9677**, and the like. The digital camera in FIG. **12**B can have a function of photographing a still image and/or a moving image, a function of automatically or manually correcting the photographed image, a function of obtaining various kinds of information from an antenna, a function of saving the photographed image or the information obtained from the antenna, a function of displaying the photographed image or the information obtained from the antenna on the display portion, and the like. Note that the digital camera in FIG. **12**B can have a variety of functions without being limited to the above.

[0146] FIG. **12**C illustrates a television set that can include a housing **9630**, a display portion **9631**, speakers **9633**, operation key **9635**, a connection terminal **9636**, and the like. The television set in FIG. **12**C has a function of converting an electric wave for television into an image signal, a function of converting an image signal into a signal suitable for display, a function of converting the frame frequency of an image signal, and the like. Note that the television set in FIG. **12**C can have a variety of functions without being limited to the above.

[0147] FIG. **12**D illustrates a monitor for electronic computers (personal computers) (the monitor is also referred to as a PC monitor) that can include a housing **9630**, a display portion **9631**, and the like. As an example, in the monitor in FIG. **12**D, a window **9653** is displayed on the display portion **9631**. Note that FIG. **12**D illustrates the window **9653** displayed on the display portion **9631** for explanation; a symbol such as an icon or an image may be displayed. Since still images are often displayed on the monitor for personal computers, the method for driving a liquid crystal display device in the above-described embodiment is preferably applied. Note that the monitor in FIG. **12**D can have various functions without being limited to the above.

[0148] FIG. **13**A illustrates a computer that can include a housing **9630**, a display portion **9631**, a speaker **9633**, operation keys **9635**, a connection terminal **9636**, a pointing device **9681**, an external connection port **9680**, and the like. The computer in FIG. **13**A can have a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion, a function of controlling processing by a variety of software (programs), a communication function such as wireless communication or wired communication, a function of being connected to various computer networks with the communication function, a function of transmitting or receiving a variety of data with the communication function, and the like. Note that the computer in FIG. **13**A is not limited to having these functions and can have a variety of functions.

[0149] FIG. **13**B illustrates a mobile phone that can include a housing **9630**, a display portion **9631**, a speaker **9633**, operation keys **9635**, a microphone **9638**, and the like. The mobile phone in FIG. **13**B can have a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion; a function of displaying a calendar, a date, the time, or the like on the display portion; a function of operating or editing the information displayed on the display portion; a function of controlling processing by various kinds of software (programs); and the like. Note that the functions of the mobile phone in FIG. **13**B are not limited to those described above, and the mobile phone can have various functions.

[0150] FIG. **13**C illustrates an electronic device including electronic paper (also referred to as an eBook or an e-book reader) that can include a housing **9630**, a display portion **9631**, operation keys **9632**, and the like. The e-book reader in FIG. **13**C can have a function of displaying a variety of information (e.g., a still image, a moving image, and a text image) on the display portion; a function of displaying a calendar, a date, the time, and the like on the display portion; a function of operating or editing the information displayed on the display portion; a function of controlling processing by various kinds of software (programs); and the like. Note that the e-book reader in FIG. **13**C can have a variety of functions without being limited to the above functions. FIG. **13**D illustrates another structure of an e-book reader. The e-book reader in FIG. **13**D has a structure obtained by adding a solar battery **9651** and a battery **9652** to the e-book reader in FIG. **13**C. When a reflective liquid crystal display device is used as the display portion **9631**, the e-book reader is expected to be used in a comparatively bright environment, in which case the structure in FIG. **13**D is preferable because the solar battery **9651** can efficiently generate power and the battery **9652** can efficiently charge power. Note that when a lithium ion battery is used as the battery **9652**, an advantage such as reduction in size can be obtained.

[0151] In the electronic device described in this embodiment, deterioration of a displayed image can be reduced when a still image is displayed.

[0152] This embodiment can be implemented in appropriate combination with any of the components described in the other embodiments.

[0153] This application is based on Japanese Patent Application serial No. 2009-295608 filed with Japan Patent Office on Dec. 25, 2009, the entire contents of which are hereby incorporated by reference.

1. (canceled)

2. A display device comprising:

a first pixel comprising:

a first transistor;

a first liquid crystal element; and

a first capacitor;

a second pixel comprising:

a second transistor;

a second liquid crystal element; and

a second capacitor; and

a holding signal generation circuit,

wherein each of the first transistor and the second transistor comprises an oxide semiconductor layer comprising a channel formation region,

wherein one of a source and a drain of the first transistor is electrically connected to a pixel electrode of the first liquid crystal element,

wherein a first electrode of the first capacitor is electrically connected to the pixel electrode of the first liquid crystal element,

wherein a second electrode of the first capacitor is electrically connected to a capacitor line,

wherein one of a source and a drain of the second transistor is electrically connected to a pixel electrode of the second liquid crystal element,

wherein a first electrode of the second capacitor is electrically connected to the pixel electrode of the second liquid crystal element,

wherein a second electrode of the second capacitor is electrically connected to the capacitor line,

wherein the holding signal generation circuit is configured to supply a constant voltage to the capacitor line during a moving image display, and

wherein the holding signal generation circuit is configured to supply a holding signal to the capacitor line during a still image display such that a change of a voltage applied to the first liquid crystal element and a change of a voltage applied to the second liquid crystal element are reduced.

3. The display device according to claim **2**,

wherein a gate of the first transistor is electrically connected to a gate line, and

wherein a gate of the second transistor is electrically connected to the gate line.

4. The display device according to claim **2**,

wherein the other of the source and the drain of the first transistor is electrically connected to a signal line, and

wherein the other of the source and the drain of the second transistor is electrically connected to the signal line.

5. The display device according to claim **2**,

wherein a gate of the first transistor is electrically connected to a first gate line,

wherein a gate of the second transistor is electrically connected to a second gate line,

wherein the other of the source and the drain of the first transistor is electrically connected to a first signal line, and

wherein the other of the source and the drain of the second transistor is electrically connected to a second signal line.

6. The display device according to claim **2**,

wherein an off-state current of the first transistor is equal to or lower than 1×10^{-17} A/μm.

7. The display device according to claim **2**,

wherein the holding signal generation circuit comprises a current source circuit, and

wherein the current source circuit is electrically connected to the second electrode of the first capacitor through the capacitor line.

8. A display device comprising:

a first pixel comprising:

a first transistor;

a first liquid crystal element; and

a first capacitor;

a second pixel comprising:

a second transistor;

a second liquid crystal element; and

a second capacitor; and

a holding signal generation circuit,

wherein each of the first transistor and the second transistor comprises an oxide semiconductor layer comprising a channel formation region,

wherein one of a source and a drain of the first transistor is electrically connected to a pixel electrode of the first liquid crystal element,

wherein a first electrode of the first capacitor is electrically connected to the pixel electrode of the first liquid crystal element,

wherein a second electrode of the first capacitor is electrically connected to a capacitor line,

wherein one of a source and a drain of the second transistor is electrically connected to a pixel electrode of the second liquid crystal element,

wherein a first electrode of the second capacitor is electrically connected to the pixel electrode of the second liquid crystal element,

wherein a second electrode of the second capacitor is electrically connected to the capacitor line,

wherein the holding signal generation circuit is configured to supply a constant voltage to the capacitor line during a first frame period,

wherein the holding signal generation circuit is configured to supply a holding signal to the capacitor line during a second frame period such that a change of a voltage applied to the first liquid crystal element and a change of a voltage applied to the second liquid crystal element are reduced, and

wherein the second frame period is longer than the first frame period.

9. The display device according to claim **8**,

wherein a gate of the first transistor is electrically connected to a gate line, and

wherein a gate of the second transistor is electrically connected to the gate line.

10. The display device according to claim **8**,

wherein the other of the source and the drain of the first transistor is electrically connected to a signal line, and

wherein the other of the source and the drain of the second transistor is electrically connected to the signal line.

11. The display device according to claim **8**,

wherein a gate of the first transistor is electrically connected to a first gate line,

wherein a gate of the second transistor is electrically connected to a second gate line,

wherein the other of the source and the drain of the first transistor is electrically connected to a first signal line, and

wherein the other of the source and the drain of the second transistor is electrically connected to a second signal line.

12. The display device according to claim **8**,

wherein an off-state current of the first transistor is equal to or lower than 1×10^{-17} A/μm.

13. The display device according to claim **8**,

wherein the holding signal generation circuit comprises a current source circuit, and

wherein the current source circuit is electrically connected to the second electrode of the first capacitor through the capacitor line.

* * * * *

专利名称(译)	用于驱动液晶显示装置的方法		
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[标]申请(专利权)人(译)	株式会社半导体能源研究所		
申请(专利权)人(译)	半导体能源研究所有限公司.		
当前申请(专利权)人(译)	半导体能源研究所有限公司.		
[标]发明人	MIYAKE HIROYUKI		
发明人	MIYAKE, HIROYUKI		
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摘要(译)

一个目的是即使在显示静止图像时降低刷新率时也抑制显示图像的劣化。一种液晶显示装置，包括：电连接到像素电极的像素晶体管;以及电容器，具有电连接到像素电极的一个电极和电连接到电容器线的另一个电极。像素晶体管导通，基于图像信号的电压被提供给像素电极，然后，像素晶体管截止，从而开始像素电极保持基于图像信号的电压的保持时段。在保持时段中基于像素电极中的图像信号对应于电压变化的保持信号被提供给电容器线，使得像素电极的电位恒定。