



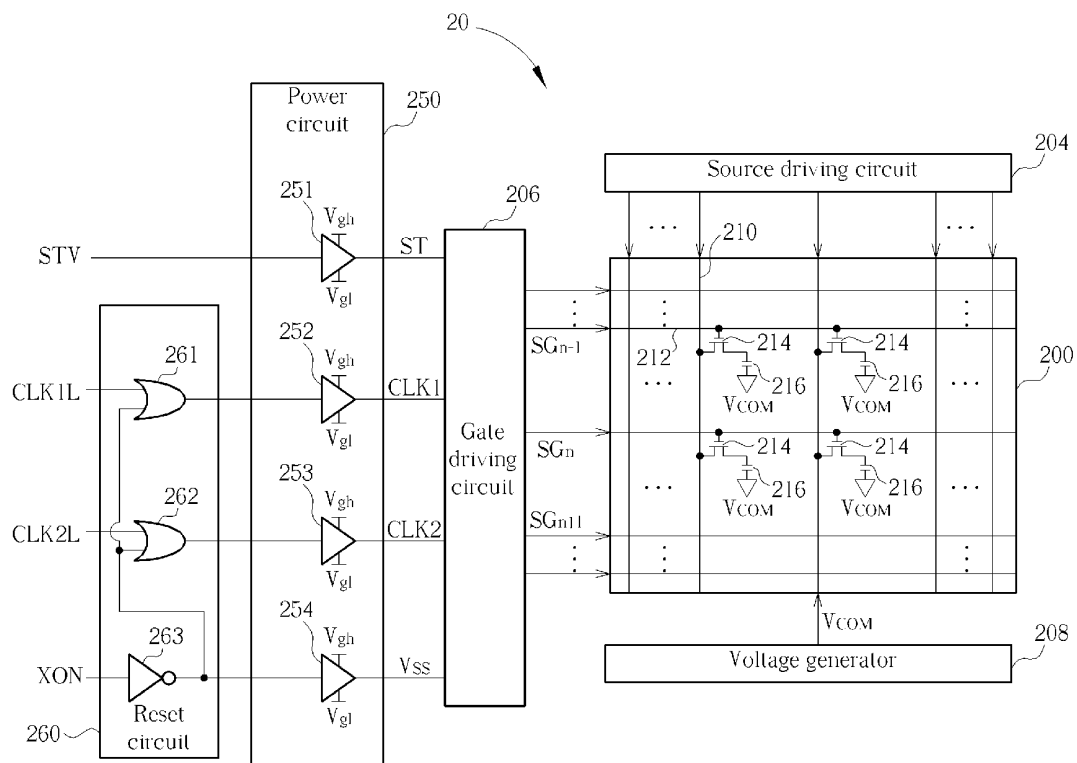
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(19) **United States**(12) **Patent Application Publication**  
**Liao**(10) **Pub. No.: US 2013/0021317 A1**(43) **Pub. Date: Jan. 24, 2013**(54) **LIQUID CRYSTAL DISPLAY DEVICE AND  
METHOD FOR DECAYING RESIDUAL  
IMAGE THEREOF****Publication Classification**(51) **Int. Cl.**  
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Apr. 25, 2012, which is a division of application No.  
11/971,213, filed on Jan. 9, 2008, now Pat. No. 8,188,  
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(57) **ABSTRACT**

By way of enabling a reset signal while turning off a liquid crystal display, a method for decaying residual image of the liquid crystal display is capable of setting the corresponding gate signal of each of a plurality of gate lines of the liquid crystal display based on the reset signal being enabled. Accordingly, enhanced discharging processes on all the storage units of the liquid crystal display for fast decaying residual image can be performed via the data switches of the liquid crystal display turned on by the gate signals being set. The reset operation for performing discharging processes in response to the reset signal can be carried out based on a reset circuit for setting all the gate signals to become high-level signals, or based on a charging/discharging module for furnishing a high-level voltage directly to all the gate lines.



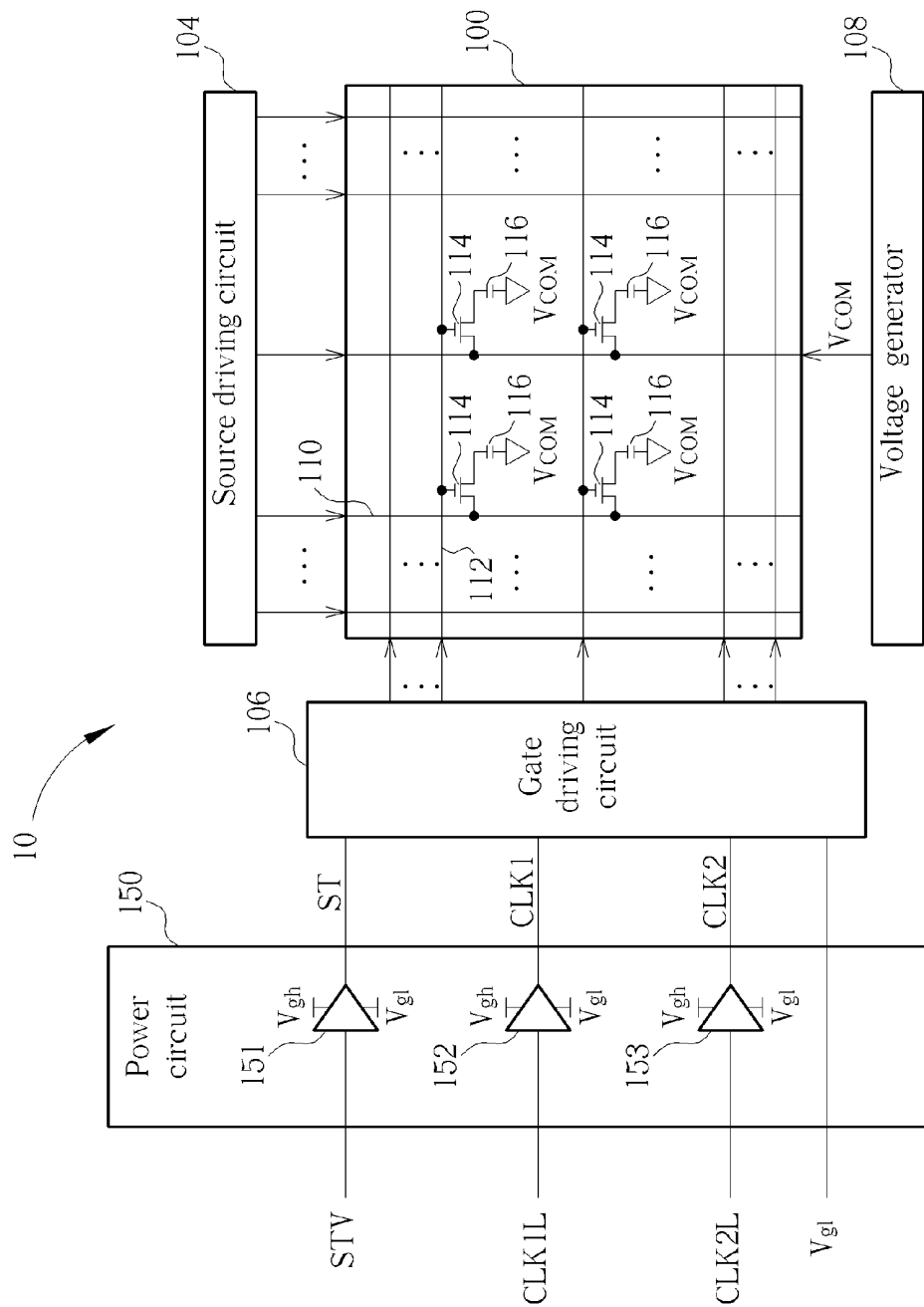


FIG. 1 PRIOR ART

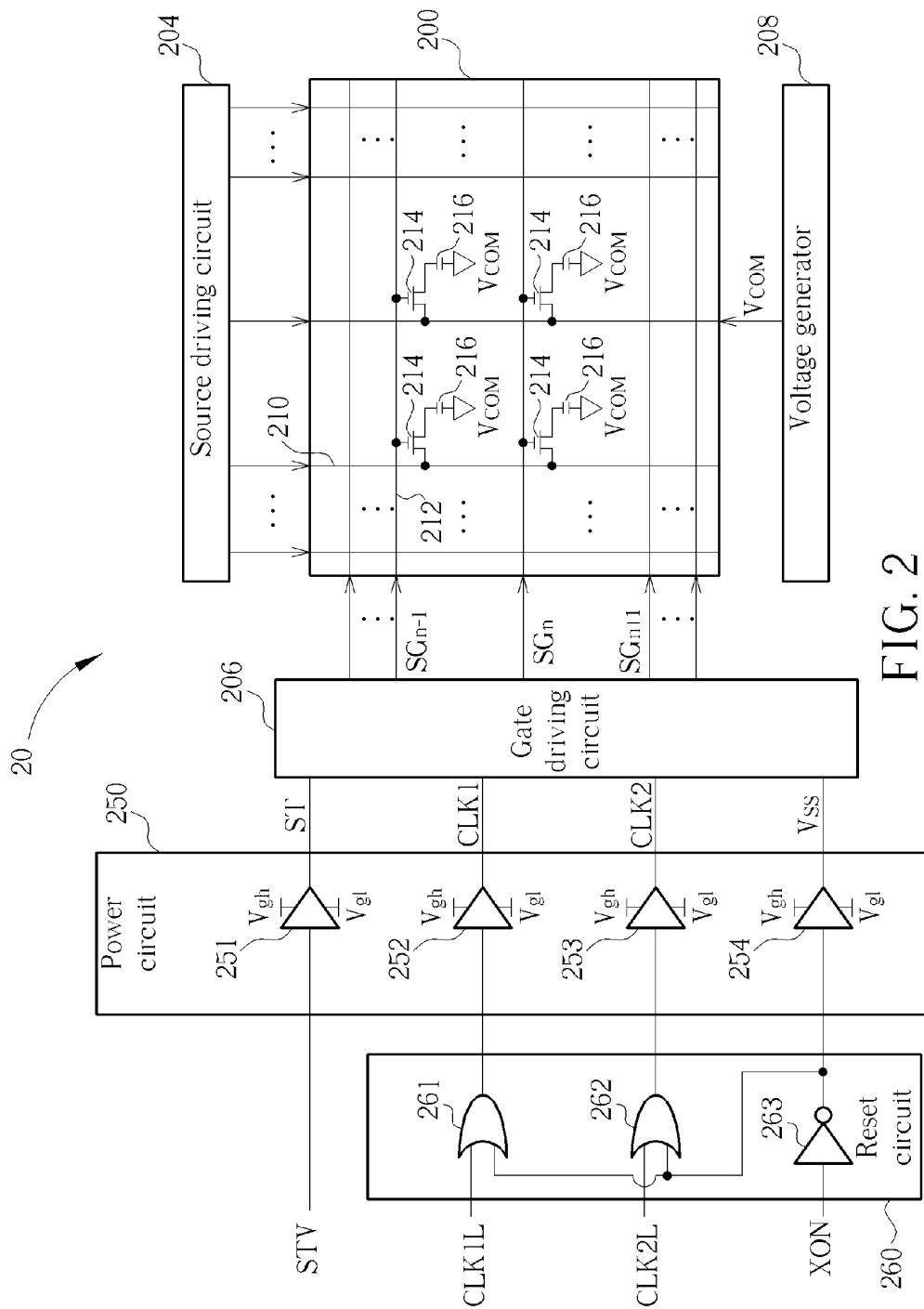


FIG. 2

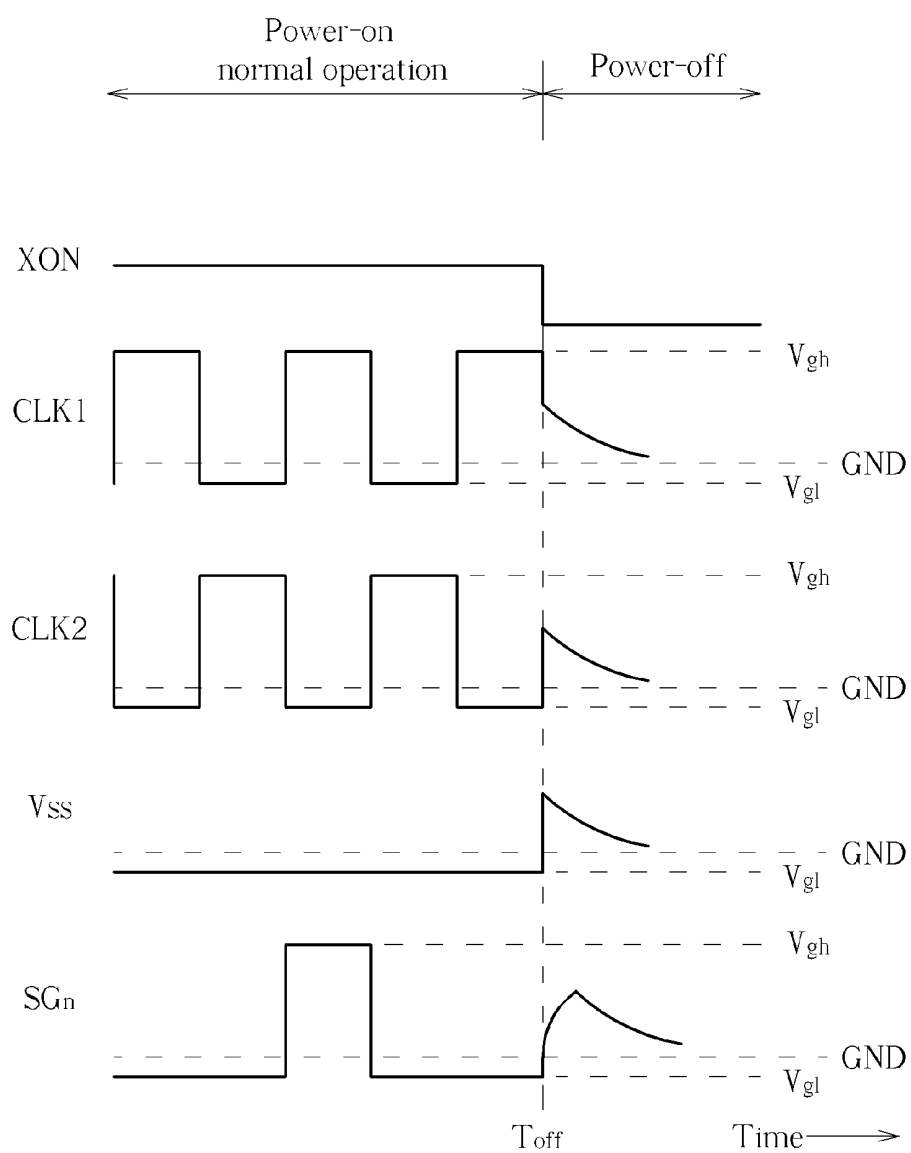


FIG. 3

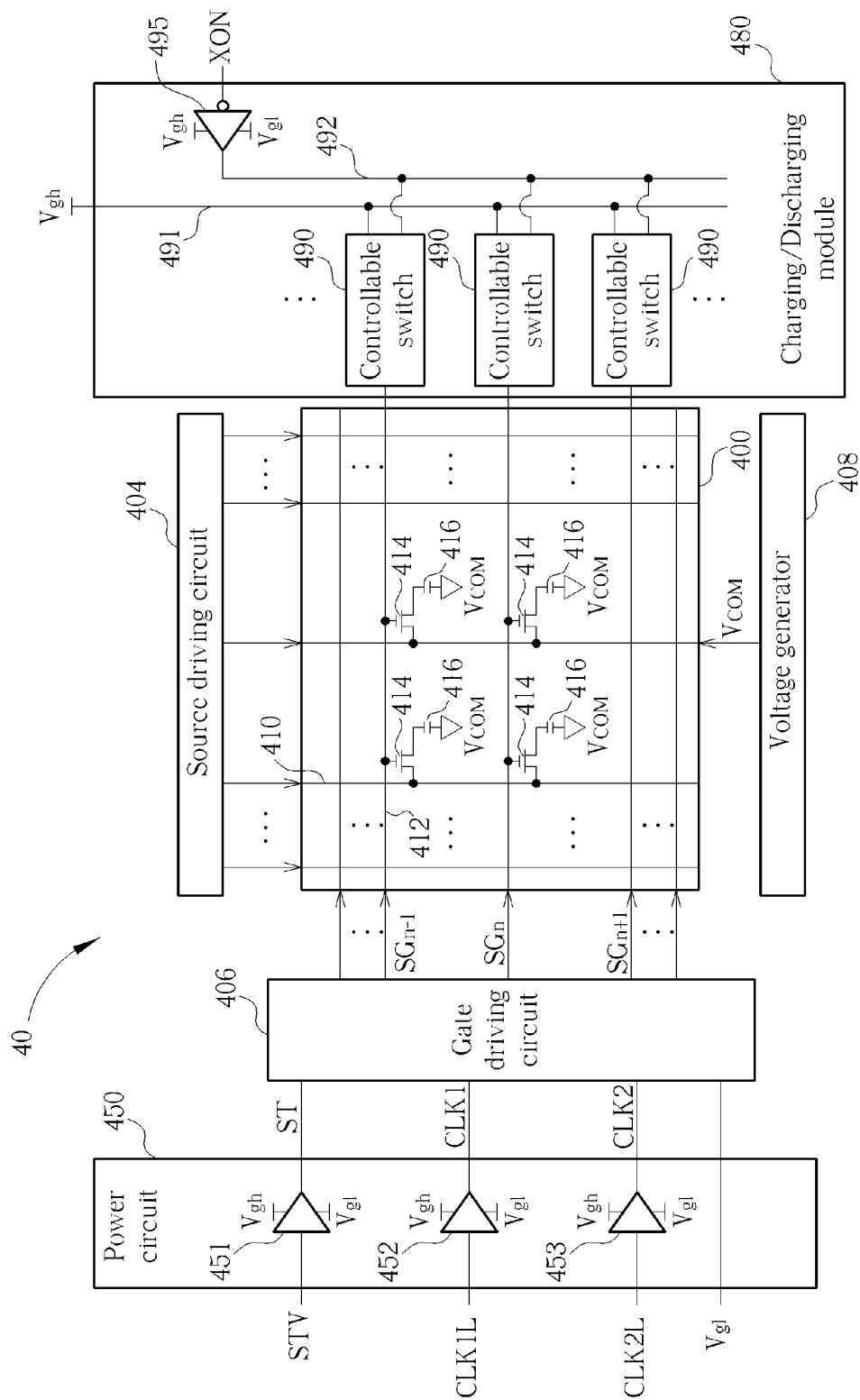


FIG. 4

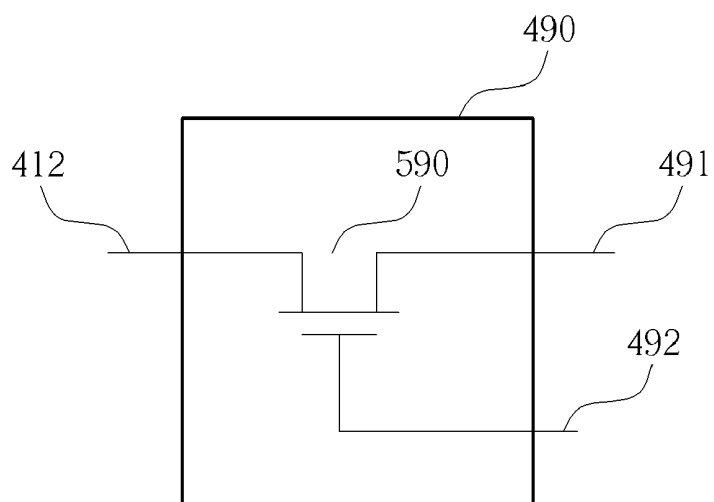


FIG. 5

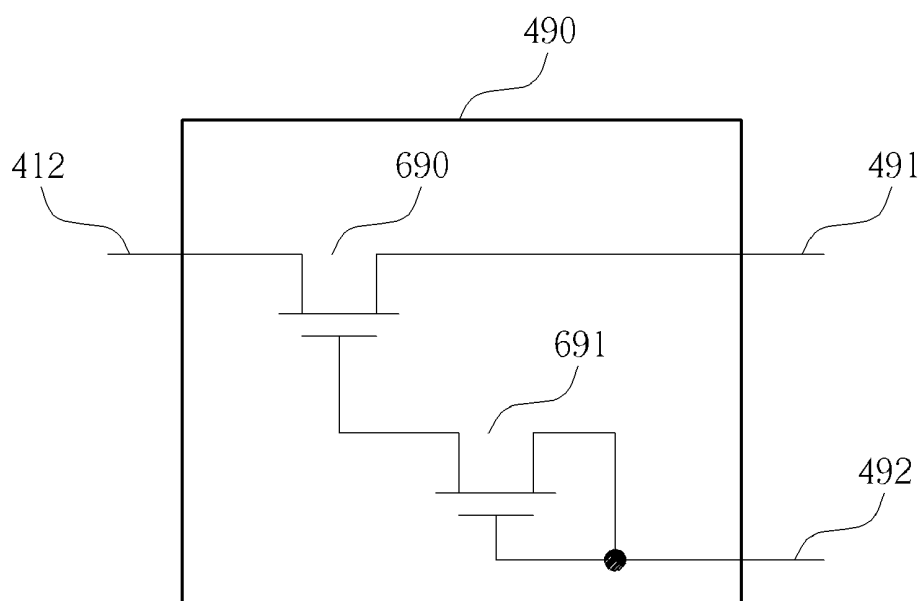


FIG. 6

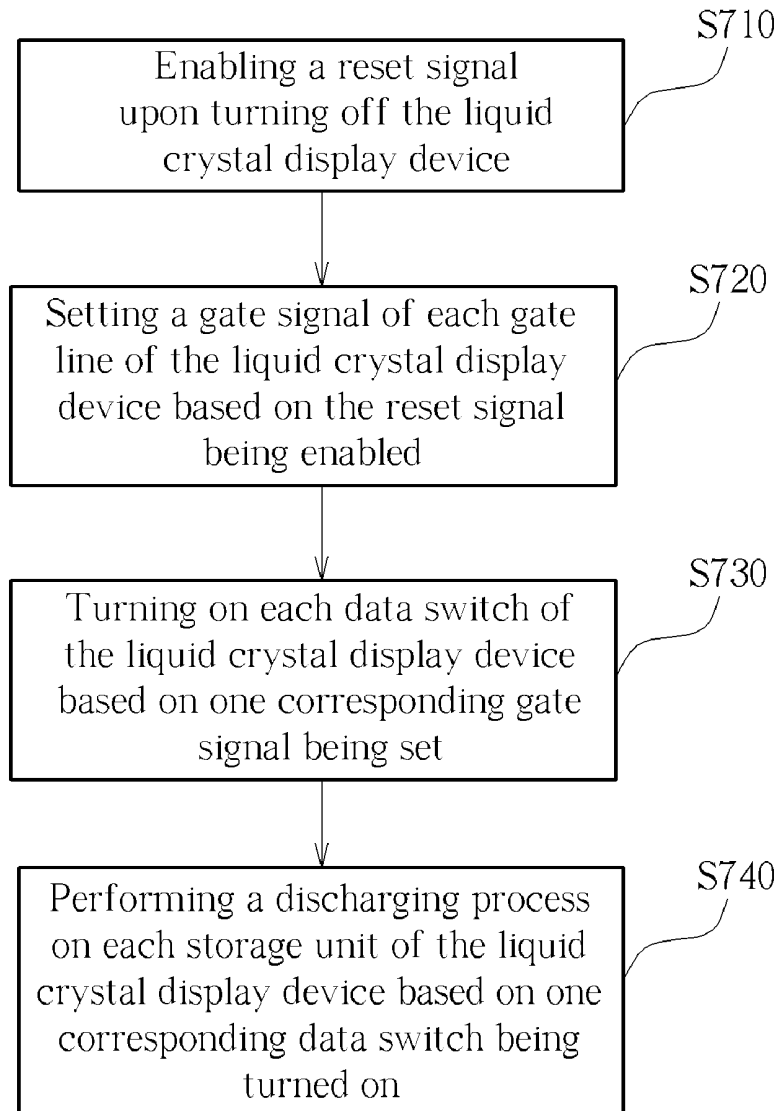


FIG. 7

# LIQUID CRYSTAL DISPLAY DEVICE AND METHOD FOR DECAYING RESIDUAL IMAGE THEREOF

## CROSS REFERENCE TO RELATED APPLICATIONS

**[0001]** This application is a continuation of U.S. patent application Ser. No. 13/455,135 filed on Apr. 25, 2012, which in turn is a division of U.S. patent application Ser. No. 11/971,213 filed on Jan. 9, 2008 and now issued as U.S. Pat. No. 8,188,961, the entire contents of both applications being hereby incorporated by reference.

## BACKGROUND OF THE INVENTION

**[0002]** 1. Field of the Invention

**[0003]** The present invention relates to a liquid crystal display device and related method, and more particularly, to a liquid crystal display device and method for decaying residual image of the liquid crystal display device.

**[0004]** 2. Description of the Prior Art

**[0005]** Because liquid crystal display (LCD) devices are characterized by thin appearance, low power consumption, and low radiation, LCD devices have been widely applied in various electronic products such as computer monitors, mobile phones, personal digital assistants (PDAs), or flat panel televisions. In general, the LCD device comprises liquid crystal layers encapsulated by two substrates. By means of varying voltage drops between opposite sides of the liquid crystal layers, the twisted angles of the liquid crystal molecules of the liquid crystal layers can be changed so that the transparency of the liquid crystal layers can also be changed accordingly for illustrating images.

**[0006]** FIG. 1 is a diagram schematically showing the structure of a prior-art thin film transistor liquid crystal display (TFT-LCD) device. As shown in FIG. 1, the TFT-LCD device 10 comprises a liquid crystal display panel 100, a power circuit 150, a source driving circuit 104, a gate driving circuit 106, and a voltage generator 108. As aforementioned, the liquid crystal display panel 100 normally comprises two substrates and liquid crystal layers being stuffed between the substrates. One of the substrates is disposed with a plurality of data lines 110, a plurality of gate lines (or scan lines) 112 perpendicular to the data lines 110, and a plurality of thin film transistors (TFTs) 114. The other one of the substrates is disposed with a common electrode for receiving a common voltage Vcom provided by the voltage generator 108. For the sake of elucidation, FIG. 1 reveals only four thin film transistors 114, but in a real case, there is one thin film transistor 114 disposed at each intersection of a data line 110 and a gate line 112 on the LCD panel 100. That is, the plurality of thin film transistors 114, each corresponding to a pixel of the TFT-LCD device 10, form a matrix on the LCD panel 100, and the data lines 110 and the gate lines 112 are corresponding to columns and rows of the matrix. In addition, an equivalent circuit resulted from the two substrates of the LCD panel 100 can be regarded as a plurality of equivalent capacitors 116. Each of the plurality of equivalent capacitors 116 comprises at least a liquid crystal capacitor and at least a storage capacitor, and functions to act as a storage unit.

**[0007]** The power circuit 150 comprises a plurality of level shifters 151, 152, and 153 for converting a vertical start logic signal STV, a first clock logic signal CLK1L, and a second clock logic signal CLK2L into a vertical start signal ST, a first

clock signal CLK1, and a second clock signal CLK2 respectively. The vertical start signal ST, the first clock signal CLK1, and the second clock signal CLK2 are furnished to the gate driving circuit 106. Besides, the power circuit 150 transfers a low-level gate signal reference voltage Vgl to the gate driving circuit 106.

**[0008]** The operation principle for driving the prior-art TFT-LCD device 10 is briefed as the following. When the power circuit 150 receives the vertical start logic signal STV, the first clock logic signal CLK1L, and the second clock logic signal CLK2L, the high/low logic levels of the signals STV, CLK1L, and CLK2L are converted to the high-level/low-level gate signal reference voltages by the power circuit 150 so as to generate the vertical start signal ST, the first clock signal CLK1, and the second clock signal CLK2 forwarded to the gate driving circuit 106. Thereafter, the gate driving circuit 106 and the source driving circuit 104 are able to generate gate signals and data signals furnished to the corresponding gate lines 112 and data lines 110 for controlling the operations of the thin film transistors 114 and the voltage drops across the equivalent capacitors 116. The twisted angles of liquid crystal molecules corresponding to the equivalent capacitors 116 are then changed in response to the voltage drops, and hence the corresponding transparency of the liquid crystal layers can be changed accordingly for illustrating images.

**[0009]** For instance, when the gate driving circuit 106 forwards a gate signal to a gate line 112 for turning on corresponding thin film transistors 114, the data signals forwarded to the data lines 110 by the source driving circuit 104 can be furnished to the corresponding equivalent capacitors 116 via the corresponding thin film transistors 114 being turned on. Consequently, the gray levels of corresponding pixels can be controlled based on the data signals.

**[0010]** However, upon turning off the TFT-LCD device 10, the electric charges accumulated in the equivalent capacitors 116 cannot be discharged rapidly and can only be released through the leakage currents of the thin film transistors 114, which is a time-consuming discharging process. That is, the displayed image cannot vanish immediately after power-off and will persist for a relatively long time, which is known as the residual image effect. The residual image displayed on the TFT-LCD device 10 may cause an unpleasant visual experience.

## SUMMARY OF THE INVENTION

**[0011]** In accordance with an embodiment of the present invention, a liquid crystal display device for decaying residual image upon power-off is provided. The liquid crystal display device comprises a source driving circuit, a gate driving circuit, a plurality of parallel data lines, a plurality of parallel gate lines, a plurality of storage units, a plurality of data switches, a reset circuit, and a power circuit.

**[0012]** The source driving circuit is utilized for generating a plurality of data signals corresponding to an image to be displayed. The gate driving circuit is utilized for generating a plurality of gate signals. The plurality of parallel data lines are coupled to the source driving circuit. Each data line is used to receive a corresponding data signal. The plurality of parallel gate lines are coupled to the gate driving circuit and are crossed with the plurality of data lines perpendicularly. Each gate line is used to receive a corresponding gate signal. Each storage unit comprises a first terminal coupled to one corresponding data switch, and a second terminal for receiving a common voltage. Each data switch comprises a first terminal

coupled to one corresponding storage unit, a second terminal coupled to one corresponding data line, and a control terminal coupled to one corresponding gate line. The reset circuit comprises a first input terminal for receiving a first clock logic signal, a second input terminal for receiving a second clock logic signal, a third input terminal for receiving a reset signal, a first output terminal, a second output terminal, and a third output terminal, wherein the first output terminal outputs the first clock signal, the second output terminal outputs the second clock signal, and the third output terminal outputs a low-level logic signal when the reset signal is a high-level logic signal, or alternatively, the first output terminal, the second output terminal and the third output terminal are set to output the high-level logic signal when the reset signal is a low-level logic signal. The power circuit comprises a first input terminal for receiving a vertical start logic signal, a second input terminal coupled to the first output terminal of the reset circuit, a third input terminal coupled to the second output terminal of the reset circuit, a fourth input terminal coupled to the third output terminal of the reset circuit, a first output terminal coupled to the gate driving circuit for outputting a vertical start signal, a second output terminal coupled to the gate driving circuit for outputting a first clock signal or a high-level gate signal reference voltage based on the logic signal outputted from the first output terminal of the reset circuit, a third output terminal coupled to the gate driving circuit for outputting a second clock signal or the high-level gate signal reference voltage based on the logic signal outputted from the second output terminal of the reset circuit, and a fourth output terminal coupled to the gate driving circuit for outputting a gate signal reference voltage based on the logic signal outputted from the third output terminal of the reset circuit.

**[0013]** The present invention further provides a liquid crystal display device for decaying residual image. The liquid crystal display device comprises a source driving circuit, a gate driving circuit, a plurality of parallel data lines, a plurality of parallel gate lines, a plurality of storage units, a plurality of data switches, a power circuit, and a charging/discharging module.

**[0014]** The source driving circuit is utilized for generating a plurality of data signals corresponding to an image to be displayed. The gate driving circuit is utilized for generating a plurality of gate signals. The gate driving circuit comprises an input terminal for receiving a low-level gate signal reference voltage. The plurality of parallel data lines are coupled to the source driving circuit. Each data line is used to receive a corresponding data signal. The plurality of parallel gate lines are coupled to the gate driving circuit and are crossed with the plurality of data lines perpendicularly. Each gate line is used to receive a corresponding gate line. Each storage unit comprises a first terminal coupled to one corresponding data line, and a second terminal for receiving a common voltage. Each data switch comprises a first terminal coupled to one corresponding storage unit, a second terminal coupled to one corresponding data line, and a control terminal coupled to one corresponding gate line. The power circuit comprises a first input terminal for receiving a vertical start logic signal, a second input terminal for receiving a first clock logic signal, a third input terminal for receiving a second clock logic signal, a first output terminal coupled to the gate driving circuit for outputting a vertical start signal, a second output terminal coupled to the gate driving circuit for outputting a first clock signal, and a third output terminal coupled to the

gate driving circuit for outputting a second clock signal. The charging/discharging module is coupled to the plurality of gate lines for receiving a high-level gate signal reference voltage and a reset signal. The charging/discharging module outputs the high-level gate signal reference voltage to the plurality of gate lines when the reset signal is enabled.

**[0015]** Furthermore, the present invention provides a method for decaying residual image of a liquid crystal display device. The method comprises enabling a reset signal upon turning off the liquid crystal display device, setting a gate signal of each gate line of a plurality of gate lines of the liquid crystal display device based on the reset signal being enabled, turning on each data switch of a plurality of data switches of the liquid crystal display device based on one corresponding gate signal being set, and performing a discharging process on each storage unit of a plurality of storage units of the liquid crystal display device based on one corresponding data switch being turned on.

**[0016]** These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0017]** FIG. 1 is a diagram schematically showing the structure of a prior-art thin film transistor liquid crystal display (TFT-LCD) device.

**[0018]** FIG. 2 is a diagram schematically showing the structure of a liquid crystal display device capable of fast decaying residual image in accordance with a first embodiment of the present invention.

**[0019]** FIG. 3 shows the related signal waveforms concerning the operation of the LCD device in FIG. 2, having time along the abscissa.

**[0020]** FIG. 4 is a diagram schematically showing the structure of a liquid crystal display device capable of fast decaying residual image in accordance with a second embodiment of the present invention.

**[0021]** FIG. 5 is a circuit diagram showing the structure of the controllable switch in FIG. 4 in accordance with an embodiment of the present invention.

**[0022]** FIG. 6 is a circuit diagram showing the structure of the controllable switch in FIG. 4 in accordance with another embodiment of the present invention.

**[0023]** FIG. 7 is a flowchart depicting a method for fast decaying residual image of a liquid crystal display device in accordance with an embodiment of the present invention.

#### DETAILED DESCRIPTION

**[0024]** Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings. Here, it is to be noted that the present invention is not limited thereto. Furthermore, the step serial numbers concerning the method for fast decaying residual image of a liquid crystal display are not meant thereto limit the operating sequence, and any rearrangement of the operating sequence for achieving same functionality is still within the spirit and scope of the invention.

**[0025]** FIG. 2 is a diagram schematically showing the structure of a liquid crystal display device for fast decaying residual image in accordance with a first embodiment of the present invention. As shown in FIG. 2, the LCD device 20

comprises a liquid crystal display panel **200**, a power circuit **250**, a source driving circuit **204**, a gate driving circuit **206**, a reset circuit **260**, and a voltage generator **208**. The source driving circuit **204** is utilized to provide a plurality of data signals for displaying images, and the gate driving circuit **206** is utilized to provide a plurality of gate signals.

**[0026]** The liquid crystal display panel **200** comprises two substrates, and liquid crystal layers are stuffed between the substrates. One substrate is disposed with a plurality of data lines **210**, a plurality of gate lines **212** perpendicular to the data lines **210**, and a plurality of thin film transistors **214**. The other substrate is disposed with a common electrode for receiving a common voltage  $V_{com}$  provided by the voltage generator **208**. The plurality of data lines **210** are coupled to the source driving circuit **204**, and each of the plurality of data lines **210** receives a corresponding data signal provided by the source driving circuit **204**. The plurality of gate lines **212** are coupled to the gate driving circuit **206**, and each of the plurality of gate lines **212** receives a corresponding gate signal provided by the gate driving circuit **206**.

**[0027]** For the sake of elucidation, FIG. 2 still reveals only four thin film transistors **214**, but in a real case, there is one thin film transistor **214** disposed at each intersection of a data line **210** and a gate line **212** on the LCD panel **200**. In other words, the plurality of thin film transistors **214**, each corresponding to a pixel of the LCD device **20**, form a matrix on the LCD panel **200**, and the data lines **210** and the gate lines **212** are corresponding to columns and rows of the matrix. Similarly, a circuit effect resulted from the two substrates of the LCD panel **200** can be regarded as a plurality of equivalent capacitors **216**. Each of the plurality of equivalent capacitors **216** comprises at least a liquid crystal capacitor and at least a storage capacitor connected in parallel, and functions to act as a storage unit, which has a first terminal coupled to one corresponding data line and a second terminal for receiving the common voltage  $V_{com}$ . Each thin film transistor **214** comprises a first terminal coupled to one corresponding equivalent capacitor **216**, a second terminal coupled to one corresponding data line **210**, and a control terminal coupled to one corresponding gate line **212**. Each thin film transistor **214** functions as a data switch for controlling a signal connection between the first terminal and the second terminal according to a gate signal received by the control terminal from one corresponding gate line **212**, which in turn controls data signal transmission from one corresponding data line **210** to the one corresponding equivalent capacitor **216**.

**[0028]** The reset circuit **260** comprises a first input terminal for receiving a first clock logic signal  $CLK1L$ , a second input terminal for receiving a second clock logic signal  $CLK2L$ , a third input terminal for receiving a reset signal  $XON$ , a first output terminal, a second output terminal, and a third output terminal. When the reset signal  $XON$  is a high-level logic signal, the first output terminal of the reset circuit **260** forwards the first clock logic signal  $CLK1L$  to the power circuit **250**, the second output terminal of the reset circuit **260** forwards the second clock logic signal  $CLK2L$  to the power circuit **250**, and the third terminal forwards a low-level logic signal to the power circuit **250**. When the reset signal  $XON$  is a low-level logic signal, all the first, second, and third output terminals of the reset circuit **260** are set to forward high-level logic signals to the power circuit **250**.

**[0029]** In one preferred embodiment, the reset circuit **260** comprises a buffer **263**, a first OR gate **261**, and a second OR gate **262**. The buffer **263** comprises an input terminal coupled

to the third input terminal of the reset circuit **260** for receiving the reset signal  $XON$ , and an output terminal coupled to the third output terminal of the reset circuit **260** for outputting an inverted signal of the reset signal  $XON$ . In the embodiment shown in FIG. 2, the reset signal  $XON$  is a low-level enabled signal, and hence the buffer **263** is an inverting buffer. In another embodiment, if the reset signal  $XON$  is a high-level enabled signal, then the buffer **263** is a non-inverting buffer. The first OR gate **261** comprises a first input terminal coupled to the first input terminal of the reset circuit **260** for receiving the first clock logic signal  $CLK1L$ , a second input terminal coupled to the output terminal of the buffer **263**, and an output terminal coupled to the first output terminal of the reset circuit **260**. The second OR gate **262** comprises a first input terminal coupled to the second input terminal of the reset circuit **260** for receiving the second clock logic signal  $CLK2L$ , a second input terminal coupled to the output terminal of the buffer **263**, and an output terminal coupled to the second output terminal of the reset circuit **260**.

**[0030]** The power circuit **250** comprises a plurality of input terminals and a plurality of corresponding output terminals. The power circuit **250** converts the low-level logic voltage of each input signal into a low-level gate signal reference voltage  $V_{gl}$ , and converts the high-level logic voltage of each input signal into a high-level gate signal reference voltage  $V_{gh}$ . In one preferred embodiment, the power circuit **250** comprises a plurality of level shifters **251-254**. The level shifter **251** comprises an input terminal for receiving a vertical start logic signal  $STV$ , an output terminal coupled to the gate driving circuit **206** for outputting a vertical start signal  $ST$ , a high-level input terminal for receiving the high-level gate signal reference voltage  $V_{gh}$ , and a low-level input terminal for receiving the low-level gate signal reference voltage  $V_{gl}$ . The level shifter **252** comprises an input terminal coupled to the first output terminal of the reset circuit **260**, an output terminal coupled to the gate driving circuit **206** for outputting a first clock signal  $CLK1$  or the high-level gate signal reference voltage  $V_{gh}$ , a high-level input terminal for receiving the high-level gate signal reference voltage  $V_{gh}$ , and a low-level input terminal for receiving the low-level gate signal reference voltage  $V_{gl}$ .

**[0031]** The level shifter **253** comprises an input terminal coupled to the second output terminal of the reset circuit **260**, an output terminal coupled to the gate driving circuit **206** for outputting a second clock signal  $CLK2$  or the high-level gate signal reference voltage  $V_{gh}$ , a high-level input terminal for receiving the high-level gate signal reference voltage  $V_{gh}$ , and a low-level input terminal for receiving the low-level gate signal reference voltage  $V_{gl}$ . The level shifter **254** comprises an input terminal coupled to the third output terminal of the reset circuit **260**, an output terminal coupled to the gate driving circuit **206** for outputting a gate signal reference voltage  $V_{ss}$ , a high-level input terminal for receiving the high-level gate signal reference voltage  $V_{gh}$ , and a low-level input terminal for receiving the low-level gate signal reference voltage  $V_{gl}$ .

**[0032]** FIG. 3 shows the related signal waveforms concerning the operation of the LCD device **20** in FIG. 2, having time along the abscissa. The signal waveforms in FIG. 3, from top to bottom, are the reset signal  $XON$ , the first clock signal  $CLK1$ , the second clock signal  $CLK2$ , the gate signal reference voltage  $V_{ss}$ , and the gate signal  $SGn$ . The operation principle of the LCD device **20** for fast decaying residual

image is detailed with reference to the related timing diagram shown in FIG. 3 as the following.

[0033] In normal operation after power-on, the reset signal XON is a high-level logic signal, and hence the buffer 263 outputs a low-level logic signal. Accordingly, the first clock logic signal CLK1L and the second clock logic signal CLK2L can be forwarded to the power circuit 250 via the first OR gate 261 and the second OR gate 262 respectively according to the low-level logic signal outputted from the buffer 263. The power circuit 250 performs signal level conversion processes on the first clock logic signal CLK1L and the second clock logic signal CLK2L for generating the first clock signal CLK1 and the second clock signal CLK2. The reset signal XON undergoes an inverting process by the buffer 263 and a signal level conversion process by the level shifter 254 so as to set the gate signal reference voltage Vss as a low-level gate signal reference voltage Vgl. Besides, the level shifter 251 performs a signal level conversion process on the vertical start logic signal STV for generating the vertical start signal ST. Therefore, the gate driving circuit 206 is able to generate a plurality of gate signals, such as SGn-1, SGn, SGn+1, etc., furnished to the corresponding gate lines 212 based on the vertical start signal ST, the first clock signal CLK1, the second clock signal CLK2, and the gate signal reference voltage Vss. Accordingly, gate scanning processes can be operated normally for illustrating the images to be displayed.

[0034] Upon turning off the LCD device 20 at time Toff, the reset signal XON switches from the high-level logic signal to a low-level logic signal, and hence the output of the buffer 263 switches from the low-level logic signal to a high-level logic signal. Accordingly, both the outputs of the first OR gate 261 and the second OR gate 262 turn out to be high-level logic signals, which means that both the first clock logic signal CLK1L and the second clock logic signal CLK2L cannot be forwarded to the power circuit 250 via the reset circuit 260. Consequently, the first clock signal CLK1 and the second clock signal CLK2 are switched to high-level signals. Meanwhile, the gate signal reference voltage Vss is also switched to a high-level signal. That is, all the gate signals on the gate lines 212 are switched to high-level signals for switching on all the thin film transistors 214, and the accumulated charges of all the equivalent capacitors 216 can be discharged speedily. It is noted that the voltage of the high-level signal can not reach the high-level gate signal reference voltage Vgh due to power-off, and the voltage of the high-level signal decreases with time as shown in FIG. 3. However, by making use of the residual power after power-off for switching on all the thin film transistors 214, fast decaying residual image by fast discharging the accumulated charges of all the equivalent capacitors 216 via the thin film transistors 214 can be achieved.

[0035] FIG. 4 is a diagram schematically showing the structure of a liquid crystal display device for fast decaying residual image in accordance with a second embodiment of the present invention. As shown in FIG. 4, the LCD device 40 comprises a liquid crystal display panel 400, a power circuit 450, a source driving circuit 404, a gate driving circuit 406, a charging/discharging module 480, and a voltage generator 408. The source driving circuit 404 is utilized to provide a plurality of data signals for displaying images, and the gate driving circuit 406 is utilized to provide a plurality of gate signals.

[0036] The liquid crystal display panel 400 comprises two substrates, and liquid crystal layers are stuffed between the

substrates. One substrate is disposed with a plurality of data lines 410, a plurality of gate lines 412 perpendicular to the data lines 410, and a plurality of thin film transistors 414. The other substrate is disposed with a common electrode for receiving a common voltage Vcom provided by the voltage generator 408.

[0037] For the sake of elucidation, FIG. 4 still reveals only four thin film transistors 414, but in a real case, there is one thin film transistor 414, corresponding to a pixel of the LCD device 40, disposed at each intersection of a data line 410 and a gate line 412 on the LCD panel 400. Similarly, a circuit effect resulted from the two substrates of the LCD panel 400 can be regarded as a plurality of equivalent capacitors 416. Each of the plurality of equivalent capacitors 416 comprises at least a liquid crystal capacitor and at least a storage capacitor connected in parallel, and functions to act as a storage unit coupled between one corresponding thin film transistor 414 and the voltage generator 408.

[0038] The power circuit 450 comprises a plurality of level shifters 451-453. The level shifter 451 comprises an input terminal for receiving a vertical start logic signal STV, an output terminal coupled to the gate driving circuit 406 for outputting a vertical start signal ST, a high-level input terminal for receiving the high-level gate signal reference voltage Vgh, and a low-level input terminal for receiving the low-level gate signal reference voltage Vgl. The level shifter 452 comprises an input terminal for receiving a first clock logic signal CLK1L, an output terminal coupled to the gate driving circuit 406 for outputting a first clock signal CLK1, a high-level input terminal for receiving the high-level gate signal reference voltage Vgh, and a low-level input terminal for receiving the low-level gate signal reference voltage Vgl.

[0039] The level shifter 453 comprises an input terminal for receiving a second clock logic signal CLK2L, an output terminal coupled to the gate driving circuit 406 for outputting a second clock signal CLK2, a high-level input terminal for receiving the high-level gate signal reference voltage Vgh, and a low-level input terminal for receiving the low-level gate signal reference voltage Vgl. Besides, the power circuit 450 may also be used to transfer a low-level gate signal reference voltage Vgl to the gate driving circuit 406. In another embodiment, the low-level gate signal reference voltage Vgl is furnished to the gate driving circuit 406 directly without the aid of the power circuit 450.

[0040] The charging/discharging module 480 comprises an inverting level shifter 495, a plurality of controllable switches 490, a power line 491, and a control signal line 492. The inverting level shifter 495 comprises an input terminal for receiving a reset signal XON, an output signal coupled to the control signal line 492, a high-level input terminal for receiving the high-level gate signal reference voltage Vgh, and a low-level input terminal for receiving the low-level gate signal reference voltage Vgl. The inverting level shifter 495 performs an inverting process and a level conversion process on the reset signal XON for generating a control signal. The control signal is transferred to the plurality of controllable switches 490 via the control signal line 492. It is noted that the reset signal XON is a low-level enabled signal for the embodiment shown in FIG. 4. However, in other embodiments, if the reset signal XON is a high-level enabled signal, then the inverting level shifter 495 should be replaced with a non-inverting level shifter. Each of the plurality of controllable switches 490 comprises an output terminal coupled to one corresponding gate line 412, an input terminal coupled to the

power line 491 for receiving the high-level gate signal reference voltage  $V_{gh}$ , and a control terminal coupled to the control signal line 492 for receiving the control signal.

[0041] FIG. 5 is a circuit diagram showing the structure of the controllable switch 490 in FIG. 4 in accordance with an embodiment of the present invention. The controllable switch 490 in FIG. 5 comprises a transistor 590. The transistor 590 comprises a first terminal coupled to one corresponding gate line 412, a second terminal coupled to the power line 491, and a control terminal coupled to the control signal line 492. The transistor 590 can be a thin film transistor, a MOS field effect transistor, or a bipolar junction transistor.

[0042] FIG. 6 is a circuit diagram showing the structure of the controllable switch 490 in FIG. 4 in accordance with another embodiment of the present invention. The controllable switch 490 in FIG. 6 comprises a first transistor 690 and a second transistor 691. The first transistor 690 comprises a first terminal coupled to one corresponding gate line 412, a second terminal coupled to the power line 491, and a control terminal. The first transistor 690 can be a thin film transistor, a bipolar junction transistor, or a MOS field effect transistor. The second transistor 691 comprises a first terminal coupled to the control terminal of the first transistor 690, a control terminal coupled to the control signal line 492, and a second terminal coupled to the control terminal of the second transistor 691. The second transistor 691 can be a thin film transistor, a bipolar junction transistor, or a MOS field effect transistor. When both the first transistor 690 and the second transistor 691 are MOS field effect transistors and are turned on by the control signal via the control signal line 492, the second transistor 691 will be turned off immediately after the first transistor 690 is turned on due to voltage bootstrap effect on the gate capacitor of the first transistor 690. Accordingly, the gate-source driving voltage of the first transistor 690 is sustained for retaining a high discharging efficiency.

[0043] The operation principle of the LCD device 40 for fast decaying residual image is detailed as the following. In normal operation after power-on, the reset signal XON is a high-level logic signal, and hence the inverting level shifter 495 outputs a low-level gate signal reference voltage  $V_{gl}$ . Then, the low-level gate signal reference voltage  $V_{gl}$  is furnished to the gates of the controllable switches 490, and the plurality of controllable switches 490 are all turned off for isolating the plurality of gate lines 412 from the power line 491. That is, the high-level gate signal reference voltage  $V_{gh}$  provided by the power line 491 cannot be furnished to the plurality of gate lines 412, and the plurality of gate lines 412 are utilized to receive the gate signals  $SGn-1$ ,  $SGn$ ,  $SGn+1$ , etc., for performing normal scanning operations so as to illustrate the images to be displayed.

[0044] Upon turning off the LCD device 40, the reset signal XON switches from the high-level logic signal to a low-level logic signal, and hence the output of the inverting level shifter 495 switches from the low-level gate signal reference voltage  $V_{gl}$  to a high-level gate signal reference voltage  $V_{gh}$ . Then, the high-level gate signal reference voltage  $V_{gh}$  is furnished to the gates of the controllable switches 490, and the plurality of controllable switches 490 are all turned on for signal connecting between the plurality of gate lines 412 and the power line 491. That is, the high-level gate signal reference voltage  $V_{gh}$  provided via the power line 491 can be furnished to the plurality of gate lines 412. In other words, the gate signals of all the gate lines 412 are switched to have the high-level gate signal reference voltage  $V_{gh}$ , which in turn switch on all the

thin film transistors 414. Accordingly, fast decaying residual image by fast discharging the accumulated charges of all the equivalent capacitors 416 via the thin film transistors 414 can be achieved.

[0045] FIG. 7 is a flowchart depicting a method for fast decaying residual image of a liquid crystal display device in accordance with an embodiment of the present invention. The method comprises the following steps:

[0046] Step S710: enabling a reset signal upon turning off the liquid crystal display device;

[0047] Step S720: setting a gate signal of each gate line of a plurality of gate lines of the liquid crystal display device based on the reset signal being enabled;

[0048] Step S730: turning on each data switch of a plurality of data switches of the liquid crystal display device based on one corresponding gate signal being set; and

[0049] Step S740: performing a discharging process on each storage unit of a plurality of storage units of the liquid crystal display device based on one corresponding data switch being turned on.

[0050] In the method for fast decaying residual image of the liquid crystal display device described above, in the step S710, enabling the reset signal upon turning off the liquid crystal display device comprises switching the reset signal to become a low-level logic signal upon turning off the liquid crystal display device. In the step S720, setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled comprises setting a high-level signal to the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled. The step S720 may further comprise decoupling the gate lines from at least one input clock signal.

[0051] Furthermore, the step S720 may comprise furnishing a high-level gate signal reference voltage directly to each gate line of the plurality of gate lines of the liquid crystal display device by a charging/discharging module based on the reset signal being enabled. Alternatively, the step S720 may comprise setting a high-level gate signal reference voltage to the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device by a reset circuit coupled to a gate driving circuit of the liquid crystal display device based on the reset signal being enabled.

[0052] In the step S730, turning on each data switch of the plurality of data switches of the liquid crystal display device based on one corresponding gate signal being set comprises turning on each thin film transistor of a plurality of thin film transistors of the liquid crystal display device based on one corresponding gate signal being set. In the step S740, performing the discharging process on each storage unit of a plurality of storage units of the liquid crystal display device based on one corresponding data switch being turned on comprises performing the discharging process on each liquid crystal capacitor and each storage capacitor of the plurality of storage units coupled to one corresponding data switch being turned on.

[0053] In summary, by way of enabling a reset signal for setting the gate signals of a plurality of gate lines of a liquid crystal display device upon turning off the liquid crystal display device, discharging processes on all the storage units of the liquid crystal display device for fast decaying residual image can be performed via the data switches of the liquid crystal display turned on by the gate signals being set. The reset operation for performing discharging processes in

response to the reset signal being enabled can be carried out based on a reset circuit for setting all the gate signals to become high-level signals, or alternatively, based on a charging/discharging module for furnishing a high-level voltage directly to all the gate lines.

**[0054]** Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A method for driving a liquid crystal display device comprising:

enabling a reset signal upon turning off the liquid crystal display device;  
 setting a gate signal of each gate line of a plurality of gate lines of the liquid crystal display device based on the reset signal being enabled;  
 turning on each data switch of a plurality of data switches of the liquid crystal display device based on one corresponding gate signal being set; and  
 performing a discharging process on each storage unit of a plurality of storage units of the liquid crystal display device based on one corresponding data switch being turned on.

2. The method of claim 1, wherein enabling the reset signal upon turning off the liquid crystal display device comprises switching the reset signal to become a low-level logic signal or a high-level logic signal upon turning off the liquid crystal display device.

3. The method of claim 1, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled comprises setting a high-level gate signal reference voltage to the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled.

4. The method of claim 1, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled comprises furnishing a high-level gate signal reference voltage directly to each gate line of the plurality of gate lines of the liquid crystal display device by a charging/discharging module coupled to the gate lines based on the reset signal being enabled.

5. The method of claim 1, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled comprises providing a first clock signal, a second clock signal, and a gate signal reference voltage with a high voltage level to a gate driving circuit generating the gate signal of each gate line such that the gate signal of each gate line is switched to the high voltage level in response to the gate driving circuit receiving the first clock signal, the second clock signal, and the gate signal reference voltage with the high voltage level.

6. The method of claim 5, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled further comprises providing the reset signal being enabled upon turning off the liquid crystal display device to a reset circuit which receives a first clock logic signal, a second clock logic signal and the reset signal being enabled.

7. The method of claim 6, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled further comprises: forwarding a first high-level logic output signal, a second high-level logic output signal and a third high-level logic output signal from the reset circuit to a power circuit in response to enabling the reset signal.

8. The method of claim 7, wherein the first high-level output logic signal is generated according to the first clock logic signal and the reset signal being enabled;

the second high-level output logic signal is generated according to the second clock logic signal and the reset signal being enabled; and

the third high-level logic output signal is generated according to the reset signal being enabled.

9. The method of claim 8 further comprising forwarding the first clock logic signal, the second clock logic signal and a low-level logic signal from the reset circuit to the power circuit before enabling the reset signal.

10. The method of claim 9, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled further comprises providing the first clock signal, the second clock signal, and the gate signal reference voltage with the high voltage level from the power circuit to the gate driving circuit in response to receiving the first high-level output logic signal, the second high-level output logic signal, and the third high-level logic output signal.

11. The method of claim 1, wherein the driving method further comprises:

before turning off the liquid crystal display device, providing a first clock signal and a second clock signal to a gate driving circuit generating the gate signal of each gate line; and

before turning off the liquid crystal display device, providing a gate signal reference voltage with a low voltage level to the gate driving circuit generating the gate signal of each gate line.

12. The method of claim 11, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled comprises:

switching the first clock signal to a first high-level signal; switching the second clock signal to a second high-level signal; and

switching the gate signal reference voltage to a third high-level signal;

providing the first high-level signal, the second high-level signal, and the third high-level signal to the gate driving circuit; and

setting the gate signal of each gate line of the plurality of gate lines in response to receiving the first high-level signal, the second high-level signal, and the third high-level signal of the gate driving circuit.

13. The method of claim 12, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled further comprises providing the reset signal being enabled upon turning off the liquid crystal display device to a reset circuit which receives a first clock logic signal, a second clock logic signal and the reset signal being enabled.

14. The method of claim 13, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled

further comprises: forwarding a first high-level logic output signal, a second high-level logic output signal and a third high-level logic output signal from the reset circuit to a power circuit in response to enabling the reset signal.

**15.** The method of claim **14**, wherein the first high-level output logic signal is generated according to the first clock logic signal and the reset signal being enabled;

the second high-level output logic signal is generated according to the second clock logic signal and the reset signal being enabled; and

the third high-level logic output signal is generated according to the reset signal being enabled.

**16.** The method of claim **15**, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled further comprises providing first high-level signal, the second high-level signal, and the third high-level signal from the

power circuit to the gate driving circuit in response to receiving the first high-level output logic signal, the second high-level output logic signal, and the third high-level logic output signal.

**17.** The method of claim **16**, wherein setting the gate signal of each gate line of the plurality of gate lines of the liquid crystal display device based on the reset signal being enabled comprises providing a high-level first clock signal, a high-level second clock signal, and a high-level gate signal reference voltage to a gate driving circuit generating the gate signal of each gate line such that the gate signal of each gate line is set to turn on each corresponding data switch in response to receiving the high-level first clock signal, high-level second clock signal, and the high-level gate signal reference voltage.

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