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KIM et al.

(54) **LIQUID CRYSTAL DISPLAY**

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(52) **U.S. Cl.**

CPC ***G02F 1/1345*** (2013.01); ***G02F 1/136286*** (2013.01); ***G02F 1/134309*** (2013.01)

(57) **ABSTRACT**

A liquid crystal display according to an exemplary embodiment of the present disclosure includes: a gate line, a data line, and a compensation voltage line disposed on an insulation substrate; a first passivation layer disposed on the gate line, the data line, and the compensation voltage line; a pixel electrode connected to the gate line and the data line, and a compensation electrode connected to the compensation voltage line, disposed on the first passivation layer; and a common electrode formed on the first passivation layer, wherein the compensation electrode overlaps at least a portion of the data line, and the compensation voltage line is formed with the same layer as the data line.

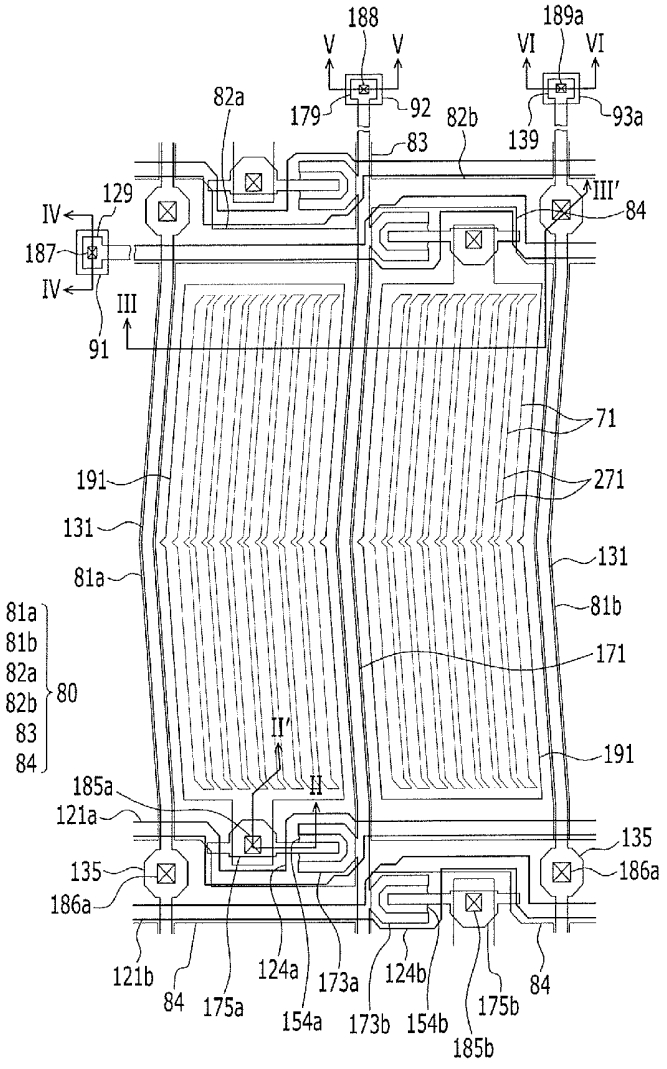
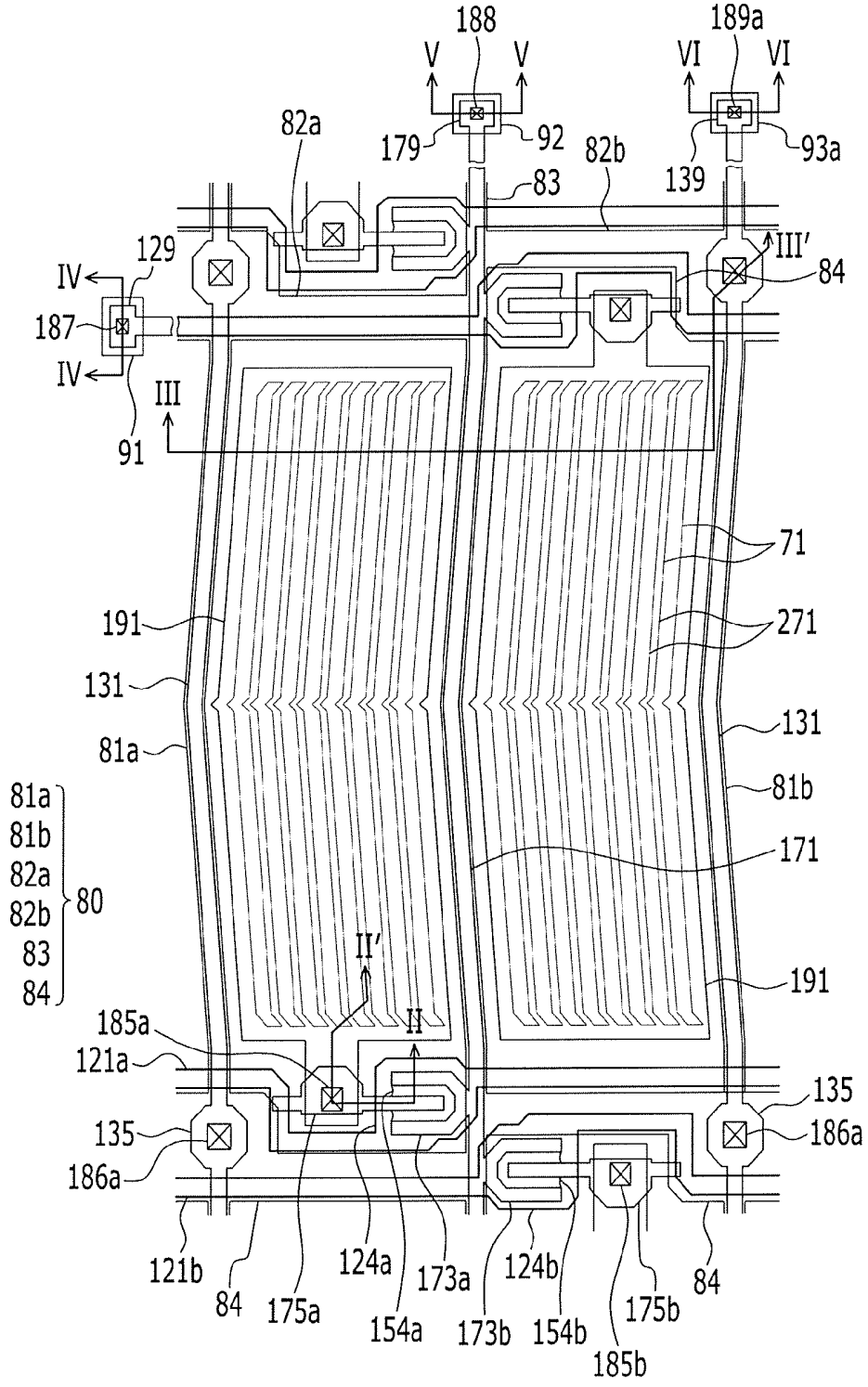


FIG. 1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189a
V
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VI
VI
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82b
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93a
83
129
III′
IV
84
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IV
III
91
71
191
271
131
131
81a
81b
81a
81b
82a
82b
83
84
80
171
II′
191
185a
II
121a
135
135
186a
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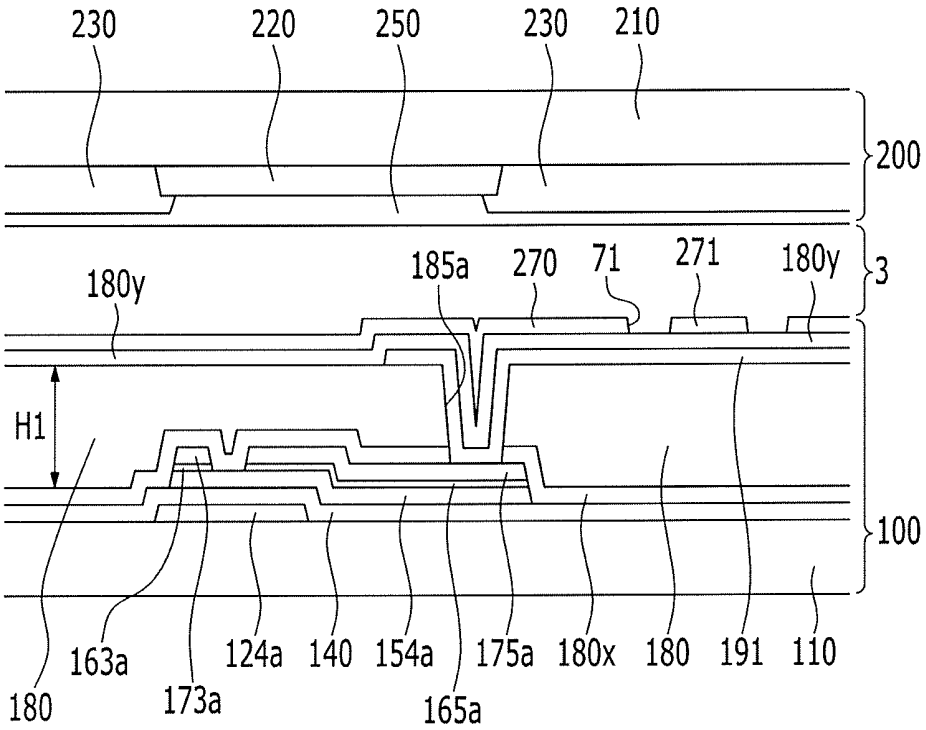
175a
124a
154a
173a
173b
124b
154b
175b
185b
84

FIG. 2


230
220
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200
180y
185a
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71
271
180y
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173a
124a
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165a
175a
180x
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191
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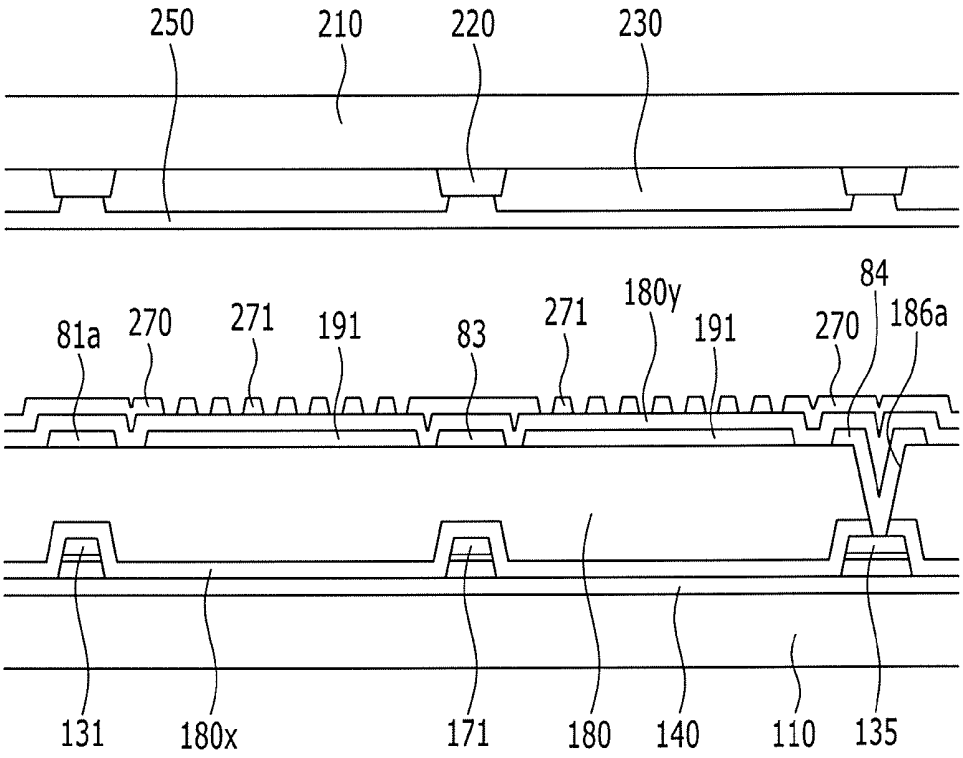
FIG. 3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270
271
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271
180y
191
270
84
186a
131
180x
171
180
140
110
135

FIG. 4

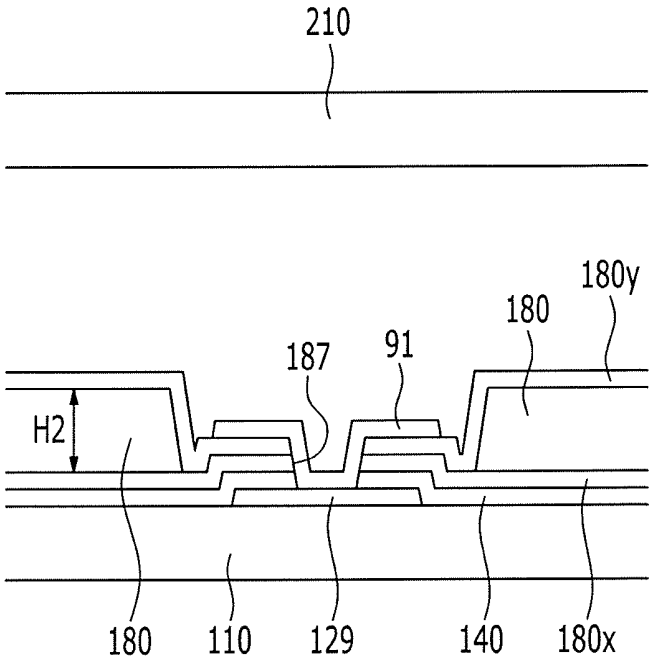


FIG. 5

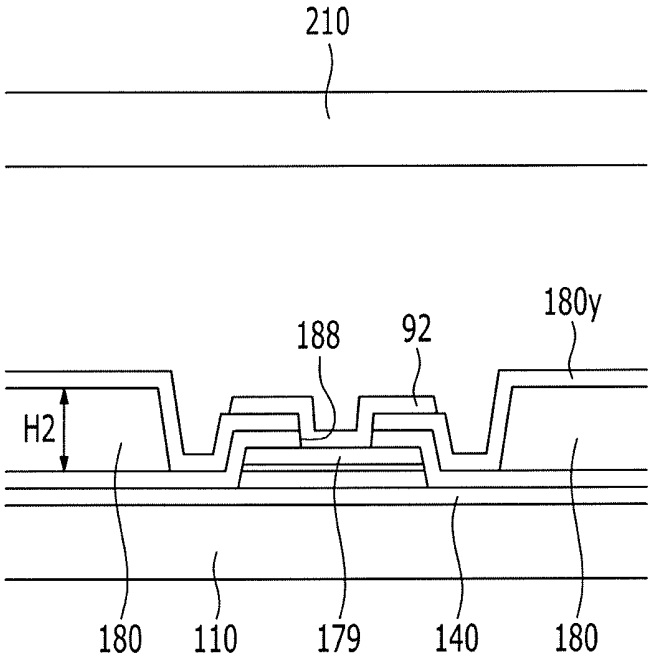


FIG. 6

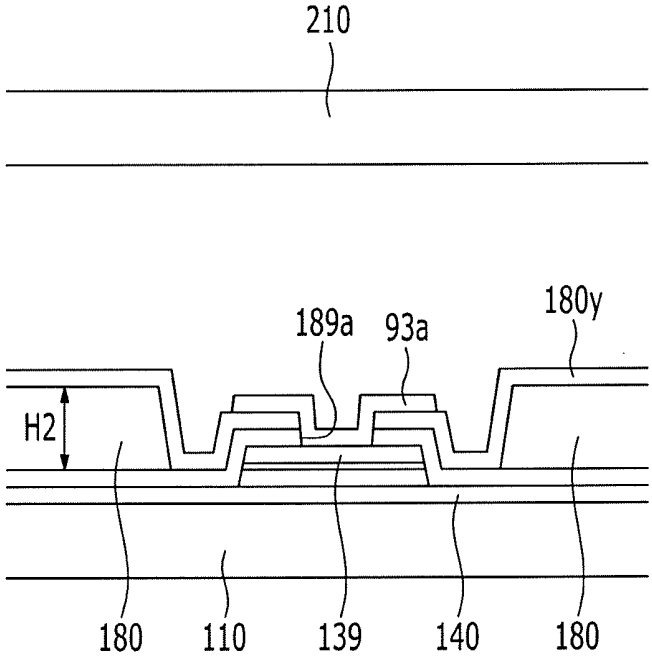


FIG. 7

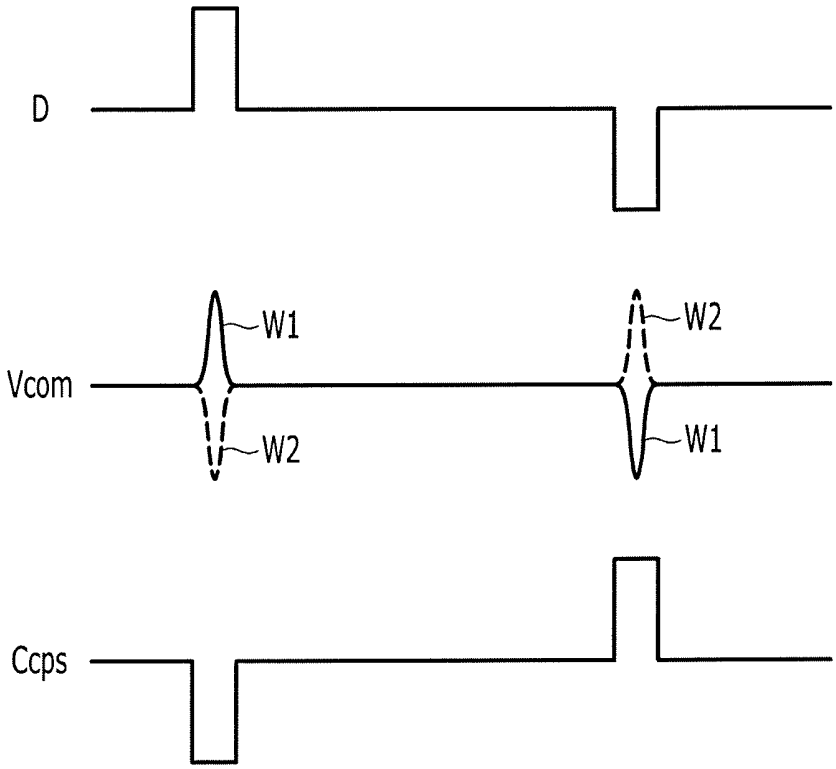
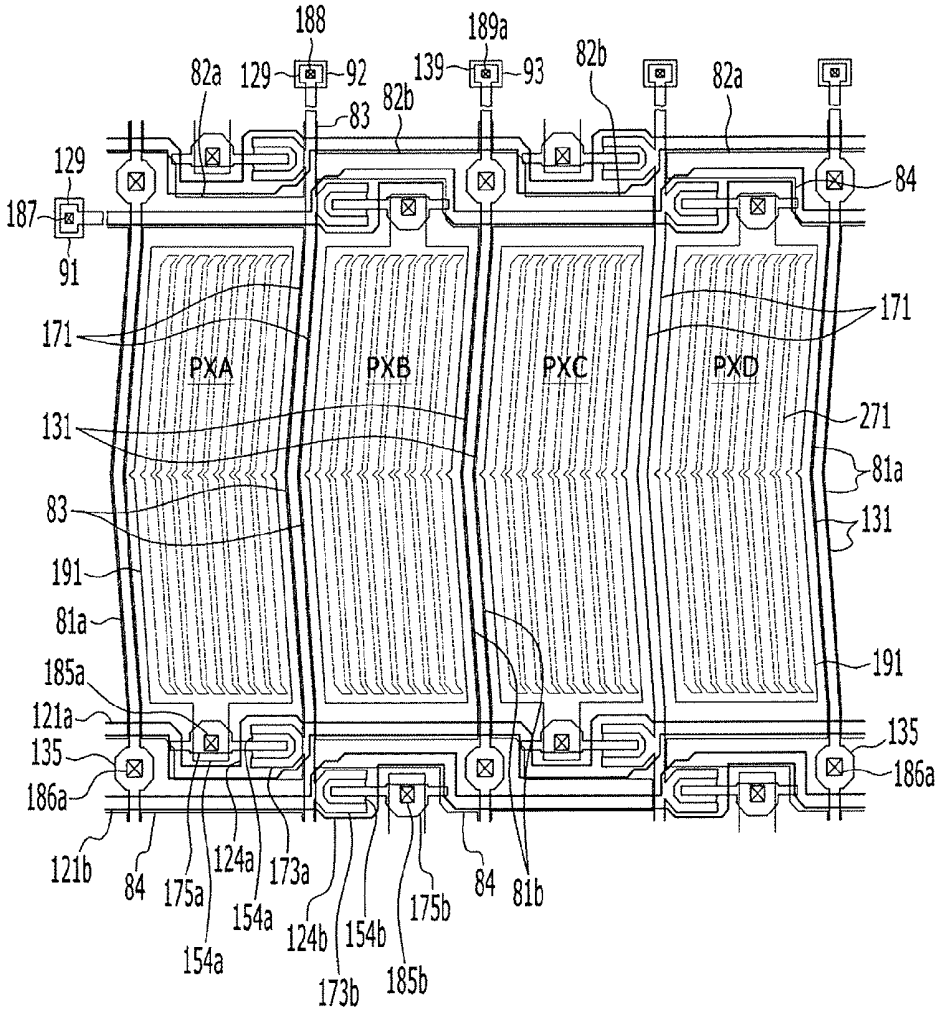


FIG. 8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189a
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82b
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82b
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187
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171
171
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PXB
PXC
PXD
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81a
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81a
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186a
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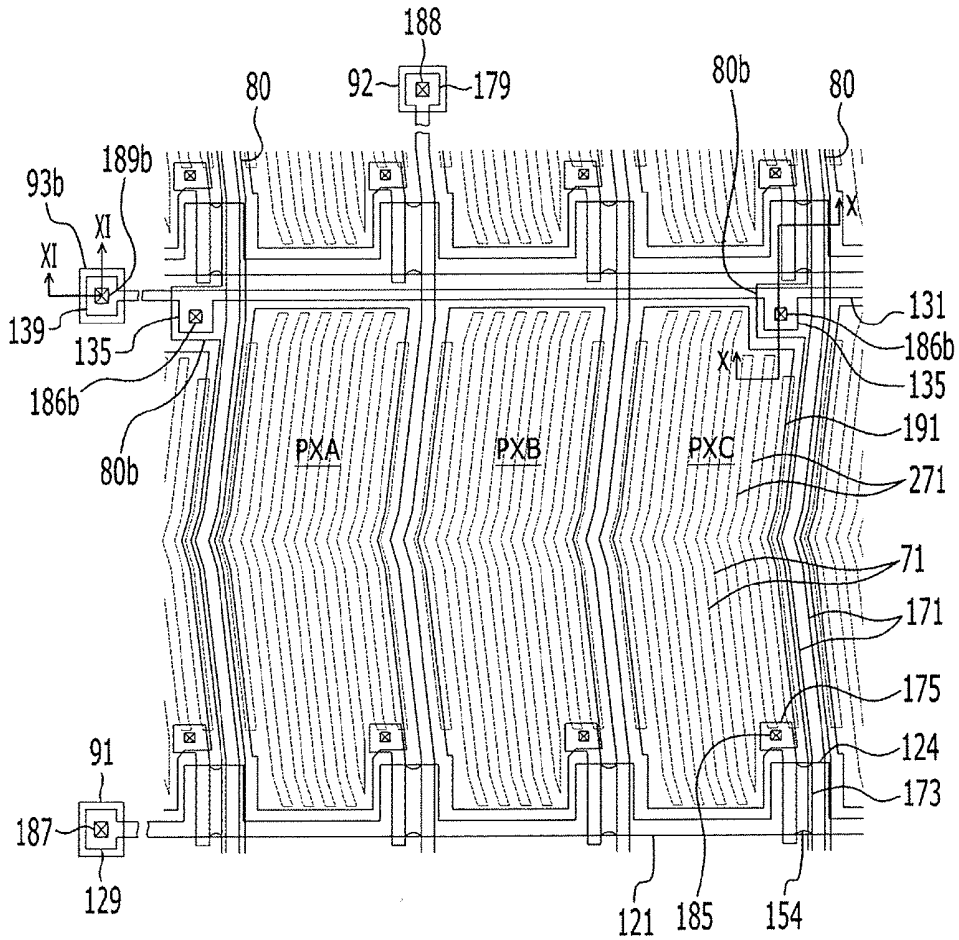
154a
124b
154b
175b
84
81b
173b
185b

FIG. 9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189b
93b
XI
XI
139
135
186b
80b
PXA
PXB
PXC
X
X
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186b
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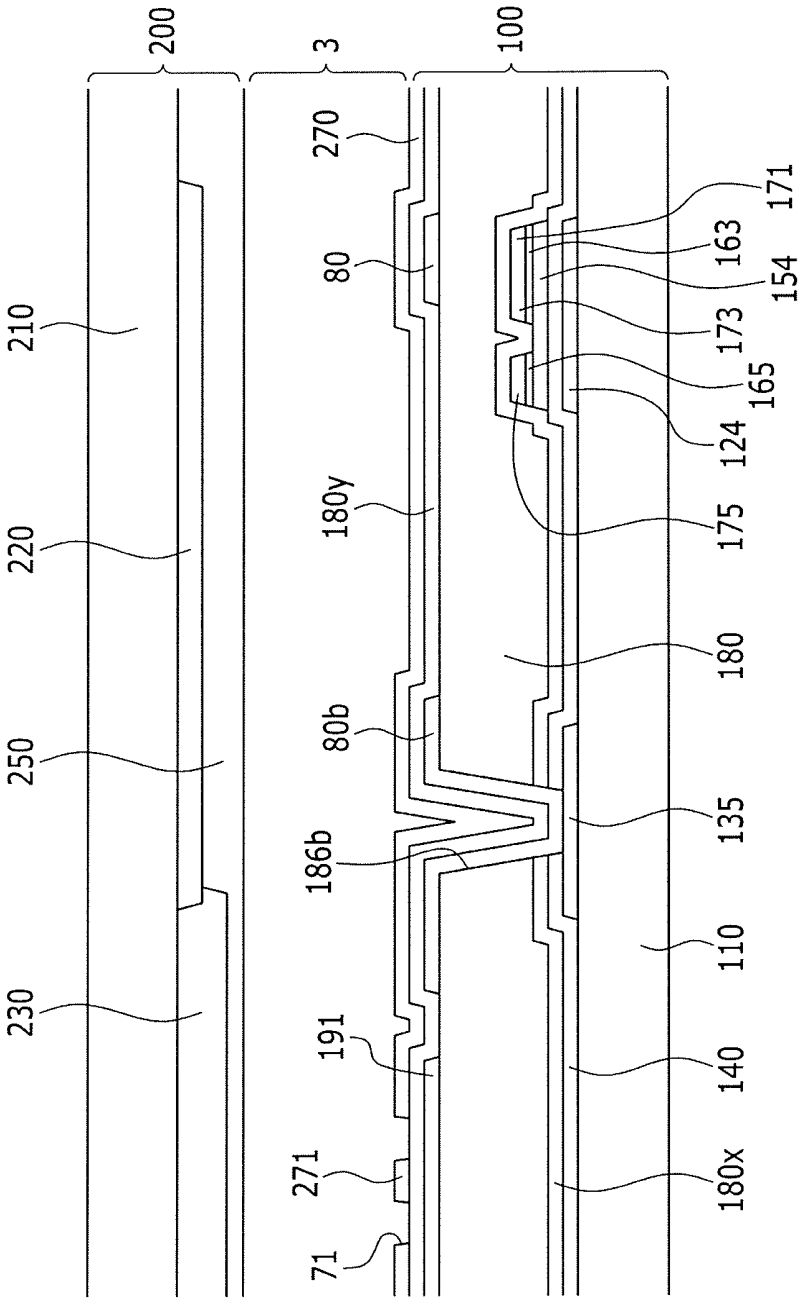
154

FIG. 10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135
110
140
180x

FIG. 11

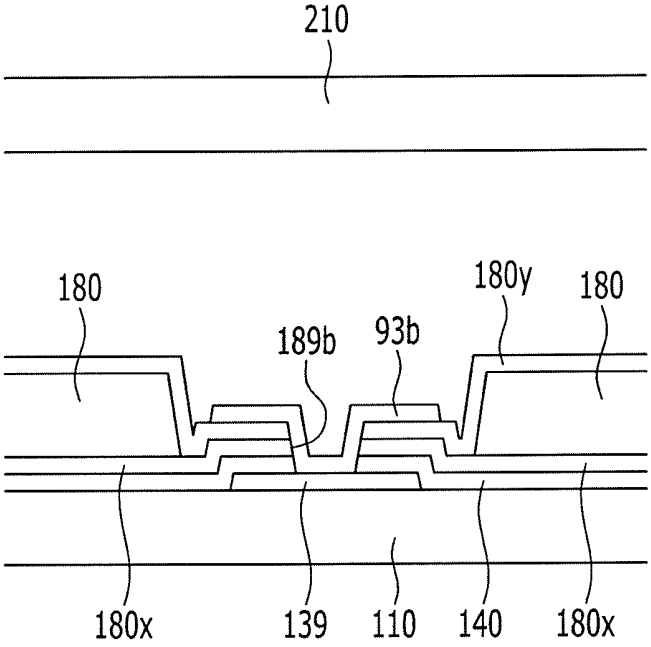
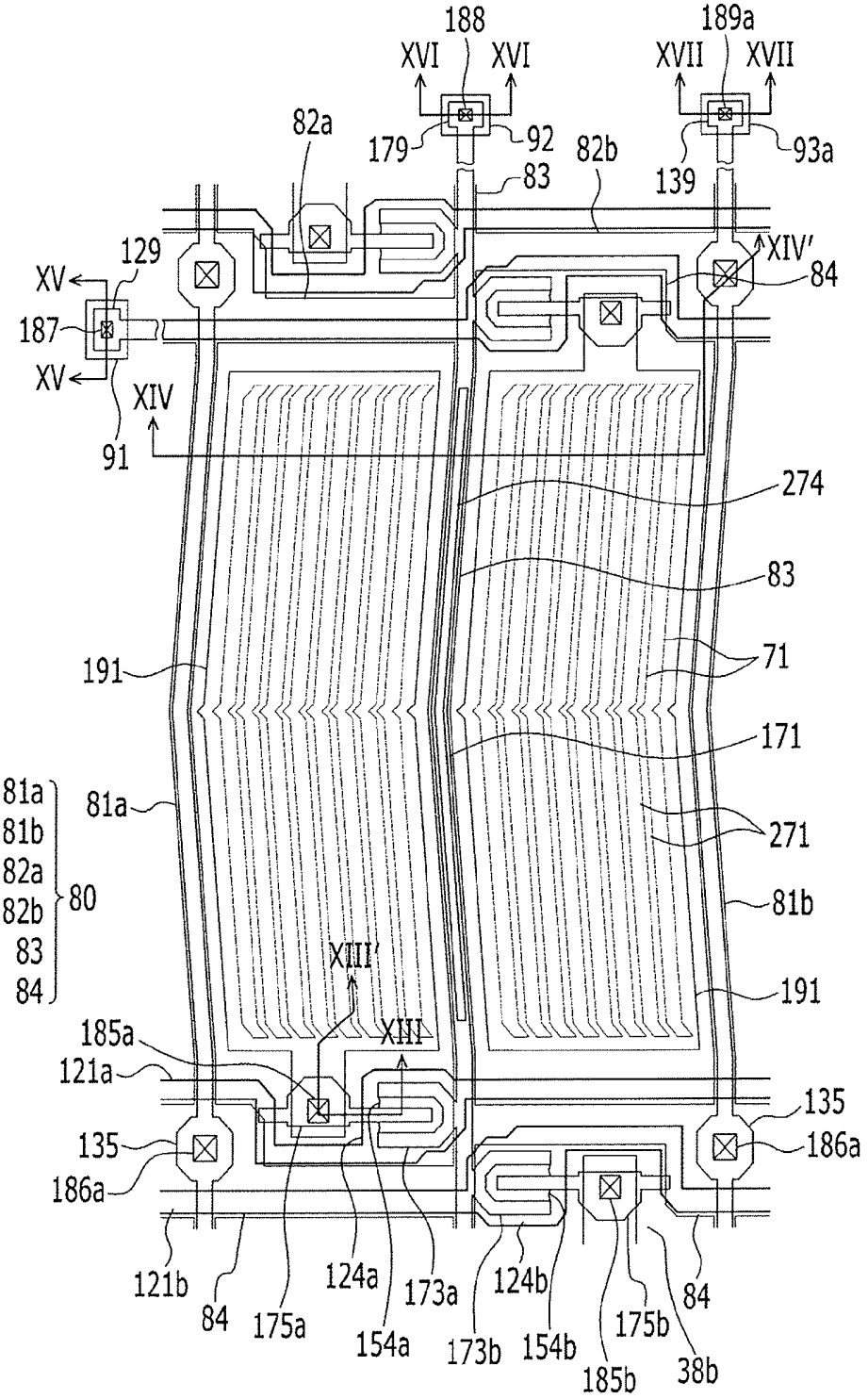


FIG. 12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XVI
XVI
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XVII
XVII
82a
179
92
82b
93a
139
83
129
XV
187
XV
XIV
91
XIV'
84
274
83
191
71
171
81a
81b
82a
82b
83
84
80
81a
271
81b
XIII'
191
XIII
185a
121a
135
186a
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186a
121b
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175a
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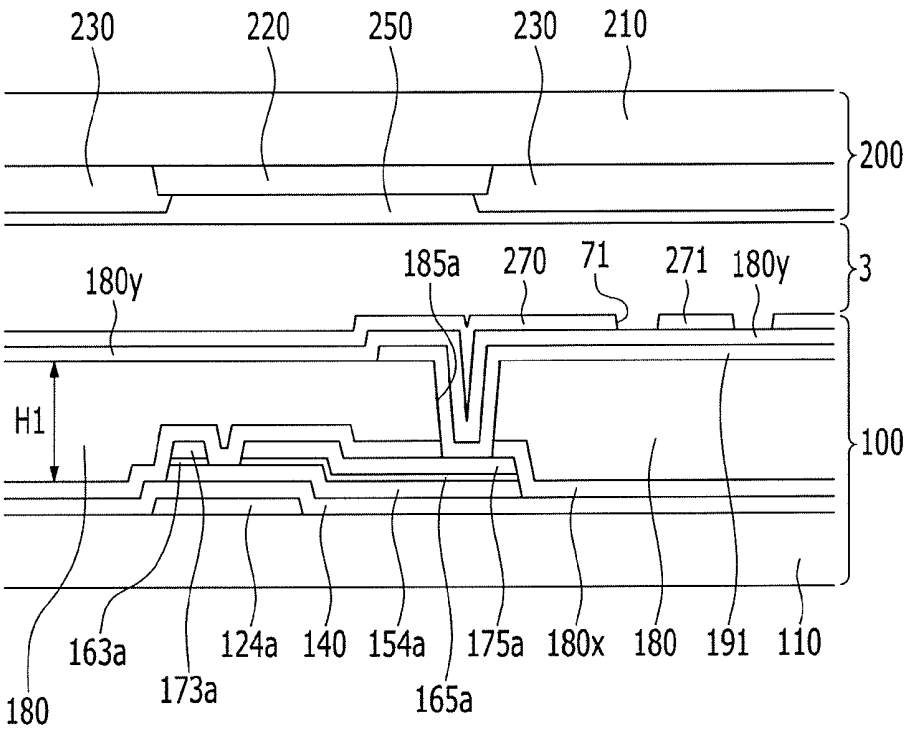
173a
173b
124b
154b
185b
175b
84
38b

FIG. 13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185a
270
71
271
180y
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H1
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163a
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124a
140
154a
165a
175a
180x
180
191
110

FIG. 14

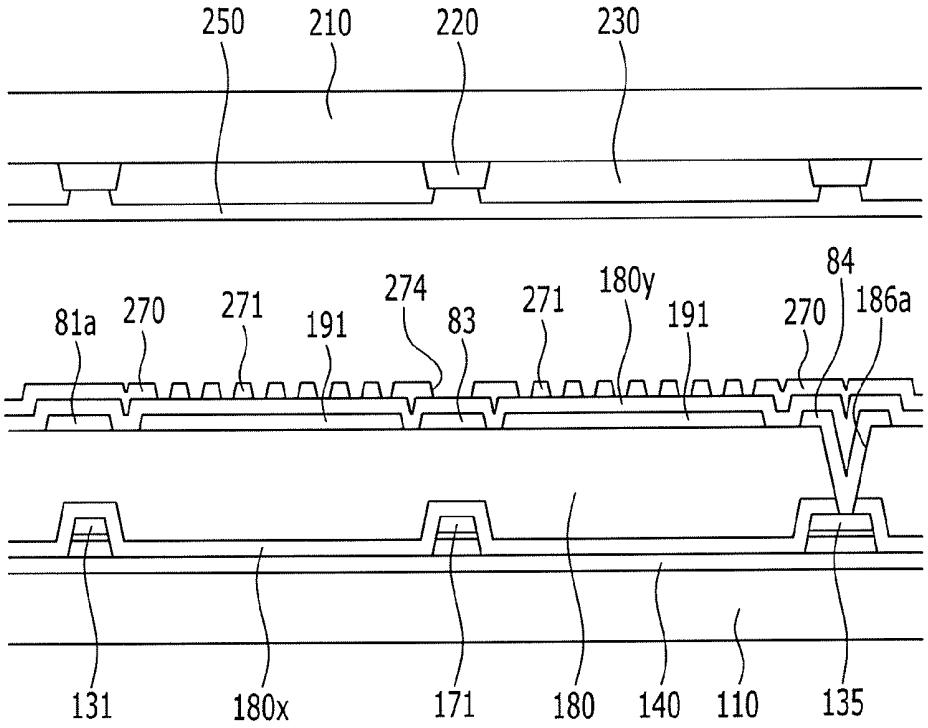
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FIG. 15

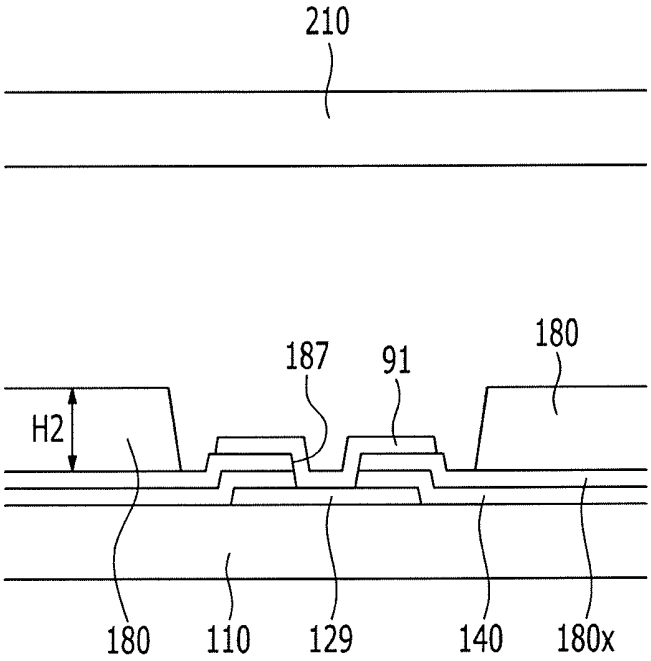


FIG. 16

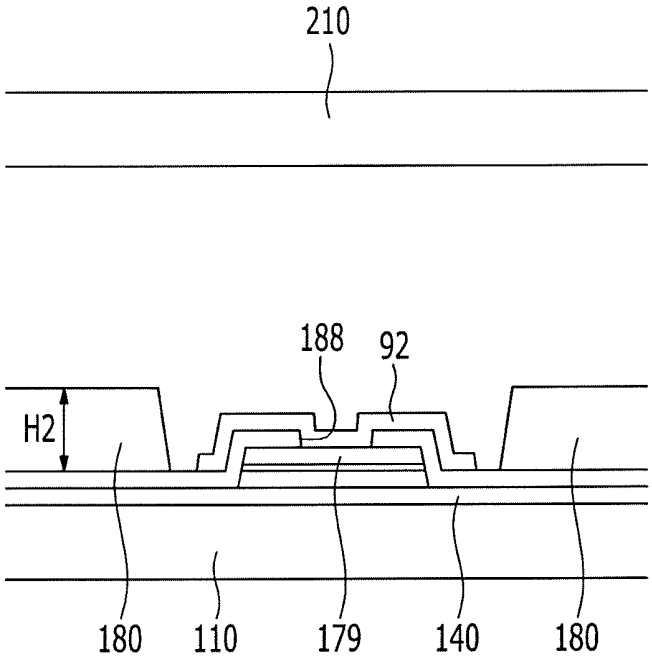


FIG. 17

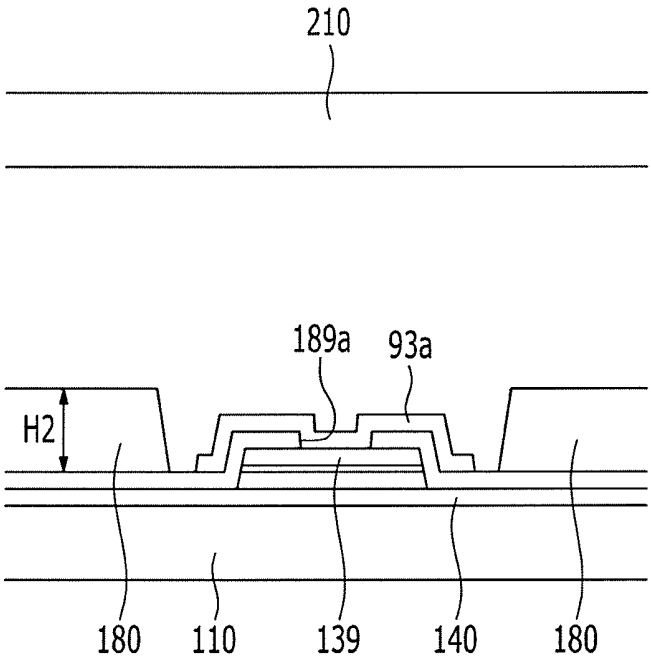
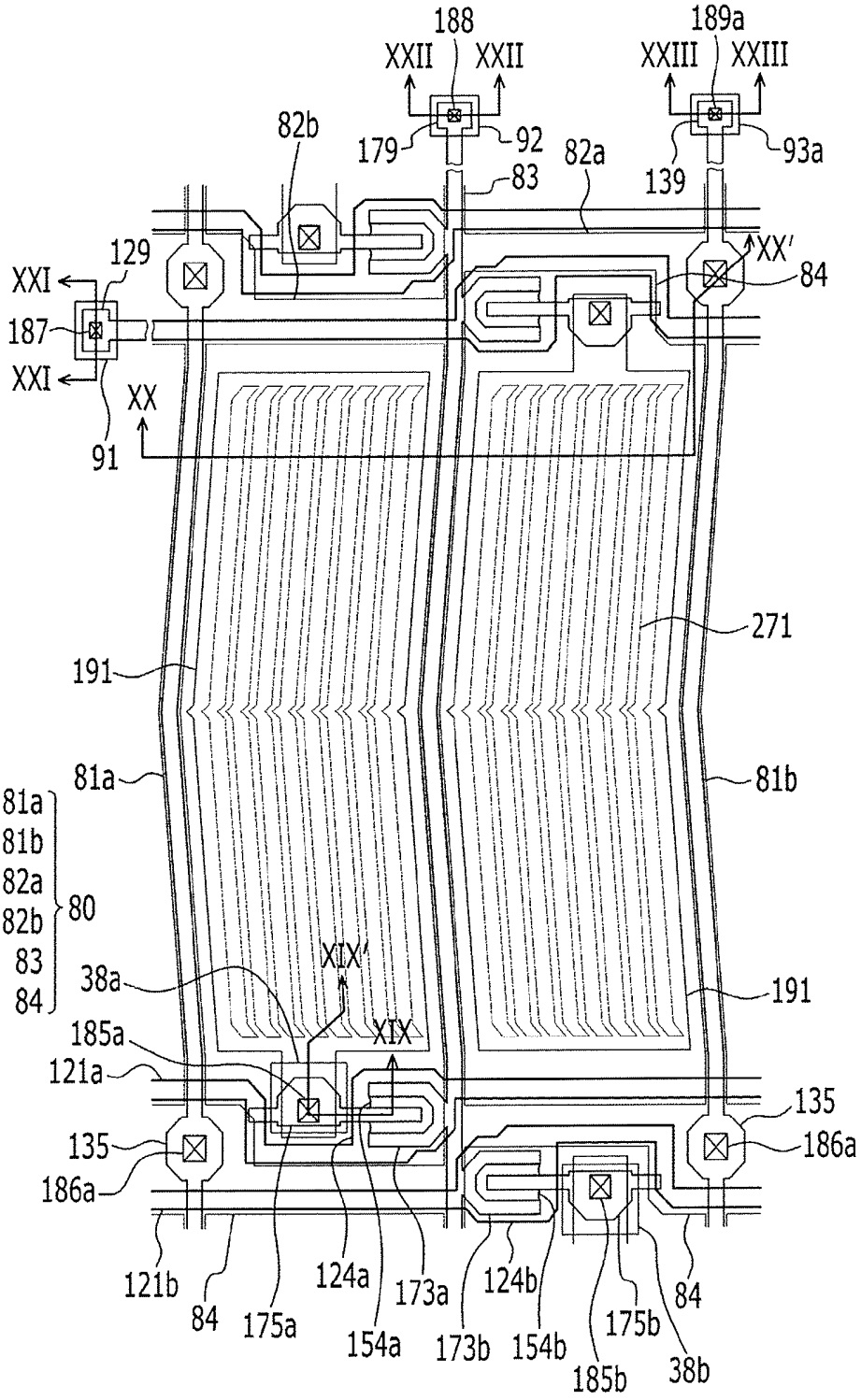


FIG. 18


188
XXII
XXII
189a
XXIII
XXIII
82b
179
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82a
139
93a
83
129
XXI
187
XXI
91
XX
XX'
84
271
191
81a
81b
81a
81b
82a
82b
83
84
80
38a
XIX'
XIX
191
185a
121a
135
186a
135
186a
121b
84
175a
124a
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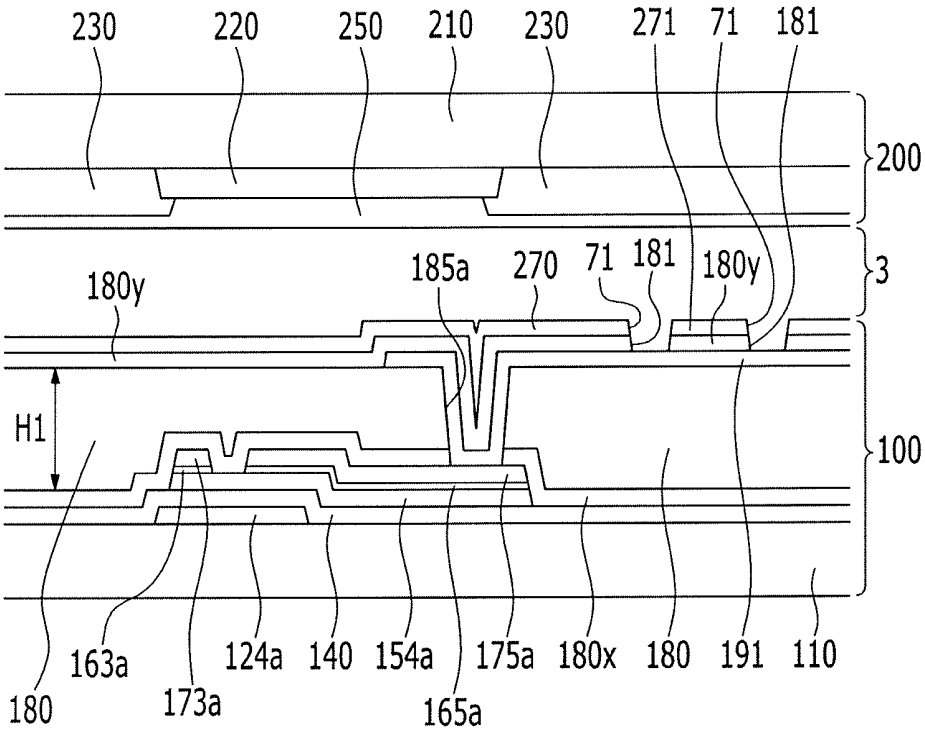
173a
173b
124b
154b
185b
175b
84
38b

FIG. 19


230
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180x
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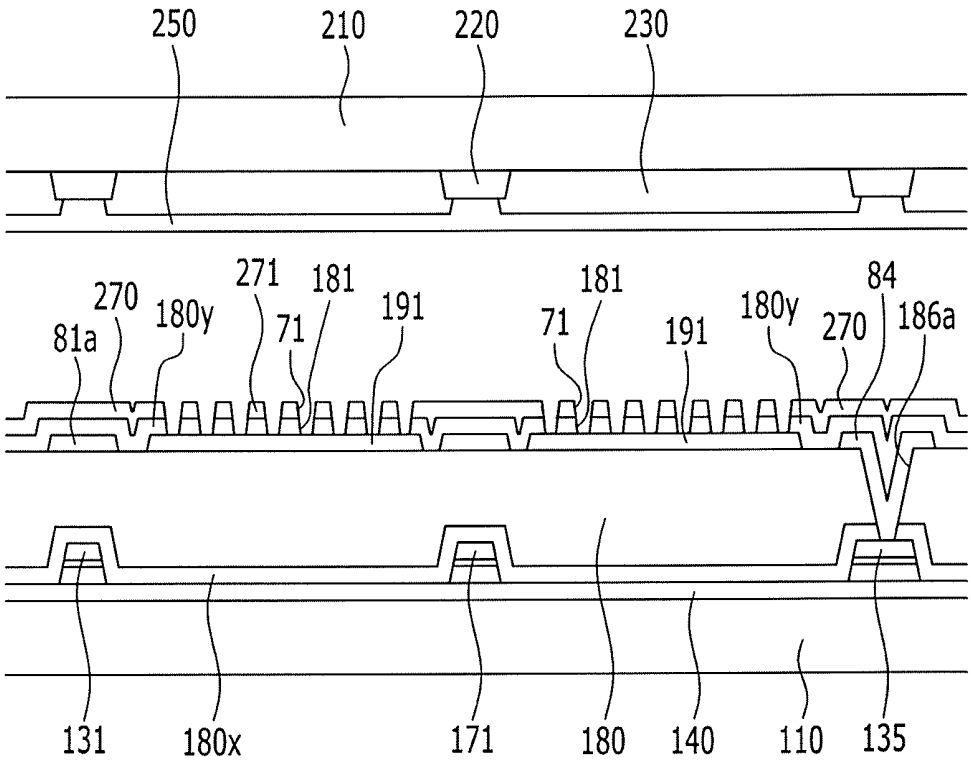
FIG. 20


250
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180y
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181
191
81a
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186a
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180x
171
180
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110
135

FIG. 21

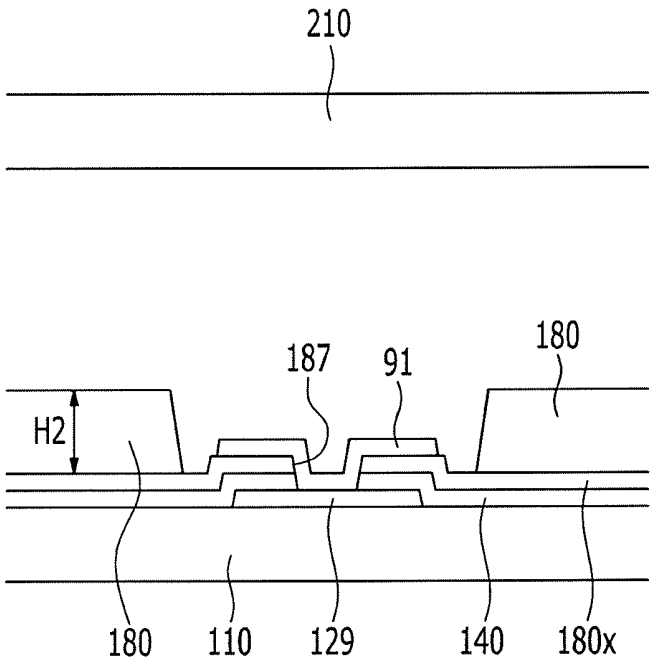


FIG. 22

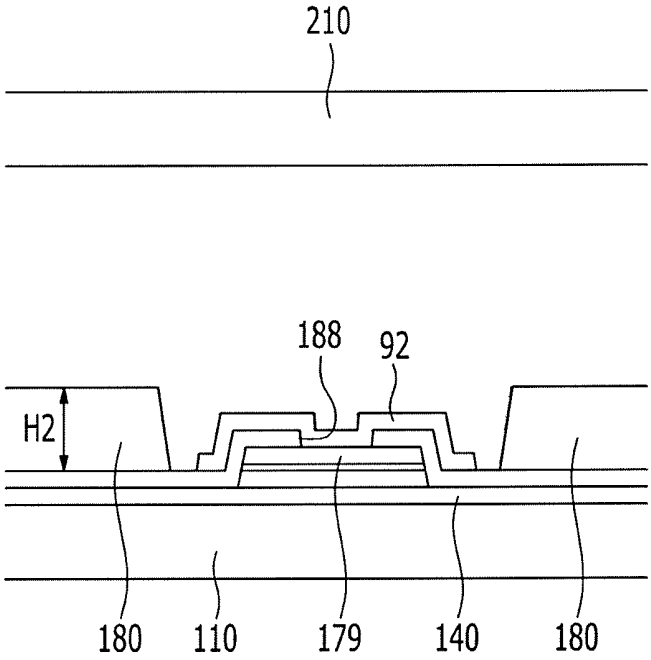


FIG. 23

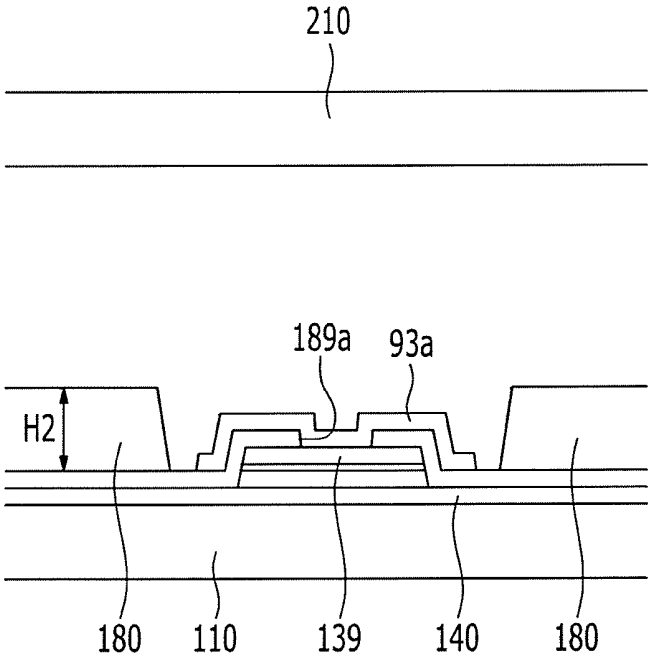
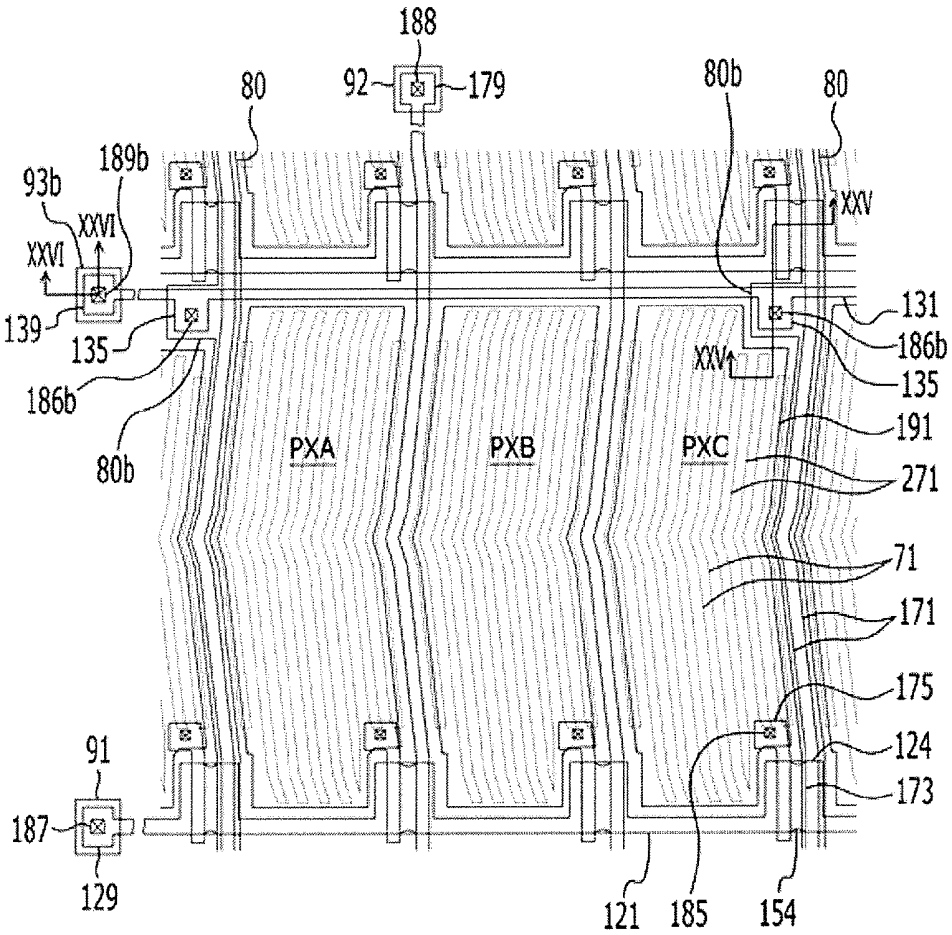


FIG. 24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80
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80b
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189b
93b
XXVI
XXVI
XXV
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186b
80b
131
186b
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173
PXA
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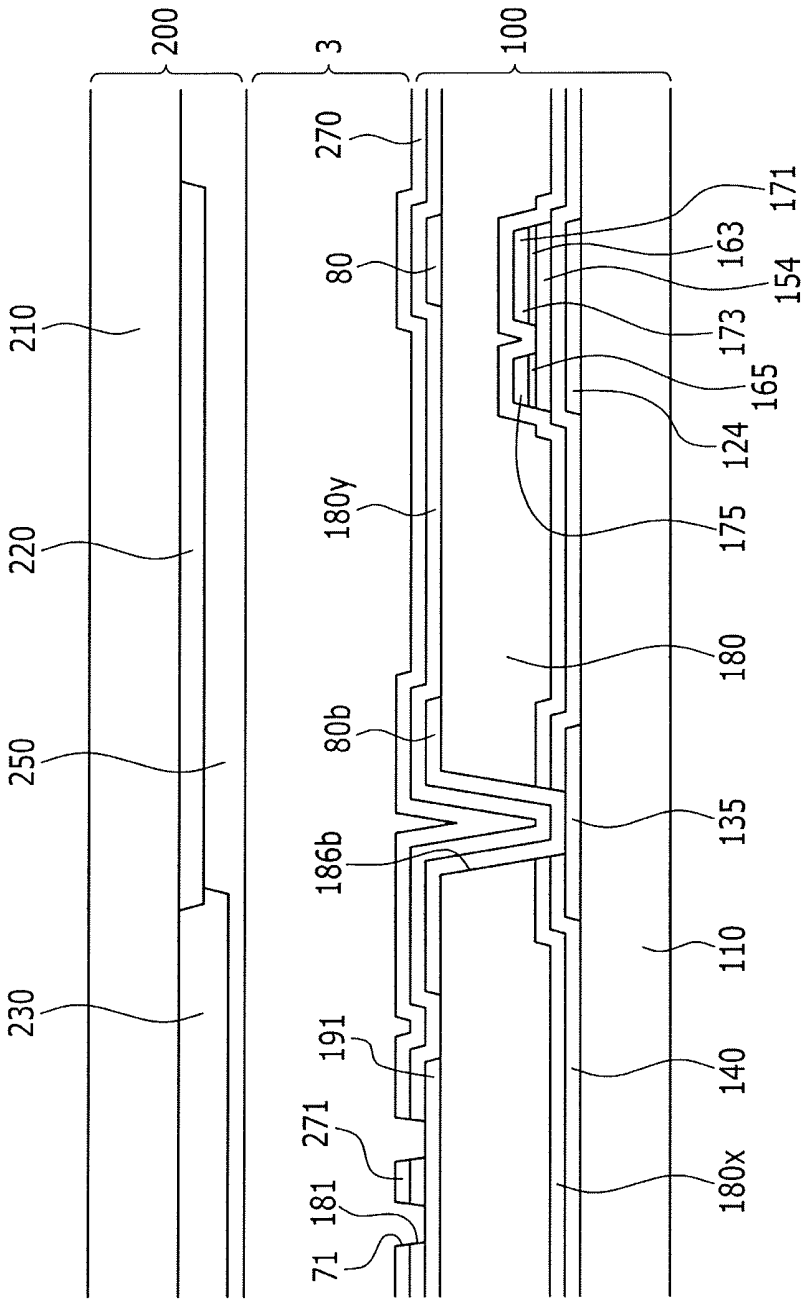
121
185
154

FIG. 25


200
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180y
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180x

FIG. 26

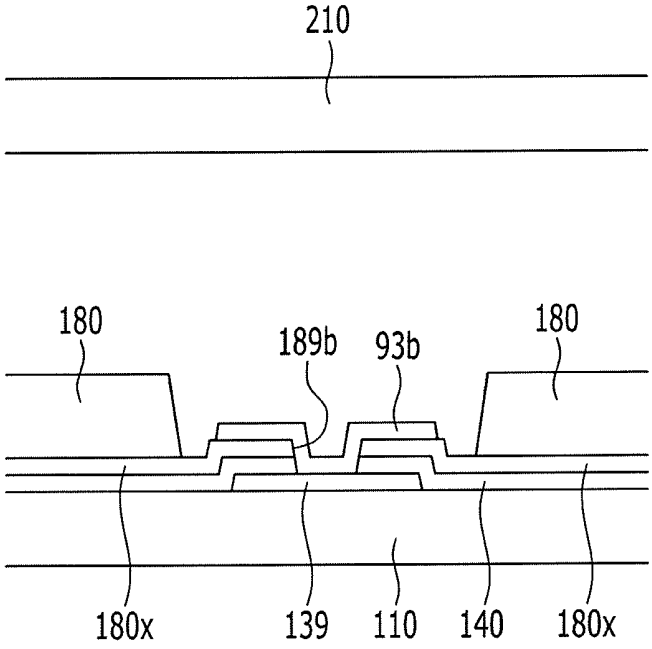
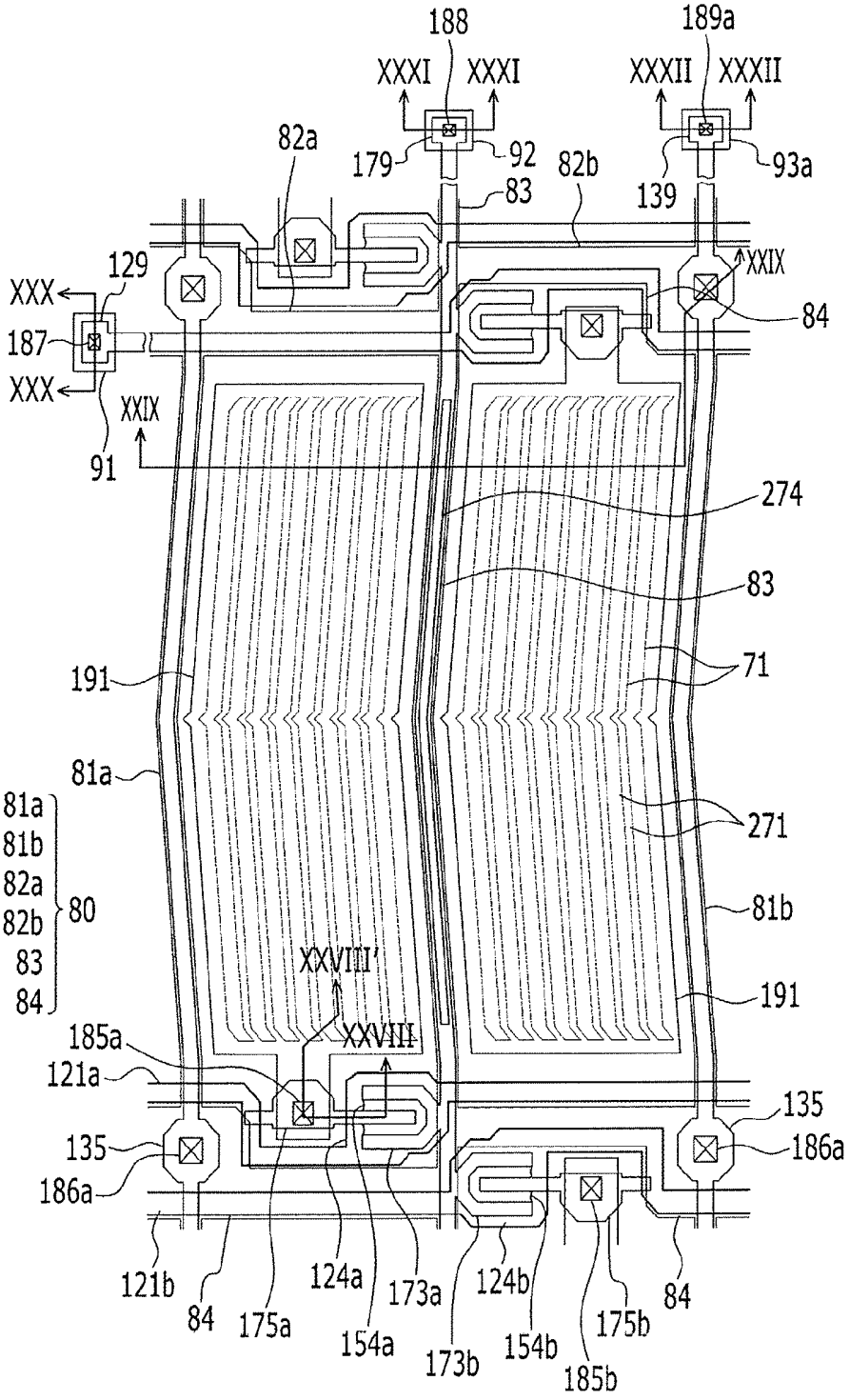


FIG. 27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189a
XXXI
XXXI
XXXII
XXXII
82a
179
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82b
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93a
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129
XXIX
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XXX
XXIX
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274
83
191
71
81a
81a
81b
82a
82b
80
83
84
271
81b
XXVIII'
191
185a
XXVIII
121a
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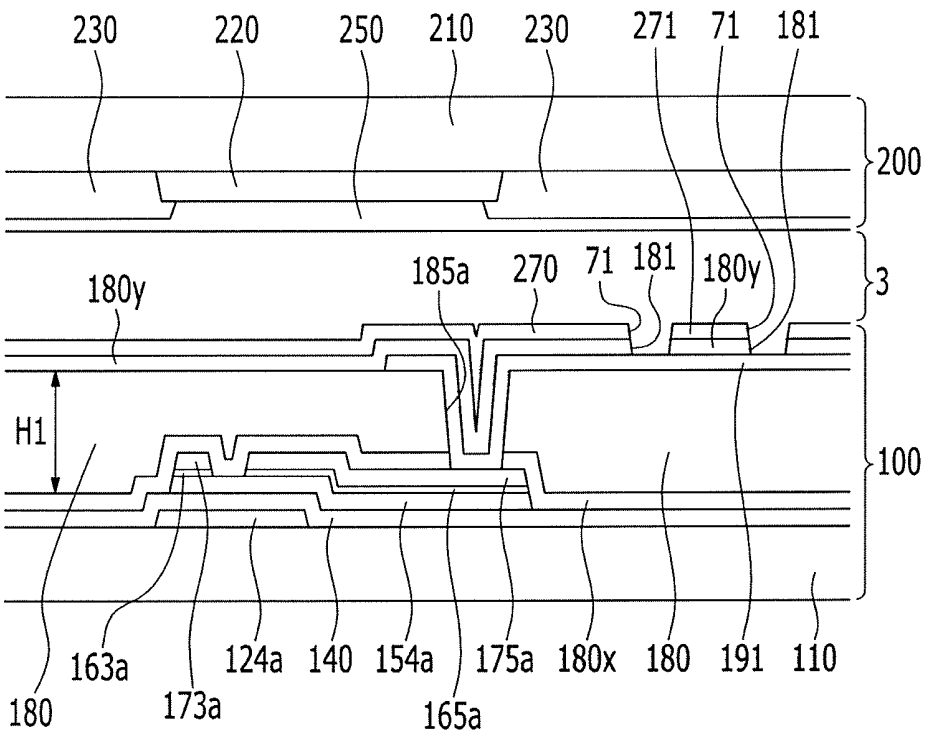
154a
173a
173b
124b
154b
175b
185b
84

FIG. 28


230
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271
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200
180y
185a
270
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180y
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124a
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180x
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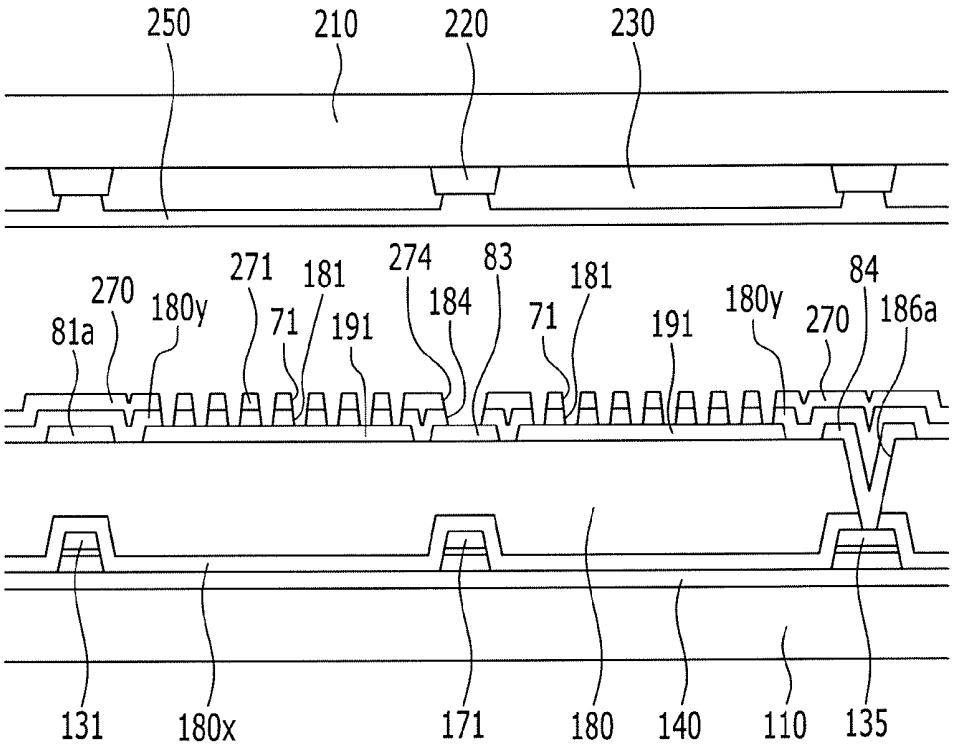
FIG. 29


250
210
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81a
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184
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186a
131
180x
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FIG. 30

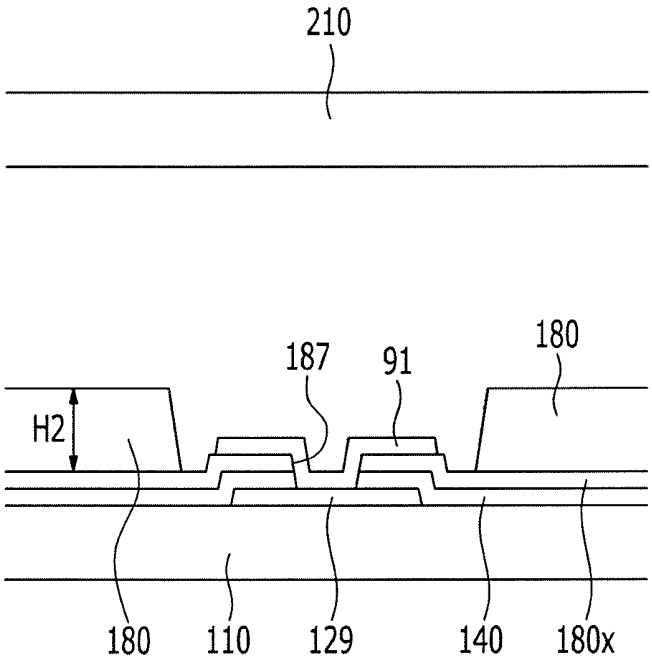


FIG. 31

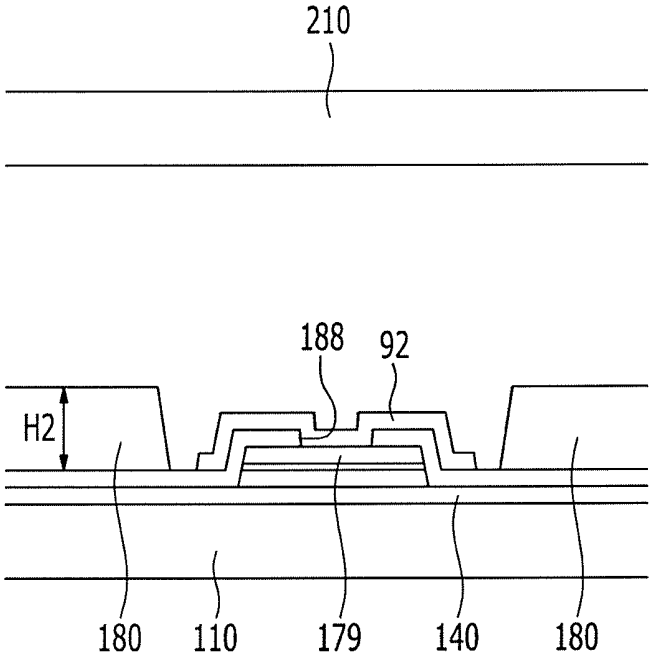


FIG. 32

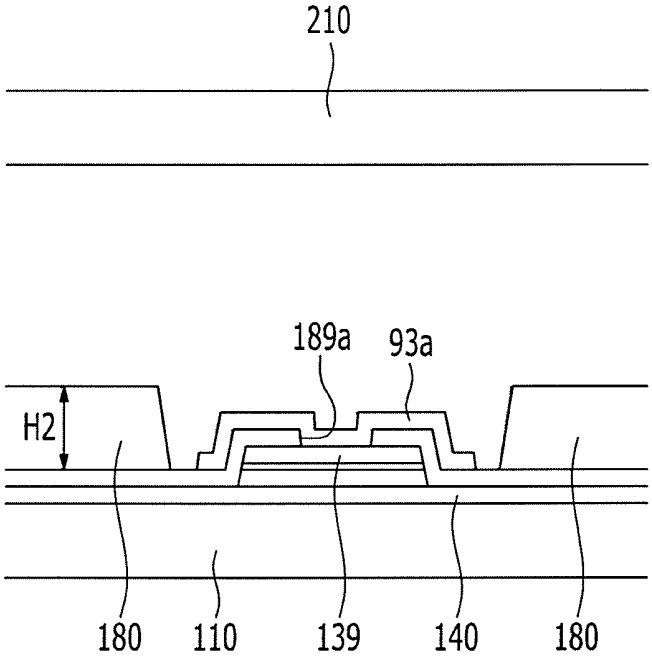
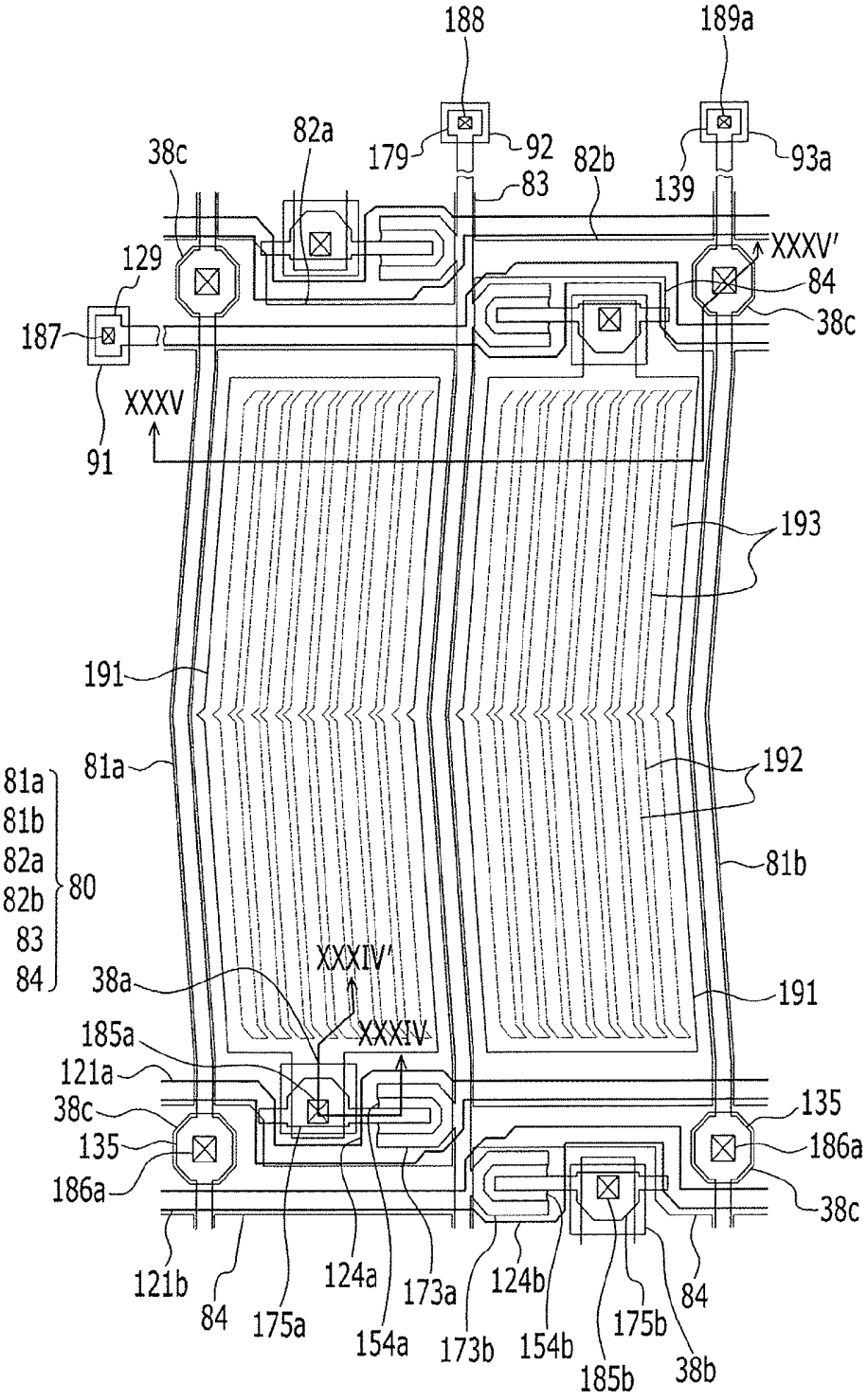


FIG. 33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82b
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93a
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XXXV'
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187
38c
XXXV
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81a
192
81a
81b
82a
82b
83
84
80
81b
XXXIV'
38a
191
XXXIV
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121a
38c
135
135
186a
186a
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173b
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154b
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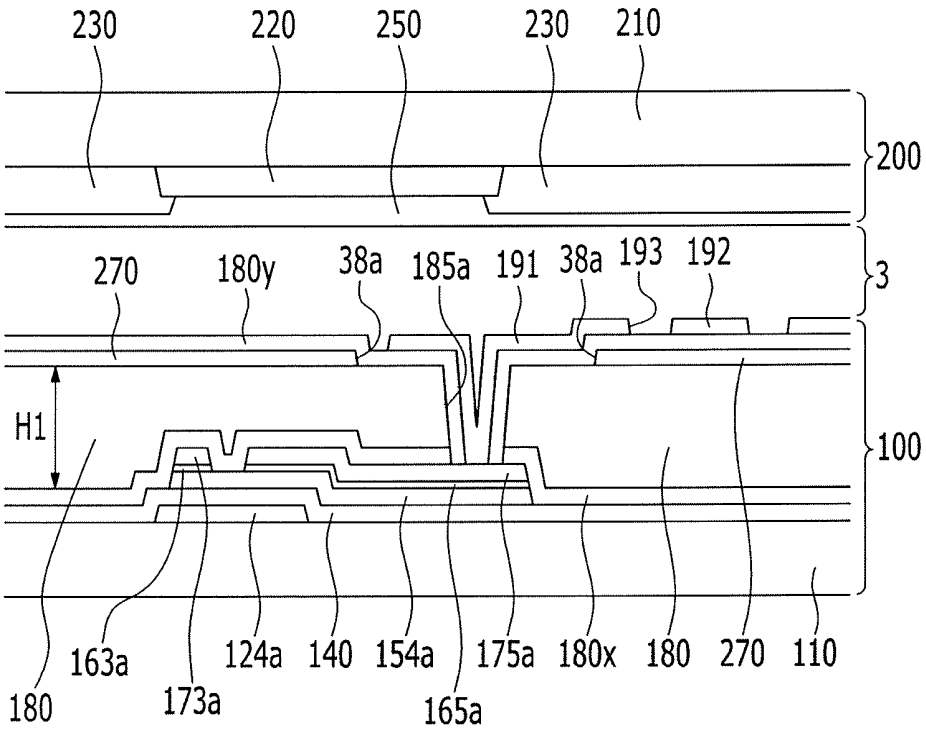
185b
84
38b

FIG. 34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124a
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154a
165a
175a
180x
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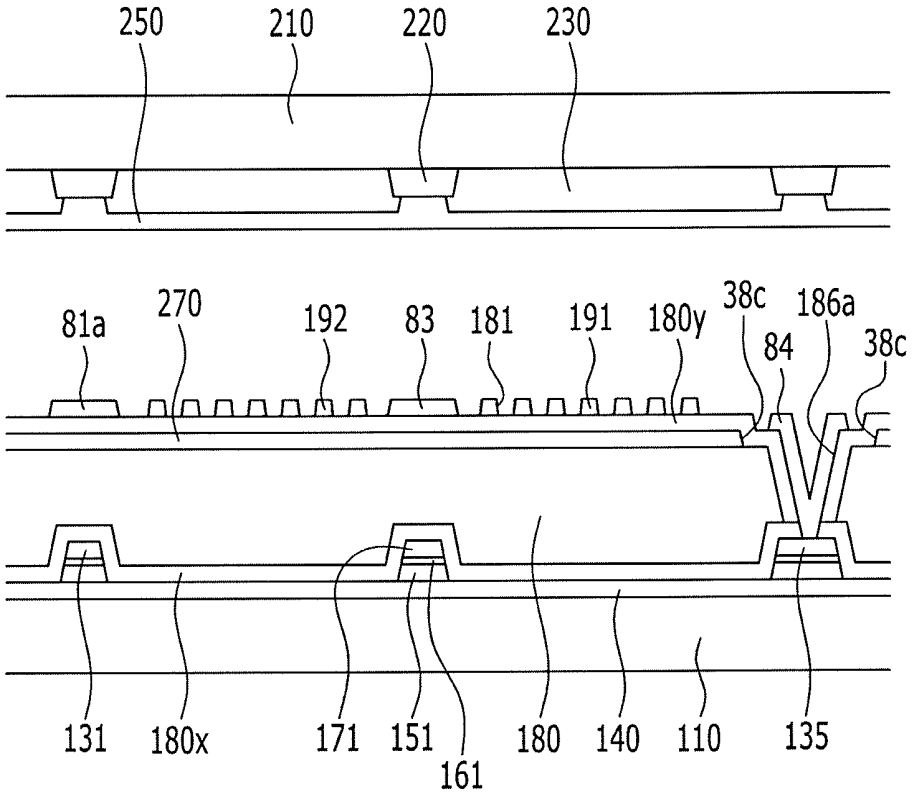
110

FIG. 35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81a
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181
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180y
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186a
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38c
131
180x
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161
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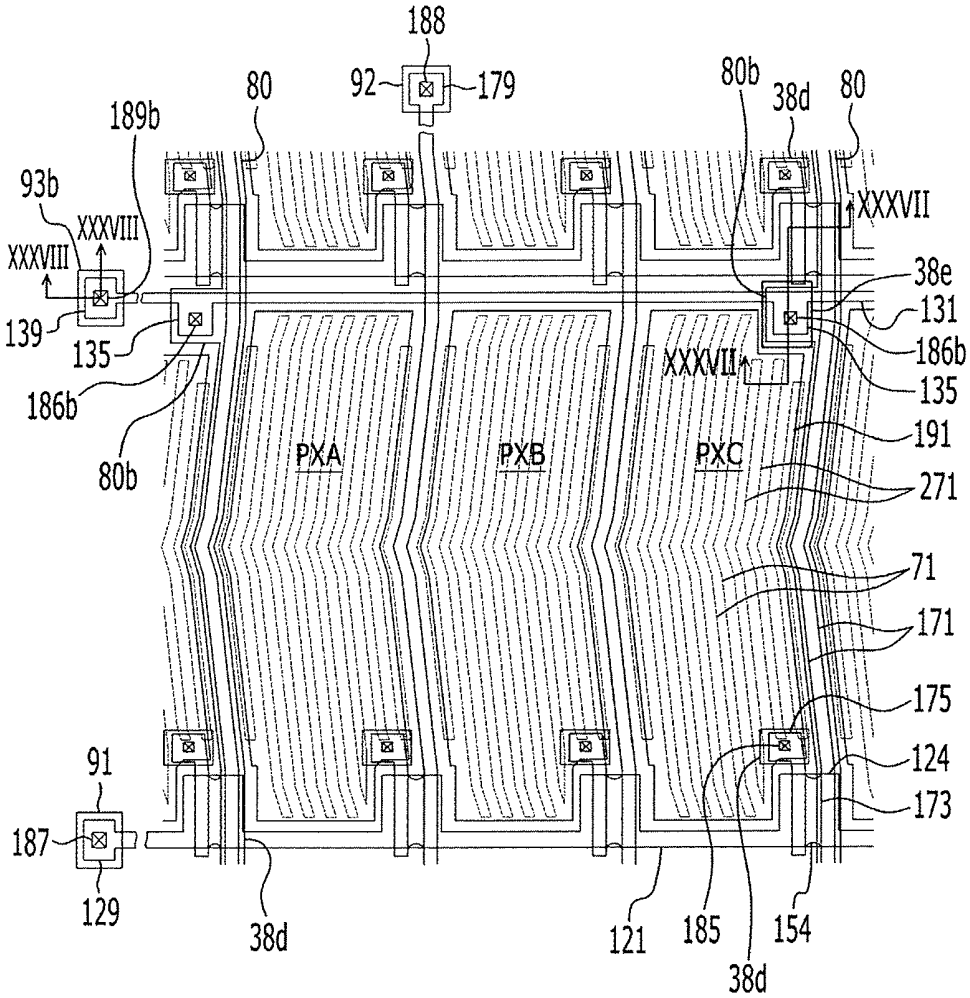
FIG. 36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80b
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93b
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XXXVII
38e
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135
186b
80b
PXA
PXB
PXC
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271
71
171
175
124
173
91
187
129
38d
121
185
154
38d

FIG. 37

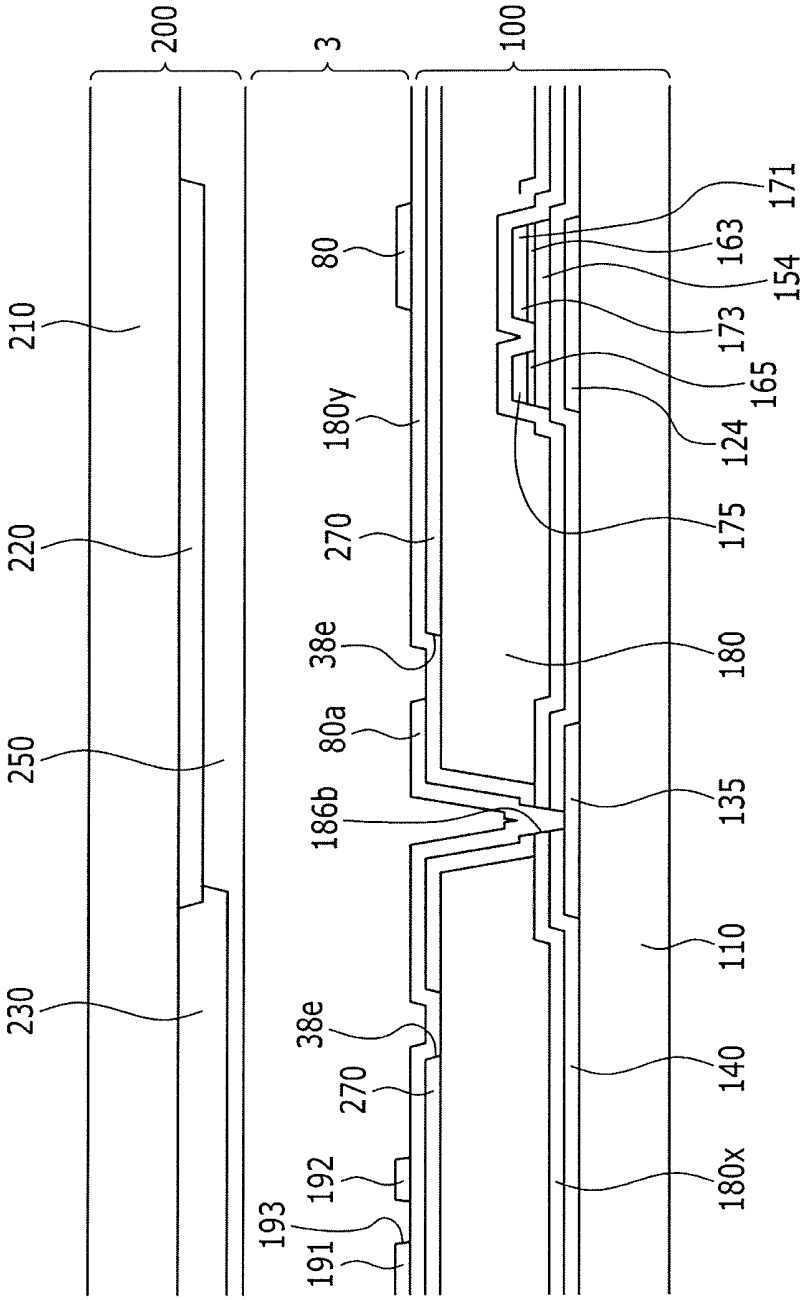

200
3
100
210
220
250
230
80
180y
270
38e
80a
186b
38e
270
192
193
191
171
163
154
173
165
124
175
180
135
110
140
180x

FIG. 38

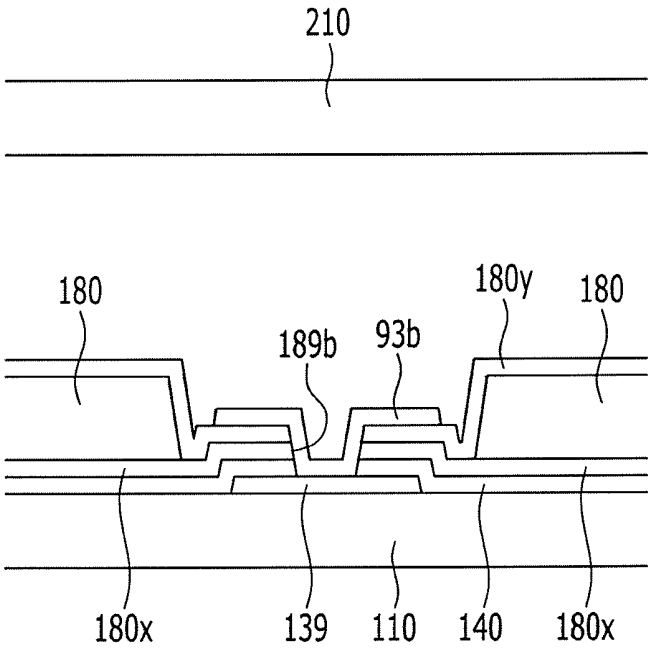
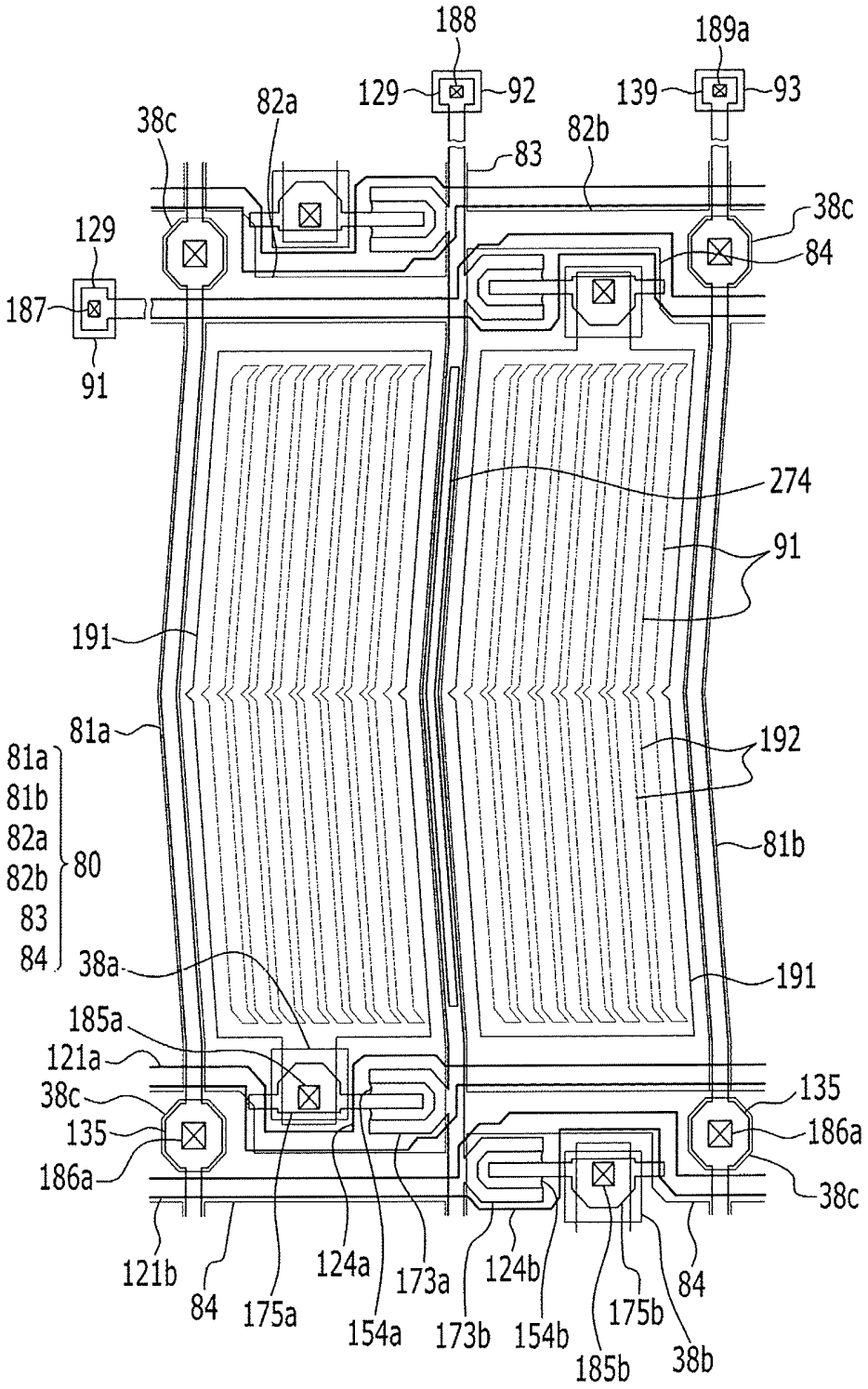


FIG. 39


188
189a
129
92
139
93
38c
82a
83
82b
38c
129
84
187
91
274
91
191
81a
192
81a
81b
82a
82b
80
83
84
81b
38a
191
185a
121a
38c
135
135
186a
186a
38c
121b
84
175a
124a
154a
173a
173b
124b
154b
175b
185b
84
38b

LIQUID CRYSTAL DISPLAY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority from Korean Patent Application No. 10-2013-0152662 filed in the Korean Intellectual Property Office on Dec. 9, 2013, and all the benefits accruing therefrom, the contents of which are herein incorporated by reference in their entirety.

BACKGROUND

[0002] (a) Technical Field

[0003] The present disclosure relates to a liquid crystal display.

[0004] (b) Discussion of the Related Art

[0005] Liquid crystal displays (LCDs) are among the most widely used flat panel displays, and they display images by applying voltages to field-generating electrodes to generate an electric field in an LC layer that determines orientations of LC molecules therein to adjust polarization of incident light.

[0006] Liquid crystal displays are lightweight and thin, but have lower lateral visibility than front visibility, and various liquid crystal arrangements and driving methods have been developed to address this phenomena. To realize a wider viewing angle, liquid crystal displays with a pixel electrode and a reference or common electrode on one substrate have been studied.

[0007] In a liquid crystal display of this form, at least one of the two field generating electrodes, i.e. the pixel electrode and the common electrode, has a plurality of cutouts and a plurality of branch electrodes defined by the plurality of cutouts.

[0008] Different photomasks are required to form two field generating electrodes on one display panel, which increases the manufacturing cost.

[0009] In addition, when connecting the common electrodes, which are applied with a constant voltage, the data line and the common electrode overlap each other and couple such that a ripple of the common voltage may be generated.

[0010] The common voltage ripple can deteriorate display quality due to, e.g., flickering.

SUMMARY

[0011] Embodiments of the present disclosure provide a liquid crystal display that can prevent an increase of a manufacturing cost and can prevent a common voltage ripple generated by coupling between a data line and a common electrode when forming two field generating electrodes on one display panel.

[0012] A liquid crystal display according to an exemplary embodiment of the present disclosure includes: a gate line, a data line, and a compensation voltage line disposed on an insulation substrate; a first passivation layer disposed on the gate line, the data line, and the compensation voltage line; a pixel electrode connected to the gate line and the data line, and a compensation electrode connected to the compensation voltage line, disposed on the first passivation layer; and a common electrode disposed on the first passivation layer, wherein the compensation electrode overlaps at least a portion of the data line, and the compensation voltage line may be formed from a same layer as the data line.

[0013] The compensation voltage line may extend parallel to the data line.

[0014] The compensation voltage line may be positioned between two adjacent data lines.

[0015] The data line may include a plurality of data lines, and the compensation electrode may overlap at least some of the plurality of data lines.

[0016] The common electrode may overlap the data line, and the common electrode may overlap the compensation electrode.

[0017] The common electrode may have a cutout disposed at a position that overlaps the data line.

[0018] The liquid crystal display may further include a second passivation layer disposed on the pixel electrode and the compensation electrode and under the common electrode.

[0019] The common electrode may have a first cutout, the second passivation layer may have a second cutout, and an edge of the first cutout may overlap an edge of the second cutout.

[0020] The liquid crystal display may further include a second passivation layer disposed on the common electrode and under the pixel electrode and the compensation electrode.

[0021] The pixel electrode and the compensation electrode may be formed from a same layer.

[0022] A liquid crystal display according to another exemplary embodiment of the present disclosure includes: a gate line, a data line, and a compensation voltage line disposed on an insulation substrate; a first passivation layer disposed on the gate line, the data line, and the compensation voltage line; a pixel electrode connected to the gate line and the data line, and a compensation electrode connected to the compensation voltage line, disposed on the first passivation layer; and a common electrode disposed on the first passivation layer, wherein the compensation electrode overlaps at least a portion of the data line, and the compensation voltage line may be formed from a same layer as the gate line.

[0023] The compensation voltage line may extend parallel to the gate line.

[0024] A liquid crystal display according to another exemplary embodiment of the present disclosure includes: a gate line, a data line, and a compensation voltage line disposed on an insulation substrate; a first passivation layer disposed on the gate line, the data line, and the compensation voltage line; a pixel electrode connected to the gate line and the data line, and a compensation electrode connected to the compensation voltage line, disposed on the first passivation layer; and a common electrode disposed on the first passivation layer, wherein the compensation electrode overlaps at least a portion of the data line, and the compensation voltage line may extend parallel to the gate line.

[0025] According to a liquid crystal display according to an exemplary embodiment of the present disclosure, when forming two field generating electrodes on one display panel, a common voltage ripple generated by the coupling between the data line and the common electrode can be prevented and the manufacturing cost may be reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] FIG. **1** is a layout view of a liquid crystal display according to an exemplary embodiment of the present disclosure.

[0027] FIG. **2** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line II-II'.

[0028] FIG. **3** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line III-III'.

[0029] FIG. **4** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line IV-IV.

[0030] FIG. **5** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line V-V.

[0031] FIG. **6** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line VI-VI.

[0032] FIG. **7** is a waveform diagram of partial signals applied to a liquid crystal display according to an exemplary embodiment of the present disclosure.

[0033] FIG. **8** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0034] FIG. **9** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0035] FIG. **10** is a cross-sectional view of the liquid crystal display of FIG. **9** taken along line X-X.

[0036] FIG. **11** is a cross-sectional view of the liquid crystal display of FIG. **9** taken along line XI-XI.

[0037] FIG. **12** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0038] FIG. **13** is a cross-sectional view of the liquid crystal display of FIG. **12** taken along line XIII-XIII'.

[0039] FIG. **14** is a cross-sectional view of the liquid crystal display of FIG. **12** taken along line XIV-XIV'.

[0040] FIG. **15** is a cross-sectional view of the liquid crystal display of FIG. **12** taken along line XV-XV.

[0041] FIG. **16** is a cross-sectional view of the liquid crystal display of FIG. **12** taken along line XVI-XVI.

[0042] FIG. **17** is a cross-sectional view of the liquid crystal display of FIG. **12** taken along line XVII-XVII.

[0043] FIG. **18** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0044] FIG. **19** is a cross-sectional view of the liquid crystal display of FIG. **18** taken along line XIX-XIX'.

[0045] FIG. **20** is a cross-sectional view of the liquid crystal display of FIG. **18** taken along line XX-XX'.

[0046] FIG. **21** is a cross-sectional view of the liquid crystal display of FIG. **18** taken along line XXI-XXI.

[0047] FIG. **22** is a cross-sectional view of the liquid crystal display of FIG. **18** taken along line XXII-XXII.

[0048] FIG. **23** is a cross-sectional view of the liquid crystal display of FIG. **18** taken along line XXIII-XXIII.

[0049] FIG. **24** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0050] FIG. **25** is a cross-sectional view of the liquid crystal display of FIG. **24** taken along line XXV-XXV.

[0051] FIG. **26** is a cross-sectional view of the liquid crystal display of FIG. **24** taken along line XXVI-XXVI.

[0052] FIG. **27** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0053] FIG. **28** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXVIII-XXVIII.

[0054] FIG. **29** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXIX-XXIX.

[0055] FIG. **30** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXX-XXX.

[0056] FIG. **31** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXXI-XXXI.

[0057] FIG. **32** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXXII-XXXII.

[0058] FIG. **33** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0059] FIG. **34** is a cross-sectional view of the liquid crystal display of FIG. **33** taken along the line XXXIV-XXXIV'.

[0060] FIG. **35** is a cross-sectional view of the liquid crystal display of FIG. **33** taken along the line XXXV-XXXV'.

[0061] FIG. **36** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0062] FIG. **37** is a cross-sectional view of the liquid crystal display of FIG. **36** taken along the line XXXVII-XXXVII.

[0063] FIG. **38** is a cross-sectional view of the liquid crystal display of FIG. **36** taken along the line XXXVIII-XXXVIII.

[0064] FIG. **39** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0065] Embodiments of the present disclosure will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the disclosure are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present disclosure.

[0066] In the drawings, the thickness of layers, films, panels, regions, etc., may be exaggerated for clarity. Like reference numerals may designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present.

[0067] Now, an exemplary embodiment of the present disclosure will be described with reference to accompanying drawings.

[0068] First, a liquid crystal display according to an exemplary embodiment of the present disclosure will be described with reference to FIG. **1** to FIG. **6**. FIG. **1** is a layout view of a liquid crystal display according to an exemplary embodiment of the present disclosure. FIG. **2** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line FIG. **3** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line FIG. **4** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line IV-IV. FIG. **5** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line V-V. FIG. **6** is a cross-sectional view of the liquid crystal display of FIG. **1** taken along line VI-VI.

[0069] Referring to FIG. **1** to FIG. **6**, a liquid crystal display according to an exemplary embodiment of the present disclosure includes a lower panel **100** and an upper panel **200** facing each other, and a liquid crystal layer **3** interposed therebetween.

[0070] Firstly, the lower panel **100** will be described.

[0071] A plurality of first and second gate lines **121***a* and **121***b* are disposed on a first insulation substrate **110** made of transparent glass or plastic.

[0072] The first gate line **121***a* and the second gate line **121***b* are disposed in pairs between pixel rows.

[0073] The first gate line **121***a* includes a first gate electrode **124***a*, and the second gate line **121***b* includes a second gate

electrode **124***b*. Each of the gate lines **121***a* and **121***b* includes a wide gate pad portion **129** for connection with another layer or an external driving circuit.

[0074] A gate insulating layer **140** is disposed on the plurality of gate lines **121***a* and **121***b*.

[0075] A first semiconductor **154***a* and a second semiconductor **154***b* are disposed on the gate insulating layer **140**. The semiconductors **154***a* and **154***b* may include an oxide semiconductor.

[0076] Ohmic contacts **163***a* and **165***a* are disposed on the semiconductors **154***a* and **154***b*. If the semiconductors **154***a* and **154***b* include an oxide semiconductor, the ohmic contacts **163***a* and **165***a* may be omitted.

[0077] A plurality of data lines **171**, a plurality of drain electrodes **175***a* and **175***b*, and a plurality of compensation voltage lines **131** are disposed on the ohmic contacts **163***a* and **165***a*.

[0078] The data line **171** transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate lines **121***a* and **121***b*. One data line **171** is associated with two columns of pixels.

[0079] The data line **171** may have a first curved portion with a curved shape to maximize transmittance of the liquid crystal display, and the first curved portion may meet a second curved portion which forms a predetermined angle with the first curved portion at a "V" shape in a middle region of the pixel area.

[0080] Each data line **171** includes a first source electrode **173***a* that extends toward the first gate electrode **124***a* and a second source electrode **173***b* that extends toward the second gate electrode **124***b*.

[0081] Each data line **171** includes a wide data pad portion **179** for connection with another layer or an external driving circuit.

[0082] The first drain electrode **175***a* includes one end facing the first source electrode **173***a* and a wide other end, and forms a thin film transistor (TFT) along with the first gate electrode **124***a* and the first semiconductor **154***a*.

[0083] The second drain electrode **175***b* includes one end facing the second source electrode **173***b* and a wide other end, and forms a thin film transistor (TFT) along with the second gate electrode **124***b* and the second semiconductor **154***b*.

[0084] The compensation voltage line **131** extends parallel to the data line **171**, and one compensation voltage line **131** may be associated with two pixel columns. The data line **171** and the compensation voltage line **131** may be alternately disposed.

[0085] The compensation voltage line **131** includes a plurality of extensions **135** and includes a wide compensation pad portion **139** for connection with another layer or an external driving circuit.

[0086] A first passivation layer **180***x* is disposed on the plurality of data lines **171**, the plurality of drain electrodes **175***a* and **175***b*, and the plurality of compensation voltage lines **131**. The first passivation layer **180***x* may be made of an organic insulating material or an inorganic insulating material.

[0087] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** may have be thicker than the first passivation layer **180***x* and may have a flat surface.

[0088] In a liquid crystal display according to another exemplary embodiment of the present disclosure, the organic layer **180** may be omitted. In a liquid crystal display according to another exemplary embodiment of the present disclosure, the organic layer **180** may be a color filter, and in this case, a layer disposed on the organic layer **180** may be further included. For example, an overcoat or capping layer may be disposed on the color filter to prevent a color pigment from flowing into the liquid crystal layer, and the overcoat may be made of an insulating material such as a silicon nitride (SiNx).

[0089] The organic layer **180** may be positioned in a display area in which a plurality of pixels are positioned, and may not be positioned in a peripheral area in which the gate pad portion **129**, the data pad portion **179**, and the compensation pad portion **139** are positioned.

[0090] A first height H1 of the organic layer **180** in the display area is greater than a second height H2 of the organic layer **180** near the gate pad portion **129**, the data pad portion **179**, and the compensation pad portion **139**.

[0091] The organic layer **180** and the first passivation layer **180***x* are penetrated by a first contact hole **185***a* that exposes the first drain electrode **175***a*, a second contact hole **185***b* that exposes the second drain electrode **175***b*, and a third contact hole **186***a* that exposes the extension **135** of the compensation voltage line **131**.

[0092] A pixel electrode **191** and a compensation electrode **80** are disposed on the organic layer **180**.

[0093] The pixel electrode **191** includes curved edges which are substantially parallel to the first curved portion and the second curved portion of the data line **171**. The pixel electrode **191** is made of a transparent conductive layer such as ITO or IZO.

[0094] The pixel electrode **191** is positioned at both sides of the data line **171**, and is connected to the first drain electrode **175***a* through the first contact hole **185***a* and the second drain electrode **175***b* through the second contact hole **185***b*.

[0095] The compensation electrode **80** includes a first longitudinal portion **81***a*, a second longitudinal portion **81***b*, a first transverse portion **82***a*, a second transverse portion **82***b*, and a shielding electrode **83**. The first longitudinal portion **81***a* and the second longitudinal portion **81***b* overlap and extend parallel to the two compensation voltage lines **131** positioned at either side of the data line **171**. The first transverse portion **82***a* extends from the first longitudinal portion **81***a* parallel to the direction of the gate lines **121***a* and **121***b* and the second transverse portion **82***b* extends from the second longitudinal portion **81***b* parallel to the direction of the gate lines **121***a* and **121***b*. The shielding electrode **83** is connected to the first transverse portion **82***a* and the second transverse portion **82***b* that overlap and are parallel to the data line **171**.

[0096] The first longitudinal portion **81***a* and the second longitudinal portion **81***b* of the compensation electrode **80** include a plurality of first connections **84** that overlap the extension **135** of the compensation voltage line **131**.

[0097] The first connection **84** of the compensation electrode **80** is connected to the compensation voltage line **131** through the third contact hole **186***a*.

[0098] The pixel electrode **191** and the compensation electrode **80** may be simultaneously formed from the same layer.

[0099] A second passivation layer **180***y* is disposed on the pixel electrode **191** and the compensation electrode **80**.

[0100] The second passivation layer **180***y*, the first passivation layer **180***x*, and the gate insulating layer **140** have a fourth contact hole **187** in a region positioned at the gate pad portion **129** where they do not overlap the organic layer **180** that

exposes the gate pad portion **129**. Similarly, the second passivation layer **180***y* and the first passivation layer **180***x* have a fifth contact hole **188** in a region positioned at the data pad portion **179** where they do not overlap the organic layer that exposes the data pad portion **179**, and the second passivation layer **180***y* and the first passivation layer **180***x* have a sixth contact hole **189***a* in a region positioned at the compensation pad portion **139** where they do not overlap the organic layer **180** that exposes the compensation pad portion **139**.

[0101] A common electrode **270**, a first contact assistant **91**, a second contact assistant **92**, and a third contact assistant **93***a* are disposed on the second passivation layer **180***y*.

[0102] The common electrode **270** has a plurality of first cutouts **71** in the pixel area, and a plurality of first branch electrodes **271** defined by the plurality of first cutouts **71**. The plurality of first branch electrodes **271** overlap the pixel electrode **191**. The plurality of first branch electrodes **271** extend substantially parallel to the data line **171**.

[0103] The first contact assistant **91** is positioned on the gate pad portion **129** exposed through the fourth contact hole, the second contact assistant **92** is positioned on the data pad portion **179** exposed through the fifth contact hole **188**, and the third contact assistant **93***a* is positioned on the compensation pad portion **139** exposed through the sixth contact hole **189***a*.

[0104] The common electrode **270**, the first contact assistant **91**, the second contact assistant **92**, and the third contact assistant **93***a* are formed from a transparent conductive layer such as ITO or IZO.

[0105] In addition, a horizontal first alignment layer that is rubbed in a predetermined direction may be disposed on the second passivation layer **180***y* and the common electrode **270**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the first alignment layer may include a photoreactive material to be photo-aligned.

[0106] Now, the upper display panel **200** will be described.

[0107] A light blocking member **220** is disposed on a second insulating substrate **210** that is made of transparent glass, plastic, etc. The light blocking member **220** is also called a black matrix and prevents light leakage.

[0108] A plurality of color filters **230** are also disposed on the second substrate **210**.

[0109] An overcoat **250** is disposed on the color filter **230** and the light blocking member **220**. The overcoat **250** is made of an organic insulator, prevents exposure of the color filter **230**, and provides a flat surface. The overcoat **250** may be omitted.

[0110] In addition, a horizontal second alignment layer that is rubbed in a predetermined direction may be disposed on the overcoat **250**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the second alignment layer may include a photoreactive material to be photo-aligned.

[0111] The liquid crystal layer **3** includes a plurality of liquid crystal molecules positioned on the pixel electrode **191** and common electrode **270** that are arranged such that long axis direction thereof is aligned parallel to the display panels **100** and **200**.

[0112] The pixel electrode **191** receives a data voltage from the drain electrodes **175***a* and **175***b*, and the common electrode **270** receives a common voltage having a predetermined magnitude from a common voltage applying unit disposed outside the display region.

[0113] The pixel electrode **191** and the common electrode **270** are field generating electrodes that generate an electric field that rotates the liquid crystal molecules of the liquid crystal layer **3** in a direction parallel with a direction of the electric field. The polarization of light passing through the liquid crystal layer **3** changes according to the rotation direction of the liquid crystal molecules as described above.

[0114] In a liquid crystal display according to an exemplary embodiment shown in FIG. **1** to FIG. **6**, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a case of a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel **100** and the color filter **230** may be omitted from the upper panel **200**. In this case, the light blocking member **220** may also be positioned on the lower panel **100** instead of the upper panel **200**.

[0115] Next, signals applied to a liquid crystal display according to an exemplary embodiment of the present disclosure will be described with reference to FIG. **7**. FIG. **7** is a waveform diagram of partial signals applied to a liquid crystal display according to an exemplary embodiment of the present disclosure.

[0116] The data line **171** and the common electrode **270** overlap each other such that a ripple of the common voltage may be generated by a coupling of the voltages applied to the data line **171** and the common electrode **270**. To compensate the common voltage ripple, the compensation electrode **80**, which includes the shielding electrode **83** overlapping the data line **171**, is applied with a voltage of a polarity opposite to the common voltage ripple, to prevent the ripple from being generated by the coupling between the data line **171** and the common electrode **270**.

[0117] This will be described with reference to FIG. **7**.

[0118] Referring to FIG. **7**, the data line **171** and the common electrode **270** overlap each other, thereby forming a first capacitor C**1**. Accordingly, by the coupling with the data voltage D applied to the data line **171**, the common voltage Vcom applied to the common electrode **270** may change by a first magnitude W1. At this time, a compensation voltage Ccps applied to the compensation electrode **80** has the opposite polarity to that of the data voltage D applied to the data line **171**.

[0119] The shielding electrode **83** of the compensation electrode **80**, which overlaps the data line **171**, also overlaps the common electrode **270**, thereby forming a second capacitor C**2**. Accordingly, by the coupling between the shielding electrode **83** and the common electrode **270**, the common voltage Vcom applied to the common electrode **270** may change by a second magnitude W2. That is, by applying a voltage having a polarity opposite to the data voltage D to the compensation electrode **80**, the first magnitude W1 change of the common voltage Vcom due to the data voltage D is compensated by the coupling due to the compensation voltage Ccps of the compensation electrode **80**, thereby maintaining a uniform common voltage magnitude Vcom applied to the common electrode **270**.

[0120] Next, an arrangement of the compensation electrode **80** of a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with

reference to FIG. **8**. FIG. **8** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0121] Referring to FIG. **8**, the compensation electrode **80** of a liquid crystal display according to a current exemplary embodiment of the present disclosure includes the shielding electrode **83** that overlaps some of the plurality of data lines **171**. For example, the shielding electrode **83** overlaps the data line **171** positioned between the first pixel PXA and the second pixel PXB of four adjacent pixels PXA, PXB, PXC, and PXD, but does not overlap the data line **171** positioned between the third pixel PXC and the fourth pixel PXD.

[0122] Many features of a liquid crystal display according to an exemplary embodiment described with reference to FIG. **1** to FIG. **6** and FIG. **7** may be applied to the liquid crystal display according to a present exemplary embodiment of FIG. **8**.

[0123] Next, a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. **9** to FIG. **11**. FIG. **9** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. **10** is a cross-sectional view of the liquid crystal display of FIG. **9** taken along line X-X. FIG. **11** is a cross-sectional view of the liquid crystal display of FIG. **9** taken along line XI-XI.

[0124] Referring to FIG. **9** to FIG. **11**, a liquid crystal display according to a present exemplary embodiment includes the lower panel **100** and the upper panel **200** facing each other and the liquid crystal layer **3** interposed therebetween.

[0125] First, the lower panel **100** will be described.

[0126] A gate line **121** and a compensation voltage line **131** are disposed on a first insulation substrate **110** made of a transparent glass or plastic. The gate line **121** and the compensation voltage line **131** are formed together from the same layer.

[0127] The gate line **121** includes the gate electrode **124** and the gate pad portion **129**.

[0128] The compensation voltage line **131** extends parallel to the gate line **121** and includes a plurality of extensions **135** and the compensation pad portion **139**.

[0129] A gate insulating layer **140** is disposed on the gate line **121** and the compensation voltage line **131**.

[0130] A semiconductor **154** is disposed on the gate insulating layer **140**.

[0131] Ohmic contacts **163** and **165** are disposed on the semiconductor **154**. The ohmic contacts **163** and **165** may be disposed in a pair on the semiconductor **154**. If the semiconductor **154** is an oxide semiconductor, the ohmic contacts **163** and **165** may be omitted.

[0132] A data conductor that includes a data line **171**, a source electrode **173** and a drain electrode **175** is disposed on the ohmic contacts **163** and **165** and the gate insulating layer **140**.

[0133] The data line **171** includes a wide end for connection with other layers or an external driving circuit. The data line **171** transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate line **121**.

[0134] In addition, the data line **171** may have a first curved portion with a curved shape to maximize transmittance of the liquid crystal display, and the first curved portion may meet a second curved portion at a center region of the pixel area thereby forming a "V" shape.

[0135] The source electrode **173** is a portion of the data line **171**. The drain electrode **175** may be disposed parallel to the source electrode **173**. Accordingly, the drain electrode **175** is parallel to the portion of the data line **171**.

[0136] The gate electrode **124**, the source electrode **173**, and the drain electrode **175** form a thin film transistor (TFT) along with the semiconductor **154**, and a channel of the thin film transistor forms in the semiconductor **154** between the source electrode **173** and the drain electrode **175**.

[0137] A liquid crystal display according to a present exemplary embodiment includes the source electrode **173** positioned on the same line as the data line **171** and the drain electrode **175** extending parallel to the data line **171** such that the width of the thin film transistor may increase without increasing the area occupied by the data conductor, thereby increasing the aperture ratio of the liquid crystal display.

[0138] However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the source electrode **173** and the drain electrode **175** have different shapes.

[0139] A first passivation layer **180***x* is disposed on the data conductor **171**, **173**, and **175**, the gate insulating layer **140**, and the portion of the semiconductor **154** exposed between the source electrode **173** and the drain electrode **175**. The first passivation layer **180***x* may be made of an organic insulating material or an inorganic insulating material.

[0140] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** is thicker than the first passivation layer **180***x* and may have a flat surface.

[0141] The organic layer **180** may be positioned in the display area where a plurality of pixels are positioned, and may not be positioned in the peripheral area where the gate pad portion and the data pad portion are positioned. Alternatively, the organic layer **180** may be positioned in the peripheral area where the gate pad portion or the data pad portion are positioned, where the organic layer **180** may have a lower surface height than the organic layer **180** positioned at the display area.

[0142] The organic layer **180** and the first passivation layer **180***x* have a seventh contact hole **185** that exposes the drain electrode **175**.

[0143] The organic layer **180**, the first passivation layer **180***x*, and the gate insulating layer **140** have an eighth contact hole **186***b* that exposes the compensation voltage line **131**.

[0144] A pixel electrode **191** and a compensation electrode **80** are disposed on the organic layer **180**. The compensation electrode **80** overlaps the data line **171** and extends along with the data line **171**. The compensation electrode **80** includes a second connection **80***b* that extends toward the extension **135** of the compensation voltage line **131**.

[0145] The second connection **80***b* of the compensation electrode **80** is connected to the compensation voltage line **131** through the eighth contact hole **186***b*.

[0146] The pixel electrode **191** and the compensation electrode **80** may be simultaneously formed from the same layer.

[0147] A second passivation layer **180***y* is disposed on the pixel electrode **191** and the compensation electrode **80**.

[0148] The second passivation layer **180***y*, the first passivation layer **180***x*, and the gate insulating layer **140** have a fourth contact hole **187** in a region positioned at the gate pad portion where they do not overlap the organic layer **180** that exposes the gate pad portion **129**. Similarly, the second passivation layer **180***y* and the first passivation layer **180***x* have a fifth contact hole **188** in a region positioned at the data pad portion

179 where they do not overlap the organic layer 180 that exposes the data pad portion 179.

[0149] Referring to FIG. 11, the first passivation layer 180*x*, the second passivation layer 180*y*, and the gate insulating layer 140 have a ninth contact hole 189*b* in a region positioned at the compensation pad portion where they do not overlap the organic layer 180 that exposes the compensation pad portion 139.

[0150] A common electrode 270, a first contact assistant 91, a second contact assistant 92, and a fourth contact assistant 93*b* are disposed on the second passivation layer 180*y*.

[0151] The common electrode 270 includes a plurality of first cutouts 71 and a plurality of first branch electrodes 271 defined by the plurality of first cutouts 71. A plurality of first branch electrodes 271 overlap the pixel electrode 191. A plurality of first branch electrodes 271 extend substantially parallel to the data line 171.

[0152] The first contact assistant 91 is disposed on the gate pad portion 129 exposed through the fourth contact hole 187, and the second contact assistant 92 is disposed on the data pad portion 179 exposed through the fifth contact hole. In addition, the fourth contact assistant 93*b* is disposed on the compensation pad portion 139 exposed through the ninth contact hole 189*b*.

[0153] The common electrode 270, the first contact assistant 91, the second contact assistant 92, and the fourth contact assistant 93*b* are formed from a transparent conductive layer such as ITO or IZO.

[0154] Next, the upper panel 200 will be described.

[0155] A light blocking member 220 and a color filter 230 are disposed on the second insulation substrate 210, and an overcoat 250 is disposed on the color filter 230 and the light blocking member 220.

[0156] As shown in FIG. 9, according to a liquid crystal display of a present exemplary embodiment, the compensation electrode 80 overlaps some, but not all data lines 171. However, according to a liquid crystal display of a current exemplary embodiment of the present disclosure, the compensation electrode 80 may overlap all data lines 171.

[0157] In a liquid crystal display according to a present exemplary embodiment, the organic layer 180 is positioned on the first passivation layer 180*x* of the lower panel 100, and the color filter 230 and the light blocking member 220 are positioned on the upper panel 200. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter 230 may replace the organic layer 180 on the lower panel 100, and the color filter 230 may be omitted from the upper panel 200. In this case, the light blocking member 220 may also be positioned on the lower panel 100 instead of the upper panel 200.

[0158] As described with reference to FIG. 7, according to a liquid crystal display according to a present exemplary embodiment, to compensate a common voltage ripple generated by the coupling of the voltage applied to the data line 171 and the common electrode 270, a voltage having a polarity opposite to the common voltage ripple is applied to the compensation electrode 80 to prevent the ripple due to the coupling between the data line 171 and the common electrode 270.

[0159] Many features of a liquid crystal display according to the exemplary embodiment described with reference to FIG. 1 to FIG. 6 may be applied to a liquid crystal display according to a present exemplary embodiment of FIG. 9 to FIG. 11.

[0160] Next, a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. 12 to FIG. 17. FIG. 12 is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. 13 is a cross-sectional view of the liquid crystal display of FIG. 12 taken along line XIII-XIII'. FIG. 14 is a cross-sectional view of the liquid crystal display of FIG. 12 taken along line XIV-XIV'. FIG. 15 is a cross-sectional view of the liquid crystal display of FIG. 12 taken along line XV-XV. FIG. 16 is a cross-sectional view of the liquid crystal display of FIG. 12 taken along line XVI-XVI. FIG. 17 is a cross-sectional view of the liquid crystal display of FIG. 12 taken along line XVII-XVII.

[0161] Referring to FIG. 12 and FIG. 17, a liquid crystal display according to a present exemplary embodiment is similar to the liquid crystal display according to the exemplary embodiment of FIG. 1 to FIG. 6. The description of the same constituent elements is omitted.

[0162] Referring to FIG. 12 to FIG. 17, a liquid crystal display according to an exemplary embodiment of the present disclosure includes a lower panel 100 and an upper panel 200 facing each other, and a liquid crystal layer 3 interposed therebetween.

[0163] First, the lower panel 100 will be described.

[0164] A plurality of first and second gate lines 121*a* and 121*b* are disposed on a first insulation substrate 110.

[0165] The first gate line 121*a* and the second gate line 121*b* are disposed in pairs between pixel rows.

[0166] The first gate line 121*a* includes a first gate electrode 124*a*, and the second gate line 121*b* includes a second gate electrode 124*b*. Each of the gate lines 121*a* and 121*b* includes a wide gate pad portion 129 for connection with another layer or an external driving circuit.

[0167] A gate insulating layer 140 is disposed on a plurality of gate lines 121*a* and 121*b*.

[0168] A first semiconductor 154*a* and a second semiconductor 154*b* are disposed on the gate insulating layer 140.

[0169] Ohmic contacts 163*a* and 165*a* are disposed on the semiconductors 154*a* and 154*b*

[0170] A plurality of data lines 171, a plurality of drain electrodes 175*a* and 175*b*, and a plurality of compensation voltage lines 131 are disposed on the ohmic contacts 163*a* and 165*a*.

[0171] The data line 171 transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate lines 121*a* and 121*b*. Each data line 171 is associated with two columns of pixels.

[0172] Each data line 171 includes a first source electrode 173*a* that extends toward the first gate electrode 124*a* and a second source electrode 173*b* that extends toward the second gate electrode 124*b*.

[0173] Each data line 171 includes a wide data pad portion 179 for connection with another layer or an external driving circuit.

[0174] The first drain electrode 175*a* faces the first source electrode 173*a* and forms a thin film transistor (TFT) along with the first gate electrode 124*a* and the first semiconductor 154*a*, and the second drain electrode 175*b* faces the second source electrode 173*b* and forms a thin film transistor (TFT) along with the second gate electrode 124*b* and the second semiconductor 154*b*.

[0175] The compensation voltage line 131 extends parallel to the data line 171, and each compensation voltage line 131

may associated with two pixel columns. The data line **171** and the compensation voltage line **131** may be alternately disposed.

[0176] The compensation voltage line **131** includes a plurality of extensions **135** and a wide compensation pad portion **139** for connection with another layer or an external driving circuit.

[0177] A first passivation layer **180***x* is disposed on the plurality of data lines **171**, the plurality of drain electrodes **175***a* and **175***b*, and the plurality of compensation voltage lines **131**.

[0178] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** may be thicker than the first passivation layer **180***x* and have a flat surface.

[0179] The organic layer **180** may be positioned in the display area in which a plurality of pixels are positioned, and may not be positioned in a peripheral area in which the gate pad portion **129**, the data pad portion **179**, and the compensation pad portion **139** are disposed.

[0180] The organic layer **180** and the first passivation layer **180***x* have a first contact hole **185***a* that exposes the first drain electrode **175***a*, a second contact hole **185***b* that exposes the second drain electrode **175***b*, and a third contact hole **186***a* that exposes the extension **135** of the compensation voltage line **131**.

[0181] A pixel electrode **191** and a compensation electrode **80** are disposed on the organic layer **180**.

[0182] The pixel electrode **191** is positioned on both sides of the data line **171**, and is connected to the first drain electrode **175***a* through the first contact hole **185***a* and the second drain electrode **175***b* through the second contact hole **185***b*.

[0183] The compensation electrode **80** includes a first longitudinal portion **81***a*, a second longitudinal portion **81***b*, a first transverse portion **82***a*, a second transverse portion **82***b*, and a shielding electrode **83**. The first longitudinal portion **81***a* and the second longitudinal portion **81***b* overlap and extend parallel to two compensation voltage lines **131** positioned at both side of the data line. The first transverse portion **82***a* extends from the first longitudinal portion **81***a* parallel to the direction of the gate lines **121***a* and **121***b*, and the second transverse portion **82***b* extends from the second longitudinal portion **81***b* parallel to the direction of the gate lines **121***a* and **121***b*. The shielding electrode **83** is connected to the first transverse portion **82***a* and the second transverse portion **82***b*, and overlaps and is parallel to the data line **171**.

[0184] The first longitudinal portion **81***a* and the second longitudinal portion **81***b* of the compensation electrode **80** include a plurality of first connections **84** that overlap the extension **135** of the compensation voltage line **131**.

[0185] The pixel electrode **191** and the compensation electrode **80** may be simultaneously formed from the same layer.

[0186] The first connection **84** of the compensation electrode **80** is connected to the compensation voltage line **131** through the third contact hole **186***a*.

[0187] A second passivation layer **180***y* is disposed on the pixel electrode **191** and the compensation electrode **80**.

[0188] The second passivation layer **180***y*, the first passivation layer **180***x*, and the gate insulating layer **140** have a fourth contact hole **187** at a region positioned at the gate pad portion **129** where they do not overlap the organic layer **180** that exposes the gate pad portion **129**. Similarly, the second passivation layer **180***y* and the first passivation layer **180***x* have a fifth contact hole **188** at a region positioned at the data pad portion **179** where they do not overlap the organic layer **180** that exposes the data pad portion **179**, and the second passivation layer **180***y* and the first passivation layer **180***x* have a sixth contact hole **189***a* at a region positioned at the compensation pad portion **139** where they do not overlap the organic layer **180** that exposes the compensation pad portion **139**.

[0189] A common electrode **270**, a first contact assistant **91**, a second contact assistant **92**, and a third contact assistant **93***a* are disposed on the second passivation layer **180***y*.

[0190] The common electrode **270** has a plurality of first cutouts **71** in the pixel area and a plurality of first branch electrodes **271** defined by the plurality of first cutouts **71**. A plurality of first branch electrodes **271** overlap the pixel electrode **191**. A plurality of first branch electrodes **271** extend in a direction substantially parallel to the data line **171**.

[0191] The common electrode **270** includes a second cutout **274** in a region that overlaps the data line **171**.

[0192] The first contact assistant **91** is positioned on the gate pad portion **129** exposed through the fourth contact hole **187**, the second contact assistant **92** is positioned on the data pad portion **179** exposed through the fifth contact hole **188**, and the third contact assistant **93***a* is positioned on the compensation pad portion **139** exposed through the sixth contact hole **189***a*.

[0193] As described above, different from the liquid crystal display according to a exemplary embodiment as described with reference to FIG. **1** to FIG. **6**, the common electrode **270** of a liquid crystal display according to a present exemplary embodiment further has a second cutout **274** that overlaps the data line **171**. The second cutouts **274** in the common electrode **270** may reduce the overlap area between the data line **171** and the common electrode **270**. Accordingly, the coupling between the data line **171** and the common electrode **270** may be reduced, which may prevent a common voltage ripple from being generated by the coupling between the data line **171** and the common electrode **270**.

[0194] Now, the upper display panel **200** will be described.

[0195] A light blocking member **220** and a color filter **230** are disposed on the second insulation substrate **210**, and an overcoat **250** is disposed on the color filter **230** and the light blocking member **220**.

[0196] The liquid crystal layer **3** includes a plurality of liquid crystal molecules positioned on the pixel electrode **191** and common electrode **270**that are aligned so that long axial directions thereof are parallel to the panels **100** and **200**.

[0197] The pixel electrode **191** receives a data voltage from the drain electrode **175**, and the common electrode **270** receives a common voltage having a predetermined magnitude from a common voltage application unit disposed outside the display area.

[0198] The pixel electrode **191** and the common electrode **270** are the field generating electrodes that generate an electric field that rotates the liquid crystal molecules of the liquid crystal layer **3** in a direction parallel with a direction of the electric field. The polarization of light passing through the liquid crystal layer **3** changes according to the rotation direction of the liquid crystal molecules as described above.

[0199] In a liquid crystal display according to a exemplary embodiment as shown in FIG. **12** to FIG. **17**, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a case of a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel

100, and the color filter 230 may be omitted from the upper panel 200. In this case, the light blocking member 220 may also be positioned on the lower panel 100 instead of the upper panel 200.

[0200] As described with reference to FIG. 7, according to a liquid crystal display according to a present exemplary embodiment, to compensate a common voltage ripple generated by the coupling of the voltage applied to the data line 171 and the common electrode 270, a voltage having a polarity opposite to the ripple voltage is applied to the compensation electrode 80 to prevent the ripple due to the coupling between the data line 171 and the common electrode 270.

[0201] In addition, in a liquid crystal display according to a present exemplary embodiment, the second cutouts 274 in the common electrode 270 may reduce the overlap area between the data line 171 and the common electrode 270. Accordingly, by reducing the coupling between the data line 171 and the common electrode 270, the common voltage ripple generated by the coupling between the data line 171 and the common electrode 270 may be further prevented.

[0202] Many features of a liquid crystal display according to an exemplary embodiment described with reference to FIG. 1 to FIG. 6 may be applied to the liquid crystal display according to a present exemplary embodiment.

[0203] Next, a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. 18 to FIG. 23. FIG. 18 is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. 19 is a cross-sectional view of the liquid crystal display of FIG. 18 taken along line XIX-XIX'. FIG. 20 is a cross-sectional view of the liquid crystal display of FIG. 18 taken along line XX-XX'. FIG. 21 is a cross-sectional view of the liquid crystal display of FIG. 18 taken along line XXI-XXI. FIG. 22 is a cross-sectional view of the liquid crystal display of FIG. 18 taken along line XXII-XXII. FIG. 23 is a cross-sectional view of the liquid crystal display of FIG. 18 taken along line XXIII-XXIII.

[0204] Referring to FIG. 18 and FIG. 23, a liquid crystal display according to a present exemplary embodiment is similar to the liquid crystal display according to the exemplary embodiment of FIG. 1 to FIG. 6. The description of the same constituent elements is omitted.

[0205] Referring to FIG. 18 to FIG. 23, a liquid crystal display according to an exemplary embodiment of the present disclosure includes a lower panel 100 and an upper panel 200 facing each other, and a liquid crystal layer 3 interposed therebetween.

[0206] First, the lower panel 100 will be described.

[0207] A plurality of first and second gate lines 121*a* and 121*b* are disposed on a first insulation substrate 110. The first gate line 121*a* and the second gate line 121*b* are disposed in pairs between pixel rows.

[0208] The first gate line 121*a* includes a first gate electrode 124*a*, and the second gate line 121*b* includes a second gate electrode 124*b*. Each of the gate lines 121*a* and 121*b* includes a wide gate pad portion 129 for connection with another layer or an external driving circuit.

[0209] A gate insulating layer 140 is disposed on the plurality of gate lines 121*a* and 121*b*.

[0210] A first semiconductor 154*a* and a second semiconductor 154*b* are disposed on the gate insulating layer 140.

[0211] Ohmic contacts 163*a* and 165*a* are disposed on the semiconductors 154*a* and 154*b*.

[0212] A plurality of data lines 171, a plurality of drain electrodes 175*a* and 175*b*, and a plurality of compensation voltage lines 131 are disposed on the ohmic contacts 163*a* and 165*a*.

[0213] The data line 171 transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate lines 121*a* and 121*b*. Each data line 171 is associated with two columns of pixels.

[0214] Each data line 171 includes a first source electrode 173*a* that extends toward the first gate electrode 124*a* and a second source electrode 173*b* that extends toward the second gate electrode 124*b*.

[0215] Each data line 171 includes a wide data pad portion 179 for connection with another layer or an external driving circuit.

[0216] The first drain electrode 175*a* faces the first source electrode 173*a* and forms a thin film transistor (TFT) along with the first gate electrode 124*a* and the first semiconductor 154*a*, and the second drain electrode 175*b* faces the second source electrode 173*b* and forms a thin film transistor (TFT) along with the second gate electrode 124*b* and the second semiconductor 154*b*.

[0217] The compensation voltage line 131 extends parallel to the data line 171 and each may be associated with two pixel columns. The data line 171 and the compensation voltage line 131 may be alternately disposed.

[0218] The compensation voltage line 131 includes a plurality of extensions 135 and a wide compensation pad portion 139 for connection with another layer or an external driving circuit.

[0219] A first passivation layer 180*x* is disposed on the plurality of data lines 171, the plurality of drain electrodes 175*a* and 175*b*, and the plurality of compensation voltage lines 131.

[0220] An organic layer 180 is disposed on the first passivation layer 180*x*. The organic layer 180 may be thicker than the first passivation layer 180*x* and have a flat surface.

[0221] The organic layer 180 may be positioned in the display area in which a plurality of pixels are positioned and may not be positioned in a peripheral area in which the gate pad portion 129, the data pad portion 179, and the compensation pad portion 139 are positioned.

[0222] A first height H1 of the organic layer 180 positioned at the display area may be greater than a second height H2 of the organic layer 180 positioned near the gate pad portion 129, the data pad portion 179, and the compensation pad portion 139.

[0223] The organic layer 180 and the first passivation layer 180*x* have a first contact hole 185*a* that exposes the first drain electrode 175*a*, a second contact hole 185*b* that exposes the second drain electrode 175*b*, and a third contact hole 186*a* that exposes the extension 135 of the compensation voltage line 131.

[0224] The second passivation layer 180*y* and the first passivation layer 180*x* have a fourth contact hole 187 at a region positioned at the gate pad portion 129 where they do not overlap the organic layer 180 that exposes the gate pad portion 129. Similarly, the first passivation layer 180*x* has a fifth contact hole 188 at a region positioned at the data pad portion 179 where it does not overlap the organic layer 180 that exposes the data pad portion 179, and the first passivation layer 180*x* has a sixth contact hole 189*a* at a region positioned

at the compensation pad portion **139** where it does not overlap the organic layer **180** that exposes the compensation pad portion **139**.

[0225] A pixel electrode **191** and a compensation electrode **80** are disposed on the organic layer **180**.

[0226] The pixel electrode **191** includes a curved edge that is substantially parallel to a first curved portion of the data line **171**. The pixel electrode **191** is formed from a transparent conductive layer such as ITO or IZO.

[0227] The pixel electrode **191** is positioned on both sides of the data line **171**, and is connected to the first drain electrode **175***a* through the first contact hole **185***a* and the second drain electrode **175***b* through the second contact hole **185***b*.

[0228] The compensation electrode **80** includes a first longitudinal portion **81***a*, a second longitudinal portion **81***b*, a first transverse portion **82***a*, a second transverse portion **82***b* and a shielding electrode **83**. The first longitudinal portion **81***a* and second longitudinal portion **81***b* overlap and extend parallel to two compensation voltage lines **131** positioned at both sides of the data line. The first transverse portion **82***a* extends from the first longitudinal portion **81***a* parallel to the direction of the gate lines **121***a* and **121***b*, and the second transverse portion **82***b* extends from the second longitudinal portion **81***b* parallel to the direction of the gate lines **121***a* and **121***b*. The shielding electrode **83** is connected to the first transverse portion **82***a* and the second transverse portion **82***b*, and overlaps and is parallel to the data line **171**.

[0229] The pixel electrode **191** and the compensation electrode **80** may be simultaneously formed from the same layer.

[0230] The first longitudinal portion **81***a* and the second longitudinal portion **81***b* of the compensation electrode **80** include a plurality of first connections **84** that overlap the extension **135** of the compensation voltage line **131**.

[0231] The first connection **84** of the compensation electrode **80** is connected to the compensation voltage line **131** through the third contact hole **186***a*.

[0232] A second passivation layer **180***y* is disposed on the pixel electrode **191** and the compensation electrode **80**, and a common electrode **270**, a first contact assistant **91**, a second contact assistant **92**, and a third contact assistant **93***a* are disposed on the second passivation layer **180***y*. The common electrode **270** is formed from a transparent conductive layer such as ITO or IZO.

[0233] The first contact assistant **91** is positioned on the gate pad portion **129** exposed through the fourth contact hole **187**, the second contact assistant **92** is positioned on the data pad portion **179** exposed through the fifth contact hole **188**, and the third contact assistant **93***a* is positioned on the compensation pad portion **139** exposed through the sixth contact hole **189***a*.

[0234] The second passivation layer **180***y* and the common electrode **270** have substantially the same planar shape.

[0235] The second passivation layer **180***y* and the common electrode **270** are positioned in the display area where a plurality of pixels are positioned, but are not positioned at the peripheral area where the gate pad portion **129** and the data pad portion **179** are positioned.

[0236] The common electrode **270** has a plurality of first cutouts **71**, and the second passivation layer **180***y* has a plurality of third cutouts **181**. The first cutouts **71** and the third cutouts **181** have substantially the same planar shape. That is, an edge of the first cutout **71** and an edge of the third cutout **181** overlap each other. Therefore, the second passivation layer **180***y* and the common electrode **270** may be formed together using one photomask.

[0237] The common electrode **270** includes a sixth cutout **38***a* and a seventh cutout **38***b* near the first drain electrode **175***a* and the second drain electrode **175***b*.

[0238] In addition, a horizontal first alignment layer rubbed in a predetermined direction may be applied on the pixel electrode **191** and the common electrode **270** exposed through the third cutout. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the first alignment layer may include a photoreactive material to be photo-aligned.

[0239] Now, the upper display panel **200** will be described.

[0240] A light blocking member **220** is disposed on a second insulating substrate **210** made of transparent glass, plastic, etc. A plurality of color filters **230** are also disposed on the second substrate **210**.

[0241] An overcoat **250** is disposed on the color filter **230** and the light blocking member **220**.

[0242] In addition, a second alignment layer may be disposed on the overcoat **250**.

[0243] The liquid crystal layer **3** includes a plurality of liquid crystal molecules positioned on the pixel electrode **191** and common electrode **270**that are arranged such that long axis direction thereof is aligned parallel to the display panels **100** and **200**.

[0244] The pixel electrode **191** receives a data voltage from the drain electrodes **175***a* and **175***b* and the common electrode **270** receives a common voltage having a predetermined magnitude from a common voltage applying unit which is disposed outside the display region.

[0245] The pixel electrode **191** and the common electrode **270** are field generating electrodes that generate an electric field that rotate the liquid crystal molecules of the liquid crystal layer **3** in a direction parallel with a direction of the electric field. The polarization of light passing through the liquid crystal layer **3** changes according to the rotation direction of the liquid crystal molecules as described above.

[0246] In a liquid crystal display according to a present exemplary embodiment, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel **100** and the color filter **230** may be omitted from the upper panel **200**. In this case, the light blocking member **220** may also be positioned on the lower panel **100** instead of the upper panel **200**.

[0247] As described above, according to a liquid crystal display of a present exemplary embodiment, different from a liquid crystal display according to a exemplary embodiment described with reference to FIG. **1** to FIG. **6**, the common electrode **270** has a plurality of first cutouts **71**, the second passivation layer **180***y* has a plurality of third cutouts **181**, and the first cutouts **71** and the third cutouts **181** have substantially the same planar shape. That is, an edge of the first cutout **71** and an edge of the third cutout **181** **180***y* overlap. Therefore, the second passivation layer **180***y* and the common electrode **270** may be formed together with one photomask.

[0248] The second passivation layer **180***y* and the common electrode **270** are positioned in the display area where a plurality of pixels are positioned, but are not positioned in the

peripheral area where the gate pad portion **129** and the data pad portion **179** are positioned.

[0249] By forming the second passivation layer **180***y* and the common electrode **270** with one photomask, manufacturing cost of the liquid crystal display may be reduced.

[0250] The data line **171** and the common electrode **270** overlap each other such that a common voltage ripple may be generated by the coupling of the voltage applied to the data line **171** and the common electrode **270**. However, as described above, the compensation electrode **80** of a liquid crystal display according to an exemplary embodiment of the present disclosure includes a shielding electrode **83** that overlaps the data line **171**, and to compensate the ripple of the common voltage, a voltage having a polarity opposite to the common voltage ripple is applied to the compensation electrode **80**, thereby preventing the ripple due to the coupling between the data line **171** and the common electrode **270**.

[0251] According to a liquid crystal display of another exemplary embodiment of the present disclosure, the shielding electrode **83** of the compensation electrode **80** overlaps some, but not all of the plurality of data lines **171**.

[0252] Many characteristics of a liquid crystal displays according to the exemplary embodiments described with reference to FIG. **1** to FIG. **6** and FIG. **8** may be applied to a liquid crystal display of a present exemplary embodiment.

[0253] Next, a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. **24** to FIG. **26**. FIG. **24** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. **25** is a cross-sectional view of the liquid crystal display of FIG. **24** taken along line XXV-XXV. FIG. **26** is a cross-sectional view of the liquid crystal display of FIG. **24** taken along line XXVI-XXVI.

[0254] Referring to FIG. **24** to FIG. **26**, the liquid crystal display according to the present exemplary embodiment includes a lower panel **100** and an upper panel **200** facing each other, and a liquid crystal layer **3** interposed therebetween.

[0255] First, the lower panel **100** will be described.

[0256] A gate line **121** and a compensation voltage line **131** are disposed on a first insulation substrate **110** made of transparent glass or plastic. The gate line **121** and the compensation voltage line **131** are formed together from a same layer.

[0257] The gate line **121** includes agate electrode **124** and a gate pad portion **129**.

[0258] The compensation voltage line **131** extends parallel to the gate line **121** and includes a plurality of extensions **135** and a compensation pad portion **139**.

[0259] A gate insulating layer **140** is disposed on the gate line **121** and the compensation voltage line **131**.

[0260] A semiconductor **154** is disposed on the gate insulating layer **140**.

[0261] Ohmic contacts **163** and **165** are disposed on the semiconductor **154**.

[0262] A data conductor that includes a data line **171**, a source electrode **173** and a drain electrode **175** is disposed on the ohmic contacts **163** and **165** and the gate insulating layer **140**.

[0263] The source electrode **173** is a portion of the data line **171**, and is positioned on the same line as the data line **171**. The drain electrode **175** may be disposed parallel to the source electrode **173**. Accordingly, the drain electrode **175** is parallel to a portion of the data line **171**.

[0264] A first passivation layer **180***x* is disposed on the data conductors **171**, **173**, and **175**, the gate insulating layer **140**, and the exposed portion of the semiconductor **154**.

[0265] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** is thicker than the first passivation layer **180***x* and may have a flat surface.

[0266] The organic layer **180** may be positioned in the display area where a plurality of pixels are positioned, and may not be positioned in the peripheral area where the gate pad portion and the data pad portion are positioned. Alternatively, the organic layer **180** may be positioned in the peripheral area where the gate pad portion and the data pad portion are positioned, where the organic layer **180** may have a lower surface height than the organic layer **180** positioned at the display area.

[0267] The organic layer **180** and the first passivation layer **180***x* have a seventh contact hole **185** that exposes the drain electrode **175**.

[0268] The organic layer **180**, the first passivation layer **180***x*, and the gate insulating layer **140** have an eighth contact hole **186***b* that exposes the compensation voltage line **131**.

[0269] The first passivation layer **180***x* and the gate insulating layer **140** have a fourth contact hole **187** at a region positioned at the gate pad portion **129** where they do not overlap the organic layer **180** that exposes the gate pad portion **129**. Similarly, the first passivation layer **180***x* has a fifth contact hole **188** at a region positioned at the data pad portion **179** where it does not overlap the organic layer **180** that exposes the data pad portion **179**. The first passivation layer **180***x* and the gate insulating layer **140** have a ninth contact hole **189***b* at a region positioned at the compensation pad portion **139** where they do not overlap the organic layer **180** that exposes the compensation pad portion **139**.

[0270] A pixel electrode **191** and a compensation electrode **80** are disposed on the organic layer **180**. The compensation electrode **80** overlaps the data line **171** and extends along with the data line **171**. The compensation electrode **80** includes a second connection **80***b* that extends toward the extension **135** of the compensation voltage line **131**.

[0271] The second connection **80***b* of the compensation electrode **80** is connected to the compensation voltage line **131** through the eighth contact hole **186***b*.

[0272] The pixel electrode **191** and the compensation electrode **80** may be simultaneously formed from a same layer.

[0273] A second passivation layer **180***y* is disposed on the pixel electrode **191** and the compensation electrode **80**, and a common electrode **270**, a first contact assistant **91**, a second contact assistant **92**, and a fourth contact assistant **93***b* are disposed on the second passivation layer **180***y*. The common electrode **270** is formed from a transparent conductive layer such as ITO or IZO.

[0274] The first contact assistant **91** is positioned on the gate pad portion **129** exposed through the fourth contact hole **187**, the second contact assistant **92** is positioned on the data pad portion **179** exposed through the fifth contact hole, and the fourth contact assistant **93***b* is positioned on the compensation pad portion **139** exposed through the nine contact hole **189***b*.

[0275] The second passivation layer **180***y* and the common electrode **270** positioned on the second passivation layer **180***y* have substantially the same planar shape.

[0276] The second passivation layer **180***y* and the common electrode **270** are positioned in the display area where a plurality of pixels are positioned, but are not positioned at the

peripheral area where the gate pad portion **129** and the data pad portion **179** are positioned.

[0277] The common electrode **270** has a plurality of first cutouts **71**, and the second passivation layer **180***y* has a plurality of third cutouts **181**. The first cutout **71** of the common electrode **270** and the third cutout **181** of the second passivation layer **180***y* have substantially the same planar shape. That is, an edge of the first cutout **71** and an edge of the third cutout **181** overlap each other. Therefore, the second passivation layer **180***y* and the common electrode **270** may be formed together using one photomask.

[0278] Now, the upper display panel **200** will be described.

[0279] A light blocking member **220** and a color filter **230** are disposed on the second insulation substrate **210**, and an overcoat **250** is disposed on the color filter **230** and the light blocking member **220**.

[0280] According to a liquid crystal display of the present exemplary embodiment, the compensation electrode **80** overlaps some, but not all data lines **171**. However, according to a liquid crystal display of another exemplary embodiment of the present disclosure, the compensation electrode **80** may overlap all data lines **171**.

[0281] In a liquid crystal display according to the present exemplary embodiment, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel **100** and the color filter **230** may be omitted from the upper panel **200**. In this case, the light blocking member **220** may also be positioned on the lower panel **100** instead of the upper panel **200**.

[0282] As described above, according to a liquid crystal display of a present exemplary embodiment, different from a liquid crystal display according to a exemplary embodiment described with reference to FIG. **9** to FIG. **11**, the common electrode **270** has a plurality of first cutouts **71**, the second passivation layer **180***y* has a plurality of third cutouts **181**, and the first cutouts **71** and the third cutouts **181** have substantially the same planar shape. That is, the edge of the first cutouts **71** and the edge of the third cutouts **181**overlap. Therefore, the second passivation layer **180***y* and the common electrode **270** may be formed together with one photomask.

[0283] The second passivation layer **180***y* and the common electrode **270** are positioned in the display area where a plurality of pixels are positioned, but are not positioned at the peripheral area where the gate pad portion **129** and the data pad portion **179** are positioned.

[0284] By forming the second passivation layer **180***y* and the common electrode **270** together with one photomask, manufacturing cost of the liquid crystal display may be reduced.

[0285] As described with reference to FIG. **7**, according to a liquid crystal display according to a present exemplary embodiment, to compensate a common voltage ripple generated by the coupling of the voltage applied to the data line **171** and the common electrode **270**, a voltage having an opposite polarity to the ripple voltage is applied to the compensation electrode **80**, to prevent the ripple due to the coupling between the data line **171** and the common electrode **270**.

[0286] Many characteristics of a liquid crystal displays according to exemplary embodiments described with reference to FIG. **1** to FIG. **6**, FIG. **9** to FIG. **11**, FIG. **12** to FIG. **17**, and FIG. **18** to FIG. **23** may be applied to a liquid crystal display of a present exemplary embodiment.

[0287] Next, the liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. **27** to FIG. **32**. FIG. **27** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. **28** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXVIII-XXVIII. FIG. **29** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXIX-XXIX. FIG. **30** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXX-XXX. FIG. **31** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXXI-XXXI. FIG. **32** is a cross-sectional view of the liquid crystal display of FIG. **27** taken along the line XXXII-XXXII.

[0288] Referring to FIG. **27** to FIG. **32**, a liquid crystal display according to a present exemplary embodiment is similar to a liquid crystal display according to an exemplary embodiment of FIG. **18** to FIG. **23**. The description of the same constituent elements is omitted.

[0289] Referring to FIG. **27** to FIG. **32**, a liquid crystal display according to an exemplary embodiment of the present disclosure includes a lower panel **100** and an upper panel **200** facing each other, and a liquid crystal layer **3** interposed therebetween.

[0290] First, the lower panel **100** will be described.

[0291] A plurality of first and second gate lines **121***a* and **121***b* are disposed on a first insulation substrate **110**. The first gate line **121***a* and the second gate line **121***b* are disposed in pairs between pixel rows.

[0292] The first gate line **121***a* includes a first gate electrode **124***a*, and the second gate line **121***b* includes a second gate electrode **124***b*. Each of the gate lines **121***a* and **121***b* includes a wide gate pad portion **129** for connection with another layer or an external driving circuit.

[0293] A gate insulating layer **140** is disposed on the plurality of gate lines **121***a* and **121***b*.

[0294] A first semiconductor **154***a* and a second semiconductor **154***b* are disposed on the gate insulating layer **140**.

[0295] Ohmic contacts **163***a* and **165***a* are disposed on the semiconductors **154***a* and **154***b*.

[0296] A plurality of data lines **171**, a plurality of drain electrodes **175***a* and **175***b*, and a plurality of compensation voltage lines **131** are disposed on the ohmic contacts **163***a* and **165***a*.

[0297] The data line **171** transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate lines **121***a* and **121***b*. Each data line **171** is associated with two columns of the pixels.

[0298] Each data line **171** includes a first source electrode **173***a* that extends toward the first gate electrode **124***a* and a second source electrode **173***b* that extends toward the second gate electrode **124***b*.

[0299] Each data line **171** includes a wide data pad portion **179** for connection with another layer or an external driving circuit.

[0300] The first drain electrode **175***a* faces the first source electrode **173***a* and forms a thin film transistor (TFT) along with the first gate electrode **124***a* and the first semiconductor **154***a*, and the second drain electrode **175***b* faces the second source electrode **173***b* and forms a thin film transistor (TFT) along with the second gate electrode **124***b* and the second semiconductor **154***b*.

[0301] The compensation voltage line **131** extends parallel to the data line **171** and each may be associated with two pixel columns. The data line **171** and the compensation voltage line **131** may be alternately disposed.

[0302] The compensation voltage line **131** includes a plurality of extensions **135** and a wide compensation pad portion **139** for connection with another layer or an external driving circuit.

[0303] A first passivation layer **180***x* is disposed on a plurality of data lines **171**, a plurality of drain electrode **175***a* and **175***b*, and a plurality of compensation voltage line **131**.

[0304] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** may be thicker than the first passivation layer **180***x* and have a flat surface.

[0305] The organic layer **180** may be positioned in the display area in which a plurality of pixels are positioned, and may not be positioned in a peripheral area in which the gate pad portion **129**, the data pad portion **179**, and the compensation pad portion **139** are positioned.

[0306] The organic layer **180** and the first passivation layer **180***x* have a first contact hole **185***a* that exposes the first drain electrode **175***a*, a second contact hole **185***b* that exposes the second drain electrode **175***b*, and a third contact hole **186***a* that exposes the extension **135** of the compensation voltage line **131**.

[0307] The first passivation layer **180***x* and the gate insulating layer **140** have a fourth contact hole **187** at a region positioned at the gate pad portion **129** where they do not overlap the organic layer **180** that exposes the gate pad portion **129**. Similarly, the first passivation layer **180***x* has a fifth contact hole **188** at a region positioned at the data pad portion **179** where it does not overlap the organic layer **180** that exposes the data pad portion **179**, and the first passivation layer **180***x* has a sixth contact hole **189***a* at a region positioned at the compensation pad portion **139** where it does not overlap the organic layer **180** that exposes the compensation pad portion **139**.

[0308] A pixel electrode **191** and a compensation electrode **80** are disposed on the organic layer **180**.

[0309] The pixel electrode **191** is positioned at both sides of the data line **171**, and is connected to the first drain electrode **175***a* through the first contact hole **185***a* and the second drain electrode **175***b* through the second contact hole **185***b*.

[0310] The compensation electrode **80** includes a first longitudinal portion **81***a*, a second longitudinal portion **81***b*, a first transverse portion **82***a*, a second transverse portion **82***b*, and a shielding electrode **83**. The first longitudinal portion **81***a* and the second longitudinal portion **81***b* overlap and extend parallel to two compensation voltage lines **131** positioned at both sides of the data line **171**. The first transverse portion **82***a* extends from the first longitudinal portion **81***a* parallel to the direction of the gate lines **121***a* and **121***b*, and the second transverse portion **82***b* extends from the second longitudinal portion **81***b* parallel to the direction of the gate lines **121***a* and **121***b*. The shielding electrode **83** is connected to the first transverse portion **82***a* and the second transverse portion **82***b*, and overlaps and is parallel to the data line **171**.

[0311] The first longitudinal portion **81***a* and the second longitudinal portion **81***b* of the compensation electrode **80** include a plurality of first connections **84** that overlap the extension **135** of the compensation voltage line **131**.

[0312] The first connection **84** of the compensation electrode **80** is connected to the compensation voltage line **131** through the third contact hole **186***a*.

[0313] The pixel electrode **191** and the compensation electrode **80** may be simultaneously formed from the same layer.

[0314] A second passivation layer **180***y* is disposed on the pixel electrode **191** and the compensation electrode **80**, and a common electrode **270**, a first contact assistant **91**, a second contact assistant **92**, and a third contact assistant **93***a* are disposed on the second passivation layer **180***y*.

[0315] The first contact assistant **91** is positioned on the gate pad portion **129** exposed through the fourth contact hole **187**, the second contact assistant **92** is positioned on the data pad portion **179** exposed through the fifth contact hole **188**, and the third contact assistant **93***a* is positioned on the compensation pad portion **139** exposed through the sixth contact hole **189***a*.

[0316] The second passivation layer **180***y* and the common electrode **270** positioned on the second passivation layer **180***y* have substantially the same planar shape.

[0317] The second passivation layer **180***y* and the common electrode **270** are positioned in the display area where a plurality of pixels are positioned, but are not positioned in the peripheral area where the gate pad portion **129** and the data pad portion **179** are positioned.

[0318] The common electrode **270** has a plurality of first cutouts **71**, and the second passivation layer **180***y* has a plurality of third cutouts **181**.

[0319] Different from a liquid crystal display according to an exemplary embodiment described with reference to FIG. **18** to FIG. **23**, the common electrode **270** of a liquid crystal display according to a present exemplary embodiment further includes a second cutout **274** at a region overlapping the data line **171**, and the second passivation layer **180***y* further includes a fourth cutout **184** at a region overlapping the data line **171**.

[0320] The first cutout **71** of the common electrode **270** and the third cutout **181** of the second passivation layer **180***y* have substantially the same planar shape, and the second cutout **274** of the common electrode **270** and the fourth cutout **184** of the second passivation layer **180***y* have substantially the same planar shape. An edge of the first cutout **71** overlaps an edge of the third cutout **181**, and an edge of the second cutout **274** overlaps an edge of the fourth cutout **184**. Therefore, the second passivation layer **180***y* and the common electrode **270** may be formed together using one photomask.

[0321] Now, the upper display panel **200** will be described.

[0322] A light blocking member **220** and a color filter **230** are disposed on the second insulation substrate **210**, and an overcoat **250** is disposed on the color filter **230** and the light blocking member **220**.

[0323] The liquid crystal layer **3** includes a plurality of liquid crystal molecules positioned on the pixel electrode **191** and the common electrode **270**, and are arranged such that long axis direction thereof is aligned parallel to the display panels **100** and **200**.

[0324] The pixel electrode **191** receives a data voltage from the drain electrodes **175***a* and **175***b*, and the common electrode **270** receives a common voltage having a predetermined magnitude from a common voltage applying unit which is disposed outside the display region.

[0325] The pixel electrode **191** and the common electrode **270** are the field generating electrodes that generate an electric field that rotates the liquid crystal molecules of the liquid crystal layer **3** in a direction parallel with a direction of the electric field. The polarization of light passing through the

liquid crystal layer **3** changes due to the rotation direction of the liquid crystal molecules as described above.

[0326] In a liquid crystal display according to a present exemplary embodiment, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel **100** and the color filter **230** may be omitted from the upper panel **200**. In this case, the light blocking member **220** may also be positioned on the lower panel **100** instead of the upper panel **200**.

[0327] As described with reference to FIG. **7**, according to a liquid crystal display according to a present exemplary embodiment, to compensate common voltage ripple generated by the coupling of the voltage applied to the data line **171** and the common electrode **270**, the voltage having a polarity opposite to the ripple voltage is applied to the compensation electrode **80** to prevent the ripple due to the coupling between the data line **171** and the common electrode **270**.

[0328] Also, in a liquid crystal display according to a present exemplary embodiment, the common electrode **270** has a second cutout **274** in the region overlapping the data line **171**, which may reduce the overlap area between the data line **171** and the common electrode **270**. Accordingly, reducing the coupling between the data line **171** and the common electrode **270** may further prevent a common voltage ripple generated by the coupling between the data line **171** and the common electrode **270**.

[0329] Many characteristics of liquid crystal displays according to exemplary embodiments described with reference to FIG. **1** to FIG. **6**, FIG. **9** to FIG. **11**, FIG. **12** to FIG. **17**, and FIG. **18** to FIG. **23** may be applied to a liquid crystal display of the present exemplary embodiment.

[0330] Next, a liquid crystal display according to an exemplary embodiment of the present disclosure will be described with reference to FIG. **33** to FIG. **35**. FIG. **33** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. **34** is a cross-sectional view of the liquid crystal display of FIG. **33** taken along the line XXXIV-XXXIV'. FIG. **35** is a cross-sectional view of the liquid crystal display of FIG. **33** taken along the line XXXV-XXXV'.

[0331] Referring to FIG. **33** to FIG. **35**, a liquid crystal display according to an exemplary embodiment of the present disclosure includes a lower panel **100** and an upper panel **200** facing each other, and a liquid crystal layer **3** interposed therebetween.

[0332] First, the lower panel **100** will be described.

[0333] A plurality of first and second gate lines **121***a* and **121***b* are disposed on a first insulation substrate **110** made of a transparent glass or plastic.

[0334] The first gate line **121***a* and the second gate line **121***b* are disposed in pairs between pixel rows.

[0335] The first gate line **121***a* includes a first gate electrode **124***a*, and the second gate line **121***b* includes a second gate electrode **124***b*. Each of the gate lines **121***a* and **121***b* includes a wide gate pad portion **129** for connection with another layer or an external driving circuit.

[0336] A gate insulating layer **140** is disposed on the plurality of gate lines **121***a* and **121***b*.

[0337] A first semiconductor **154***a* and a second semiconductor **154***b* are disposed on the gate insulating layer **140**. The semiconductors **154***a* and **154***b* may include an oxide semiconductor.

[0338] Ohmic contacts **163***a* and **165***a* are disposed on the semiconductors **154***a* and **154***b*. If the semiconductors **154***a* and **154***b* include an oxide semiconductor, the ohmic contacts **163***a* and **165***a* may be omitted.

[0339] A plurality of data lines **171**, a plurality of drain electrodes **175***a* and **175***b*, and a plurality of compensation voltage lines **131** are disposed on the ohmic contacts **163***a* and **165***a*.

[0340] The data line **171** transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate lines **121***a* and **121***b*. Each data line **171** is associated with two columns of pixels.

[0341] The data line **171** may have a first curved portion with a curved shape to acquire maximize transmittance of the liquid crystal display, and the first curved portion may meet a second curved portion which forms a predetermined angle with the first curved portion at a "V" shape in a middle region of the pixel area.

[0342] Each data line **171** includes a first source electrode **173***a* that extends toward the first gate electrode **124***a* and a second source electrode **173***b* that extends toward the second gate electrode **124***b*.

[0343] Each data line **171** includes a wide data pad portion **179** for connection with another layer or an external driving circuit.

[0344] The first drain electrode **175***a* includes one end that faces the first source electrode **173***a* and a wide other end, and forms a thin film transistor (TFT) along with the first gate electrode **124***a* and the first semiconductor **154***a*.

[0345] The second drain electrode **175***b* includes one end that faces the second source electrode **173***b* and a wide other end, and forms a thin film transistor (TFT) along with the second gate electrode **124***b* and the second semiconductor **154***b*.

[0346] The compensation voltage line **131** extends parallel to the data line **171** and each may be associated with two pixel columns. The data line **171** and the compensation voltage line **131** may be alternately disposed.

[0347] The compensation voltage line **131** includes a plurality of extensions **135**, and includes a wide compensation pad portion **139** for connection with another layer or an external driving circuit.

[0348] A first passivation layer **180***x* is disposed on the plurality of data lines **171**, the plurality of drain electrodes **175***a* and **175***b*, and the plurality of compensation voltage lines **131**. The first passivation layer **180***x* may be made of an organic insulating material or an inorganic insulating material.

[0349] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** may be thicker than the first passivation layer **180***x*, and have a flat surface.

[0350] In a liquid crystal display according to another exemplary embodiment of the present disclosure, the organic layer **180** may be omitted. In a liquid crystal display according to another exemplary embodiment of the present disclosure, the organic layer **180** may be a color filter, and in this case, a layer disposed on the organic layer **180** may be further included. For example, an overcoat or capping layer may be disposed on the color filter to prevent a color filter pigment

from flowing into the liquid crystal layer, and the overcoat may be made of an insulating material such as a silicon nitride (SiNx).

[0351] The organic layer **180** may be positioned in the display area in which a plurality of pixels are positioned, and may not be positioned in a peripheral area in which the gate pad portion **129**, the data pad portion **179**, and the compensation pad portion **139** are positioned.

[0352] A first height H1 of the organic layer **180** positioned in the display area is greater than a second height H2 of the organic layer **180** positioned near the gate pad portion **129**, the data pad portion **179**, and the compensation pad portion **139**.

[0353] A common electrode **270** is disposed on the organic layer **180**.

[0354] The common electrode **270** is disposed on the whole display area and may have a plate-type planar shape, and is connected to a common electrode **270** disposed in an adjacent pixel. A plate type means a planar shape without splitting.

[0355] The common electrode **270** includes a sixth cutout **38***a* at a region that overlaps the first drain electrode **175***a*, a seventh cutout **38***b* at a region that overlaps the second drain electrode **175***b*, and an eighth cutout **38***c* at a region that overlaps the extension **135** of the compensation voltage line **131**.

[0356] A second passivation layer **180***y* is disposed on the common electrode **270**.

[0357] The second passivation layer **180***y*, the organic layer **180**, and the first passivation layer **180***x* have a first contact hole **185***a* that exposes the first drain electrode **175***a*, a second contact hole **185***b* that exposes the second drain electrode **175***b*, and a third contact hole **186***a* that exposes the extension **135** of the compensation voltage line **131**. The first contact hole **185***a* is disposed in the sixth cutout **38***a* of the common electrode **270**, the second contact hole **185***b* is disposed in the seventh cutout **38***b* of the common electrode **270**, and the third contact hole **186***a* is disposed in the eighth cutout **38***c* of the common electrode **270**.

[0358] The second passivation layer **180***y*, the first passivation layer **180***x*, and the gate insulating layer **140** have a fourth contact hole **187** in a region positioned at the gate pad portion **129** where they do not overlap the organic layer **180** that exposes the gate pad portion **129**. Similarly, the second passivation layer **180***y* and the first passivation layer **180***x* have a fifth contact hole **188** in a region positioned at the data pad portion where they do not overlap the organic layer that exposes the data pad portion **179**, and the second passivation layer **180***y* and the first passivation layer **180***x* have a sixth contact hole **189***a* in a region positioned at the compensation pad portion **139** where they do not overlap the organic layer **180** that exposes the compensation pad portion **139**.

[0359] A pixel electrode **191**, a compensation electrode **80**, a first contact assistant **91**, a second contact assistant **92**, and a third contact assistant **93***a* are disposed on the second passivation layer **180***y*.

[0360] The pixel electrode **191** has a plurality of fifth cutouts **193**. The pixel electrode **191** includes a plurality of second branch electrodes **192** defined by the plurality of fifth cutouts **193**. A plurality of second branch electrodes **192** of the pixel electrode **191** extend substantially parallel to the data line **171** and overlap the common electrode **270**.

[0361] The pixel electrode **191** is positioned at both sides of the data line **171**, and is connected to the first drain electrode **175***a* through the first contact hole **185***a* and the second drain electrode **175***b* through the second contact hole **185***b*.

[0362] The compensation electrode **80** includes a first longitudinal portion **81***a*, a second longitudinal portion **81***b*, a first transverse portion **82***a*, a second transverse portion **82***b*, and a shielding electrode **83**. The first longitudinal portion **81***a* and the second longitudinal portion **81***b* extend parallel to and overlap two compensation voltage lines **131** positioned at both sides of the data line **171**. The first transverse portion **82***a* extends from the first longitudinal portion **81***a* parallel to the direction of the gate lines **121***a* and **121***b*, and the second transverse portion **82***b* extends from the second longitudinal portion **81***b* parallel to the direction of the gate lines **121***a* and **121***b*. The shielding electrode **83** is connected to the first transverse portion **82***a* and the second transverse portion **82***b* and is parallel to and overlaps the data line **171**.

[0363] The first longitudinal portion **81***a* and the second longitudinal portion **81***b* of the compensation electrode **80** include a plurality of first connections **84** that overlap the extension **135** of the compensation voltage line **131**.

[0364] The first connection **84** of the compensation electrode **80** is connected to the compensation voltage line **131** through the third contact hole **186***a*.

[0365] The first contact assistant **91** is positioned on the gate pad portion **129** exposed through the fourth contact hole **187**, the second contact assistant **92** is positioned on the data pad portion **179** exposed through the fifth contact hole **188**, and the third contact assistant **93***a* is positioned on the compensation pad portion **139** exposed through the sixth contact hole **189***a*.

[0366] The pixel electrode **191**, the compensation electrode **80**, the first contact assistant **91**, the second contact assistant **92**, and the third contact assistant **93***a* are formed from a transparent conductive layer such as ITO or IZO. The pixel electrode **191**, the compensation electrode **80**, the first contact assistant **91**, the second contact assistant **92**, and the third contact assistant **93***a* may be simultaneously formed from a same layer.

[0367] In addition, a horizontal first alignment layer rubbed in a predetermined direction may be applied on the second passivation layer **180***y* and the pixel electrode **191**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the first alignment layer may include a photoreactive material to be photo-aligned.

[0368] Now, the upper display panel **200** will be described.

[0369] A light blocking member **220** is disposed on a second insulating substrate **210** made of transparent glass, plastic, etc. The light blocking member **220** is also called a black matrix and prevents light leakage.

[0370] A plurality of color filters **230** are also disposed on the second substrate **210**.

[0371] An overcoat **250** is disposed on the color filter **230** and the light blocking member **220**. The overcoat **250** is made of an organic insulator, prevents exposure of the color filter **230**, and provides a flat surface. The overcoat **250** may be omitted.

[0372] In addition, a horizontal second alignment layer rubbed in a predetermined direction may be disposed on the overcoat **250**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the second alignment layer may include a photoreactive material to be photo-aligned.

[0373] The liquid crystal layer **3** includes a plurality of liquid crystal molecules positioned on the pixel electrode **191** and the common electrode **270** that are arranged such that long axis direction thereof is aligned parallel to the display panels **100** and **200**.

[0374] The pixel electrode **191** receives a data voltage from the drain electrodes **175***a* and **175***b* and the common electrode **270** receives a common voltage having a predetermined magnitude from a common voltage applying unit which is disposed outside the display region.

[0375] The pixel electrode **191** and the common electrode **270** are field generating electrodes that generate an electric field that rotates the liquid crystal molecules of the liquid crystal layer **3** in a direction parallel with a direction of the electric field. The polarization of light passing through the liquid crystal layer **3** changes due to the rotation direction of the liquid crystal molecules as described above.

[0376] In a liquid crystal display according to a present exemplary embodiment, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel **100** and the color filter **230** may be omitted from the upper panel **200**. In this case, the light blocking member **220** may also be positioned on the lower panel **100** instead of the upper panel **200**.

[0377] In a liquid crystal display according to the present exemplary embodiment, different from liquid crystal displays according to exemplary embodiments described with reference to FIG. **1** to FIG. **6** and FIG. **8** to FIG. **32**, the common electrode **270** has a planar shape, the second passivation layer **180***y* is an insulating layer disposed on the common electrode **270**, the pixel electrode **191** has a plurality of second branch electrodes **192**, and a plurality of second branch electrodes **192** of the pixel electrode **191** overlap the common electrode **270**.

[0378] As described with reference to FIG. **7**, according to a liquid crystal display according to a present exemplary embodiment, to compensate a common voltage ripple generated by the coupling of the voltage applied to the data line **171** and the common electrode **270**, a voltage having a polarity opposite to the common voltage ripple is applied to the compensation electrode **80** to prevent the ripple due to the coupling between the data line **171** and the common electrode **270**.

[0379] The shielding electrode **83** of the compensation electrode **80** of the liquid crystal display according to the present exemplary embodiment may overlap some or all of the data lines **171**.

[0380] Many characteristics of liquid crystal displays according to previously described exemplary embodiments may be applied to a liquid crystal display of a present exemplary embodiment.

[0381] Next, a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. **36** to FIG. **38**. FIG. **36** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure. FIG. **37** is a cross-sectional view of the liquid crystal display of FIG. **36** taken along the line XXXVII-XXXVII. FIG. **38** is a cross-sectional view of the liquid crystal display of FIG. **36** taken along the line XXXVIII-XXXVIII.

[0382] Referring to FIG. **36** to FIG. **38**, a liquid crystal display according to an exemplary embodiment of the present disclosure includes a lower panel **100** and an upper panel **200** facing each other, and a liquid crystal layer **3** interposed therebetween.

[0383] First, the lower panel **100** will be described.

[0384] A gate line **121** and a compensation voltage line **131** are disposed on a first insulation substrate **110** made of transparent glass or plastic. The gate line **121** and the compensation voltage line **131** are formed together from a same layer.

[0385] The gate line **121** includes a gate electrode **124** and the gate pad portion **129**.

[0386] The compensation voltage line **131** extends parallel to the gate line **121**, and includes a plurality of extensions **135** and the compensation pad portion **139**.

[0387] A gate insulating layer **140** is disposed on the gate line **121** and the compensation voltage line **131**.

[0388] A semiconductor **154** is disposed on the gate insulating layer **140**.

[0389] Ohmic contacts **163** and **165** are disposed on the semiconductor **154**. The ohmic contacts **163** and **165** may be disposed as a pair on the semiconductor **154**. If the semiconductor **154** is an oxide semiconductor, the ohmic contacts **163** and **165** may be omitted.

[0390] A data conductor that includes a data line **171**, a source electrode **173** and a drain electrode **175** is disposed on the ohmic contacts **163** and **165** and the gate insulating layer **140**.

[0391] The data line **171** includes a wide end for connection with other layers or an external driving circuit. The data line **171** transmits a data signal and extends in a substantially longitudinal direction thereby intersecting the gate line **121**.

[0392] In addition, the data line **171** may have a first curved portion with a curved shape to maximize transmittance of the liquid crystal display, and the first curved portions may meet second curved portions which form a predetermined angle with the first curved portions at a center region of the pixel area thereby forming a "V" shape.

[0393] The source electrode **173** is a portion of the data line **171**, and is positioned on the same line as the data line **171**. The drain electrode **175** may be parallel to the source electrode **173**. Accordingly, the drain electrode **175** is parallel to the data line **171**.

[0394] The gate electrode **124**, the source electrode **173**, and the drain electrode **175** form a thin film transistor (TFT) along with the semiconductor **154**, and a channel of the thin film transistor forms in the semiconductor **154** between the source electrode **173** and the drain electrode **175**.

[0395] A liquid crystal display according to a present exemplary embodiment includes the source electrode **173** positioned on the same line as the data line **171** and the drain electrode **175** extending parallel to the data line **171** such that a width of the thin film transistor may increase without increasing an area occupied by the data conductor, thereby increasing an aperture ratio of the liquid crystal display.

[0396] However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the source electrode **173** and the drain electrode **175** have different shapes.

[0397] A first passivation layer **180***x* is disposed on the data conductors **171**, **173**, and **175**, the gate insulating layer **140**, and the exposed portion of the semiconductor **154**. The first passivation layer **180***x* may be made of an organic insulating material or an inorganic insulating material.

[0398] An organic layer **180** is disposed on the first passivation layer **180***x*. The organic layer **180** is thicker than the first passivation layer **180***x* and may have a flat surface.

[0399] The organic layer **180** may be positioned in the display area where a plurality of pixels are positioned, and may not be positioned in the peripheral area where the gate pad portion and the data pad portion are positioned. Alternatively, the organic layer **180** may be positioned in the peripheral area where the gate pad portion or the data pad portion are positioned, and may have a lower surface height than the organic layer **180** positioned in the display area.

[0400] A common electrode **270** is disposed on the organic layer **180**.

[0401] The common electrode **270** is disposed on the whole display area and may have a planar shape, and is connected to a common electrode **270** disposed in an adjacent pixel. The common electrode **270** has a plate-type plane shape without splitting.

[0402] The common electrode **270** includes a ninth cutout **38***d* at a region that overlaps the drain electrode **175** and a tenth cutout **38***e* at a region that overlaps the extension **135** of the compensation voltage line **131**.

[0403] A second passivation layer **180***y* is disposed on the common electrode **270**.

[0404] The second passivation layer **180***y*, the organic layer **180**, and the first passivation layer **180***x* have a seventh contact hole **185** that exposes the drain electrode **175**.

[0405] The organic layer **180**, the first passivation layer **180***x*, and the gate insulating layer **140** have an eighth contact hole **186***b* that exposes the compensation voltage line **131**.

[0406] The seventh contact hole **185** is disposed in the ninth cutout **38***d* of the common electrode **270**, and the eighth contact hole **186***b* is disposed in a tenth cutout **38***e* of the common electrode **270**.

[0407] The second passivation layer **180***y*, the first passivation layer **180***x*, and the gate insulating layer **140** have a fourth contact hole **187** in a region positioned at the gate pad portion **129** where they do not overlap the organic layer **180** that exposes the gate pad portion **129**. Similarly, the second passivation layer **180***y*, the first passivation layer **180***x*, and the gate insulating layer **140** have a ninth contact hole **189***b* in a region positioned at the compensation pad portion **139** where they do not overlap the organic layer **180** that exposes the compensation pad portion **139**. The second passivation layer **180***y* and the first passivation layer have a fifth contact hole **188** in a region positioned at the data pad portion **179** where they do not overlap the organic layer that exposes the data pad portion **179**.

[0408] A pixel electrode **191**, a compensation electrode **80**, a first contact assistant **91**, a second contact assistant **92**, and a fourth contact assistant **93***b* are disposed on the second passivation layer **180***y*.

[0409] The pixel electrode **191** has a plurality of fifth cutouts **193**. The pixel electrode **191** includes a plurality of second branch electrodes **192** defined by a plurality of fifth cutouts **193**. The plurality of second branch electrodes **192** extend substantially parallel to the data line **171** and overlap the common electrode **270**.

[0410] The compensation electrode **80** overlaps and extends along with the data line **171**. The compensation elertrode **80** includes a second connection **80***b* that extends toward the extension **135** of the compensation voltage line **131**.

[0411] The second connection **80***b* of the compensation electrode **80** is connected to the compensation voltage line **131** through the eighth contact hole **186***b*.

[0412] The first contact assistant **91** is disposed on the gate pad portion **129** exposed through the fourth contact hole **187**, and the second contact assistant **92** is disposed on the data pad portion **179** exposed through the fifth contact hole **188**. Also, the fourth contact assistant **93***b* is disposed on the compensation pad portion **139** exposed through the ninth contact hole **189***b*.

[0413] The pixel electrode **191**, the compensation electrode **80**, the first contact assistant **91**, the second contact assistant **92**, and the fourth contact assistant **93***b* are formed from a transparent conductive layer such as ITO or IZO. The pixel electrode **191**, the compensation electrode **80**, the first contact assistant **91**, the second contact assistant **92**, and the fourth contact assistant **93***b* may be simultaneously formed from a same layer.

[0414] Next, the upper panel **200** will be described.

[0415] A light blocking member **220** and a color filter **230** are disposed on the second insulation substrate **210**, and an overcoat **250** is disposed on the color filter **230** and the light blocking member **220**.

[0416] According to a liquid crystal display of a present exemplary embodiment, the compensation electrode **80** overlaps some, but not all of the data lines **171**. However, according to a liquid crystal display of another exemplary embodiment of the present disclosure, the compensation electrode **80** may overlap all data lines **171**.

[0417] In a liquid crystal display according to a present exemplary embodiment, the organic layer **180** is positioned on the first passivation layer **180***x* of the lower panel **100**, and the color filter **230** and the light blocking member **220** are positioned on the upper panel **200**. However, in a liquid crystal display according to another exemplary embodiment of the present disclosure, the color filter **230** may replace the organic layer **180** on the lower panel **100** and the color filter **230** may be omitted from the upper panel **200**. In this case, the light blocking member **220** may also be positioned on the lower panel **100** instead of the upper panel **200**.

[0418] In a liquid crystal display according to a present exemplary embodiment, different from liquid crystal displays according to exemplary embodiments described with reference to FIG. **1** to FIG. **6** and FIG. **8** to FIG. **32**, the common electrode **270** has a planar shape, the second passivation layer **180***y* is an insulating layer disposed on the common electrode **270**, the pixel electrode **191** has a plurality of second branch electrodes **192**, and a plurality of second branch electrodes **192** of the pixel electrode **191** overlap the common electrode **270**.

[0419] As described with reference to FIG. **7**, according to a liquid crystal display according to a present exemplary embodiment, to compensate a common voltage ripple generated by the coupling of the voltage applied to the data line **171** and the common electrode **270**, a voltage having an opposite polarity to the common voltage ripple is applied to the compensation electrode **80** to prevent the ripple due to the coupling between the data line **171** and the common electrode **270**.

[0420] Many characteristics of liquid crystal displays according to previously described exemplary embodiments may be applied to a liquid crystal display of a present exemplary embodiment.

[0421] Next, a liquid crystal display according to another exemplary embodiment of the present disclosure will be described with reference to FIG. **39**. FIG. **39** is a layout view of a liquid crystal display according to another exemplary embodiment of the present disclosure.

[0422] Referring to FIG. **39**, a liquid crystal display according to a present exemplary embodiment is similar to a liquid crystal display according to an exemplary embodiment described with reference to FIG. **33** to FIG. **35**. The description of the same constituent elements is omitted.

[0423] Referring to FIG. **39**, different from an exemplary embodiment shown in FIG. **33** to FIG. **35**, the common electrode **270** of the liquid crystal display according to a present exemplary embodiment further includes a second cutout **274** at the region overlapping the data line **171**.

[0424] The common electrode **270** further includes the second cutout **274** at the region overlapping the data line **171** to reduce the overlap area between the data line **171** and the common electrode **270**. Accordingly, the coupling between the data line **171** and the common electrode **270** may be reduced to prevent a common voltage ripple generated by the coupling between the data line **171** and the common electrode **270**.

[0425] Many features of a liquid crystal display according to previously described exemplary embodiments may be applied to a liquid crystal display according to a present exemplary embodiment.

[0426] As described above, according to a liquid crystal display according to an exemplary embodiment of the present disclosure, when forming two field generating electrodes on one display pane, manufacturing cost may be reduced while preventing a common voltage ripple generated by the coupling between the data line and the common electrode.

[0427] While this disclosure has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the disclosure is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A liquid crystal display comprising:

a gate line, a data line, and a compensation voltage line disposed on an insulation substrate;

a first passivation layer disposed on the gate line, the data line, and the compensation voltage line;

a pixel electrode connected to the gate line and the data line, and a compensation electrode connected to the compensation voltage line, disposed on the first passivation layer; and

a common electrode disposed on the first passivation layer,

wherein the compensation electrode overlaps at least a portion of the data line, and the compensation voltage line is formed from a same layer as the data line.

2. The liquid crystal display of claim **1**, wherein

the compensation voltage line is formed from a same layer as the data line

3. The liquid crystal display of claim **2**, wherein

the compensation voltage line extends parallel to the data line.

4. The liquid crystal display of claim **3**, wherein

the compensation voltage line is positioned between two adjacent data lines.

5. The liquid crystal display of claim **4**, wherein

the data line includes a plurality of data lines, and

the compensation electrode overlaps at least some of the plurality of data lines.

6. The liquid crystal display of claim **5**, wherein

the common electrode overlaps the data line, and

the common electrode overlaps the compensation electrode.

7. The liquid crystal display of claim **6**, wherein

the common electrode has a cutout formed at a position that overlaps the data line.

8. The liquid crystal display of claim **6**, further comprising

a second passivation layer disposed on the pixel electrode and the compensation electrode, and under the common electrode.

9. The liquid crystal display of claim **8**, wherein

the common electrode has a first cutout, the second passivation layer has a second cutout, and

an edge of the first cutout overlaps an edge of the second cutout.

10. The liquid crystal display of claim **5**, further comprising

a second passivation layer disposed on the common electrode and under the pixel electrode and the compensation electrode.

11. The liquid crystal display of claim **6**, wherein

the pixel electrode and the compensation electrode are formed from a same layer.

12. The liquid crystal display of claim **1**, wherein

the compensation voltage line is formed from a same layer as the gate line.

13. The liquid crystal display of claim **12**, wherein

the compensation voltage line extends parallel to the gate line.

14. The liquid crystal display of claim **12**, wherein

the common electrode overlaps the data line, and

the common electrode overlaps the compensation electrode.

15. The liquid crystal display of claim **12**, further comprising

a second passivation layer disposed on the pixel electrode and the compensation electrode, and under the common electrode.

16. The liquid crystal display of claim **15**, wherein

the common electrode has a first cutout, the second passivation layer has a second cutout, and

an edge of the first cutout overlaps an edge of the second cutout.

17. The liquid crystal display of claim **12**, further comprising

a second passivation layer disposed on the common electrode and under the pixel electrode and the compensation electrode.

18. The liquid crystal display of claim **12**, wherein

the pixel electrode and the compensation electrode are formed from a same layer.

19. The liquid crystal display of claim **1**, wherein

the data line includes a plurality of data lines, and

the compensation electrode overlaps at least some of the plurality of data lines.

20. The liquid crystal display of claim **19**, wherein

the common electrode overlaps the data line, and

the common electrode overlaps the compensation electrode.

21. The liquid crystal display of claim **20**, wherein

the common electrode has a cutout formed at a position that overlaps the data line.

22. The liquid crystal display of claim **20**, further comprising

a second passivation layer disposed on the pixel electrode and the compensation electrode, and under the common electrode.

23. The liquid crystal display of claim **22**, wherein

the common electrode has a first cutout, the second passivation layer has a second cutout, and

an edge of the first cutout overlaps an edge of the second cutout.

24. The liquid crystal display of claim **20**, further comprising

a second passivation layer disposed on the common electrode and under the pixel electrode and the compensation electrode.

25. The liquid crystal display of claim **20**, wherein

the pixel electrode and the compensation electrode are formed from a same layer.

26. The liquid crystal display of claim **1**, wherein

the common electrode overlaps the data line, and

the common electrode overlaps the compensation electrode.

27. The liquid crystal display of claim **26**, wherein

the common electrode has a cutout formed at a position that overlaps the data line.

28. The liquid crystal display of claim **26**, further comprising

a second passivation layer disposed on the pixel electrode and the compensation electrode, and under the common electrode.

29. The liquid crystal display of claim **1**, wherein

the pixel electrode and the compensation electrode are formed from a same layer.

* * * * *

专利名称(译)	液晶显示器		
公开(公告)号	US20150160489A1	公开(公告)日	2015-06-11
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[标]申请(专利权)人(译)	三星显示有限公司		
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摘要(译)

根据本公开示例性实施例的液晶显示器包括：栅极线，数据线和设置在绝缘基板上的补偿电压线;第一钝化层，设置在栅极线，数据线和补偿电压线上;连接到栅极线和数据线的像素电极，以及连接到补偿电压线的补偿电极，设置在第一钝化层上;形成在第一钝化层上的公共电极，其中补偿电极与数据线的至少一部分重叠，并且补偿电压线形成有与数据线相同的层。