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(54) LIQUID CRYSTAL DISPLAY

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(52) **U.S. Cl.** **349/38**

(57) **ABSTRACT**

A liquid crystal display according to exemplary embodiments of the present invention includes: an insulation substrate; a first gate line and a second gate line formed on the insulation substrate; a data line intersecting the first gate line and the second gate line; a plurality of pixels respectively including a first subpixel and a second subpixel connected to the first gate line and the data line; a first switching element connected to the first gate line and to control a voltage of the first capacitor connected to the first subpixel electrode of the first subpixel; and a second switching element connected to the second gate line to control the voltage of the first capacitor.

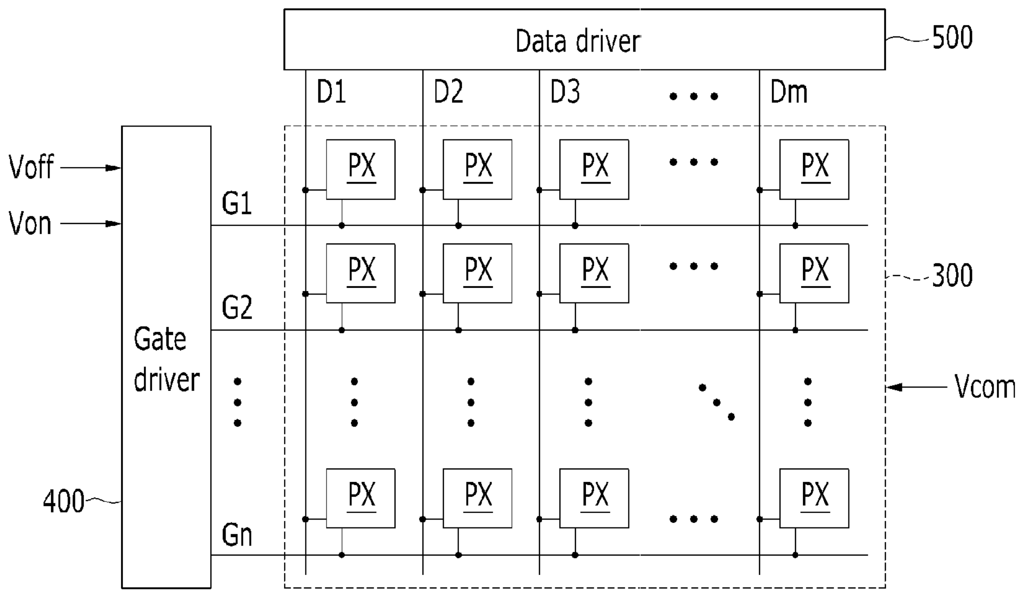


FIG. 1

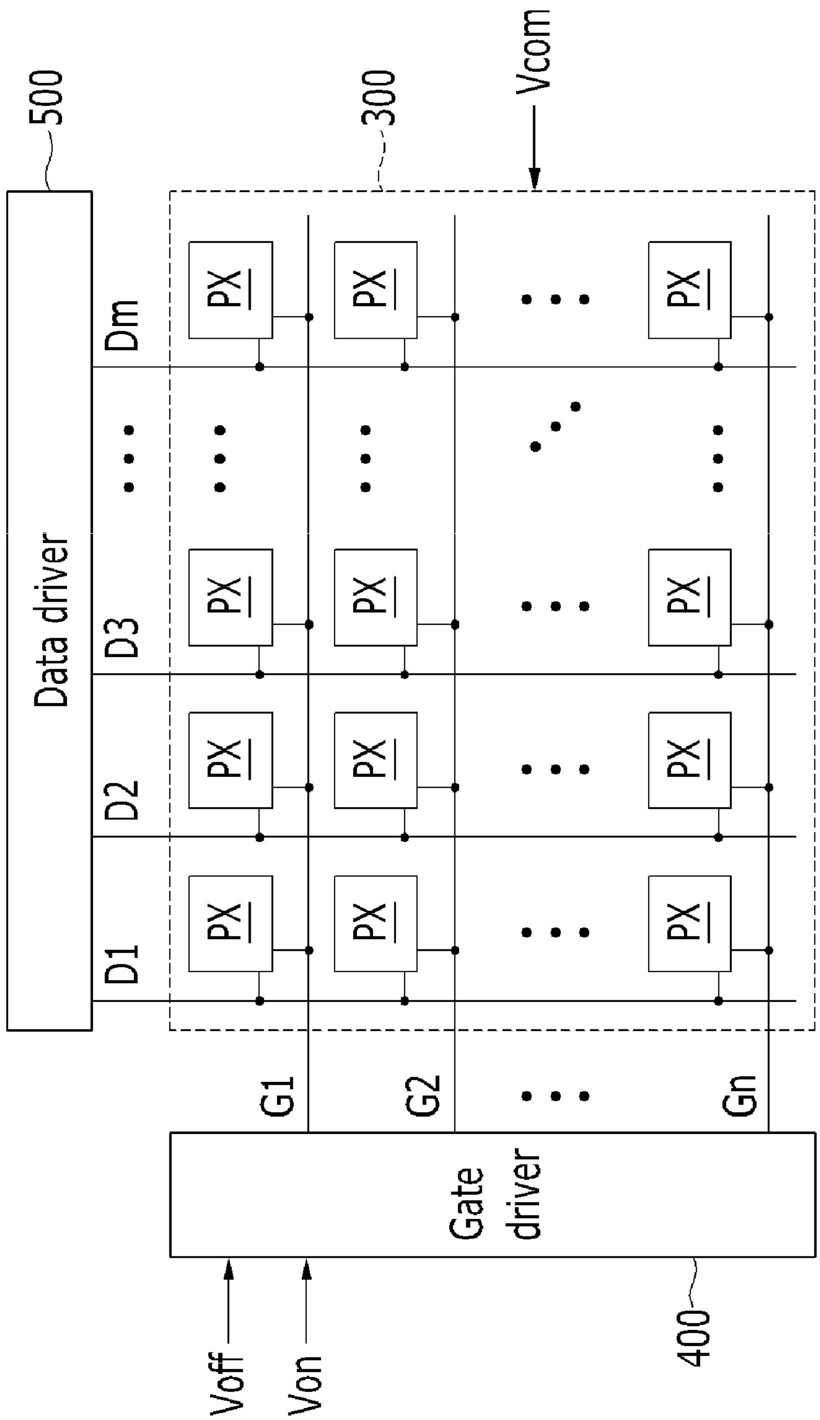

500
Data driver
300
Vcom
D1
D2
D3
Dm
PX
G1
G2
Gn
Gate driver
400
Voff
Von

FIG. 2

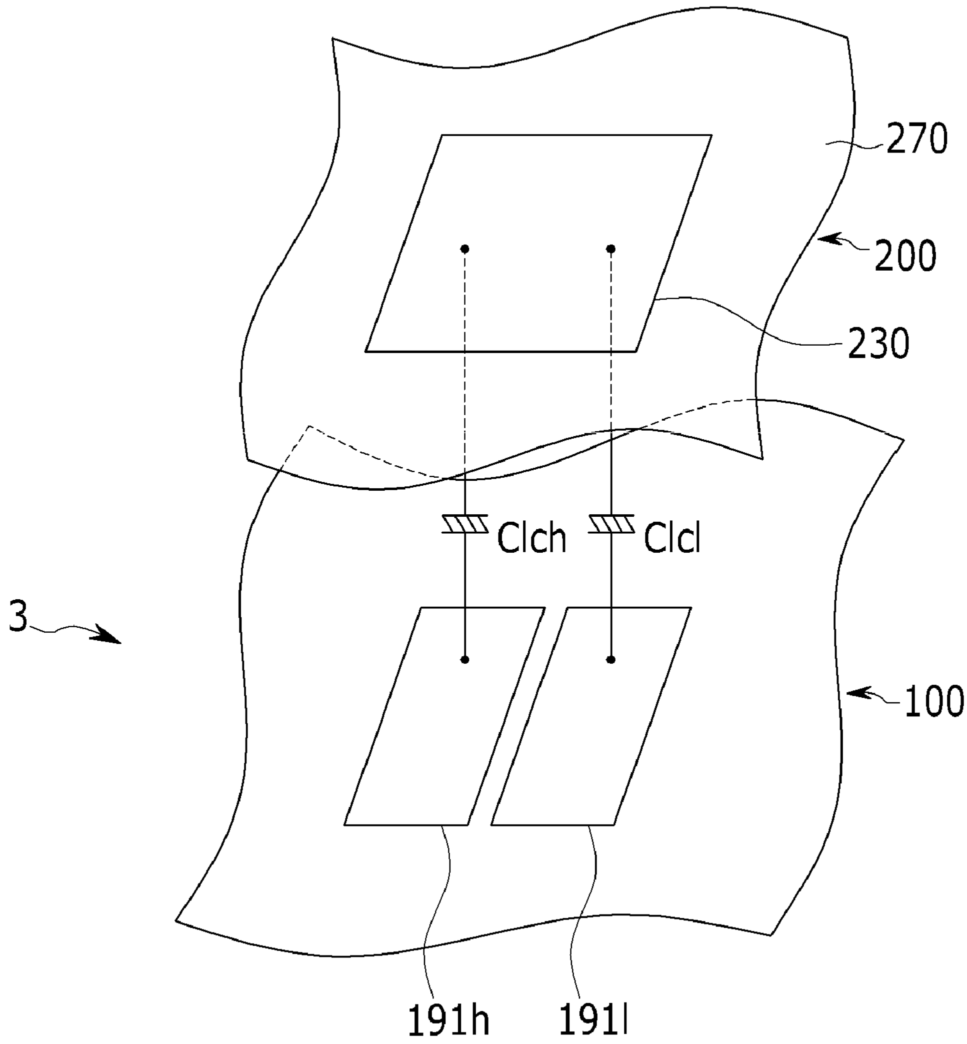


FIG. 3

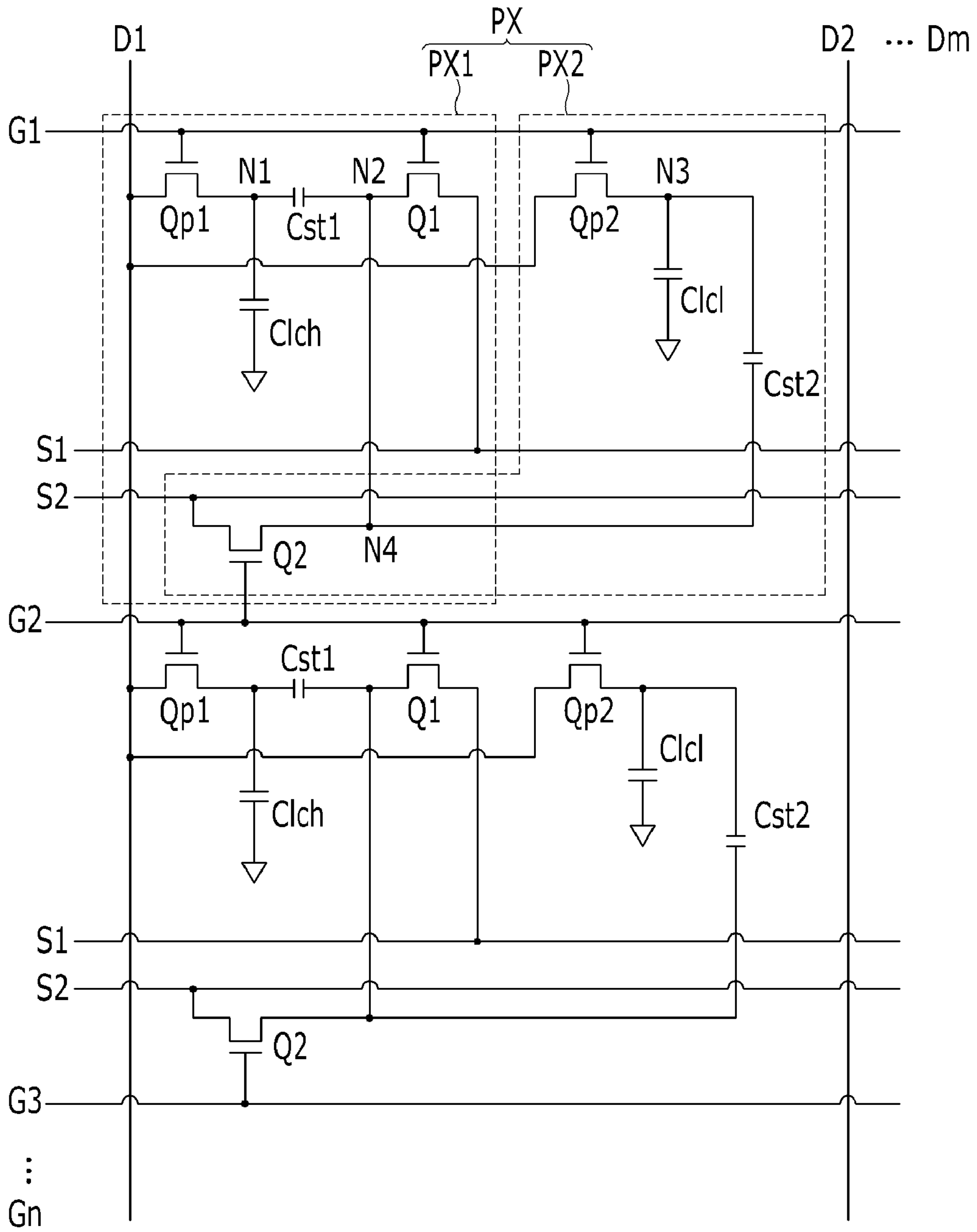

PX
D1
PX1
PX2
D2
··· Dm
G1
N1
N2
N3
Qp1
Cst1
Q1
Qp2
Clch
Clcl
Cst2
S1
S2
Q2
N4
G2
Cst1
Qp1
Q1
Qp2
Clcl
Clch
Cst2
S1
S2
Q2
G3
⋮
Gn

FIG. 4

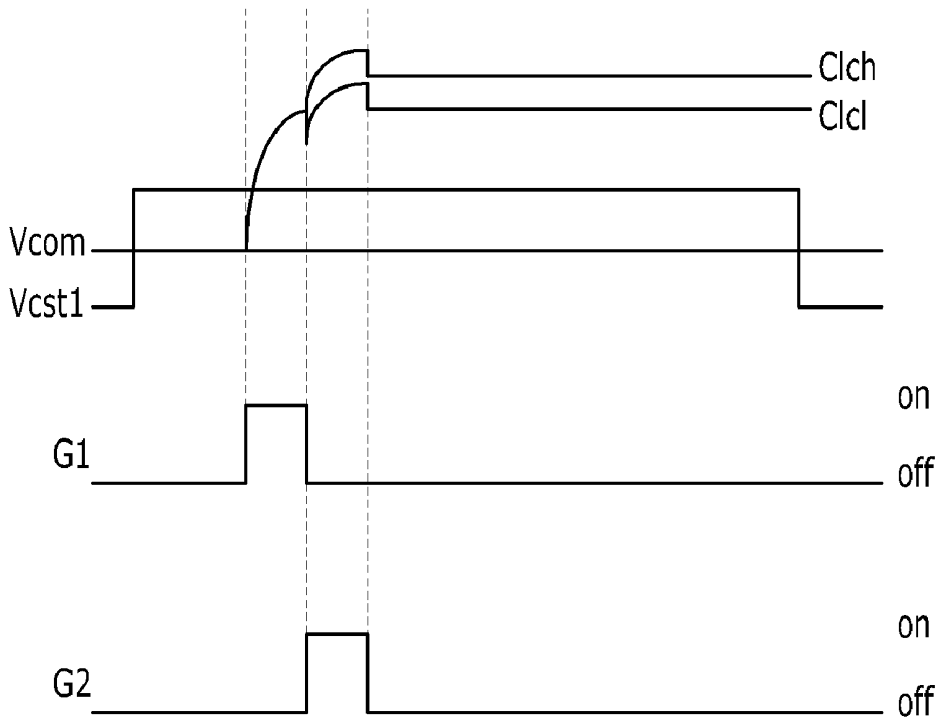


FIG. 5

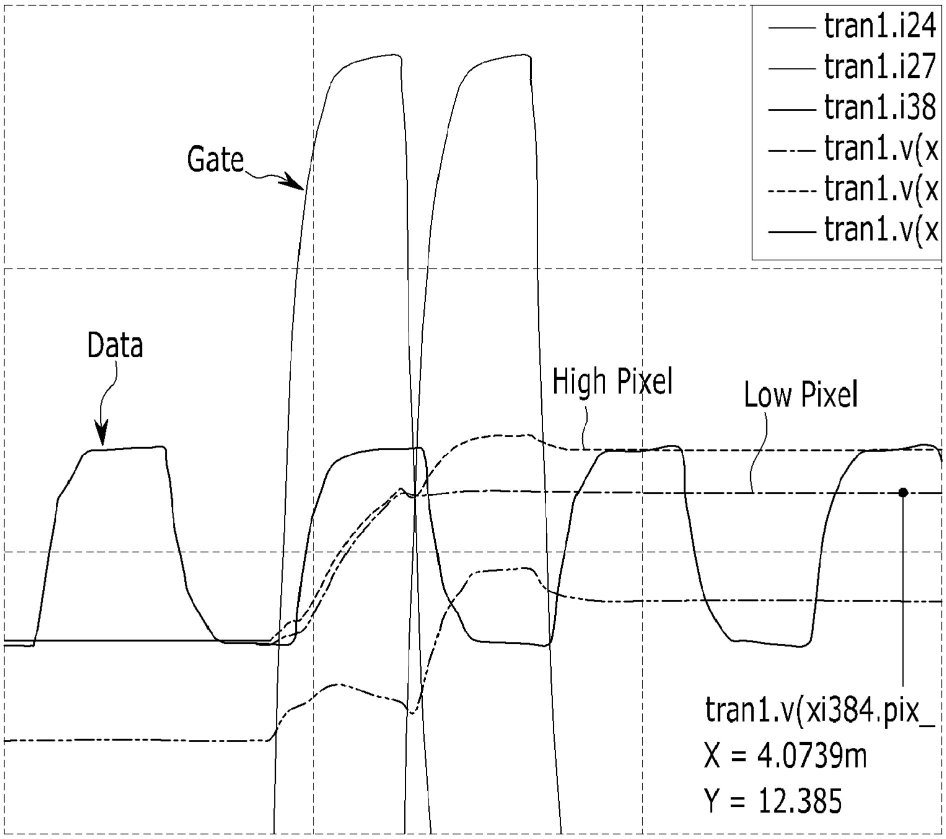
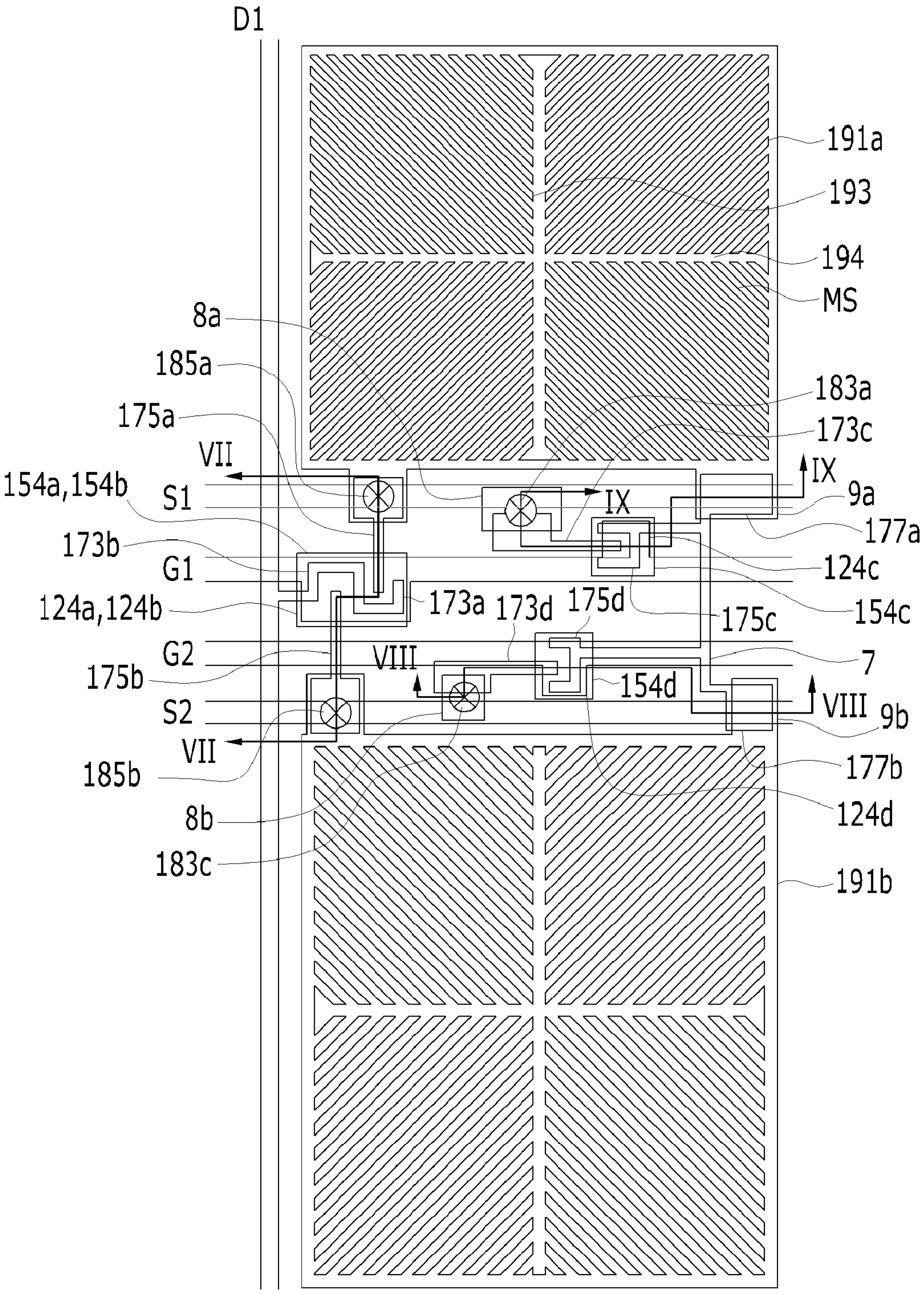

tran1.i24
tran1.i27
tran1.i38
tran1.v(x
tran1.v(x
tran1.v(x
Gate
Data
High Pixel
Low Pixel
tran1.v(xi384.pix_
X = 4.0739m
Y = 12.385

FIG. 6



D1
191a
193
194
MS
8a
185a
183a
173c
175a
VII
IX
IX
154a,154b
S1
9a
177a
173b
G1
124c
124a,124b
173a
173d
175d
154c
175c
G2
7
VIII
175b
154d
S2
VIII
9b
VII
185b
177b
8b
124d
183c
191b

FIG. 7

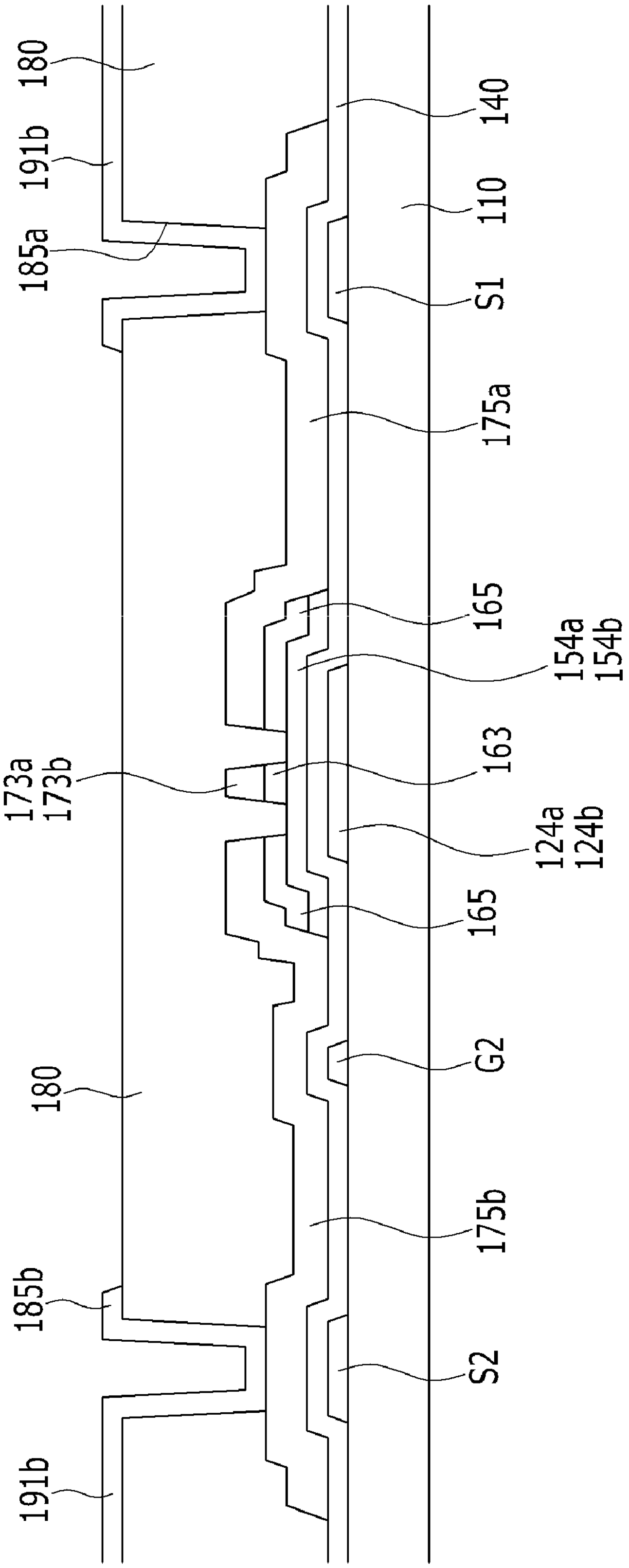

180
191b
185a
140
110
S1
175a
165
154a
154b
163
173a
173b
124a
124b
165
G2
180
175b
185b
S2
191b

FIG. 8

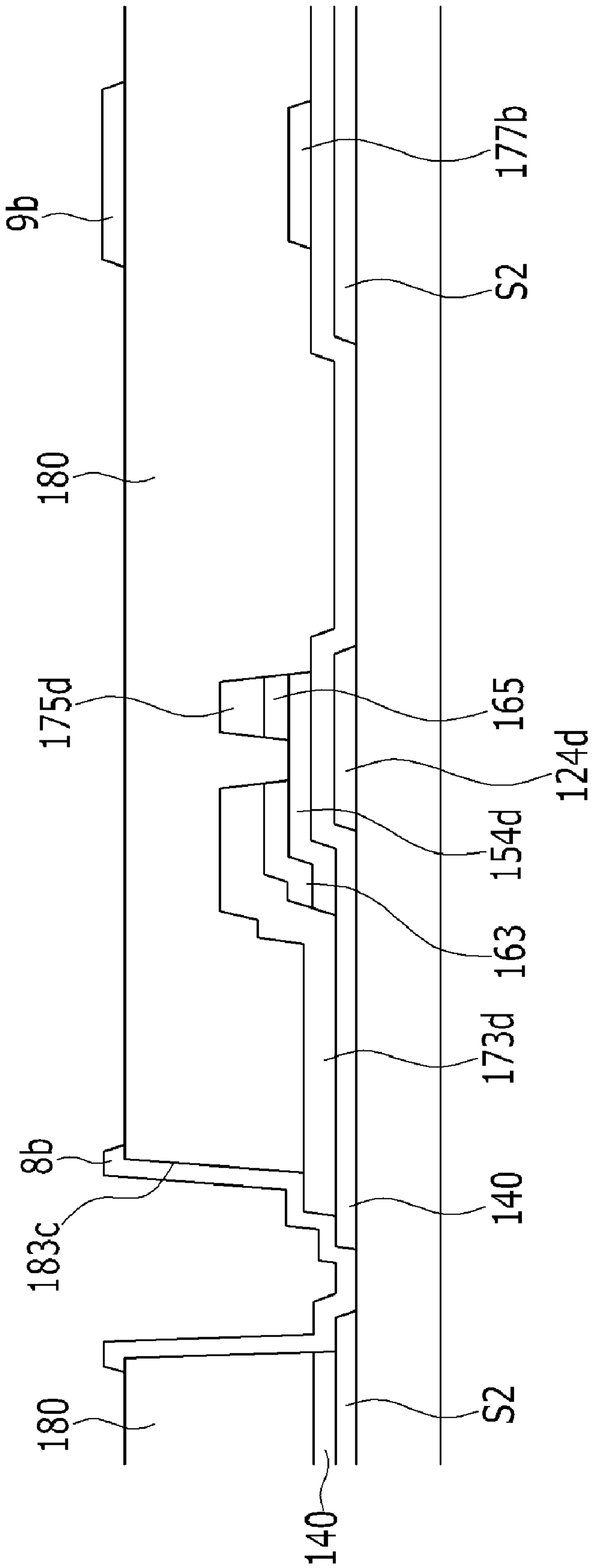

9b
177b
S2
180
175d
165
124d
154d
163
173d
8b
183c
140
180
S2
140

FIG. 9

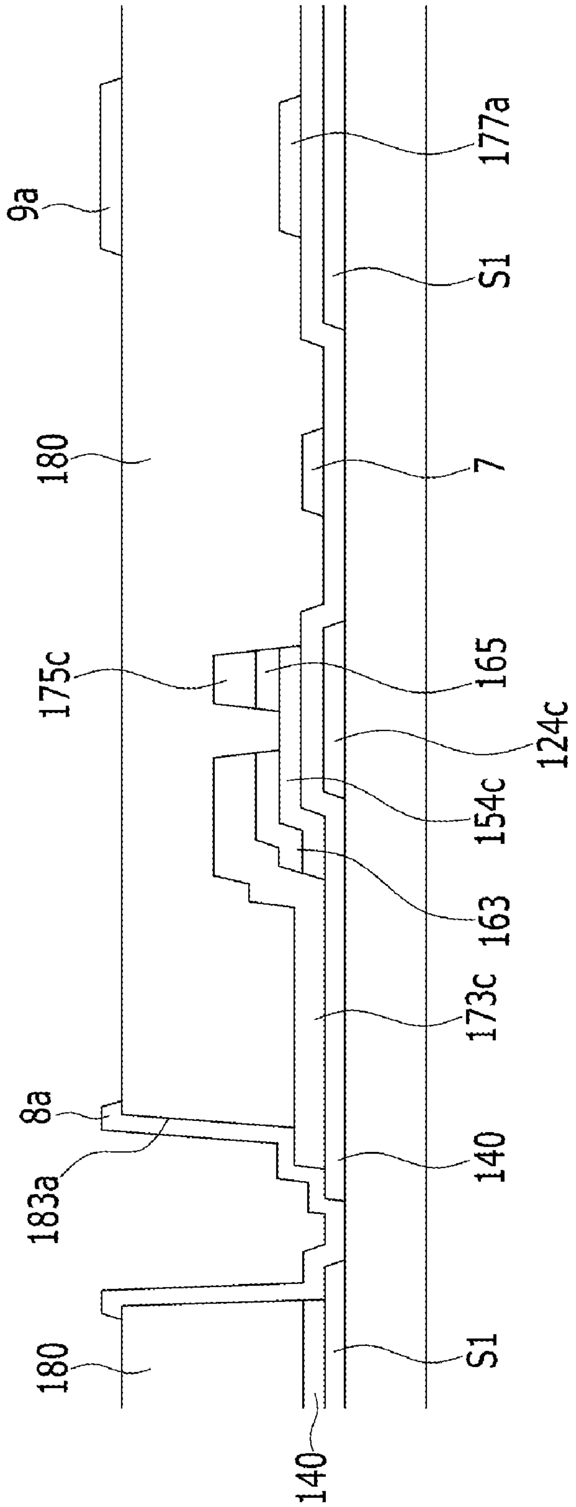
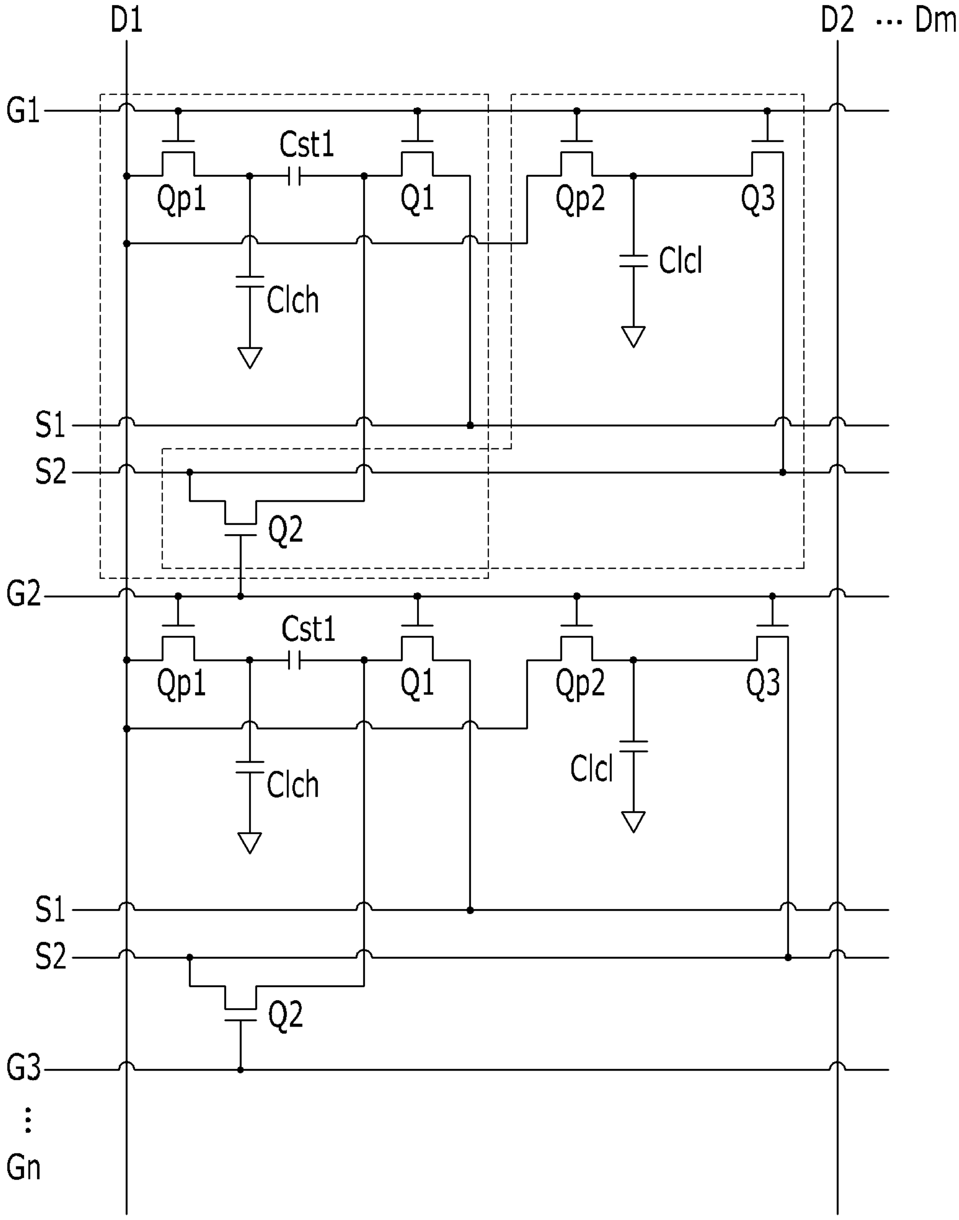

9a
177a
S1
180
7
175c
165
124c
154c
163
173c
8a
183a
140
180
S1
140

FIG. 10



D1
D2 ··· Dm
G1
Cst1
Qp1
Q1
Qp2
Q3
Clch
Clcl
S1
S2
Q2
G2
Cst1
Qp1
Q1
Qp2
Q3
Clch
Clcl
S1
S2
Q2
G3
⋮
Gn

FIG. 11

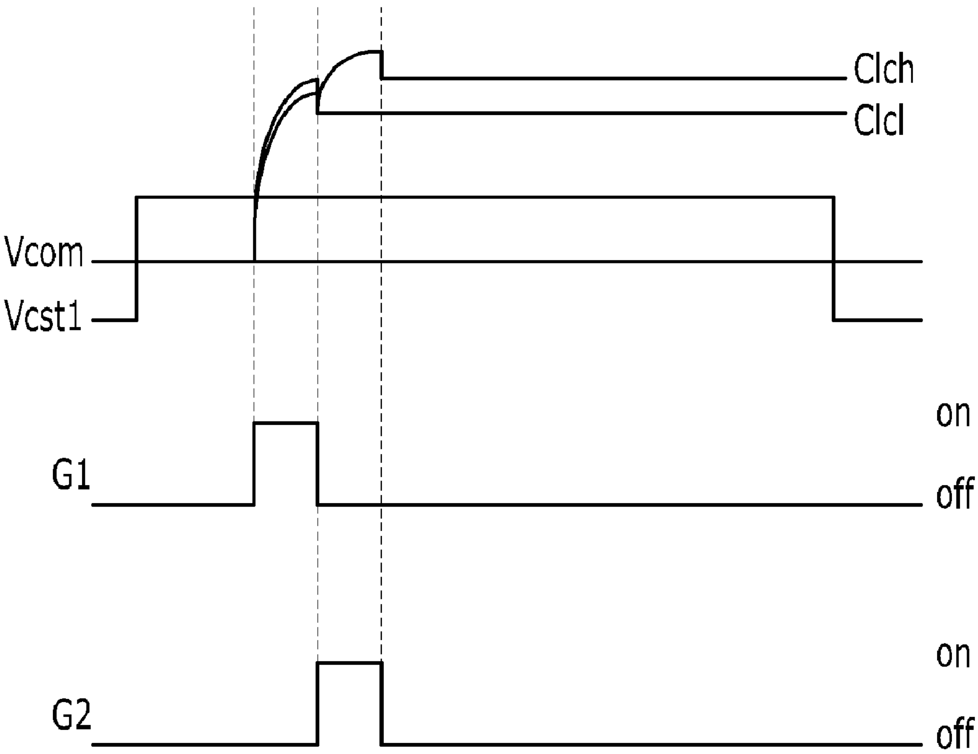


FIG. 12

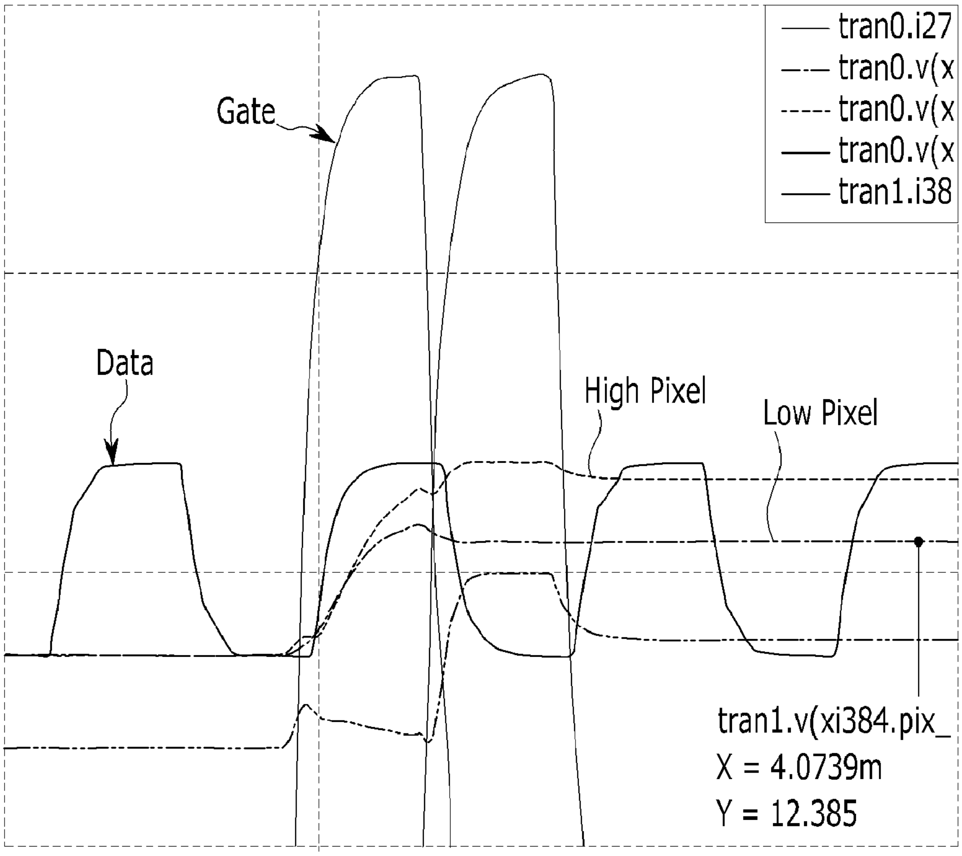

tran0.i27
tran0.v(x
tran0.v(x
tran0.v(x
tran1.i38
Gate
Data
High Pixel
Low Pixel
tran1.v(xi384.pix_
X = 4.0739m
Y = 12.385

FIG. 13

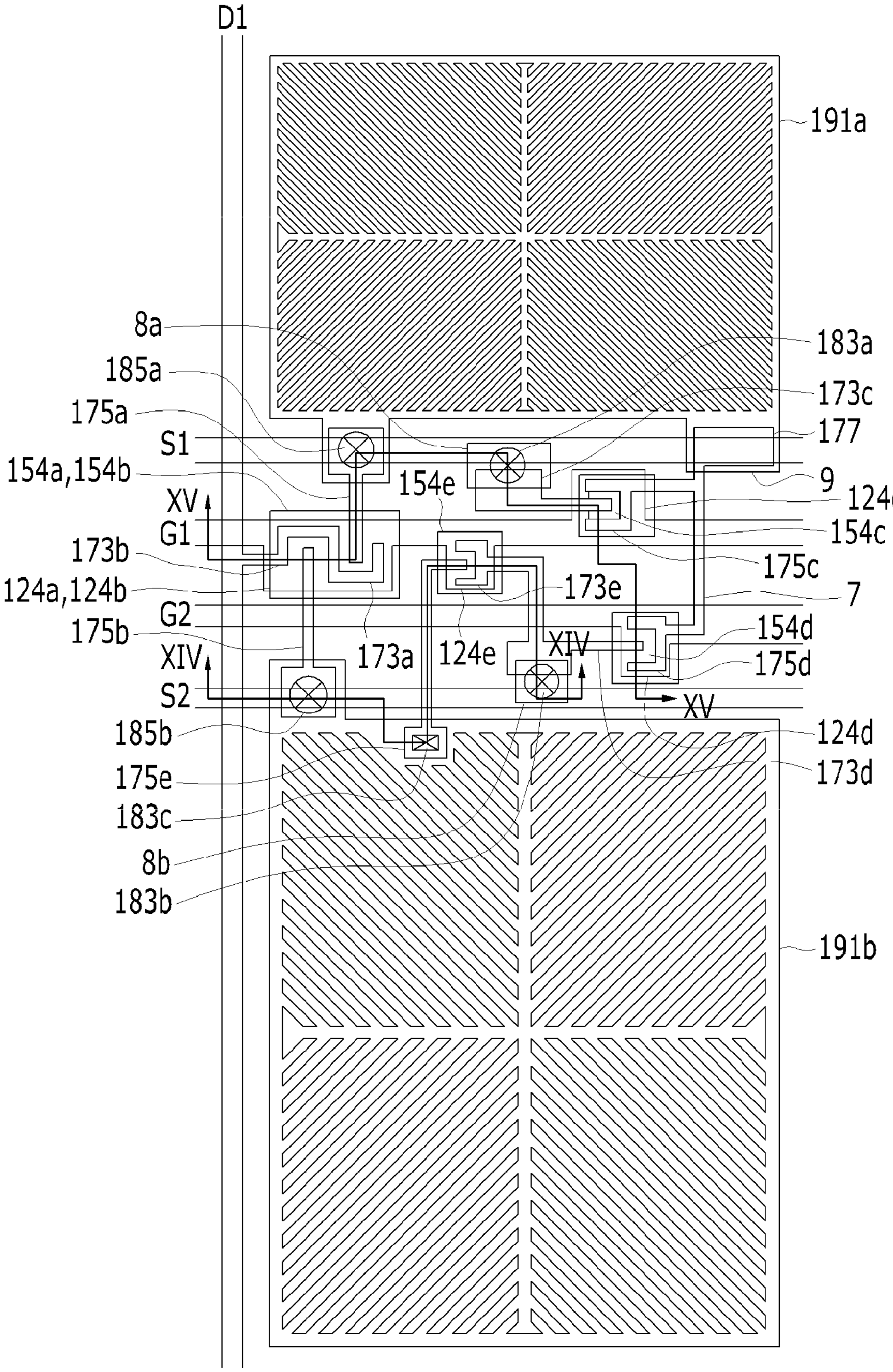
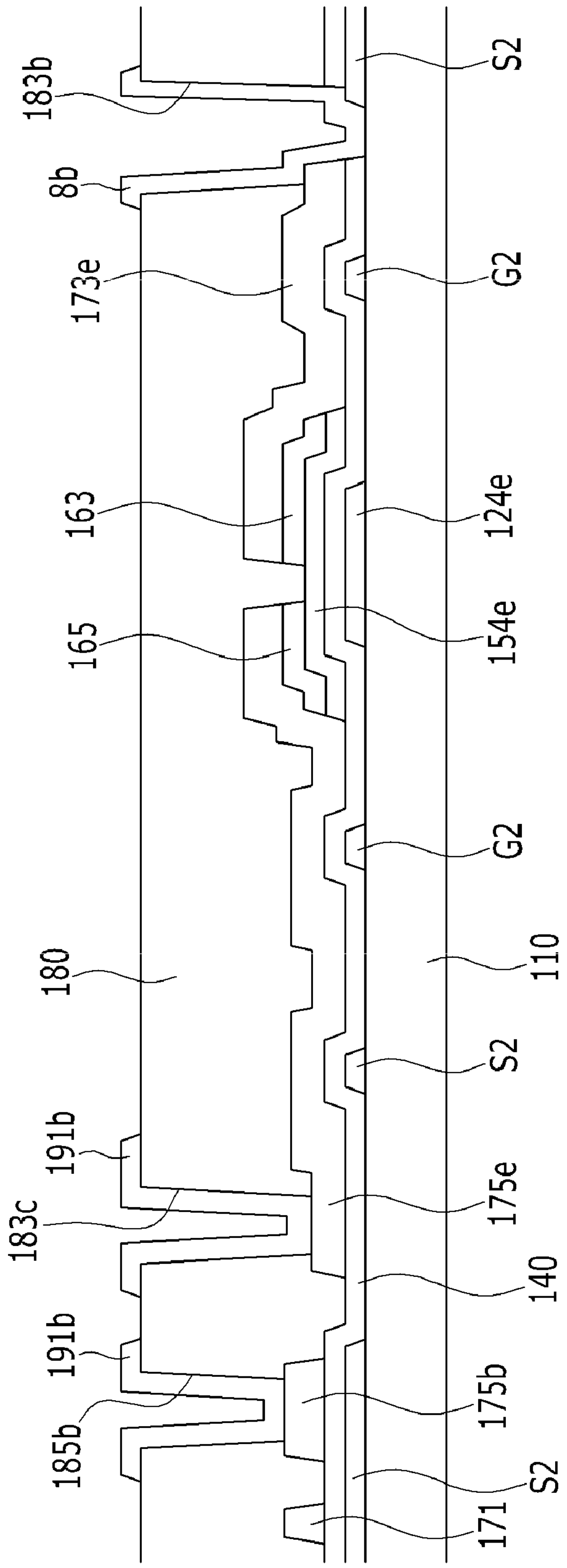
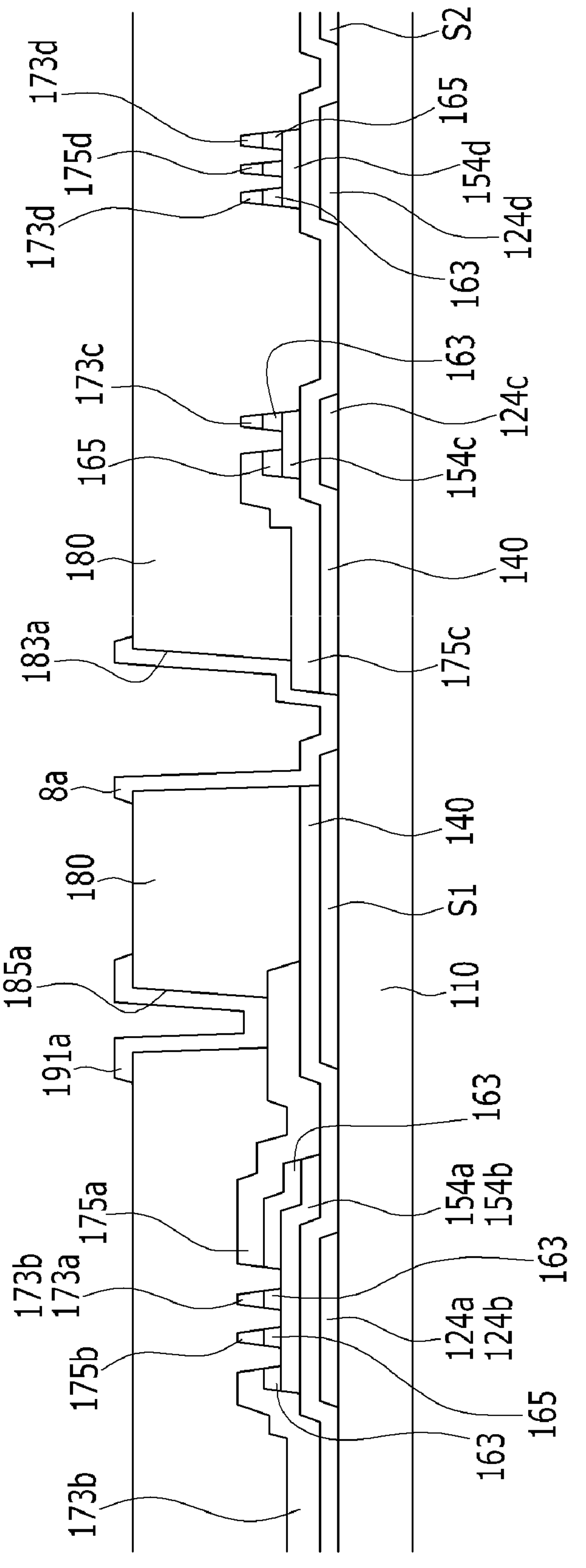

D1
191a
8a
183a
185a
173c
175a
177
S1
9
154a,154b
154e
124c
XV
154c
G1
175c
173b
173e
7
124a,124b
G2
154d
175b
173a
124e
XIV
175d
XIV
S2
XV
185b
124d
175e
173d
183c
8b
183b
191b

FIG. 14



183b
8b
173e
163
165
180
191b
183c
191b
185b
S2
G2
124e
154e
G2
110
S2
175e
140
175b
S2
171

FIG. 15



173d
175d
173d
165
154d
124d
163
S2
163
173c
124c
165
154c
180
140
183a
175c
8a
140
180
S1
185a
110
191a
163
175a
154a
154b
173b
173a
163
124a
124b
175b
165
163
173b

LIQUID CRYSTAL DISPLAY

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2011-0038517 filed on Apr. 25, 2011, which is hereby incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] Exemplary embodiments of the present invention relates to a liquid crystal display.

[0004] 2. Description of the Background

[0005] A liquid crystal display (LCD) has been adopted as one of the most widely used flat panel displays (FPD) applicable to various electronics devices.

[0006] Typically, the liquid crystal display includes switching elements each connected to pixel electrodes, and a plurality of signal lines such as data lines and gate lines are configured to apply voltages to the pixel electrodes by controlling the switching elements.

[0007] The liquid crystal display receives an input image signal from an external graphics controller, the input image signal contains luminance information of each pixel PX, and the luminance has grays of a given quantity. Each pixel is applied with the data voltage corresponding to the desired luminance information. The data voltage applied to the pixel appears as a pixel voltage according to a difference with reference to the common voltage, and each pixel displays the luminance representing a gray of the image signal according to the pixel voltage. Here, the range of the pixel voltage that is applicable to the liquid crystal display is determined according to a driver.

[0008] However, a conventional approach may have a cost problem as the driver of the liquid crystal display requires to be mounted on the display panel in a form of a plurality of IC chips or a flexible circuit film that increase a manufacturing cost of the liquid crystal display. Particularly, as the number of data lines applying the data voltage increases, the cost of the driver of the liquid crystal display is increased.

[0009] Thus, there is a need for an approach to provide a liquid crystal display capable of providing enhanced side visibility yet reducing cost of a driver of the liquid crystal display.

[0010] The above information disclosed in this Background section is merely to address problems of conventional approaches in light of understanding of the background of the invention.

SUMMARY OF THE INVENTION

[0011] Exemplary embodiments of the present invention provides a liquid crystal display capable of improving side visibility of a liquid crystal display and reducing the cost of a driver of the liquid crystal display by reducing a number of data lines, and improving a driving method.

[0012] Additional features of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention.

[0013] Exemplary embodiments of the present invention disclose a display. The display includes a substrate. The display also includes a gate line including a first gate line and a second gate line, and a data line that are formed on the substrate. The display includes a plurality of pixels comprising a first subpixel and a second subpixel connected to the first gate line and the data line. The first subpixel includes a first subpixel electrode and the second subpixel includes a second subpixel electrode. The display includes a switching element including a first switching element and a second switching element. The first switching element is connected to the first gate line and to control a voltage of a first capacitor which is connected to the first subpixel electrode of the first subpixel. And, the second switching element is connected to the second gate line and to control the voltage of the first capacitor.

[0014] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0016] FIG. **1** is a block diagram of a liquid crystal display according to exemplary embodiments of the present invention.

[0017] FIG. **2** is a circuit diagram showing a structure of a liquid crystal display and one pixel according to exemplary embodiments of the present invention.

[0018] FIG. **3** is a circuit diagram of a liquid crystal display according to exemplary embodiments of the present invention.

[0019] FIG. **4** is a diagram explaining a voltage variation associated with timing of a gate signal applied to the driving circuit of FIG. **3**.

[0020] FIG. **5** is a graph showing exemplary simulations of driving of a liquid crystal display including the driving circuit of FIG. **4**.

[0021] FIG. **6** is a layout view of a pixel of a thin film transistor array panel including the driving circuit of FIG. **3**.

[0022] FIG. **7** is a cross-sectional view taken along the line VII-VII of FIG. **6**.

[0023] FIG. **8** is a cross-sectional view taken along the line VIII-VIII of FIG. **6**.

[0024] FIG. **9** is a cross-sectional view taken along the line IX-IX of FIG. **6**.

[0025] FIG. **10** is a circuit diagram of a driving circuit of a liquid crystal display according to exemplary embodiments of the present invention.

[0026] FIG. **11** is a diagram explaining a voltage variation of timing of a gate signal applied to the driving circuit of FIG. **10**.

[0027] FIG. **12** is a graph showing simulations of driving of a liquid crystal display including the driving circuit of FIG. **10**.

[0028] FIG. **13** is a layout view of a pixel of a thin film transistor array panel including the driving circuit of FIG. **10**.

[0029] FIG. **14** is a cross-sectional view taken along the line XIV-XIV of FIG. **13**.

[0030] FIG. 15 is a cross-sectional view taken along the line XV-XV of FIG. 13.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0031] The invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure is thorough, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the size and relative sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements.

[0032] In the drawings, the thickness of layers, films, panels, and regions may be exaggerated for clarity illustrations. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate can be referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there may be no intervening elements present.

[0033] A liquid crystal display according to exemplary embodiments of the present invention will be described with reference to FIG. 1 and FIG. 2.

[0034] FIG. 1 is a block diagram of a liquid crystal display according to exemplary embodiments of the present invention, and FIG. 2 is a circuit diagram showing a structure of a liquid crystal display and one pixel according to exemplary embodiments of the present invention.

[0035] As shown in FIG. 1, a liquid crystal display according to exemplary embodiments of the present invention may include a liquid crystal panel assembly **300**, a gate driver **400**, and a data driver **500**.

[0036] In a circuit, the liquid crystal panel assembly **300** may include a plurality of signal lines G1-Gn and D1-Dm, and a plurality of pixels PX that are connected to the signal lines and are arranged in an approximate matrix. Meanwhile, referring to the structure shown in FIG. 2, the liquid crystal panel assembly **300** may include lower and upper display panels **100** and **200** that face each other, and a liquid crystal layer **3** interposed therebetween.

[0037] For example, the signal lines G1-Gn and D1-Dm are provided on the lower panel **100**, and include a plurality of gate lines G1-Gn that transmit gate signals (also referred to as "scanning signals"), and a plurality of data lines D1-Dm that transmit data signals. The gate lines G1-Gn substantially extend in a row direction and parallel to each other, and the data lines D1-Dm substantially extend in a column direction and parallel to each other.

[0038] Each pixel PX, for example the pixel PX connected to the i-th (i=1, 2, . . . , n) gate line G1) and the j-th (j=1, 2, . . . , m) data line Dj) includes a pair of subpixels, and each subpixel includes first and second liquid crystal capacitors Clch and Clcl. Two subpixels further include a switching element (not shown) connected to the gate lines G1-Gn, the data lines D1-Dm, and the liquid crystal capacitors Clch and Clcl.

[0039] For example, the first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl include first subpixel electrode **191***h* and second subpixel electrode **191***l* of the lower panel **100** and a common electrode **270** of the upper panel **200** as two terminals. The liquid crystal layer **3** between the two terminals serves as a dielectric material

[0040] The pair of subpixel electrodes **191***h* and **191***l* are separated from each other and form one pixel electrode **191**. The common electrode **270** is formed on the whole surface of the upper panel **200** and is applied with the common voltage Vcom. The liquid crystal layer **3** has negative dielectric anisotropy, and liquid crystal molecules of the liquid crystal layer **3** may be aligned such that their major axes are perpendicular to the surfaces of the two display panels when an electric field is not applied. Differently from FIG. 2, for example, the common electrode **270** may be formed on the lower panel **100**, and at least one of the two electrodes **191** and **270** may have a linear shape or a bar shape.

[0041] Meanwhile, for color display, each pixel PX uniquely displays one of three primary colors (spatial division) or each pixel PX alternately displays the three primary colors (temporal division) as time passes, and a desired color is recognized by a spatial or temporal sum of the primary colors. For example, the primary colors can be three primary colors of red, green, and blue. FIG. 2 shows a color filter **230** displaying one of primary colors on a region of the upper panel **200** by each of the pixels as an example of spatial division. Unlike the case of FIG. 2, the color filter **230** may be provided on or under the subpixel electrodes **191***h* and **191***l* of the lower panel **100**.

[0042] Polarizers (not shown) may be provided on the outer surface of the display panels **100** and **200**, and polarization axis of the two polarizers may be crossed.

[0043] Referring again to FIG. 1, for example, the data driver **500** is connected to the data lines D1-Dm of the liquid crystal panel assembly **300**, and applies the data voltage to the data lines D1-Dm.

[0044] The gate driver **400** is connected to the gate lines G1 to Gn of the liquid crystal panel assembly **300**, and applies gate signals obtained by combining a gate-on voltage Von for turning on a switching element and a gate-off voltage Voff for turning off the switching element to the gate lines G1 to Gn.

[0045] Next, a driving method of a liquid crystal display will be described with reference to a circuit according to exemplary embodiments of the present invention including this pixel.

[0046] FIG. 3 is a circuit diagram of a liquid crystal display according to exemplary embodiments of the present invention, and FIG. 4 is a view to explain a voltage variation of timing of a gate signal applied to the driving circuit of FIG. 3.

[0047] Referring to FIG. 3, for example, the liquid crystal display includes a plurality of first signal lines G1-Gn and second signal lines D1-Dm intersecting each other, and third signal lines S1 and S2. The first signal lines G1-Gn (hereafter referred to as "gate lines") transmit the gate signal (hereafter referred to as "scanning signal"), the second signal lines D1-Dm (hereafter referred to as "data lines") transmit the data voltage (hereafter referred to as "image signal"), and the third signal lines S1 and S2 include the first voltage line S1 and the second voltage line S2 transmitting a predetermined voltage.

[0048] The pixel PX includes a first pixel switching element Qp1, a second pixel switching element Qp2 connected to the first gate line and the data line, and a first liquid crystal capacitor Clch and a second liquid crystal capacitor Clcl respectively connected thereto.

[0049] The first pixel switching element Qp1 and the second pixel switching element Qp2 are three-terminal elements of a thin film transistor, and the first pixel switching element Qp1 includes the control terminal connected to the first gate line G1, the input terminal connected to the data line D1, and the output terminal connected to the first liquid crystal capacitor Clch. Also, the second pixel switching element Qp2 includes the control terminal connected to the first gate line G1, the input terminal connected to the data line D1, and the output terminal connected to the second liquid crystal capacitor Clcl.

[0050] The pixel PX includes a first capacitor Cst1 connected to the first liquid crystal capacitor Clch and a second capacitor Cst2 connected to the second liquid crystal capacitor Clcl. The first capacitor Cst1 is connected to the first switching element Q1 and the second switching element Q2 to control a voltage Vcst1 of the first capacitor Cst1, and the second capacitor Cst2 is connected to the second switching element Q2.

[0051] In the first switching element Q1 and the second switching element Q2 as three-terminal elements such as thin film transistors, the first switching element Q1 includes the control terminal connected to the first gate line G1 and the input terminal connected to the first voltage line S1. Also, the second switching element Q2 includes the control terminal connected to the second gate line G2, the input terminal connected to the second voltage line S2, and the output voltage connected to the first capacitor Cst1 and the second capacitor Cst2.

[0052] Referring to FIG. 3 and FIG. 4, for example, if the first gate line G1 is applied with the gate on voltage, the data voltage is respectively applied to the first pixel electrode and the second pixel electrode through the turned on first pixel switching element Qp1 and second pixel switching element Qp2. The first pixel switching element Qp1 and the second pixel switching element Qp2 are connected to the same data line D1, thereby receiving the same data voltage. The data voltage is a voltage corresponding to luminance for display by the first pixel and the second pixel, and the difference between a reference voltage Vcom and the data voltages transmitted to the first pixel electrode and the second pixel electrode becomes the charge voltage of the first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl. Also, the electric field value of the first subpixel PX1 and the second subpixel PX2 is determined according to the charge voltage of the first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl. In exemplary embodiments of the present invention, the input terminals of the first pixel switching element Qp1 and the second pixel switching element Qp2 are applied with the same data voltage during turn-on of the first gate line G1 such that the charge voltage of the first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl are equal to each other.

[0053] Also, the first capacitor Cst1 is charged by the first voltage Vcst1 flowing to the first voltage line S1 through the turned-on first switching element Q1 during of the on state of the first gate line G1.

[0054] Next, when the second gate line G2 of the next gate line is in the on state, the first pixel switching element Qp1 and the second pixel switching element Qp2 are in the off state such that the first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl of the first subpixel PX1 and the second subpixel PX2 are no longer charged.

[0055] Also, the second voltage Vcst2 flowing to the second voltage line S2 is transmitted to the first capacitor Cst1 and the second capacitor Cst2 through the turned-on second switching element Q2. The voltage of the first capacitor Cst1 and the second capacitor Cst2 is increased by a difference between the first voltage Vcst1 and the second voltage Vcst2 such that the voltage of the first liquid crystal capacitor Clch connected to the first capacitor Cst1 and the voltage of the second liquid crystal capacitor Clcl connected to the second capacitor Cst2 are increased. Accordingly, although the on signal of the gate line is not long, the pixel voltage may be sufficiently obtained. Here, the first voltage Vcst1 applied to the first voltage line S1 and the second voltage Vcst2 of the second voltage line Vcst2 have inverted polarities with respect to the common voltage Vcom.

[0056] This will be described with reference to FIG. 5.

[0057] FIG. 5 is a graph showing exemplary simulations of driving of a liquid crystal display including the driving circuit of FIG. 3. Here, Cst1 is about 0.063 pF, Csth is about 0.059 pF, Clcl is about 0.796 pF, and Clch is about 0.359 pF such that Cst1/Clcl of about 0.08 and Csth/Clch of about 0.16 are input.

[0058] As shown in FIG. 5, it is illustrated that the voltage of the first subpixel and the second subpixel is increased (a red colored line) during the period that the first gate line G1 represented by a yellow colored line is in the on state, however the first subpixel and the second subpixel are not charged to the desired data voltage such as to a green colored line. The first subpixel and the second subpixel are charged with the same value.

[0059] Next, it is illustrated that the voltage of the first subpixel is increased to the desired data voltage if the second gate line G2 is in the on state. Also, the voltage of the second subpixel is also increased, however it is increased with a lesser value than the voltage of the first subpixel, as described above. Here, the ratio of the voltage of the second subpixel to the voltage of the first subpixel is about 0.893, and the charging ratio of the first liquid crystal capacitor Clch is about 101.5% of the data voltage, thereby obtaining the desired data voltage.

[0060] In the conventional art, the on period of the first gate line G1 is short such that the liquid crystal capacitor is charged during a period of two times the period in which the first gate line G1 of the present invention is turned on by applying the gate-on signal to two row pixels to obtain the luminance required in the first subpixel. As described above, although the liquid crystal capacitor is charged during the period of two times, the charging ratio is less than the present invention as about 95.27% of the data voltage.

[0061] Also, like the conventional art, if the charging time of the pixel is increased by using the gate lines of two rows, different data lines must be connected for the row to transmit the different data voltages, and thereby the number of the data line is increased.

[0062] However, in exemplary embodiments of the present invention, the desired luminance may be obtained by using the second switching element Q2 and the voltage line even though the same data line is used by two neighboring data lines such that the number of data lines may be reduced.

[0063] Meanwhile, in FIG. 3, when the voltage at the position N1 is referred to as Vh1, the voltage at the position N2 is referred to as Vh2, the voltage at the position N3 is referred to as V11, and the voltage at the position N4 is referred to as V12, the voltage of Vh1 may be obtained by Equation 1.

$$CVh2=Clch*Vh1$$

$$Vh1=C/Clch*Vh2$$

$$Vh1=Cst1/Cst1+Clch*Vh2$$

$$Vh1=1/(1+Clch/Cst1*Vh2=1/(1+1/Cst1/Clch*Vh2 \quad \text{Equation 1}$$

[0064] Accordingly, when the first gate line G1 becomes off and the second gate line G2 becomes on, the increased voltage of Vh1 may be obtained by Equation 2.

$$\Delta Vh1=1/(1+Clch/Cst1*Vh2=1/(1+1/Cst1/Clch*\Delta Vh2 \quad \text{[Equation 2]}$$

[0065] The voltage of N3 and N4 is obtained as in the following Equation 3.

$$\Delta V11=1/(1+Clcl/Cst2)*V12=1/(1+1/Cst2/Clc2)*\Delta V12 \quad \text{[Equation 3]}$$

[0066] Referring to Equation 1, Equation 2 and Equation 3, ΔVh1 and ΔV11 may be changed by the value of Cst1 and Cst2. Accordingly, in the exemplary embodiments of the present invention, ΔVh1/ΔV11>1 may be obtained by controlling an electrode area of the first capacitor and the second capacitor.

[0067] In this example, if the voltages of the first liquid crystal capacitor and the second liquid crystal capacitor according to ΔVh1 and ΔV11 are different, the luminance of the first pixel and the second pixel are also different. Accordingly, the side visibility of the liquid crystal display may be improved by controlling the charge capacitances of the first capacitor and the second capacitor. FIG. **6** is a layout view of a pixel of a thin film transistor array panel including the driving circuit of FIG. **3**, FIG. **7** is a cross-sectional view taken along the line V11-V11 of FIG. **6**, FIG. **8** is a cross-sectional view taken along the line VIII-V111 of FIG. **6**, and FIG. **9** is a cross-sectional view taken along the line IX-IX of FIG. **6**.

[0068] Referring to FIG. **6**, FIG. **7**, FIG. **8** and FIG. **9**, for example, a gate conductor including the first gate line G1, the second gate line G2, the first voltage line S1, and the second voltage line S2 is formed on an insulation substrate **110** made of transparent glass or plastic.

[0069] The first gate line G1 has a first gate electrode **124***a*, a second gate electrode **124***b*, and a third gate electrode **124***c* protruding from the first gate line G1 up or down, and the second gate line G2 has a fourth gate electrode **124***d*. The first gate line G1 and the second gate line G2 have an end portion (not shown) having a wide area for connection to other layers or an external driving circuit. The first gate electrode **124***a* and the second gate electrode **124***b* may be connected.

[0070] The first voltage line S1 and the second voltage line S2 extend in the same direction as the first gate line G1 and the second gate line G2, and the first gate line G1 and the second gate line G2 are positioned between the first voltage line S1 and the second voltage line S2.

[0071] As an example, a gate insulating layer **140** is formed on the gate conductor.

[0072] A first semiconductor **154***a*, a second semiconductor **154***b*, a third semiconductor **154***c*, and a fourth semiconductor **154***d* that may be made of amorphous silicon or crystalline silicon are positioned on the gate insulating layer **140**.

[0073] The first semiconductor **154***a*, the second semiconductor **154***b*, the third semiconductor **154***c*, and the fourth semiconductor **154***d* respectively overlap the first gate electrode **124***a*, the second gate electrode **124***b*, the third gate electrode **124***c*, and the fourth gate electrode **124***d*. The first semiconductor **154***a* and the second semiconductor **154***b* may be connected.

[0074] Ohmic contacts **163** and **165** are respectively formed in pairs on the first semiconductor **154***a*, the second semiconductor **154***b*, the third semiconductor **154***c*, and the fourth semiconductor **154***d*.

[0075] The ohmic contacts **163** and **165** may be made of a material such as n+ hydrogenated amorphous silicon in which an n-type impurity such as phosphorus is doped at a high concentration, or of silicide.

[0076] A data conductor including a data line D1, a third source electrode **173***c*, a fourth source electrode **173***d*, a first drain electrode **175***a* to a fourth drain electrode **175***d*, a first metal pattern **177***a*, a second metal pattern **177***b*, and a metal pattern connection **7** is formed on the ohmic contacts **163** and **165** and the gate insulating layer **140**.

[0077] The data line D1 transmits the data signal and extends mainly in a longitudinal direction, thereby intersecting the gate lines G1 and G2. The data line D1 has a second source electrode **173***b* extending toward the first gate electrode **124***a* and the second gate electrode **124***b* and a first source electrode **173***a* connected to the second source electrode **173***b*. The third source electrode **173***c* and the fourth source electrode **173***d* respectively overlap the third semiconductor **154***c* and the fourth semiconductor **154***d*. For example, the first source electrode **173***a*, the second source electrode **173***b*, the third source electrode **173***c* and the fourth source electrode **173***d* are curved with a ∩ shape, a ∪ shape, a ⊂ shape, or a ⊃ shape.

[0078] The first drain electrode **175***a*, the second source electrode **173***b*, the third source electrode **173***c* and the fourth drain electrode **175***d* include a bar portion extending in an upper, a lower, a right, or a left direction, and an expansion being wider than the bar portion and positioned at one end of the bar portion. The bar portions are respectively enclosed by the first source electrode **173***a*, the second source electrode **173***b*, the third source electrode **173***c* and the fourth source electrode **173***d*.

[0079] The first metal pattern **177***a* overlaps the first voltage line S1, and the second metal pattern **177***b* overlaps the second voltage line S2. The first metal pattern **177***a* and the second metal pattern **177***b* are connected by the metal pattern connection **7**. The third drain electrode **175***c* and the fourth drain electrode **175***d* are connected to the metal pattern connection **7**.

[0080] The first gate electrode **124***a*, the first semiconductor **154***a*, the first source electrode **173***a*, and the first drain electrode **175***a* form the first pixel switching element Qp1, the channel of the first pixel switching element Qp1 is formed in the first semiconductor **154***a* between the first source electrode **173***a* and the first drain electrode **175***a*, the second gate electrode **124***b*, the second semiconductor **154***b*, the second source electrode **173***b*, and the second drain electrode **175***b* form the second pixel switching element Qp2, and the channel of the second pixel switching element Qp2 is formed in the second semiconductor **154***b* between the second source electrode **173***b* and the second drain electrode **175***b*.

[0081] Also, the third gate electrode **124***c*, the third semiconductor **154***c*, the third source electrode **173***c*, and the third drain electrode **175***c* form the first switching element Q1, the channel of the first switching element Q1 is formed in the third semiconductor **154***c* between the third source electrode **173***c* and the third drain electrode **175***c*, the fourth gate electrode **124***d*, the fourth semiconductor **154***d*, the fourth source electrode **173***d*, and the fourth drain electrode **175***d* form the second switching element Q**2**, and the channel of the second switching element Q**2** is formed in the fourth semiconductor **154***d* between the fourth source electrode **173***d* and the fourth drain electrode **175***d*.

[0082] For example, a passivation layer **180** made of an organic insulator is formed on the data conductor.

[0083] In this example, the passivation layer **180** has a first contact hole **185***a* exposing the first drain electrode **175***a*, a second contact hole **185***b* exposing the second drain electrode **175***b*, a third contact hole **183***a* exposing the third drain electrode **175***c* and the first voltage line S**1**, and a fourth contact hole **183***b* exposing the fourth drain electrode **175***d* and the second voltage line S**2**.

[0084] The third contact hole **183***a* simultaneously exposes the third drain electrode **175***c* and the first voltage line S**1**, however it may be formed to separately expose the third drain electrode **175***c* and the first voltage line S**1** (not shown). The fourth contact hole **183***b* may be divided like the third contact hole **183***a*.

[0085] A plurality of first pixel electrodes **191***a* and second pixel electrodes **191***b* and connecting members **8***a* and **8***b* that may be made a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO) or a reflective metal such as aluminum, silver, chromium, or alloys thereof are formed on the passivation layer **180**.

[0086] For example, the first pixel electrode **191***a* is connected to the first drain electrode **175***a* through the first contact hole **185***a*, thereby receiving the data signal from the first drain electrode **175***a*. Also, the second pixel electrode **191***b* is connected to the second drain electrode **175***b* through the second contact hole **185***b*, thereby receiving the data signal from the second drain electrode **175***b*.

[0087] The first pixel electrode **191***a* and the second pixel electrode **191***b* are formed in an approximate quadrangle and are positioned at the other side with respect to the first voltage line S**1** and the second voltage line S**2**, and the area of the second pixel electrode **191***b* may be about two times the area of the first pixel electrode **191***a*. The first pixel electrode and the second pixel electrode have different areas such that the charge capacitances of the first liquid crystal capacitor and the second liquid crystal capacitor are different, thereby obtaining the different luminances. Accordingly, the side visibility of the liquid crystal display may be improved by appropriately controlling the areas of the first pixel electrode and the second pixel electrode along with the charge capacitance of the first capacitor and the second capacitor.

[0088] The first pixel electrode **191***a* and the second pixel electrode **191***b* respectively include a plurality of minute slits MS. The first pixel electrode **191***a* and the second pixel electrode **191***b* respectively include a cross-shaped stem that is formed of a transverse stem **193** and a vertical stem **194** that is perpendicular thereto. They are respectively divided into four subregions by the transverse stem **193** and the longitudinal stem **194**, and each region includes a plurality of minute slits MS.

[0089] The minute slits MS obliquely extend from the transverse stem **193** and the longitudinal stem **194**, and the minute slit MS in each subregion extend in the same direction. The width of the minute slit MS is in the range of about 2.5 μm to about 5.0 μm, and the interval between two neighboring minute slits MS is in the range of about 2.5 μm to about 5.0 μm.

[0090] Meanwhile, the first pixel electrode **191***a* has a protrusion **9***a* overlapping the first metal pattern **177***a*, and the second pixel electrode **191***b* has a protrusion **9***b* overlapping the second metal pattern **177***b*.

[0091] In this example, if the minute slit is formed, the edges of the minute slits distort the electric field thereby making the horizontal component perpendicular to the edges of the minute slits and an inclination direction of liquid crystal molecules (not shown) is determined in the direction determined by the horizontal component. For example, the liquid crystal molecules initially tend to incline in the direction perpendicular to the edge of the minute slits. However, the directions of the horizontal components of the electric field by the edge of the neighboring minute slits are opposite, and the interval between the minute slits is very narrow such that the liquid crystal molecules that tend to incline in the opposite direction to each other are tilted in the direction parallel to the length direction of the minute slits.

[0092] Here, in exemplary embodiments of the present invention, the length direction in which the minute slits of one pixel extend is four directions such that the inclined directions of the liquid crystal molecules are four directions. Therefore, the viewing angle of the liquid crystal display is widened by varying the inclined directions of the liquid crystal molecules.

[0093] FIG. **10** is a circuit diagram of a driving circuit of a liquid crystal display according to exemplary embodiments of the present invention, and FIG. **11** is a view to explain a voltage variation of timing of a gate signal applied to the driving circuit of FIG. **10**.

[0094] Referring to FIG. **10** and FIG. **11**, a driving method of a liquid crystal display according to exemplary embodiments of the present invention will be described.

[0095] Firstly, referring to FIG. **10** and FIG. **11**, if the first gate line G**1** is applied with the gate-on voltage, the data voltage is applied to the first pixel electrode and the second pixel electrode through the turned on first pixel switching element Qp**1** and second pixel switching element Qp**2**. Also, the first voltage flowing through the first voltage line S**1** is applied to the first capacitor Cst**1** through the turned on first switching element Q**1**, and the second voltage flowing through the second voltage line S**2** is applied to the third switching element Q**3** through the turned on second switching element Q**2**.

[0096] The first pixel switching element Qp**1** and the second pixel switching element Qp**2** are transmitted with the same data voltage, however the second pixel electrode is applied with a lower voltage than the first pixel electrode because of the size difference between the first pixel switching element Qp**1** and the second pixel switching element Qp**2**.

[0097] Also, when the second pixel switching element Qp**2** and the third switching element Q**3** are turned on, it may be regarded that the second pixel switching element Qp**2** and the third switching element Q**3** function as a conductor and the second pixel switching element Qp**2** and the third switching element Q**3** are resistors having the different values, and thereby the voltage division is generated between the second pixel switching element and the third switching element Q**3** such that the voltage transmitted to the second pixel electrode through the second pixel switching element Qp**2** is always lower than the voltage transmitted to the first pixel electrode through the first pixel switching element Qp**1**.

[0098] The data voltage of the first subpixel PX**1** and the second subpixel PX**2** and the first voltage applied to the first voltage line S**1** have opposite polarities with respect to the common voltage Vcom, and the polarities of the first voltage and the second voltage are opposite to each other.

[0099] Next, if the second gate line **G2** as the next gate line enters the on state, the first pixel switching element Qp**1** connected to the first gate line G**1** and the second pixel switching element Qp**2** connected to the first gate line G**1** enter the off state such that the first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl of the first subpixel PX**1** and the second subpixel PX**2** are no longer charged. Also, the third switching element Q**3** connected to the first gate line G**1** is in the off state such that the second voltage line S**2** is not connected to the second liquid crystal capacitor Clcl of the second subpixel PX**2** any longer.

[0100] Also, the second voltage Vcst**2** flowing to the second voltage line S**2** through the turned on second switching element Q**2** is transmitted to the first capacitor Cst**1**. The voltage of the first capacitor Cst**1** is increased by the difference between the first voltage and the second voltage such that the voltage of the first liquid crystal capacitor Clch connected to the first capacitor Cst**1** is increased. Accordingly, the pixel voltage of the first subpixel is increased. This is the same as the increasing method of the voltage of the first subpixel PX**1** of the driving circuit of FIG. **3**.

[0101] However, no more voltage is transmitted to the second liquid crystal capacitor Clcl of the second subpixel PX**2** from the second voltage line S**2** such that the pixel voltage of the second subpixel is not increased.

[0102] In the exemplary embodiment of FIG. **3**, the voltages of the first subpixel PX**1** and the second subpixel PX**2** are increased together to increase the entire driving voltage, however in the exemplary embodiment of FIG. **10**, the difference between the driving voltages of the first subpixel PX**1** and the second subpixel PX**2** may be increased.

[0103] FIG. **12** is a graph showing simulations of a liquid crystal display including the driving circuit of FIG. **6**. Here, Cst**1** is 0.063 pF, Csth is 0.059 pF, Clcl is 0.796 pF, and Clch is 0.359 pF such that Cst**1**/Clcl of 0.08 and Csth/Clch of 0.16 are input.

[0104] As shown in FIG. **12**, when the first gate line G**1** indicated by the yellow colored line is on, it may be seen that the voltage of the first pixel is increased (the red colored line), however the voltage is not charged to the desired data voltage (the green colored line).

[0105] However, if the second gate line G**2** is on, it is illustrated that the voltage of the first subpixel PX**1** is increased to the desired data voltage. The voltage of the second subpixel PX**2** is charged less than the voltage of the first subpixel PX**1** by a predetermined magnitude.

[0106] Next, if the second gate line G**2** is on, it is illustrated that the voltage of the first subpixel PX**1** is increased to the desired data voltage. However, the voltage of the second subpixel PX**2** is no longer increased. Accordingly, the voltage difference between the first subpixel PX**1** and the second subpixel PX**2** is increased differently from the exemplary embodiment of FIG. **3** such that the ratio of the pixel voltage of the second subpixel PX**2** for the pixel voltage of the first subpixel PX**1** is about 0.815. Here, it may be known that the voltage charging ratio of the first subpixel PX**1** is about 98.05% that is close to the desired data voltage.

[0107] FIG. **13** is a layout view of a pixel of a thin film transistor array panel including the driving circuit of FIG. **10**, FIG. **14** is a cross-sectional view taken along the line XIV-XIV of FIG. **13**, and FIG. **15** is a cross-sectional view taken along the line XV-XV of FIG. **13**.

[0108] Referring to FIG. **13**, FIG. **14** and FIG. **15**, for example, a gate conductor including a first gate line G**1**, a second gate line G**2**, a first voltage line S**1**, and a second voltage line S**2** is formed on an insulation substrate **110** made of transparent glass or plastic.

[0109] In this example, the first gate line G**1** has a first gate electrode **124***a*, a second gate electrode **124***b*, a third gate electrode **124***c*, and a fifth gate electrode **124***e* protruded from the first gate line G**1** up or down, and the second gate line G**2** has a fourth gate electrode **124***d*. The first gate line G**1** and the second gate line G**2** have an end portion (not shown) having a wide area for connection to other layers or an external driving circuit. The first gate electrode **124***a* and the second gate electrode **124***b* may be connected.

[0110] The first voltage line S**1** and the second voltage line S**2** extend in the same direction as the first gate line G**1** and the second gate line G**2**, and the first gate line G**1** and the second gate line G**2** are positioned between the first voltage line S**1** and the second voltage line S**2**.

[0111] For example, a gate insulating layer **140** is formed on the gate conductor.

[0112] A first semiconductor **154***a*, a second semiconductor **154***b*, a third semiconductor **154***c*, a fourth semiconductor **154***d*, and a fifth semiconductor **154***e* that may be made of amorphous silicon or crystalline silicon are positioned on the gate insulating layer **140**.

[0113] The first semiconductor **154***a*, the second semiconductor **154***b*, the third semiconductor **154***c*, the fourth semiconductor **154***d*, and the fifth semiconductor **154***e* respectively overlap the first gate electrode **124***a*, the second gate electrode **124***b*, the third gate electrode **124***c*, the fourth gate electrode **124***d*, and the fifth gate electrode **124***e*. The first semiconductor **154***a* and the second semiconductor **154***b* may be connected.

[0114] For example, ohmic contacts **163** and **165** are respectively formed in pairs on the first semiconductor **154***a*, the second semiconductor **154***b*, the third semiconductor **154***c*, the fourth semiconductor **154***d*, and the fifth semiconductor **154***e*.

[0115] The ohmic contacts **163** and **165** may be made of a material such as n+ hydrogenated amorphous silicon in which an n-type impurity such as phosphorus is doped at a high concentration, or of silicide.

[0116] A data conductor including a data line D**1**, a third source electrode **173***c*, a fourth source electrode **173***d*, a fifth source electrode **173***e*, a first drain electrode **175***a* to a fifth drain electrode **175***e*, a metal pattern **177**, and a metal pattern connection **7** is formed on the ohmic contacts **163** and **165** and the gate insulating layer **140**.

[0117] The data line D**1** transmits the data signal and extends in a mainly longitudinal direction, thereby intersecting the gate lines G**1** and G**2**. The data line D**1** has the second source electrode **173***b* extending toward the first gate electrode **124***a* and the second gate electrode **124***b* and the first source electrode **173***a* connected to the second source electrode **173***b*. The third source electrode **173***c* and the fourth source electrode **173***d* respectively overlap the third semiconductor **154***c* and the fourth semiconductor **154***d*. For example, the first source electrode **173***a*, the second source electrode **173***b*, the third source electrode **173***c*, the fourth source electrode **173***d* and the fifth source electrode **173***e* are curved with a ∩ shape, a ∪ shape, a ⊂ shape, or a ⊃ shape.

[0118] The first drain electrode **175***a*, the second source electrode **173***b*, the third source electrode **173***c*, the fourth source electrode **173***d* and the fifth drain electrode **175***e* include a bar portion extending in upper, lower, right, or left directions, and an expansion having a wider area than the bar portion and positioned at one end of the bar portion. The bar portions are respectively enclosed by the first source electrode **173***a*, the second source electrode **173***b*, the third source electrode **173***c*, the fourth source electrode **173***d* and the fifth source electrode **173***e*.

[0119] The metal pattern **177** overlaps the first voltage line S**1**, and is connected to the third drain electrode **175***c* and the fourth drain electrode **175***d* by the metal pattern connection **177***c*.

[0120] The first gate electrode **124***a*, the first semiconductor **154***a*, the first source electrode **173***a*, and the first drain electrode **175***a* form the first pixel switching element Qp**1**, and the second gate electrode **124***b*, the second semiconductor **154***b*, the second source electrode **173***b*, and the second drain electrode **175***b* form the second pixel switching element Qp**2**.

[0121] Also, the third gate electrode **124***c*, the third semiconductor **154***c*, the third source electrode **173***c*, and the third drain electrode **175***c* form the first switching element Q**1**, the fourth gate electrode **124***d*, the fourth semiconductor **154***d*, the fourth source electrode **173***d*, and the fourth drain electrode **175***d* form the second switching element Q**2**, and the fifth gate electrode **124***e*, the fifth semiconductor **154***e*, the fifth source electrode **175***e*, and the fifth drain electrode **175***e* form the third switching element Q**3**.

[0122] A passivation layer **180** made of the organic insulator is formed on the data conductor.

[0123] For example, the passivation layer **180** has a first contact hole **185***a* exposing the first drain electrode **175***a*, a second contact hole **185***b* exposing the second drain electrode **175***b*, a third contact hole **183***a* exposing the third drain electrode **175***c* and the first voltage line S**1**, a fourth contact hole **183***b* exposing the fourth drain electrode **175***d* and the second voltage line S**2**, and a fifth contact hole **183***c* exposing the fifth drain electrode **175***e*.

[0124] A plurality of the first pixel electrodes **191***a* and second pixel electrodes **191***b* and connecting members **8***a* and **8***b* that may be made a transparent conductive material such as indium tin oxide (ITO) or indium zinc oxide (IZO) or a reflective metal such as aluminum, silver, chromium, or alloys thereof are formed on the passivation layer **180**.

[0125] The first pixel electrode **191***a* is connected to the first drain electrode **175***a* through the first contact hole **185***a*, thereby receiving the data signal from the first drain electrode **175***a*. Also, the second pixel electrode **191***b* is connected to the second drain electrode **175***b* through the second contact hole **185***b*, thereby receiving the data signal from the second drain electrode **175***b*, and is connected to the fifth drain electrode **175***e* through the fifth contact hole **183***c*, thereby receiving the second voltage through and the fifth drain electrode **175***e* when the third switching element Q**3** is turned on.

[0126] The area of the second pixel electrode **191***b* may be about two times the area of the first pixel electrode **191***a*.

[0127] For example, the first pixel electrode **191***a* and the second pixel electrode **191***b* respectively include a plurality of minute slits MS. The first pixel electrode **191***a* and the second pixel electrode **191***b* respectively include a cross-shaped stem that is formed of a transverse stem **193** and a vertical stem **194** that is perpendicular thereto. They are respectively divided into four subregions by the transverse stem **193** and the longitudinal stem **194**, and each region includes a plurality of minute slits MS.

[0128] The minute slits MS obliquely extend from the transverse stem **193** and the longitudinal stem **194**, and the minute slits MS in each subregion extend in the same direction. The width of the minute slits MS is in the range of about 2.5 μm to about 5.0 μm, and the interval between two neighboring minute slits MS is in the range of about 2.5 μm to about 5.0 μm. Meanwhile, the first pixel electrode **191***a* has a protrusion **9** overlapping the metal pattern **177**.

[0129] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A display comprising:
a substrate;
a first gate line, a second gate line, and a data line formed on the substrate;
a plurality of pixels comprising a first subpixel and a second subpixel connected to the first gate line and the data line, the first subpixel comprising a first subpixel electrode and the second subpixel comprising a second subpixel electrode;
a first switching element connected to the first gate line and configured to control a voltage of a first capacitor connected to the first subpixel electrode; and
a second switching element connected to the second gate line and configured to control the voltage of the first capacitor.

2. The liquid crystal display of claim **1**, wherein
the second switching element is configured to control the voltage of a second capacitor connected to the second subpixel electrode.

3. The liquid crystal display of claim **2**, wherein
an on signal is provided to the second gate line in response to detection of an off signal subsequent to receiving the on signal at the first gate line; and
the first pixel voltage of the first subpixel and the second pixel voltage of the second subpixel are increased in response to detection of an on signal at the second gate line.

4. The liquid crystal display of claim **3**, wherein
the first pixel voltage and the second pixel voltage are different.

5. The liquid crystal display of claim **4**, wherein
the first pixel voltage is greater than the second pixel voltage.

6. The liquid crystal display of claim **3**, further comprising:
a first voltage line and a second voltage line being separated from the first gate line and the second gate line,
wherein the first voltage line is connected to the first switching element, and
the second voltage line is connected to the second switching element.

7. The liquid crystal display of claim **6**, wherein
the first voltage line and the second voltage line are applied with voltages comprising different polarities.

8. The liquid crystal display of claim **6**, wherein
in response to detection of turned on of the second gate line, the first pixel voltage is increased according to a charge

capacitance variation of the first capacitor, and the second pixel voltage is increased according to a voltage variation of the second capacitor.

9. The liquid crystal display of claim **8**, wherein

the capacitance of the first capacitor is greater than the charge capacitance of the second capacitor.

10. The liquid crystal display of claim **9**, wherein

the electrode area of the first capacitor is greater than the electrode area of the second capacitor.

11. The liquid crystal display of claim **2**, further comprising:

a first pixel switching element connected to the first gate line and the data line, and the first subpixel electrode; and

a second pixel switching element connected to the first gate line, data line, and the second subpixel electrode.

12. The liquid crystal display of claim **1**, further comprising:

a second capacitor connected to the second subpixel electrode; and

a third switching element connected to the second capacitor and configured to control the voltage of the second capacitor.

13. The liquid crystal display of claim **12**, wherein

an on signal is provided to the second gate line in response to detection of an off signal subsequent to receiving the on signal at the first gate line; and

the first pixel voltage of the first subpixel is increased in response to detection of an on signal at the second gate line.

14. The liquid crystal display of claim **13**, wherein

the first pixel voltage and the second pixel voltage of the second subpixel are different.

15. The liquid crystal display of claim **14**, wherein

the first pixel voltage is greater than the second pixel voltage.

16. The liquid crystal display of claim **13**, further comprising:

a first voltage line and a second voltage line being separated from the first gate line and the second gate line,

wherein the first voltage line is connected to the first switching element and

the second voltage line is connected to the second switching element.

17. The liquid crystal display of claim **16**, wherein

the first voltage line and the second voltage line are applied with voltages comprising different polarities.

18. The liquid crystal display of claim **17**, wherein

in response to detection of turned on of the second gate line, the first pixel voltage is increased according to the charge capacitance variation of the first capacitor.

19. The liquid crystal display of claim **18**, wherein

the first pixel voltage and the second pixel voltage of the second subpixel are different.

20. The liquid crystal display of claim **19**, wherein

the first pixel voltage is greater than the second pixel voltage.

21. The liquid crystal display of claim **12**, further comprising:

a first pixel switching element connected to the first gate line, data line, and the first subpixel electrode; and

a second pixel switching element connected to the first gate line, the data line and the second subpixel electrode.

22. The liquid crystal display of claim **1**, wherein

the first subpixel and the second subpixel comprise four domains having different directions of liquid crystal molecules.

* * * * *

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摘要(译)

根据本发明示例性实施例的液晶显示器包括：绝缘基板;形成在绝缘基板上的第一栅极线和第二栅极线;与第一栅极线和第二栅极线交叉的数据线;多个像素，分别包括连接到第一栅极线和数据线的第一子像素和第二子像素;第一开关元件，连接到第一栅极线并控制连接到第一子像素电极的第一电容器的电压;第二开关元件连接到第二栅极线以控制第一电容器的电压。