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(54) **PERIPHERAL TEST CIRCUIT OF DISPLAY ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY PANEL**

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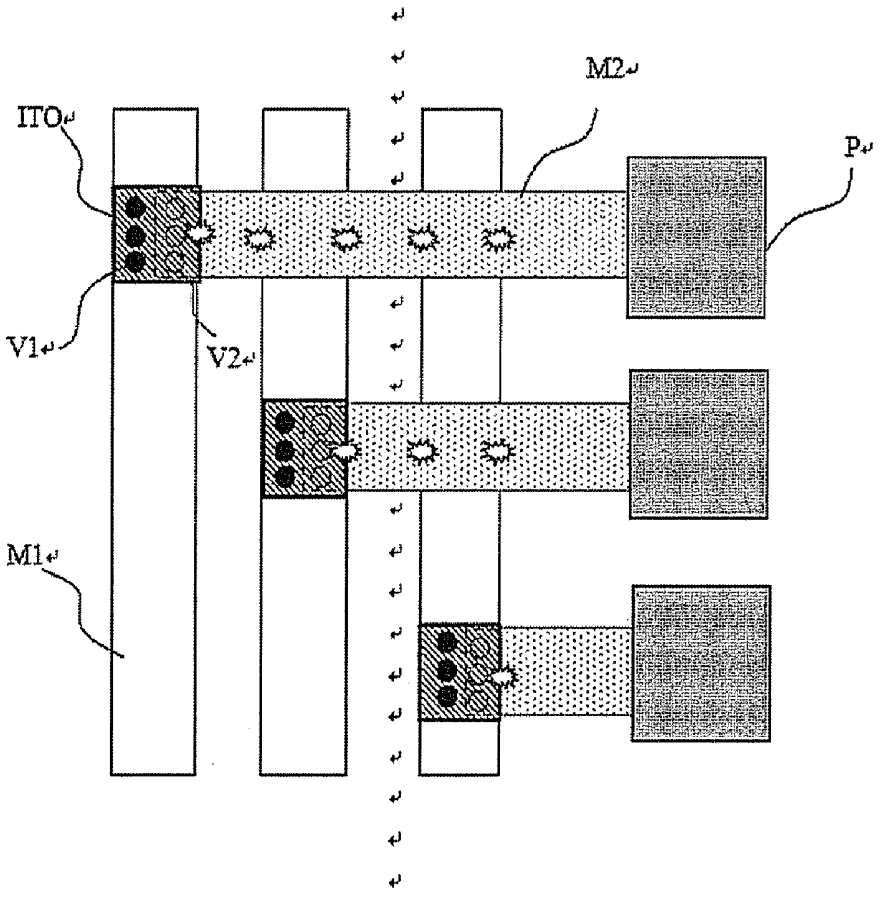
(57) **ABSTRACT**

The present disclosure relates to a peripheral test circuit of a display array substrate, and a liquid crystal display panel. The peripheral test circuit of a display array substrate includes: multiple groups of test signal lines, each group consisting of a first and a second test signal lines spaced from each other; a plurality of test pad leads, each being arranged in an interval formed between the first and the second test signal lines of a respective group, and connected with the first and the second test signal lines but not overlapped with the first and the second test signal lines of other groups; and a plurality of test pads, each being arranged on a respective test pad lead. According to the peripheral test circuit of the present disclosure, the problem existing in the current peripheral test circuit, i.e., a short circuit formed between the test pad lead and the test signal line due to electrostatic discharge caused by crossover between the test pad lead and the test signal line, can be overcome, thus reducing the injury risk of electrostatic discharge.



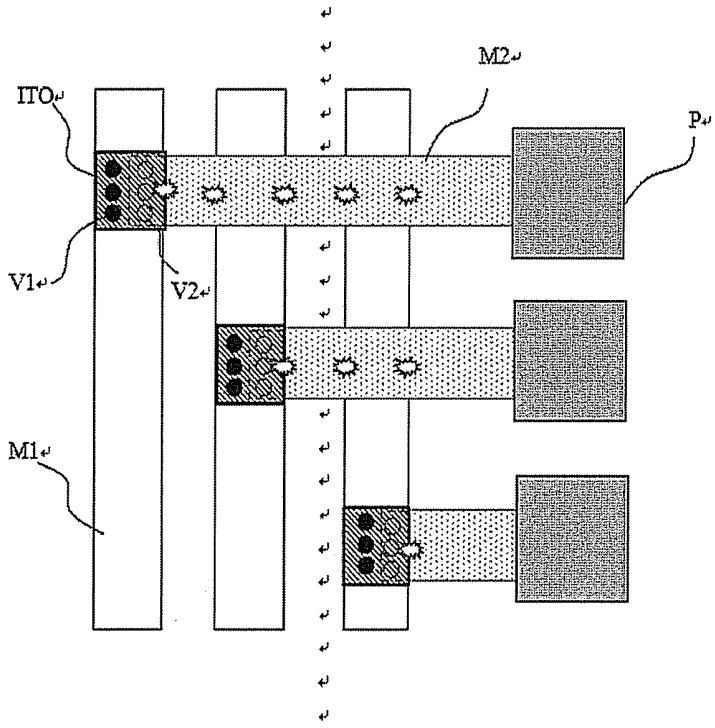


Fig. 1

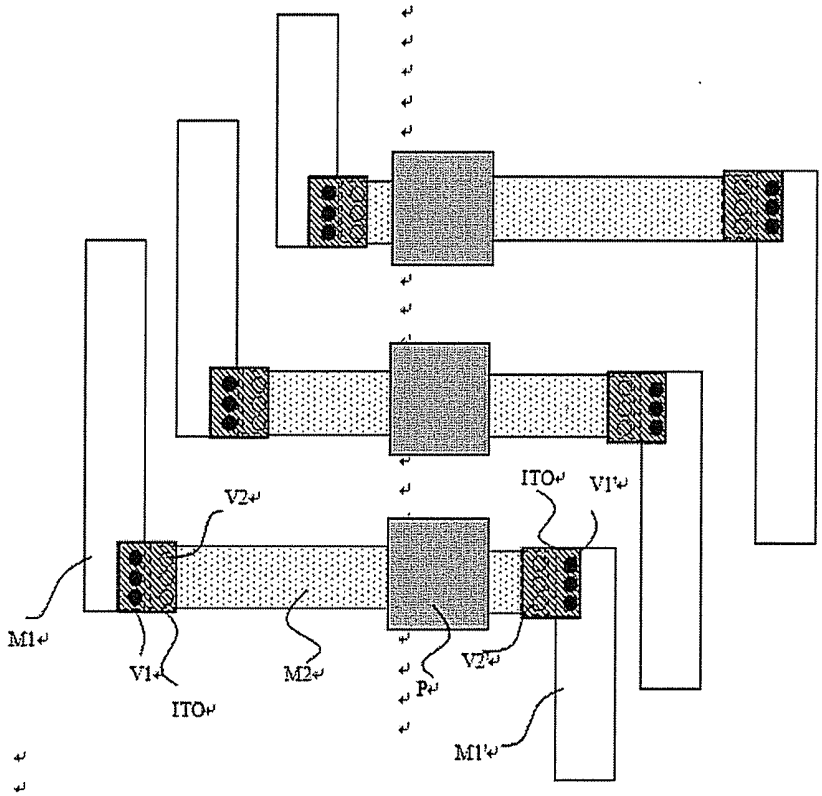


Fig. 2

PERIPHERAL TEST CIRCUIT OF DISPLAY ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY PANEL

[0001] The present disclosure claims the priority of Chinese Patent Application CN 201410216387.4, filed on May 21, 2014 and entitled "Peripheral test circuit of display array substrate and liquid crystal display panel", the entire contents of which are herein incorporated by reference.

FIELD OF THE INVENTION

[0002] The present disclosure relates to the field of liquid crystal display, in particular to a peripheral test circuit of a display array substrate and a liquid crystal display panel.

BACKGROUND OF THE INVENTION

[0003] Generally, in the previous process of manufacturing a liquid crystal display, millions of thin film transistors are formed on a substrate through an epitaxial method to serve as control units. However, if the quality of part of the thin film transistors cannot achieve the desired effect during manufacturing, the switching control characteristic cannot be presented, so that the defect of bright spots or dark spots will be produced, and thus the quality of the liquid crystal display will be significantly reduced. Therefore, the thin film transistors must be effectively tested to maintain the quality of the liquid crystal display.

[0004] In the existing solutions for testing the thin film transistors of the display, for the structure of connecting test signal lines on the peripheral area of a TFT array substrate with test pads, reference may be made to FIG. **1**. As shown in FIG. **1**, a test signal line M**1** on the peripheral area of the substrate passes through a passivation layer via hole V**1** through which ITO is connected with the test signal line M**1** and a passivation layer via hole V**2** through which ITO is connected with a test pad lead M**2**, and then is connected with the test pad lead M**2** and further connected to a corresponding test pad P. It could be seen from the figure that, in the process of connecting different test signal lines M**1** to the corresponding test pads P through the test pad leads M**2**, the test pad leads M**2** will have to run across other test signal lines M**1**. Electrostatic discharge is easily caused in the crossover process of the test signal lines M**1** and the test pad leads M**2**, so that the test signal lines M**1** and the test pad leads M**2** will be in short circuit with each other. In this case, the test signal lines are short-circuited and no detction can be performed, thus reducing the yield of a product.

[0005] Therefore, a solution is needed to solve the problem that the test signal lines and the test pad leads are easily in short circuit with each other in the prior art, reduce the injury risk of electrostatic discharge, improve the test accuracy of the product, and then improve the yield of the product.

SUMMARY OF THE INVENTION

[0006] One of the technical problems to be solved by the present disclosure is to provide a peripheral test circuit of a display array substrate, which may solve the problem that test signal lines and test pad leads are easily in short circuit with each other, and may further reduce the injury risk of electrostatic discharge. In addition, the display array substrate and a liquid crystal display panel are further provided.

[0007] To solve the above-mentioned technical problem, the present disclosure provides a peripheral test circuit of a display array substrate, including: multiple groups of test signal lines, each group of test signal lines consisting of a first test signal line and a second test signal line spaced from each other; a plurality of test pad leads, each test pad lead being arranged in an interval formed between the first test signal line and the second test signal line of a respective group, and connected with the first test signal line and the second test signal line but not overlapped with the first test signal line and the second test signal line of other groups; and a plurality of test pads, each test pad being arranged on a respective test pad lead.

[0008] In an embodiment, each test pad lead is connected with the first test signal line of the group associated with said test pad lead in a non-overlapping manner through a first passivation layer via hole and a second passivation layer via hole, and connected with the second test signal line of the group associated with said test pad lead in a non-overlapping manner through a third passivation layer via hole and a fourth passivation layer via hole. In this arrangement, the first passivation layer via hole is a passivation layer via hole through which an ITO layer is connected with the first test signal line, the second passivation layer via hole is a passivation layer via hole through which the ITO layer is connected with the test pad lead, the third passivation layer via hole is a passivation layer via hole through which another ITO layer is connected with the second test signal line, and the fourth passivation layer via hole is a passivation layer via hole through which said another ITO layer is connected with the test pad lead.

[0009] In an embodiment, the plurality of test pad leads are arranged in parallel but staggered from each other.

[0010] In an embodiment, the first test signal line and the second test signal line of each group are respectively connected with a corresponding test pad lead along a direction perpendicular thereto.

[0011] According to another aspect of the present disclosure, further provided is a display array substrate, including a display area and a peripheral test circuit located around the display area. The peripheral test circuit includes: multiple groups of test signal lines, each group of test signal lines consisting of a first test signal line and a second test signal line spaced from each other; a plurality of test pad leads, each test pad lead being arranged in an interval formed between the first test signal line and the second test signal line of a respective group, and connected with the first test signal line and the second test signal line but not overlapped with the first test signal line and the second test signal line of other groups; and a plurality of test pads, each test pad being arranged on a respective test pad lead.

[0012] In an embodiment, each test pad lead is connected with the first test signal line of the group associated with said test pad lead in a non-overlapping manner through a first passivation layer via hole and a second passivation layer via hole, and connected with the second test signal line of the group associated with said test pad lead in a non-overlapping manner through a third passivation layer via hole and a fourth passivation layer via hole. In this arrangement, the first passivation layer via hole is a passivation layer via hole through which an ITO layer is connected with the first test signal line, the second passivation layer via hole is a passivation layer via hole through which the ITO layer is connected with the test pad lead, the third passivation layer via hole is a passivation layer via hole through which another ITO layer is connected with the second test signal line, and the fourth passivation

layer via hole is a passivation layer via hole through which said another ITO layer is connected with the test pad lead.

[0013] In an embodiment, a plurality of test pad leads are arranged in parallel but staggered from each other.

[0014] In an embodiment, the first test signal line and the second test signal line of each group are respectively connected with a corresponding test pad lead along a direction perpendicular thereto.

[0015] According to a further aspect, also provided is a liquid crystal display panel including the above-mentioned display array substrate.

[0016] Compared with the prior art, one or more embodiments of the present disclosure may have the following advantages. According to the peripheral test circuit of the present disclosure, a crossover phenomenon between the test pad leads and the test signal lines can be avoided by changing the mode of connection between the test signal lines and the test pads. The test pad leads will not cross over the test signal lines through the via holes at the connection positions of the test pad leads and the test signal lines, so that the injury risk of electrostatic discharge is reduced, the test accuracy of a product is improved, and the yield of the product is improved.

[0017] Other features and advantages of the present disclosure will be set forth in the following description, and in part will be made obvious from the description, or be learned by implementing the present disclosure. The objectives and other advantages of the present disclosure may be achieved and obtained by structures particularly pointed out in the description, the claims and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] The accompanying drawings are configured to provide a further understanding of the present disclosure, constitute a part of the description, and explain the present disclosure together with the embodiments of the present disclosure without limiting the present disclosure. In the accompanying drawings:

[0019] FIG. **1** is a schematic diagram of a structure of connecting test signal lines on the peripheral area of a TFT array substrate with test pads in the prior art; and

[0020] FIG. **2** is a schematic, diagram of a peripheral test circuit of a display array substrate according to an embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0021] In order that the objectives, technical solutions and advantages of the present disclosure are clearer, a further detailed illustration to the present disclosure will be given below, in combination with the accompanying drawings.

[0022] FIG. **2** is a schematic diagram of a peripheral test circuit of a display array substrate according to an embodiment of the present disclosure.

[0023] As shown in FIG. **2**, the peripheral test circuit includes: multiple groups of test signal lines, each group of test signal lines consisting of a first test signal line M**1** and a second test signal line M**1'** spaced from each other; a plurality of test pad leads M**2**, each test pad M**2** lead being arranged in an interval formed between the first test signal line M**1** and the second test signal line M**1'** of a respective group, and connected with said first test signal line M**1** and said second test signal line M**1'** but not overlapped with the first test signal line M**1** and the second test signal line M**1'** of other groups; and a plurality of test pads P, each test pad P being arranged on a respective test pad lead M**2**. The test pads P may transmit test signals generated by a signal generator to corresponding data lines or scan lines through the test signal lines M**1** and M**1'**, in order to detect whether the data lines or the scan lines are open-circuit.

[0024] In an embodiment, one end of each test pad lead M**2** is connected with the first test signal line M**1** of the same group as said test pad lead M**2** in a non-overlapping manner through a first passivation layer via hole V**1** and a second passivation layer via hole V**2**, and the other end of each test pad lead M**2** is connected with the second test signal line M**1'** of the same group as said test pad lead M**2** in a non-overlapping manner through a third passivation layer via hole V**1'** and a fourth passivation layer via hole V**2'**. In this arrangement, the first passivation layer via hole V**1**. is a passivation layer via hole through which an ITO layer is connected with the first test signal line M**1**, the second passivation layer via hole V**2** is a passivation layer via hole through which the ITO layer is connected with one end of the test pad lead M**2**, the third passivation layer via hole V**1'** is a passivation layer via hole through which another ITO layer is connected with the second test signal line M**1'**, and the fourth passivation layer via hole V**2'** is a passivation layer via hole through which the another ITO layer is connected with the other end the test pad lead M**2**. Preferably, the plurality of test pad leads M**2** are arranged in parallel, but staggered with each other, and the first test signal line M**1** and the second test signal line M**1'** of each group are respectively connected with a corresponding test pad lead M**2** along a direction perpendicular thereto, in particular as shown in FIG. **2**.

[0025] The peripheral test circuit according to the embodiment of the present disclosure solves the problem that the test pad leads are in short circuit with the test signal lines due to high electrostatic discharge possibility caused by overlapping crossover of the test pad leads and the test signal lines in the existing peripheral test circuit. The injury risk of electrostatic discharge may be reduced. Therefore, the test accuracy of a product may be improved, and the yield of the product may be improved.

[0026] The present disclosure further provides a display array substrate, including a display area and a peripheral test circuit located around the display area, wherein the peripheral test circuit is one with the above structure. In addition, the present disclosure further provides a liquid crystal display panel, including the above-mentioned display array substrate.

[0027] The foregoing descriptions are merely specific embodiments of the present disclosure, rather than limiting the protection scope of the present disclosure. Variations or substitutions made to the present disclosure by any skilled one familiar with this art within the technical specification of the present disclosure shall fall into the protection scope of the present disclosure.

1. A peripheral test circuit of a display array substrate, including:

multiple groups of test signal lines, each group of test signal lines consisting of a first test signal line and a second test signal line spaced from each other;

a plurality of test pad leads, each test pad lead being arranged in an interval formed between the first test signal line and the second test signal line of a respective group, and connected with the first test signal line and

the second test signal line but not overlapped with the first test signal line and the second test signal line of other groups; and

a plurality of test pads, each test pad being arranged on a respective test pad lead.

2. The peripheral test circuit according to claim **1**, wherein each test pad lead is connected with the first test signal line of the group associated with said test pad lead in a non-overlapping manner through a first passivation layer via hole and a second passivation layer via hole, and is connected with the second test signal line of the group associated with said the test pad lead in a non-overlapping manner through a third passivation layer via hole and a fourth passivation layer via hole, and

wherein the first passivation layer via hole is a passivation layer via hole through which an ITO layer is connected with the first test signal line, the second passivation layer via hole is a passivation layer via hole through which the ITO layer is connected with the test pad lead, the third passivation layer via hole is a passivation layer via hole through which another ITO layer is connected with the second test signal line, and the fourth passivation layer via hole is a passivation layer via hole through which said another ITO layer is connected with the test pad lead.

3. The peripheral test circuit according to claim **2**, wherein the plurality of test pad leads are arranged in parallel but staggered from each other.

4. The peripheral test circuit according to claim **3**, wherein the first test signal line and the second test signal line of each group are respectively connected with a corresponding test pad lead along a direction perpendicular thereto.

5. A display array substrate, including a display area and a peripheral test circuit arranged around the display area,

said peripheral test circuit including:

multiple groups of A display array substrate test signal lines, each group of test signal lines consisting of a first test signal line and a second test signal line spaced from each other;

a plurality of test pad leads, each test pad lead being arranged in an interval formed between the first test signal line and the second test signal line of a respective group, and connected with the first test signal line and the second test signal line but not overlapped with the first test signal line and the second test signal line of other groups; and

a plurality of test pads, each test pad being arranged on a respective test pad lead.

6. The display array substrate according to claim **5**, wherein each test pad lead is connected with the first test signal line of the group associated with said test pad lead in a non-overlapping manner through a first passivation layer via hole and a second passivation layer via hole, and is connected with the second test signal line of the group associated with said the test pad lead in a non-overlapping manner through a third passivation layer via hole and a fourth passivation layer via hole, and

wherein the first passivation layer via hole is a passivation layer via hole through which an ITO layer is connected with the first test signal line, the second passivation layer via hole is a passivation layer via hole through which the ITO layer is connected with the test pad lead, the third passivation layer via hole is a passivation layer via hole through which another ITO layer is connected with the second test signal line, and the fourth passivation layer via hole is a passivation layer via hole through which said another ITO layer is connected with the test pad lead.

7. The display array substrate according to claim **5**, wherein the plurality of test pad leads are arranged in parallel but staggered from each other.

8. The display array substrate according to claim **7**, wherein the first test signal line and the second test signal line of each group are respectively connected with a corresponding test pad lead along a direction perpendicular thereto.

9. A liquid crystal display panel, having a display array substrate including a display area and a peripheral test circuit arranged around the display area,

said peripheral test circuit including:

multiple groups of test signal lines, each group of test signal lines consisting of a first test signal line and a second test signal line spaced from each other;

a plurality of test pad leads, each test pad lead being arranged in an interval formed between the first test signal line and the second test signal line of a respective group, and connected with the first test signal line and the second test signal line but not overlapped with the first test signal line and the second test signal line of other groups; and

a plurality of test pads, each test pad being arranged on a respective test pad lead.

10. The liquid crystal display panel according to claim **9**, wherein each test pad lead is connected with the first test signal line of the group associated with said test pad lead in a non-overlapping manner through a first passivation layer via hole and a second passivation layer via hole, and is connected with the second test signal line of the group associated with said the test pad lead in a non-overlapping manner through a third passivation layer via hole and a fourth passivation layer via hole, and

wherein the first passivation layer via hole is a passivation layer via hole through which an ITO layer is connected with the first test signal line, the second passivation layer via hole is a passivation layer via hole through which the ITO layer is connected with the test pad lead, the third passivation layer via hole is a passivation layer via hole through which another ITO layer is connected with the second test signal line, and the fourth passivation layer via hole is a passivation layer via hole through which said another ITO layer is connected with the test pad lead.

11. The liquid crystal display panel according to claim **9**, wherein the plurality of test pad leads are arranged in parallel but staggered from each other.

12. The liquid crystal display panel according to claim **11**, wherein the first test signal line and the second test signal line of each group are respectively connected with a corresponding test pad lead along a direction perpendicular thereto.

* * * * *

专利名称(译)	显示阵列基板和液晶显示面板的外围测试电路		
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当前申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
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摘要(译)

本发明涉及显示阵列基板的外围测试电路和液晶显示面板。显示阵列基板的外围测试电路包括：多组测试信号线，每组由彼此隔开的第一测试信号线和第二测试信号线组成;多个测试焊盘引线，每个被布置在形成在相应组的第一测试信号线和第二测试信号线之间的间隔中，并且与第一测试信号线和第二测试信号线连接，但是不与第一测试信号和第二测试信号重叠其他组的线;以及多个测试焊盘，每个测试焊盘布置在相应的测试焊盘引线上。根据本公开的外围测试电路，存在于当前外围测试电路中的问题，即，由于测试焊盘引线与测试焊盘引线之间的交叉导致的静电放电，在测试焊盘引线和测试信号线之间形成的短路，测试信号线，可以克服，从而减少静电放电的伤害风险。