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(54) **SHIFT REGISTER UNIT AND GATE DRIVE DEVICE FOR LIQUID CRYSTAL DISPLAY**

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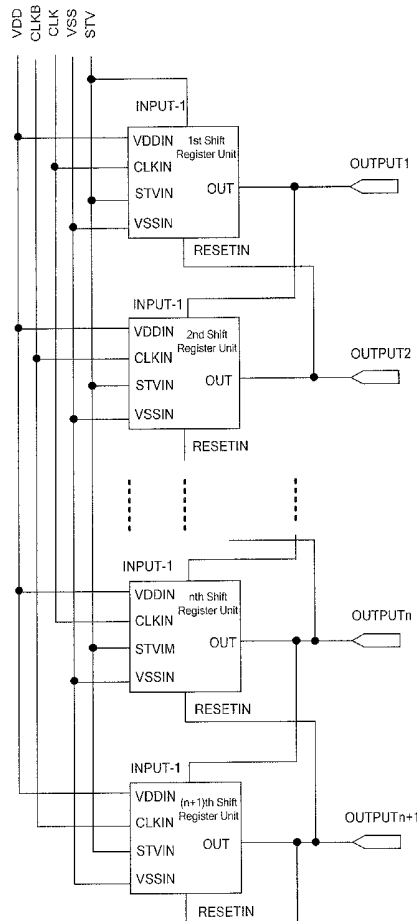
(57) **ABSTRACT**

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A shift register unit and a gate drive device for a liquid crystal display are disclosed. Both gate and drain of the tenth thin film transistor are connected to the source of the fifth thin film transistor, a source thereof is connected to a low voltage signal input terminal, threshold voltages of the eighth thin film transistor and the ninth thin film transistor are equal to or less than threshold voltage of the tenth thin film transistor. The shift register unit and the gate drive device for liquid crystal display provided in the present invention, could enable the thin film transistor used to suppress the noise in the shift register unit to maintain turning on, therefore it guarantees the reliability of the shift register unit.

Related U.S. Application Data

(60) Continuation-in-part of application No. 14/011,006, filed on Aug. 27, 2013, now Pat. No. 8,666,019, which is a division of application No. 12/878,151, filed on Sep. 9, 2010, now Pat. No. 8,548,115.



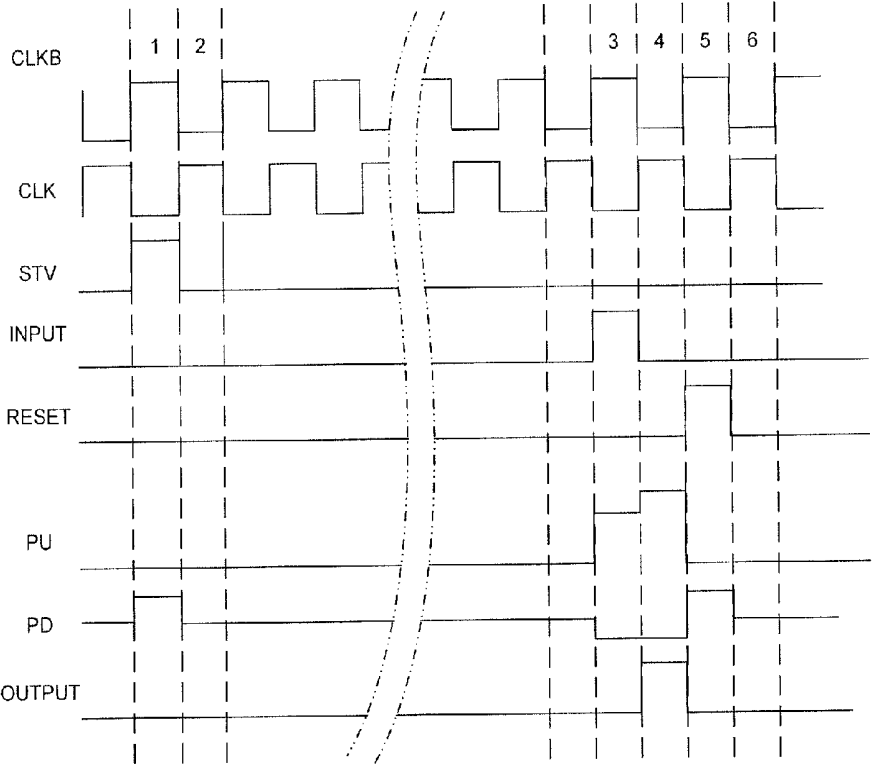


Fig. 1b

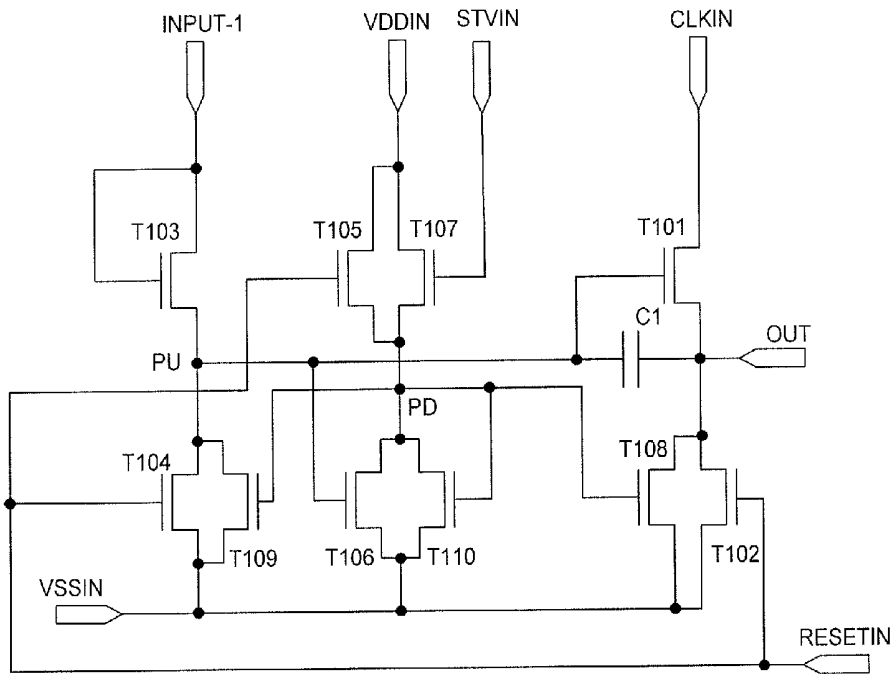


Fig. 2a

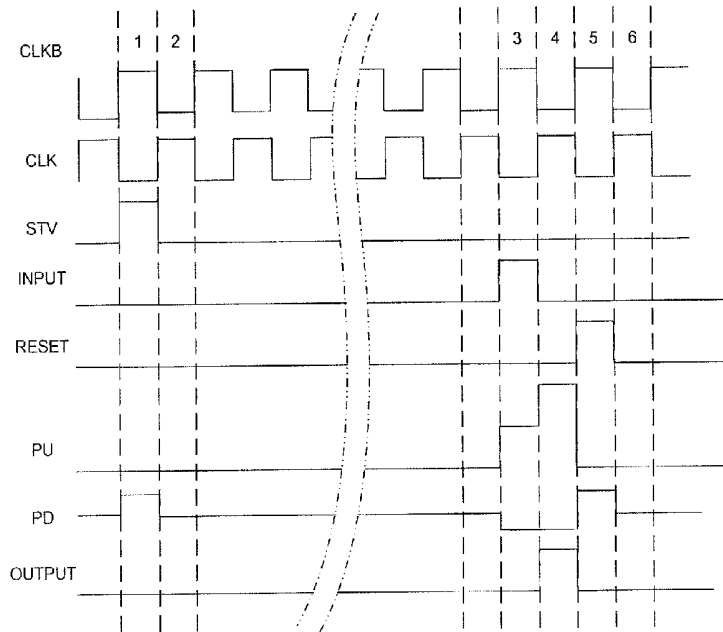


Fig. 2b

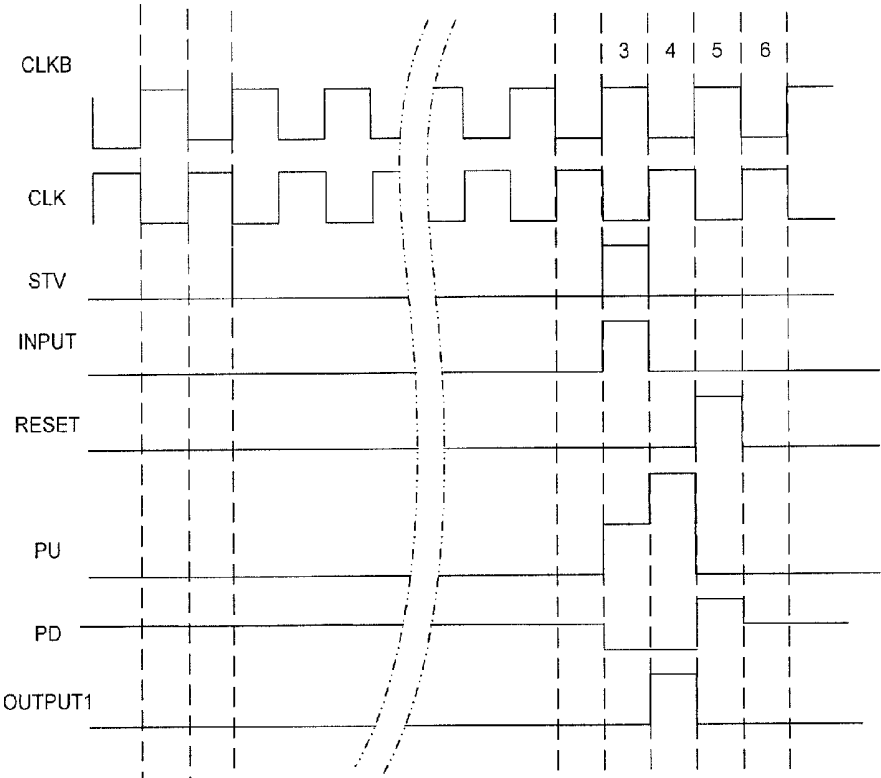


Fig. 3

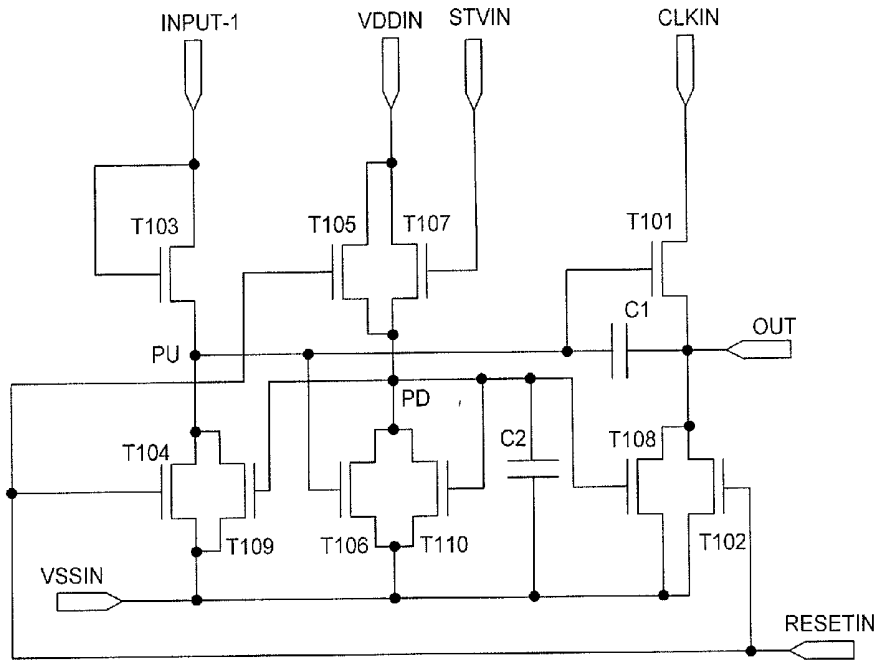


Fig. 4a

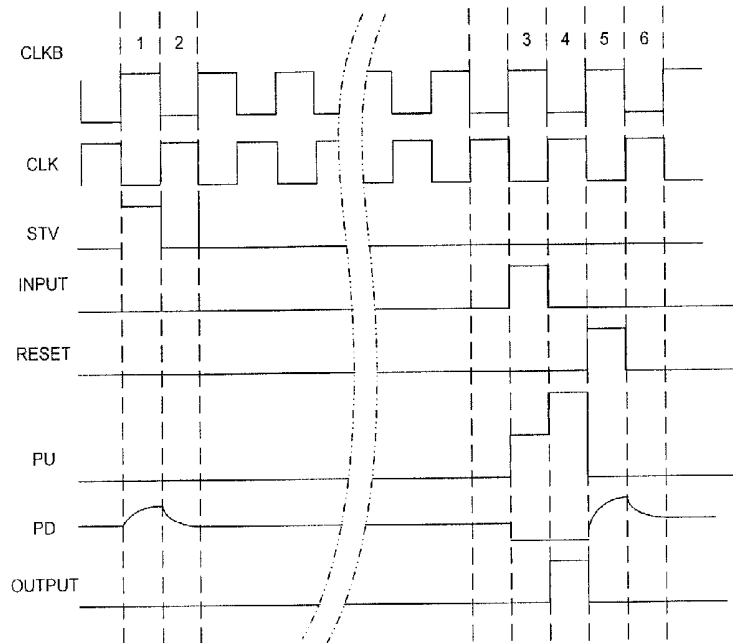


Fig. 4b

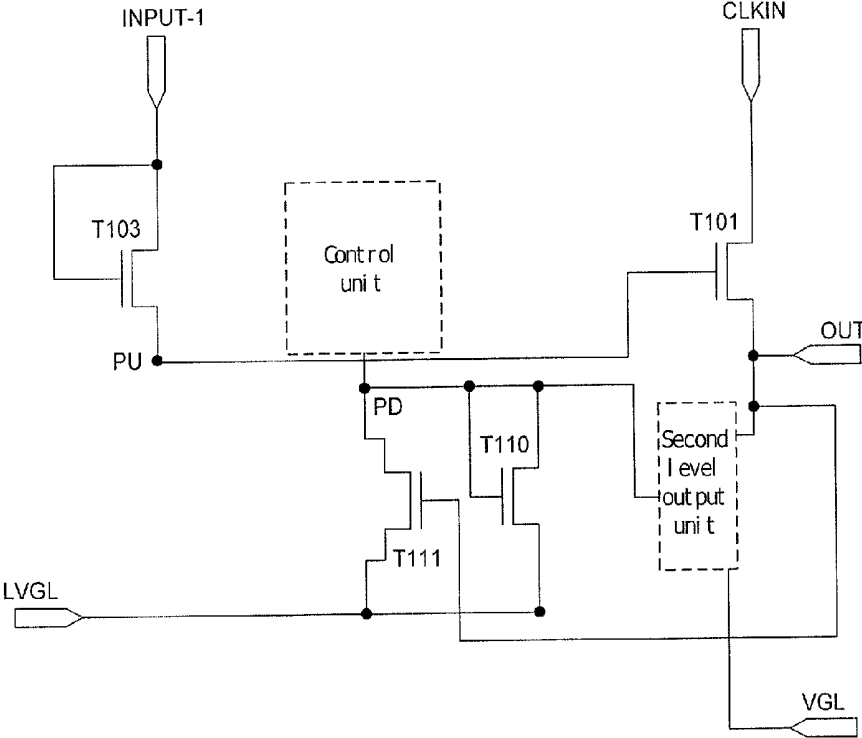


Fig. 5a

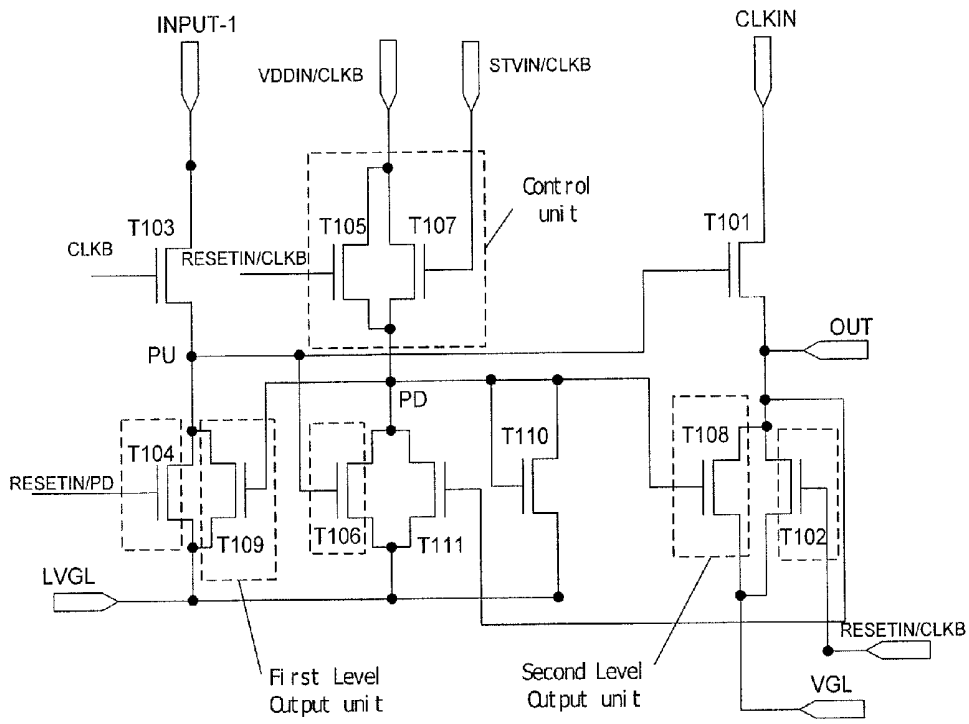


Fig. 5b

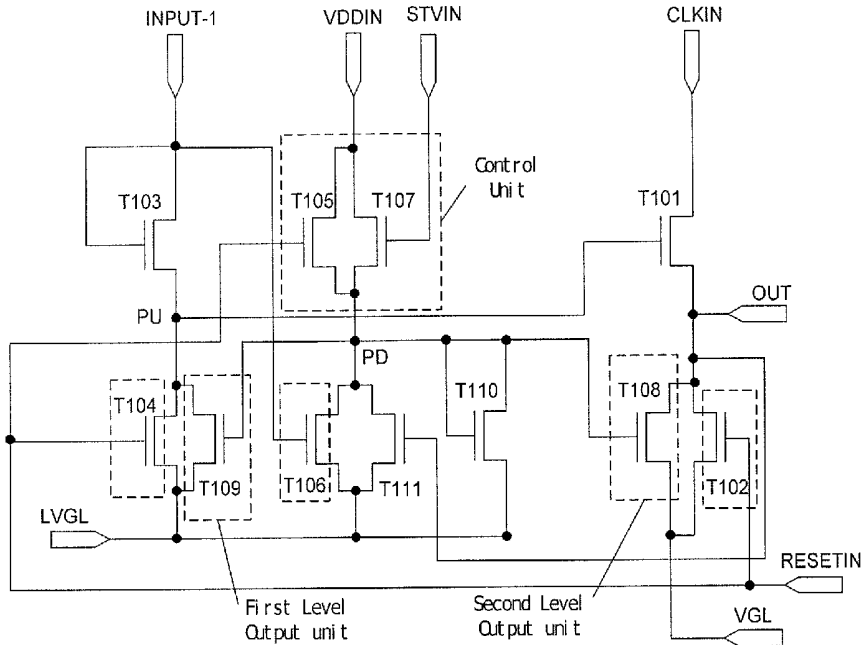


Fig. 5c

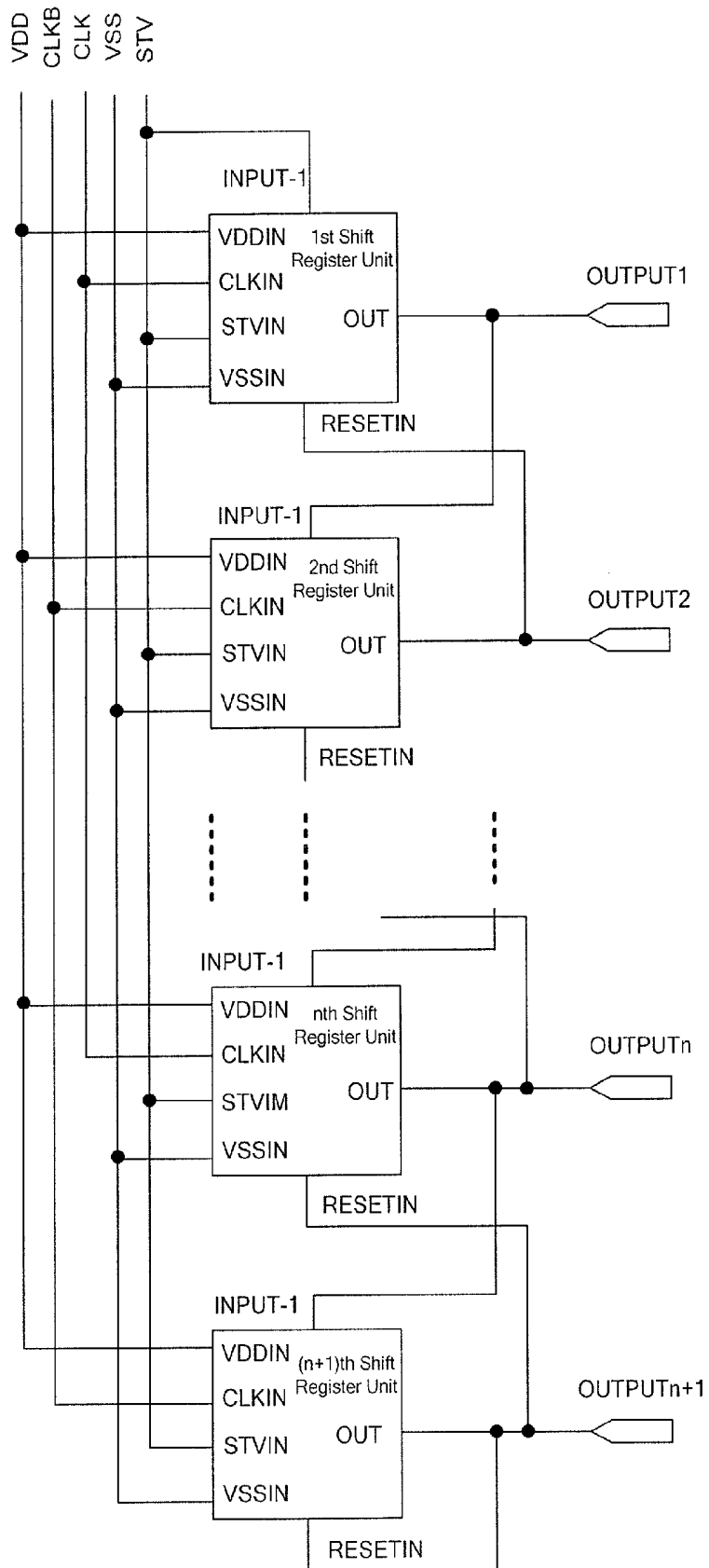


Fig. 7a

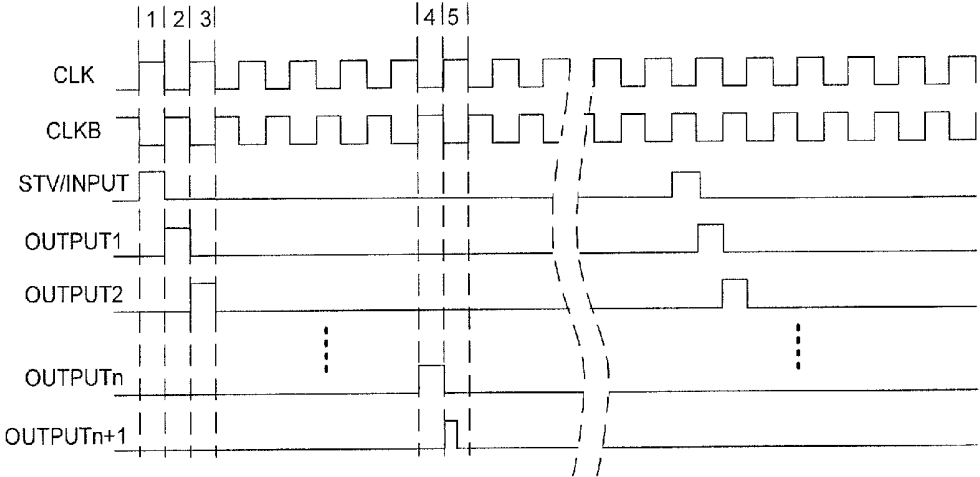


Fig. 7b

SHIFT REGISTER UNIT AND GATE DRIVE DEVICE FOR LIQUID CRYSTAL DISPLAY

BACKGROUND

[0001] The embodiments of present invention relates to a field for a liquid crystal display, in particular to a shift register unit and a gate drive device for the liquid crystal display.

[0002] A shift register unit in the prior art includes a signal output terminal outputting a gate drive signal. When the gate drive signal is at high level, the shift register unit controls a row of thin film transistors to be turned on; when the gate drive signal is at low level, the shift register unit controls a row of thin film transistors to be turned off.

[0003] The liquid crystal display generally utilizes a scan manner of row by row, when scanning a certain row, the corresponding shift register unit outputs a gate drive signal with high level, the remaining shift register units output a gate drive signal with low level, it is obvious that, for a shift register unit, the gate drive signal is at low level for the most time.

[0004] During the time that the gate drive signal is at low level, the gate drive signal would be easily suffer the interference of an inputted clock signal and than produce noise. In order to suppress the noise, the shift register unit normally includes a pull-down thin film transistor which is used to pull down the gate drive signal during the gate drive signal is at low level. A node connected to a gate of the pull-down thin film transistor controls the pull-down thin film transistor to be turned on, such that it can pull down the level of the gate drive signal at the signal output terminal.

[0005] The existing problems of the shift register unit in the prior art are: usually the node connected to the gate of the pull-down thin film transistor maintains high level at most time, in this way the pull-down thin film transistor maintains turning on at most time, such that it makes a threshold voltage of the pull-down thin film transistor subjected to a large offset. If the threshold voltage of the pull-down thin film transistor keeps increasing, then it would cause the pull-down thin film transistor unable to be turned on, thereby unable to make the contribution of suppressing the noise, and then the performance of the whole shift register unit would be affected.

SUMMARY

[0006] The embodiments of present invention provide a shift register unit and a gate drive device for the liquid crystal display capable of making the thin film transistor used to suppressing the noise in the shift register unit maintain turning on, so as to guarantee the reliability of the shift register unit.

[0007] An embodiment of the present invention provides a shift register unit, comprising:

[0008] a third thin film transistor for controlling a level at a pull-up node under a control of a first control signal;

[0009] a first thin film transistor for outputting a first clock signal to a signal output terminal under a control of a level at the pull-up node;

[0010] a control unit for controlling a level at a pull-down node;

[0011] a second level output unit for outputting a second level signal to the signal output terminal under a control of the level at the pull-down node;

[0012] a tenth thin film transistor for inputting a first level signal to the pull-down node under a control of the level at the pull-down node; and

[0013] an eleventh thin film transistor for inputting a first level signal to the pull-down node under a control of a level at the signal output terminal

[0014] Optionally, wherein the first thin film transistor, has a drain connected to a first clock signal input terminal, a source connected to a signal output terminal;

[0015] a second thin film transistor, has a drain connected to the source of the first thin film transistor, a gate connected to a reset signal input terminal, a source connected to a low voltage signal input terminal;

[0016] a third thin film transistor, has a drain and a gate both connected to a signal input terminal, a source connected to the gate of the first thin film transistor;

[0017] a fourth thin film transistor, has a drain connected to the source of the third thin film transistor, a gate connected to the reset signal input terminal, a source connected to the low voltage signal input terminal;

[0018] a fifth thin film transistor, has a drain connected to a high voltage signal input terminal, a gate connected to the reset signal input terminal;

[0019] a sixth thin film transistor, has a drain connected to the source of the fifth thin film transistor, a gate connected to the source of the third thin film transistor, a source connected to the low voltage signal input terminal;

[0020] a seventh thin film transistor, has a drain connected to the high voltage signal input terminal, a gate connected to a frame start signal input terminal, a source connected to the drain of the sixth thin film transistor;

[0021] an eighth thin film transistor, has a drain connected to the source of the first thin film transistor, a source connected to the low voltage signal input terminal, a gate connected to the source of the fifth thin film transistor,

[0022] a ninth thin film transistor, has a drain connected to the source of the third thin film transistor, a gate connected to the source of the fifth thin film transistor, a source connected to the low voltage signal input terminal; and

[0023] a tenth thin film transistor, has a drain and a gate both connected to the source of the fifth thin film transistor, a source connected to the low voltage signal input terminal;

[0024] wherein threshold voltages of the eighth thin film transistor and the ninth thin film transistor are equal to or less than threshold voltage of the tenth thin film transistor.

[0025] Another embodiment of the present invention also provides a gate drive device for liquid crystal display, comprising a plurality of shift register units defined as above, deposited on an array substrate of the liquid crystal display;

[0026] except for a first shift register unit and a last shift register unit, the signal output terminal of each of the rest of the shift register units is connected to a signal input terminal of a next adjacent shift register unit and to a reset signal input terminal of a previous adjacent shift register unit, a signal output terminal of the first shift register unit is connected to a signal input terminal of a second shift register unit, a signal output terminal of the last shift register unit is connected to a reset signal input terminal of a previous adjacent shift register unit and the reset signal input terminal itself;

[0027] a signal input terminal of the first shift register unit inputs a frame start signal;

[0028] the first clock signal input terminal of the odd-numbered shift register unit inputs a first clock signal; the first

clock signal input terminal of the even-numbered shift register unit inputs a second clock signal;

[0029] a low voltage signal input terminal of each shift register unit inputs a low voltage signal; and

[0030] a high voltage signal input terminal of each shift register unit inputs a high voltage signal.

[0031] Another embodiment of the present invention also provides a shift register unit, comprising:

[0032] a first thin film transistor, whose drain is connected to a first clock signal input terminal, a source thereof is connected to a signal output terminal;

[0033] a second thin film transistor, whose drain is connected to the source of the first thin film transistor, a gate thereof is connected to a reset signal input terminal, a source thereof is connected to a low voltage signal input terminal;

[0034] a third thin film transistor, whose drain and gate are both connected to a signal input terminal, a source thereof is connected to the gate of the first thin film transistor;

[0035] a fourth thin film transistor, whose drain is connected to the source of the third thin film transistor, a gate thereof is connected to the reset signal input terminal, a source thereof is connected to the low voltage signal input terminal;

[0036] a fifth thin film transistor, whose drain is connected to a high voltage signal input terminal, a gate thereof is connected to the reset signal input terminal;

[0037] a sixth thin film transistor, whose drain is connected to the source of the fifth thin film transistor, a gate thereof is connected to the signal input terminal, a source thereof is connected to the low voltage signal input terminal;

[0038] a seventh thin film transistor, whose drain is connected to the high voltage signal input terminal, a gate thereof is connected to a frame start signal input terminal, a source thereof is connected to the drain of the sixth thin film transistor;

[0039] an eighth thin film transistor, whose drain is connected to the source of the first thin film transistor, a source thereof is connected to the low voltage signal input terminal, a gate thereof is connected to the source of the fifth thin film transistor;

[0040] a ninth thin film transistor, whose drain is connected to the source of the third thin film transistor, a gate thereof is connected to the source of the fifth thin film transistor, a source thereof is connected to the low voltage signal input terminal;

[0041] a tenth thin film transistor, whose drain and gate are both connected to the source of the fifth thin film transistor, a source thereof is connected to the low voltage signal input terminal; and

[0042] an eleventh thin film transistor, whose drain is connected to the source of the fifth thin film transistor, a source thereof is connected to the low voltage signal input terminal, a gate thereof is connected to the signal output terminal;

[0043] wherein threshold voltages of the eighth thin film transistor and the ninth thin film transistor are equal to or less than threshold voltage of the tenth thin film transistor.

[0044] Still another embodiment of the present invention provides a gate drive device for liquid crystal display, comprising a plurality of shift register units defined as above, deposited on an array substrate of the liquid crystal display;

[0045] except for a first shift register unit and a last shift register unit, the signal output terminal of each of the rest of the shift register units is connected to a signal input terminal of a next adjacent shift register unit and a reset signal input

terminal of a previous adjacent shift register unit, a signal output terminal of the first shift register unit is connected to a signal input terminal of a second shift register unit, a signal output terminal of the last shift register unit is connected to a reset signal input terminal of a previous adjacent shift register unit and the reset signal input terminal of itself;

[0046] a signal input terminal of the first shift register unit inputs a frame start signal;

[0047] the first clock signal input terminal of the odd-numbered shift register unit inputs a first clock signal; the first clock signal input terminal of the even-numbered shift register unit inputs a second clock signal;

[0048] a low voltage signal input terminal of each shift register unit inputs a low voltage signal; and

[0049] a high voltage signal input terminal of each shift register unit inputs a high voltage signal.

[0050] In the shift register unit and the gate drive device for liquid crystal display provided in the embodiments of the present invention, when the threshold voltages of the eighth thin film transistor and the ninth thin film transistor increase, the voltages applied on the gate electrodes of the eighth thin film transistor and the ninth thin film transistor also increase, such that it can enable the eighth thin film transistor and the ninth thin film transistor used to suppress the noise in the shift register unit to maintain turning on, therefore it guarantees the reliability of the shift register unit.

[0051] A further detailed description of the embodiments of the present invention is made below by the certain embodiments in connection with figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0052] The present invention will become more fully understood from the detailed description given hereinafter and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the present invention and wherein:

[0053] FIG. 1a illustrates a schematic diagram of a structure of the shift register unit of an embodiment of the present invention;

[0054] FIG. 1b illustrates a timing diagram of the input and output of the shift register unit of FIG. 1a;

[0055] FIG. 2a illustrates a schematic diagram of a structure of the shift register unit according to a first embodiment of the presenting invention;

[0056] FIG. 2b illustrates a timing diagram of the input and output of the shift register unit of FIG. 2a;

[0057] FIG. 3 illustrates a timing diagram of the input and output of the first shift register unit in the gate drive device for the liquid crystal display of an embodiment of the present invention;

[0058] FIG. 4a illustrates a schematic diagram of a structure of the shift register unit according to a second embodiment of the presenting invention;

[0059] FIG. 4b illustrates a timing diagram of the input and output of the shift register unit of FIG. 4a;

[0060] FIG. 5a illustrates a schematic diagram of a structure of a shift register unit according to a third embodiment of the presenting invention;

[0061] FIG. 5b illustrates a schematic diagram of a structure of a shift register unit according to a fourth embodiment of the presenting invention;

[0062] FIG. 5c illustrates a schematic diagram of a structure of a shift register unit according to a fifth embodiment of the presenting invention;

[0063] FIG. 6 illustrates a schematic diagram of a structure of the shift register unit according to a sixth embodiment of the presenting invention;

[0064] FIG. 7a illustrates a schematic diagram of a structure of the gate drive device for the liquid crystal display according to the presenting invention; and

[0065] FIG. 7b illustrates a timing diagram of the input and output of the gate drive device for the liquid crystal display of FIG. 7a.

DETAILED DESCRIPTION

[0066] FIG. 1a illustrates a schematic diagram of a structure of the shift register unit of an embodiment of the present invention, the shift register unit comprises: a first thin film transistor T101, a second thin film transistor T102, a third thin film transistor T103, a fourth thin film transistor T104, a fifth thin film transistor T105, a sixth thin film transistor T106, a seventh thin film transistor T107, an eighth thin film transistor T108, a ninth thin film transistor T109, and a tenth thin film transistor T110. A drain of the first thin film transistor T101 is connected to a first clock signal input terminal (CLKIN), a source thereof is connected to a signal output terminal (OUTPUT); a drain of the second thin film transistor T102 is connected to the source of T101, a gate thereof is connected to a reset signal input terminal (RESETIN), a source thereof is connected to a low voltage signal input terminal (VSSIN); a drain and a gate of the third thin film transistor T103 are both connected to a signal input terminal (INPUT-1), a source thereof is connected to the gate of the first thin film transistor T101; a drain of the fourth thin film transistor T104 is connected to the source of the third thin film transistor T103, a gate thereof is connected to the reset signal input terminal (RESETIN), a source thereof is connected to the low voltage signal input terminal (VSSIN); a drain of the fifth thin film transistor T105 is connected to a high voltage signal input terminal (VDDIN), a gate thereof is connected to the reset signal input terminal (RESETIN); a drain of the sixth thin film transistor T106 is connected to the source of the fifth thin film transistor T105, a gate thereof is connected to the source of the third thin film transistor T103, a source thereof is connected to the low voltage signal input terminal (VSSIN); a drain of the seventh thin film transistor T107 is connected to the high voltage signal input terminal (VDDIN), a gate thereof is connected to a frame start signal input terminal (STVIN), a source thereof is connected to the drain of the sixth thin film transistor T106; a gate of the eighth thin film transistor T108 is connected to the source of the fifth thin film transistor T105, a drain thereof is connected to the source of the first thin film transistor T101, a source thereof is connected to the low voltage signal input terminal (VSSIN); a drain of the ninth thin film transistor T109 is connected to the source of the third thin film transistor T103, a gate thereof is connected to the source of the fifth thin film transistor T105, a source thereof is connected to the low voltage signal input terminal (VSSIN); a drain and a gate of the tenth thin film transistor T110 are both connected to the source of the fifth thin film transistor T105, a source thereof is connected to the low voltage signal input terminal (VSSIN). The connection node for the source of the fifth thin film transistor T105, the drain of the sixth thin film transistor T106, the gate of the ninth thin film transistor T109, the gate of the tenth thin film transistor T110 and the gate of the eighth thin film transistor T108 is PD node. The connection node for the source of the third thin film transistor T103 and the gate of the sixth thin

film transistor T106 is PU node. Among each embodiment of the present invention, the eighth thin film transistor T108 and the ninth thin film transistor T109 are pull-down thin film transistors used to suppress the noise, and the PD node is a node connected to the pull-down thin film transistor.

[0067] It should be noted that, as for the thin film transistor in the field of liquid crystal display, there is no substantial difference between the drain and the source, thus the source of the thin film transistor mentioned in the embodiment of the present invention could be the drain of the thin film transistor, while the drain of the thin film transistor also could be the source of the thin film transistor.

[0068] FIG. 1b illustrates a timing diagram of the input and output of the shift register unit of FIG. 1a. The gate drive device for the liquid crystal display usually includes a plurality of shift register units, a first clock signal input terminal (CLKIN) of the odd-numbered shift register unit is inputted a first clock signal (CLK), a second clock signal (CLKB) is inputted to a first clock signal input terminal (CLKIN) of the even-numbered shift register unit, a frame start signal (STV) is inputted to a signal input terminal (INPUT-1) of the first shift register unit, the signal input terminal (INPUT-1) of the rest of the shift register units is inputted a output signal of an adjacent shift register unit of the previous stage, the frame start signal input terminal (STVIN) of each shift register unit is all inputted a frame start signal (STV), PD is a signal at PD node, PU is a signal at PU node, OUTPUT is a output signal of the shift register unit, RESET is a reset signal, the reset signal (RESET) is inputted into a reset signal input terminal (RESETIN), a high voltage signal (VDD) is inputted into a high voltage signal input terminal (VDDIN), a low voltage signal (VSS) is inputted into a low voltage signal input terminal (VSSIN). The high voltage signal (VDD) is a signal which always keeps high level, while the low voltage signal (VSS) is a signal which always keeps low level, both of them are not shown in FIG. 1b.

[0069] The operation principle of the shift register unit of an embodiment of the present invention is illustrated below in connection with FIG. 1a and FIG. 1b.

[0070] A part of the timing diagram shown in FIG. 1b is selected and is divided into six stages, in the first stage, the signal at PU node is at low level, the input signal (RESET) of the reset signal input terminal (RESETIN) is at low level, the fifth thin film transistor T105 and the sixth thin film transistor T106 are turned off, the output signal (OUTPUT) of the signal output terminal (OUT) is at low level. The input signal (STV) of the frame start signal input terminal (STVIN) is at high level, the seventh thin film transistor T107 is turned on and charge to the PD node, then the voltage of the PD node increases. When the size ratio between the seventh thin film transistor T107 and the tenth thin film transistor T110 meets the requirement, it is possible to make the PD node at high level.

[0071] In the second stage, the PU node is at low level, the frame start signal (STV) is at low level, the reset signal (RESET) is also low level, the fifth thin film transistor T105, the sixth thin film transistor T106 and the seventh thin film transistor T107 are turned off, the output signal (OUTPUT) at the signal output terminal (OUT) is at low level. The tenth thin film transistor T110 is turned on under the effect of the high level of PD node, the high level of PD node is released through the tenth thin film transistor T110, until the voltage at the PD node is equal to a threshold voltage of the tenth thin film transistor T110. In this way, the eighth thin film transistor

T108 and the ninth thin film transistor T109 suffer a bias voltage which is equal to or slightly higher than respective threshold voltage thereof. When fabricating the shift register unit, it should make the threshold voltage of the eighth thin film transistor T108 and the ninth thin film transistor T109 equal to or less than the threshold voltage of the tenth thin film transistor T110, at the same bias effect, the threshold voltage offsets of the eighth thin film transistor T108, the ninth thin film transistor T109 and the tenth thin film transistor T110 can maintain the same. When the threshold voltage of the eighth thin film transistor T108, the ninth thin film transistor T109 and the tenth thin film transistor T110 arise, the voltage at the PD node increases accordingly, which could make sure the eighth thin film transistor T108 and the ninth thin film transistor T109 being turned on.

[0072] In the third stage, the signal (INPUT) inputted from the signal input terminal (INPUT-1) is at high level, the third thin film transistor T103 is turned on, PU node is at high level, the first thin film transistor T101 and the sixth thin film transistor T106 are turned on, since the source of the sixth thin film transistor T106 is connected to the low voltage signal input terminal (VSSIN), the PD node becomes low level. When the PD node becomes low level, the eighth thin film transistor T108 and the ninth thin film transistor T109 are turned off. The reset signal (RESET) and the frame start signal (STV) are low level, the fifth thin film transistor T105 and the seventh thin film transistor T107 are turned off. The reset signal (RESET) is at low level, the second thin film transistor T102 and the fourth thin film transistor T104 are turned off. Since the first clock signal (CLK) is at low level, the signal (OUTPUT) outputted from the signal output terminal (OUT) is at low level.

[0073] In the fourth stage, the input signal (INPUT) of the signal input terminal (INPUT-1) is at low level, the third thin film transistor T103 is turned off. The reset signal (RESET) is at low level, the second thin film transistor T102, the fourth thin film transistor T104 and the fifth thin film transistor T105 are turned off, therefore the PU node maintains high level, the first thin film transistor T101 and the sixth thin film transistor T106 maintain turning on. The frame start signal (STV) is at low level, the seventh thin film transistor T107 is turned off, PD node maintains low level, the eighth thin film transistor T108 and the ninth thin film transistor T109 are turned off. The first clock signal (CLK) becomes high level, so the signal (OUTPUT) outputted from the signal output terminal (OUT) is at high level.

[0074] In the fifth stage, the signal (INPUT) inputted from the signal input terminal (INPUT-1) is at low level, the third thin film transistor T103 is turned off. The reset signal (RESET) is at high level, the second thin film transistor T102 and the fourth thin film transistor T104 are turned on. Because the sources of the second thin film transistor T102 and the fourth thin film transistor T104 are connected to the low voltage signal input terminal (VSSIN), the PU node becomes low level, the first thin film transistor T101 and the sixth thin film transistor T106 are turned off. The frame start signal (STV) is at low level, the seventh thin film transistor T107 is turned off. The reset signal (RESET) is at high level, the fifth thin film transistor T105 is turned on. Because the drain of the fifth thin film transistor T105 is connected to the high voltage signal input terminal (VDDIN), the sixth thin film transistor T106 is turned off, then the PD node becomes high level, the eighth thin film transistor T108 and the ninth thin film transistor T109 are turned on. Since the source of the eighth thin film

transistor T108 is connected to the low voltage signal input terminal (VSSIN), so the signal (OUTPUT) outputted from the signal output terminal (OUT) is at low level.

[0075] In the sixth stage, the signal (INPUT) inputted from the signal input terminal (INPUT-1) is at low level, the third thin film transistor T103 is turned off, PU node is maintained at low level, the first thin film transistor T101 and the sixth thin film transistor T106 are turned off. The reset signal (RESET) is at low level, the fifth thin film transistor T105 is turned off. The frame start signal (STV) is at low level, the seventh thin film transistor T107 is turned off. Since the fifth thin film transistor T105 and the seventh thin film transistor T107 are turned off, the PD node maintains high level, the tenth thin film transistor T110 is turned on, PD node releases the voltage through the tenth thin film transistor T110, and the voltage of the PD node drops, until the voltage at the PD node is equal to the threshold voltage of the tenth thin film transistor T110. The eighth thin film transistor T108 and the ninth thin film transistor T109 suffer a bias voltage which is equal to or higher than respective threshold voltage. Since the source of the eighth thin film transistor T108 is connected to the low voltage signal input terminal (VSSIN), the signal (OUTPUT) outputted from the signal output terminal (OUT) is at low level.

[0076] Among above six stages, in the third stage, the signal input terminal (INPUT-1) inputs high level, in the fourth stage the signal output terminal (OUT) outputs high level, by which a shift is finished, in the fifth stage, the reset signal input terminal (RESETIN) is at high level, by which the reset operation is performed, it makes the signal output terminal (OUT) outputs low level, after the sixth stage, the signal output terminal (OUT) maintains low level output, the voltage at PD node maintains a state after the sixth stage, until the timing sequences as shown in the first stage, the second stage, the third stage, the fourth stage and the fifth stage occur again. When the shift register unit is applied to the gate drive device for the liquid crystal display, the third, fourth, fifth stage could be regarded as a working time of the shift register unit, FIG. 1b shows only part of the timing diagram of the shift register unit, whenever the liquid crystal display displays one frame image, the shift register unit controlling the liquid crystal pixels of a certain row will output a high level, the signal input terminal (INPUT-1), the reset signal input terminal (RESETIN) and the first clock signal input terminal (CLKIN) will repeat once the input timing sequence of the third stage, the fourth stage and the fifth stage.

[0077] FIG. 2a illustrates a schematic diagram of a structure of the shift register unit according to a first embodiment of the presenting invention; FIG. 2b illustrates a timing diagram of the input and output of the shift register unit of FIG. 2a. The embodiment shown in FIG. 2a adds a first capacitor C1 on the basis of the shift register unit shown in FIG. 1a, the two ends of the first capacitor C1 are connected to the gate of the first thin film transistor T101 and the signal output terminal (OUT) respectively. The difference between the timing diagram shown in FIG. 2b and the timing diagram shown in FIG. 1b is: in the fourth stage, the level of the signal at PU node in FIG. 2b is higher than that of FIG. 1b due to the coupling effect of the first capacitor C1.

[0078] In the embodiment of FIG. 2a, the threshold voltage of the tenth thin film transistor is equal to or higher than the threshold voltages of the eighth thin film transistor and the ninth thin film transistor, which could make sure the eighth thin film transistor and the ninth thin film transistor being

turned on, it enables the eighth thin film transistor and the ninth thin film transistor to function to suppress the noise, therefore it guarantees the reliability of the shift register unit.

[0079] As for the shift register units in the gate drive device for the liquid crystal display other than the first shift register unit, the timing sequences of input and output of the shift register units are similar to the timing diagram of FIG. 2*b*. As for the first shift register unit of the gate drive device for the liquid crystal display, both the frame start signal (STV) and the signal (INPUT) inputted from the signal input terminal (INPUT-1) are high level, FIG. 3 illustrates a timing diagram of the input and output of the first shift register unit in the gate drive device for the liquid crystal display of an embodiment of the present invention, as for the first shift register unit, the first stage, the second stage are overlapped with the third stage and the fourth stage respectively, it requires that the timing diagrams of the first stage and the second stage are replaced by those of the third stage and the fourth stage respectively, that is, the first stage and the second stage of FIG. 2*b* is not appearing.

[0080] FIG. 4*a* illustrates a schematic diagram of a structure of the shift register unit according to a second embodiment of the present invention; FIG. 4*b* illustrates a timing diagram of the input and output of the shift register unit module of FIG. 4*a*. The shift register unit shown in FIG. 4*a* adds a second capacitor C2 on the basis of the shift register unit shown in FIG. 2*a*, the two ends of the second capacitor C2 are connected to the source of the fifth thin film transistor T105 and the low voltage signal input terminal (VSSL) respectively. When the thin film transistor is turned off, the thin film transistor could be treated as a resistor, but the thin film transistor itself would produce a slight leakage, by adding the second capacitor C2, it could make the drop speed of the voltage at PD node slow down, wherein the voltage at PD node is dropped due to the leakage of the eighth thin film transistor T108, the ninth thin film transistor T109 and the tenth thin film transistor T110 which are connected to the PD node. Furthermore, as shown in FIG. 4*b*, because of the addition of the second capacitor, it makes the voltage at PD node in the first, fifth stages increase slowly, and makes the voltage at PD node in the second, sixth stages drop slowly.

[0081] FIG. 5*a* illustrates a schematic diagram of a structure of the shift register unit according to a third embodiment of the present invention, wherein as shown in FIG. 5*a*, the shift register unit comprises: a third thin film transistor T103 for controlling a level at a pull-up node PU under a control of a first control signal; a first thin film transistor T101 for outputting a first clock signal to a signal output terminal OUT under a control of a level at the pull-up node PU; a control unit for controlling a level at a pull-down node PD; a second level output unit for outputting a second level signal to the signal output terminal OUT under a control of the level at the pull-down node PD; a tenth thin film transistor T110 for inputting a first level signal to the pull-down node PD under a control of the level at the pull-down node PD; and an eleventh thin film transistor T111 for inputting a first level signal to the pull-down node PD under a control of a level at the signal output terminal OUT.

[0082] Optionally, FIGS. 5*b* and 5*c* show the schematic diagram of the structures of the shift register units according to the fourth and fifth embodiments of the present invention respectively, in the shift register units, a drain of the first thin film transistor T101 is connected to a first clock signal input terminal CLKIN, a source thereof is connected to the signal

output terminal OUT, and a gate thereof is connected to the pull-up node PU; a drain of the third thin film transistor T103 is connected to a signal input terminal INPUT-1, a source thereof is connected to the pull-up node PU, and a gate thereof is connected to the signal input terminal INPUT-1 or a second clock signal input terminal CLKB; a drain and gate of the tenth thin film transistor T110 are both connected to the pull-down node PD, a source thereof is connected to a first low voltage signal input terminal LVGL; a drain of the eleventh thin film transistor T111 is connected to the pull-down node PD, a source thereof is connected to the first low voltage signal input terminal LVGL, and a gate thereof is connected to the signal output terminal OUT.

[0083] Optionally, the shift register unit further comprises a first level output unit for outputting the first level signal to the pull-up node PU under the control of the level at the pull-down node PD.

[0084] Optionally, the second level output unit comprises an eighth thin film transistor T108 having a drain connected to the signal output terminal OUT, a source connected to a second low voltage signal input terminal VGL, and a gate connected to the pull-down node PD, wherein a threshold voltage of the eighth thin film transistor is equal to or less than a threshold voltage of the tenth thin film transistor.

[0085] Optionally, the first level output unit comprises a ninth thin film transistor T109 having a drain connected to the pull-up node PU, a gate connected to the pull-down node PD, and a source connected to a first low voltage signal input terminal LVGL, wherein a threshold voltage of the ninth thin film transistor is equal to or less than a threshold voltage of the tenth thin film transistor.

[0086] Optionally, the control unit comprises: a fifth thin film transistor T105 having a drain connected to a high voltage signal input terminal VDDIN or a second clock signal input terminal CLKB, a gate connected to a reset signal input terminal RESETIN or the second clock signal input terminal CLKB, and a source connected to the pull-down node PD.

[0087] Optionally, the control unit further comprises: a seventh thin film transistor T107 having a drain connected to a high voltage signal input terminal VDDIN or a second clock signal input terminal CLKB, a gate connected to a frame start signal input terminal STV or the second clock signal input terminal CLKB, and a source connected to the pull-down node PD.

[0088] Optionally, the control unit further comprises: a second thin film transistor T102 having a drain connected to the signal output terminal OUT, a source connected to a second low voltage signal input terminal VGL, a gate connected to a reset signal input terminal RESETIN or a second clock signal input terminal CLKB.

[0089] Optionally, the shift register unit further comprising: a fourth thin film transistor T104 having a drain connected to the pull-up node PU, a source connected to a first low voltage signal input terminal LVGL, a gate connected to a reset signal input terminal RESETIN or the pull-down node PD.

[0090] Optionally, the shift register unit further comprises: a sixth thin film transistor T106 having a drain connected to the pull-down node PD, a source connected to a first low voltage signal input terminal LVGL, a gate connected to a signal input terminal INPUT-1 or the pull-up node PU.

[0091] Optionally, the shift register unit further comprises a first capacitor C1, whose two ends are connected to a gate of the first thin film transistor T101 and the signal output terminal OUT, respectively.

[0092] Optionally, the shift register unit further comprises a second capacitor C2, whose two ends are connected to the pull-down node PD and the second low voltage signal input terminal VGL, respectively.

[0093] Optionally, when the eighth thin film transistor is a depletion mode TFT, the first level signal and the second level signal are a low level signal, the first level signal is less than the second level signal, an absolute value of a difference between the first level signal and the second level signal is larger than an absolute value of a depletion threshold voltage of the eighth thin film transistor.

[0094] Although in the above embodiments, all the Thin Film Transistors (TFTs) in the shift register unit are N type TFTs, it is possible that all the TFTs are P type TFTs, or some of them are N type TFTs and others are P type TFTs as long as levels of respective signals are adjusted accordingly. In addition, the TFTs in the shift register unit can be enhancement mode TFTs or depletion mode TFTs. For the depletion mode TFTs, the first level signal is less than the second level signal, an absolute value of a difference between the first level signal and the second level signal is larger than an absolute value of a threshold voltage of the depletion mode TFTs.

[0095] FIG. 6 shows a schematic diagram of a structure of a shift register unit according to the sixth embodiment of the present invention. The structural difference between the shift register unit shown in FIG. 6 and shown in FIG. 2a is: in FIG. 6, it adds an eleventh thin film transistor T111, a drain of the eleventh thin film transistor T111 is connected to the source of the fifth thin film transistor T105, a source thereof is connected to low voltage signal input terminal (VSSIN), the gate thereof is connected to the signal output terminal (OUT); in FIG. 6, the gate of the sixth thin film transistor T106 is connected to the signal input terminal (INPUT-1), while in FIG. 4a, the gate of the sixth thin film transistor T106 is connected to the source of the third thin film transistor T103. By the addition of the eleventh thin film transistor T111, the shift register unit shown in FIG. 6 could quickly pull down the voltage of PD node, therefore it makes the eighth thin film transistor T108 and the ninth thin film transistor T109 to be turned off as quickly as possible, which makes the voltage of PU node becomes higher, it would benefit for cutting short the ascent time of the signal outputted from the signal output terminal (OUT). The operation principle of the shift register unit shown in FIG. 6 is similar to the operation principle of the shift register unit shown in FIG. 2a, the details of that is no longer repeated herein.

[0096] The structural difference between the shift register unit shown in FIG. 6 and that shown in FIG. 2a is further in that: the shift register unit shown in FIG. 6 adds a first capacitor C1 and a second capacitor C2, the first capacitor C1 and the second capacitor C2 in the shift register unit shown in FIG. 6 play the same role as those in the shift register unit shown in FIG. 4a.

[0097] FIG. 7a illustrates a schematic diagram of a structure of the gate drive device for the liquid crystal display according to the presenting invention; FIG. 7b illustrates a timing diagram of the input and output of the gate drive device for the liquid crystal display of FIG. 7a. STV is a frame start signal, which is inputted to the signal input terminal (INPUT-1) of the first shift register unit, a high voltage signal is

inputted to the high voltage signal input terminal (VDDIN) of each shift register unit, a low voltage signal is inputted to the low voltage signal input terminal (VSSIN) of each shift register unit, a first clock signal (CLK) is inputted into the first clock signal input terminal (CLKIN) of the odd numbered shift register unit, a second clock signal (CLKB) is inputted into the first clock signal input terminal (CLKIN) of the even numbered shift register unit, except for the first shift register unit and the last shift register unit, the signal output terminal of each shift register unit is all connected to the reset signal input terminal (RESETIN) of previous adjacent shift register unit and the signal input terminal (INPUT-1) of the next adjacent shift register unit, the signal output terminal (OUT) of the first shift register unit is only connected to the signal input terminal (INPUT-1) of the second shift register unit, the output terminal (OUT) of the last shift register unit (e.g. the (n+1)th shift register unit shown in FIG. 7a) is connected to the reset signal input terminal (RESETIN) of the adjacent n^{th} shift register unit and the reset signal input terminal (RESETIN) of itself, respectively. The high voltage signal (VDD) and the low voltage signal (VSS) are not shown in FIG. 7b, the high voltage signal (VDD) is a signal always keeping at high level, the low voltage signal (VSS) is a signal always keeping at low level. The liquid crystal display with thin film transistor adopts a scan manner of row by row, the gates of thin film transistors connected in series with the liquid crystal pixels in the same row are all connected to the same shift register unit, the shift register unit of the gate drive device for liquid crystal display can control the turning on and off of all the thin film transistors in the same row. The particular principle of the gate drive device for liquid crystal display in FIG. 7a is: assuming there are n rows of liquid crystal pixels in the panel of the liquid crystal display, with reference to the timing diagram of FIG. 7b, in the first stage, the frame start signal is inputted to the signal input terminal (INPUT-1) of the first shift register unit; in the second stage, the signal output terminal (OUT) of the first shift register unit outputs a high level signal (OUTPUT1), at the same time the high level signal (OUTPUT1) is inputted to the signal input terminal (INPUT-1) of the second shift register unit; in the third stage, the signal output terminal (OUT) of the second shift register unit outputs a high level signal (OUTPUT2), thereafter each shift register unit sequentially outputs a high level signal, which is used to control the turning on of the thin film transistors of the same row connected with the shift register unit, the principle is the same as that of the second and the third stage; in the fourth stage, the nth shift register unit outputs a high level signal (OUTPUTn), meanwhile the high level signal (OUTPUTn) outputted from the nth shift register unit is used as the input signal of the signal input terminal (INPUT-1) of the (n+1)th shift register unit; in the fifth stage, the (n+1)th shift register unit outputs a high level signal (OUTPUTn+1), which is not used to drive the load, that is, the (n+1)th shift register unit is not responsible for driving the thin film transistors controlling one row liquid crystal pixels, the high level signal (OUTPUTn+1) outputted therefrom is only used as the reset signal of the nth shift register unit and itself.

[0098] In FIG. 7a, the last shift register unit, i.e. the (n+1)th shift register unit is not used to driving the thin film transistor, and could be considered as a redundant shift register unit. The gate drive device of FIG. 7a only includes one redundant shift register unit, in practice, which could include more redundant

shift register units, each of which could be combined to guarantee the gate drive device for liquid crystal display being reset more reliably.

[0099] The respective shift register unit of FIG. 7a could be the shift register units shown in FIG. 1, FIG. 2a, FIG. 4a, FIGS. 5a-5c or FIG. 6.

[0100] In the shift register unit and the gate drive device for liquid crystal display provided in the embodiment of the present invention, the threshold voltage of the tenth thin film transistor is equal to or higher than the threshold voltage of the eighth thin film transistor and the ninth thin film transistor, which could make sure the eighth thin film transistor and the ninth thin film transistor being turned on, it enables the eighth thin film transistor and the ninth thin film transistor to function as pull-down thin film transistor so as to suppress the noise, therefore it guarantees the reliability of the shift register unit.

[0101] Finally, it should be noted that, the above embodiments are used only to explain the technical solution of the embodiments of the present invention, not to limit the invention; although the embodiments of the present invention has been described in details with reference to the preferred embodiments thereof, it would be obvious to those skilled in the art that he can still make variations or equal replacement to the technical solutions of the embodiments of the present invention, such variations or equal replacements are not to be regarded as rendering the nature of the amended technical solutions departing from the spirit and scope of the invention.

What is claimed is:

1. A shift register unit, comprising:

a third thin film transistor for controlling a level at a pull-up node under a control of a first control signal;

a first thin film transistor for outputting a first clock signal to a signal output terminal under a control of a level at the pull-up node;

a control unit for controlling a level at a pull-down node;

a second level output unit for outputting a second level signal to the signal output terminal under a control of the level at the pull-down node;

a tenth thin film transistor for inputting a first level signal to the pull-down node under a control of the level at the pull-down node; and

an eleventh thin film transistor for inputting a first level signal to the pull-down node under a control of a level at the signal output terminal.

2. The shift register unit of claim 1, wherein

a drain of the first thin film transistor is connected to a first clock signal input terminal, a source thereof is connected to the signal output terminal, and a gate thereof is connected to the pull-up node;

a drain of the third thin film transistor is connected to a signal input terminal, a source thereof is connected to the pull-up node, and a gate thereof is connected to the signal input terminal or a second clock signal input terminal;

a drain and gate of the tenth thin film transistor are both connected to the pull-down node, a source thereof is connected to a first low voltage signal input terminal;

a drain of the eleventh thin film transistor is connected to the pull-down node, a source thereof is connected to the first low voltage signal input terminal, and a gate thereof is connected to the signal output terminal.

3. The shift register unit of claim 1, further comprising a first level output unit for outputting the first level signal to the pull-up node under the control of the level at the pull-down node.

4. The shift register unit of claim 1, wherein the second level output unit comprises an eighth thin film transistor having a drain connected to the signal output terminal, a source connected to a second low voltage signal input terminal, and a gate connected to the pull-down node, wherein a threshold voltage of the eighth thin film transistor is equal to or less than a threshold voltage of the tenth thin film transistor.

5. The shift register unit of claim 3, wherein the first level output unit comprises a ninth thin film transistor having a drain connected to the pull-up node, a gate connected to the pull-down node, and a source connected to a first low voltage signal input terminal, wherein a threshold voltage of the ninth thin film transistor is equal to or less than a threshold voltage of the tenth thin film transistor.

6. The shift register unit of claim 1, wherein the control unit comprises:

a fifth thin film transistor having a drain connected to a high voltage signal input terminal or a second clock signal input terminal, a gate connected to a reset signal input terminal or the second clock signal input terminal, and a source connected to the pull-down node.

7. The shift register unit of claim 1, wherein the control unit further comprises:

a seventh thin film transistor having a drain connected to a high voltage signal input terminal or a second clock signal input terminal, a gate connected to a frame start signal input terminal or the second clock signal input terminal, and a source connected to the pull-down node.

8. The shift register unit of claim 1, wherein the control unit further comprises:

a second thin film transistor having a drain connected to the signal output terminal, a source connected to a second low voltage signal input terminal, a gate connected to a reset signal input terminal or a second clock signal input terminal.

9. The shift register unit of claim 1, further comprising:

a fourth thin film transistor having a drain connected to the pull-up node, a source connected to a first low voltage signal input terminal, a gate connected to a reset signal input terminal or the pull-down node.

10. The shift register unit of claim 1, further comprising:

a sixth thin film transistor having a drain connected to the pull-down node, a source connected to a first low voltage signal input terminal, a gate connected to a signal input terminal or the pull-up node.

11. The shift register unit of claim 1, further comprising a first capacitor, whose two ends are connected to a gate of the first thin film transistor and the signal output terminal, respectively.

12. The shift register unit of claim 11, further comprising a second capacitor, whose two ends are connected to the pull-down node and the second low voltage signal input terminal, respectively.

13. The shift register unit of claim 4, wherein the first level signal and the second level signal are a low level signal, the first level signal is less than the second level signal, an absolute value of a difference between the first level signal and the second level signal is larger than an absolute value of a depletion threshold voltage of the eighth thin film transistor.

14. A gate drive device for a liquid crystal display, comprising a plurality of shift register units according to claim 1, deposited on an array substrate of the liquid crystal display; wherein except for a first shift register unit and a last shift register unit, a signal output terminal of each of the shift register units is connected to a signal input terminal of a next adjacent shift register unit and a reset signal input terminal of a previous adjacent shift register unit, a signal output terminal of the first shift register unit is connected to a signal input terminal of a second shift register unit, a signal output terminal of the last shift register unit is connected to a reset signal input terminal of a previous adjacent shift register unit and a reset signal input terminal of itself;

a signal input terminal of the first shift register unit inputs a frame start signal;

a first clock signal input terminal of an odd-numbered shift register unit inputs a first clock signal; a first clock signal input terminal of an even-numbered shift register unit inputs a second clock signal;

a low voltage signal input terminal of each shift register unit inputs a low voltage signal; and

a high voltage signal input terminal of each shift register unit inputs a high voltage signal.

15. The gate drive device for a liquid crystal display of claim 14, in the shift register unit,

a drain of the first thin film transistor is connected to a first clock signal input terminal, a source thereof is connected to the signal output terminal, and a gate thereof is connected to the pull-up node;

a drain of the third thin film transistor is connected to a signal input terminal, a source thereof is connected to the pull-up node, and a gate thereof is connected to the signal input terminal or a second clock signal input terminal;

a drain and gate of the tenth thin film transistor are both connected to the pull-down node, a source thereof is connected to a first low voltage signal input terminal;

a drain of the eleventh thin film transistor is connected to the pull-down node, a source thereof is connected to the

first low voltage signal input terminal, and a gate thereof is connected to the signal output terminal.

16. The gate drive device for a liquid crystal display of claim 14, wherein the shift register unit further comprises a first level output unit for outputting the first level signal to the pull-up node under the control of the level at the pull-down node.

17. The gate drive device for a liquid crystal display of claim 14, in the shift register unit, the second level output unit comprises an eighth thin film transistor having a drain connected to the signal output terminal, a source connected to a second low voltage signal input terminal, and a gate connected to the pull-down node, wherein a threshold voltage of the eighth thin film transistor is equal to or less than a threshold voltage of the tenth thin film transistor.

18. The gate drive device for a liquid crystal display of claim 14, in the shift register unit, wherein the first level output unit comprises a ninth thin film transistor having a drain connected to the pull-up node, a gate connected to the pull-down node, and a source connected to a first low voltage signal input terminal, wherein a threshold voltage of the ninth thin film transistor is equal to or less than a threshold voltage of the tenth thin film transistor.

19. The gate drive device for a liquid crystal display of claim 14, in the shift register unit, wherein the control unit comprises:

a fifth thin film transistor having a drain connected to a high voltage signal input terminal or a second clock signal input terminal, a gate connected to a reset signal input terminal or the second clock signal input terminal, and a source connected to the pull-down node.

20. The gate drive device for a liquid crystal display of claim 14, in the shift register unit, wherein the control unit further comprises:

a seventh thin film transistor having a drain connected to a high voltage signal input terminal or a second clock signal input terminal, a gate connected to a frame start signal input terminal or the second clock signal input terminal, and a source connected to the pull-down node.

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摘要(译)

公开了一种用于液晶显示器的移位寄存器单元和栅极驱动装置。第十薄膜晶体管的栅极和漏极都连接到第五薄膜晶体管的源极，其源极连接到低压信号输入端子，第八薄膜晶体管和第九薄膜晶体管的阈值电压是等于或小于第十薄膜晶体管的阈值电压。本发明提供的移位寄存器单元和液晶显示器的栅极驱动装置，能够使用于抑制移位寄存器单元中的噪声的薄膜晶体管保持导通，因此保证了移位寄存器单元的可靠性。。

