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(54) **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING THE SAME**

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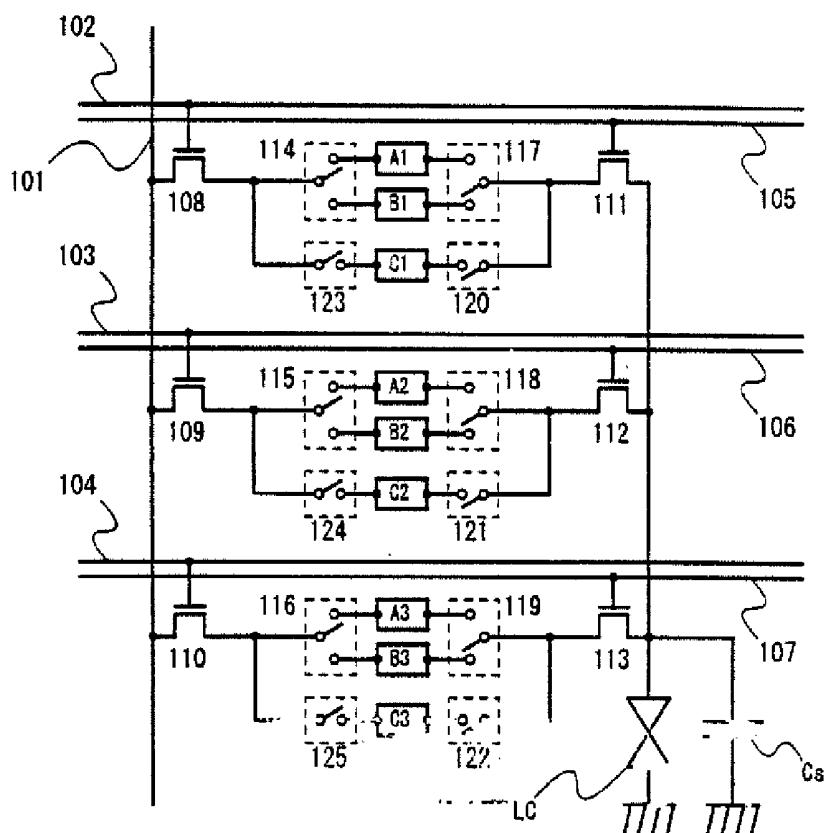
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(57) **ABSTRACT**

A liquid crystal display device with low power consumption is provided by using a driver circuit and a pixel that have novel circuit structures. In a liquid crystal display device using  $n$  ( $n$  is a natural number and satisfies  $n \geq 2$ ) bit digital video signals to display an image,  $n \times m$  ( $m$  is a natural number) memory circuits and  $n \times k$  ( $k$  is a natural number) non-volatile memory circuits are provided in each pixel, thereby giving the device a function of storing  $m$  frames of digital video signals in the memory circuits and a function of storing  $k$  frames of digital video signals in the non-volatile memory circuits. Once stored in the memory circuits, the digital video signals are repeatedly read out for every new frame to display a still image, so that driving of a source signal line driver circuit can be stopped during still image display. Moreover, digital video signals stored in the non-volatile memory circuits are kept stored after power supply is shut off and hence the image of the stored data can immediately be displayed next time the display device is turned on.



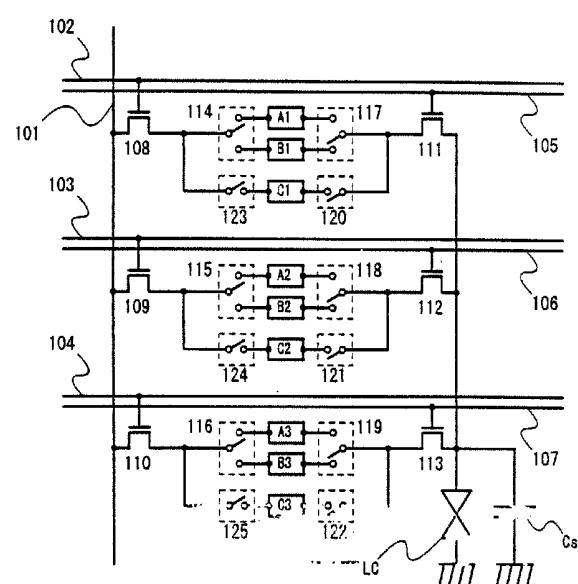


FIG. 1

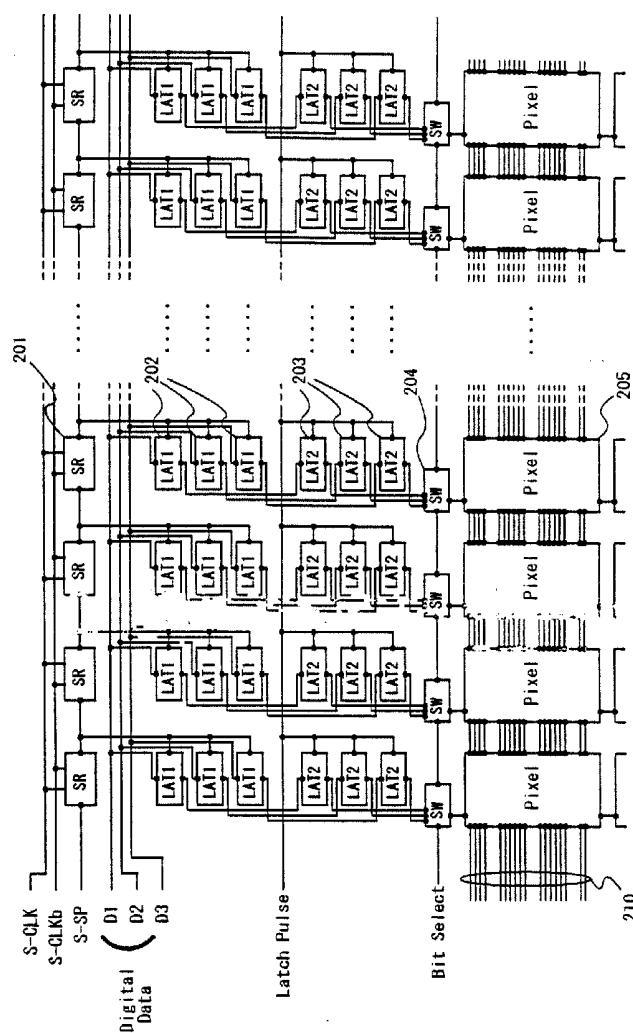
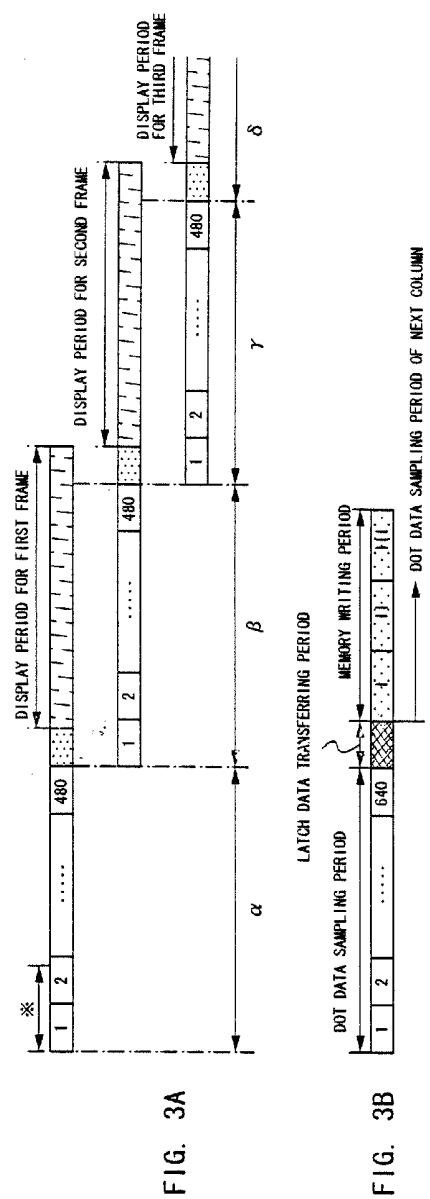


FIG. 2



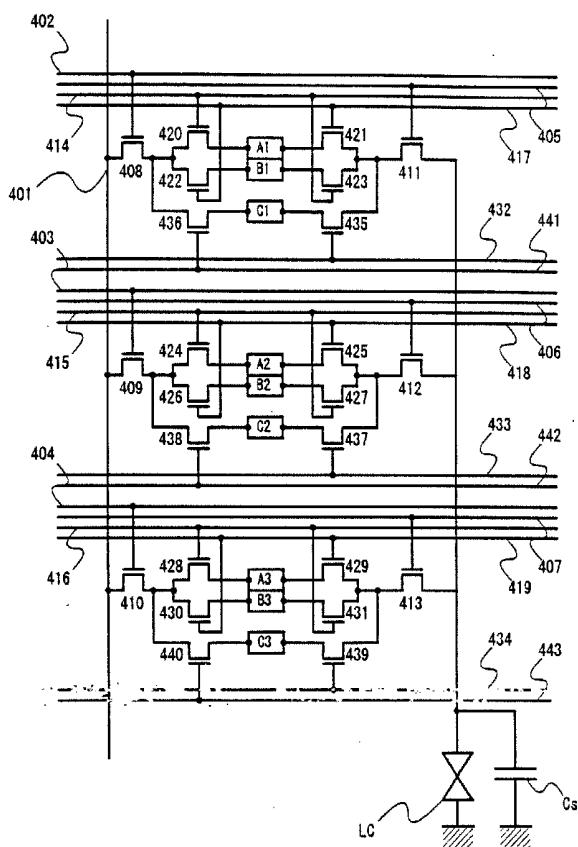
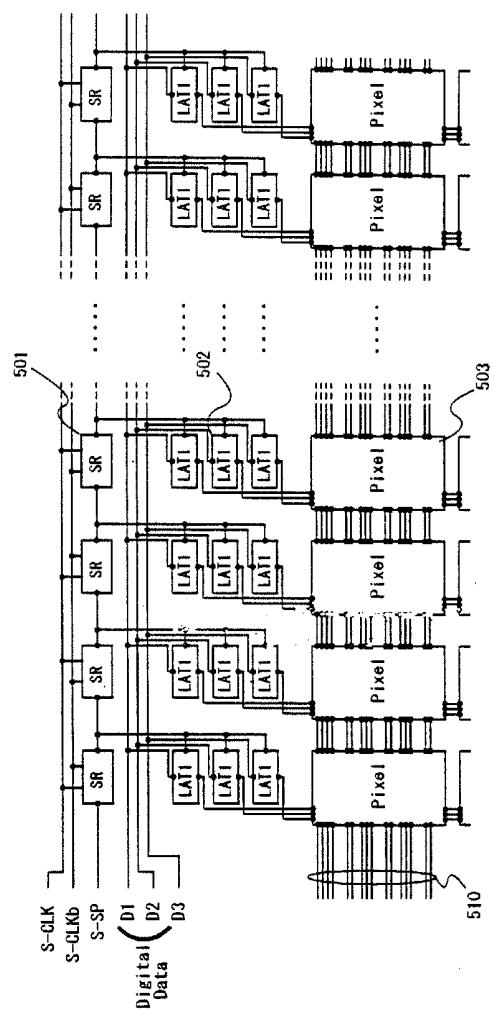


FIG. 4



5  
6

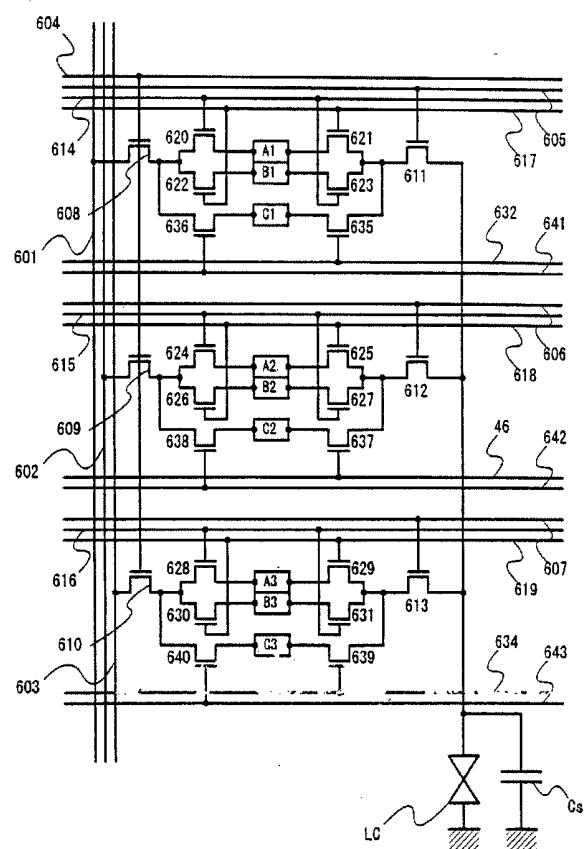


FIG. 6

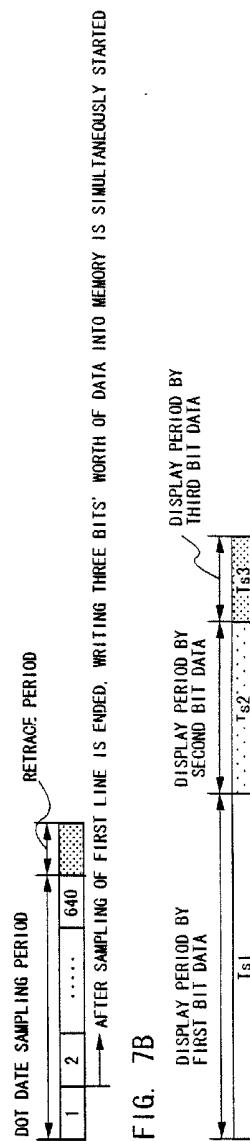
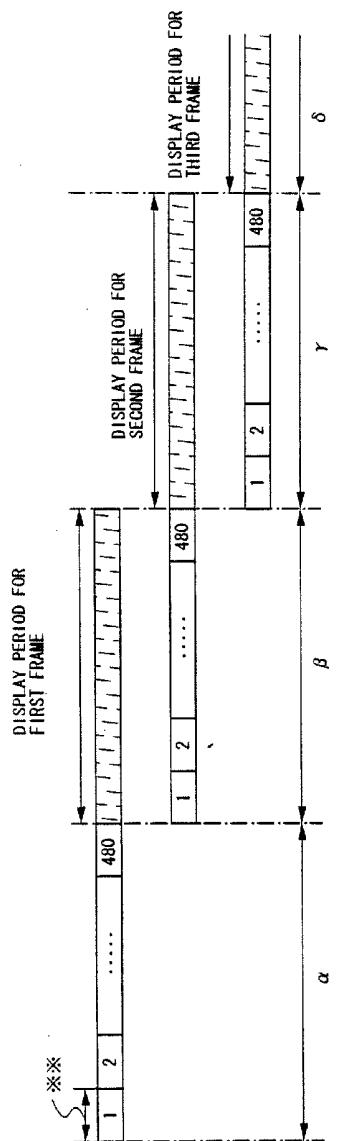


FIG. 7C

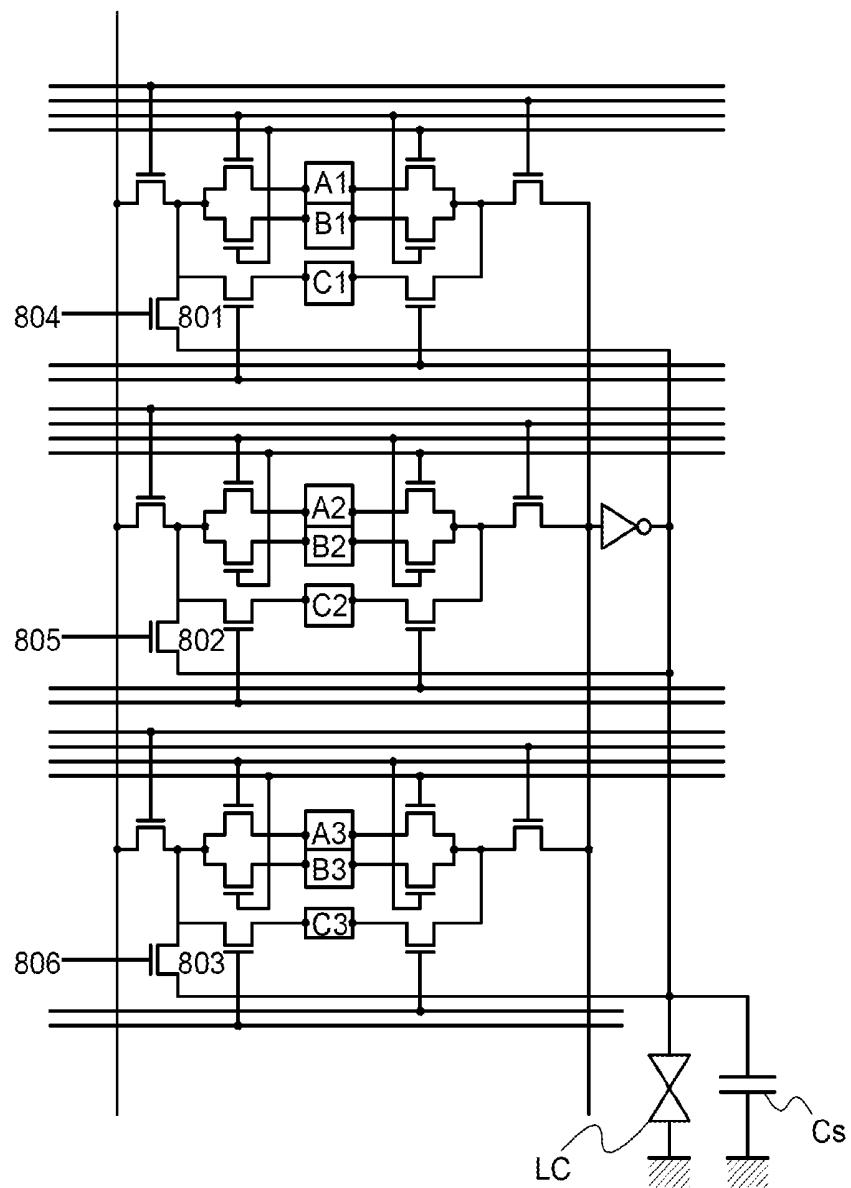
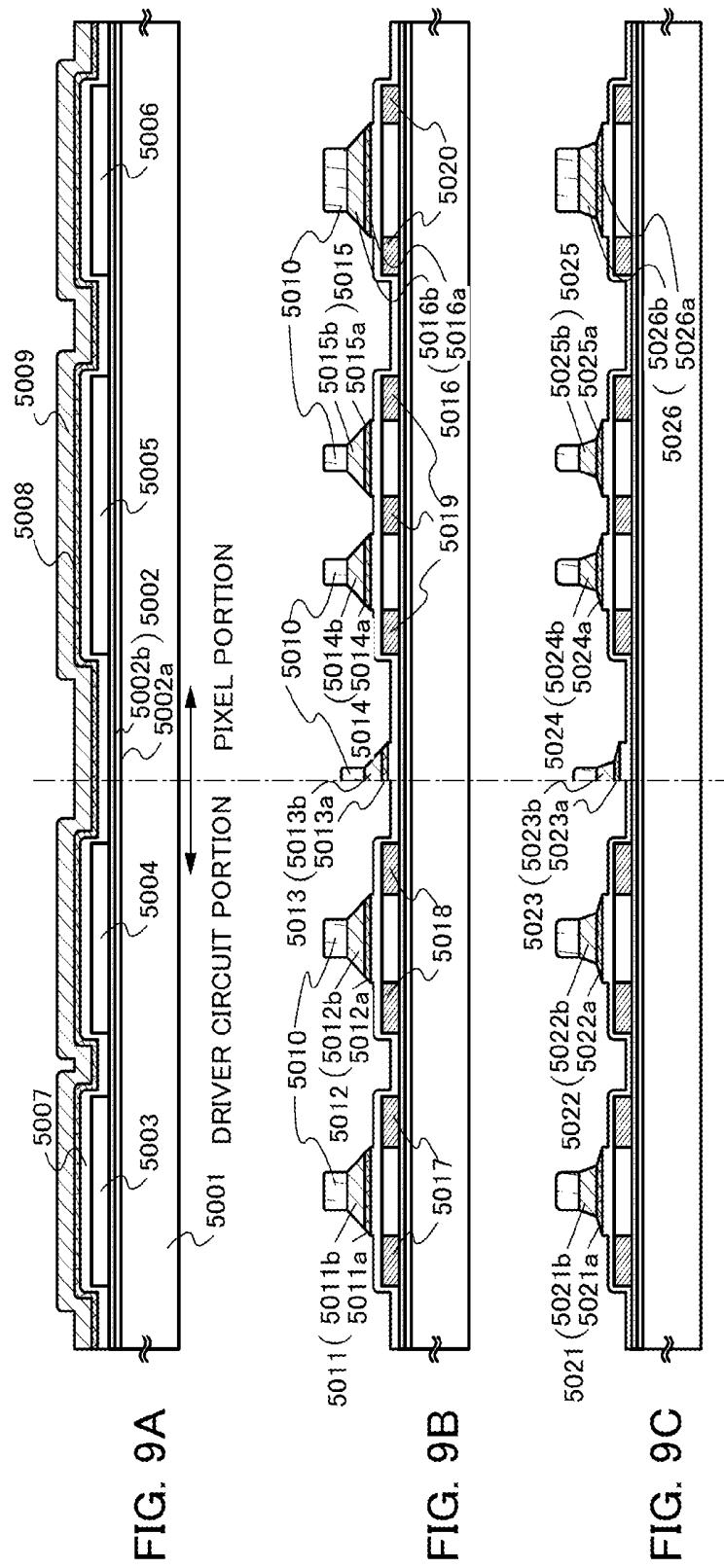
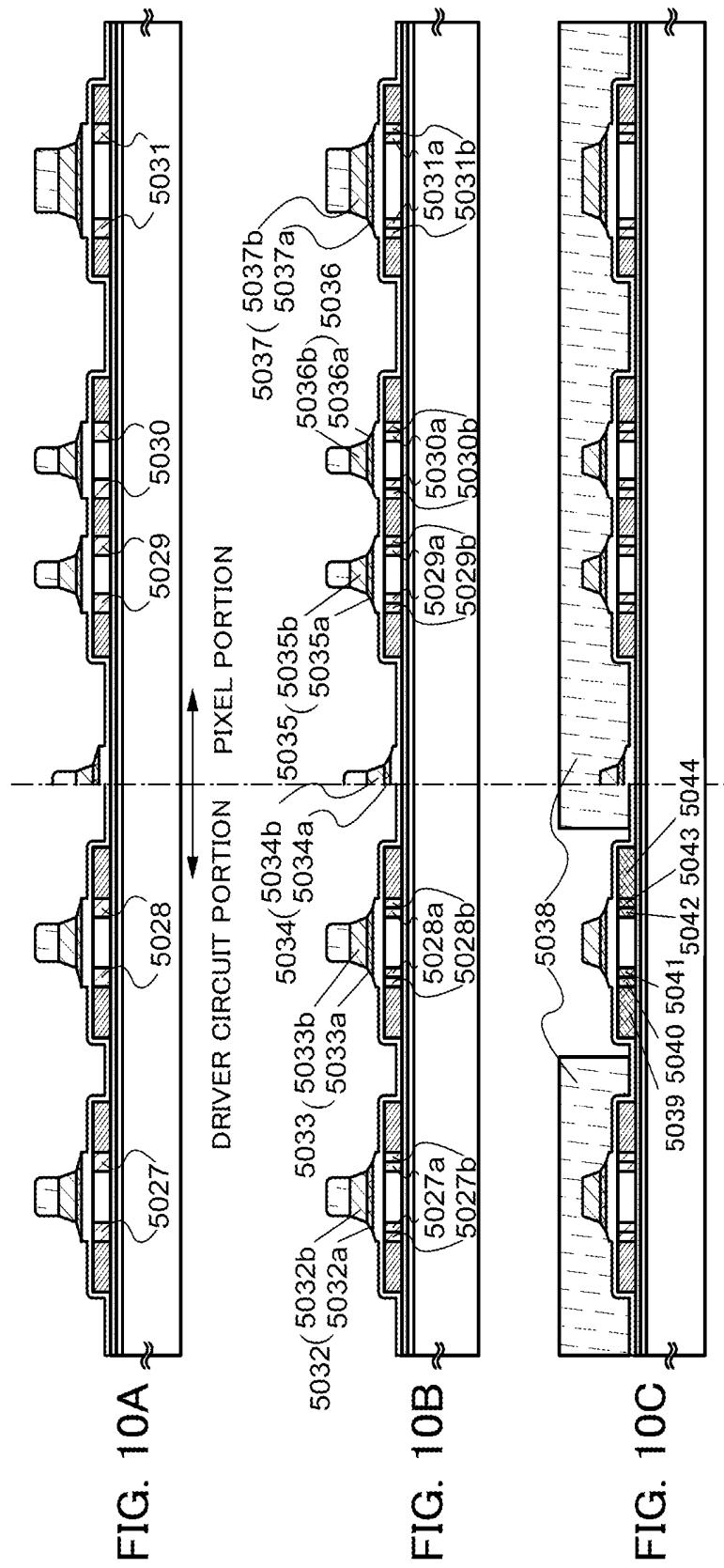
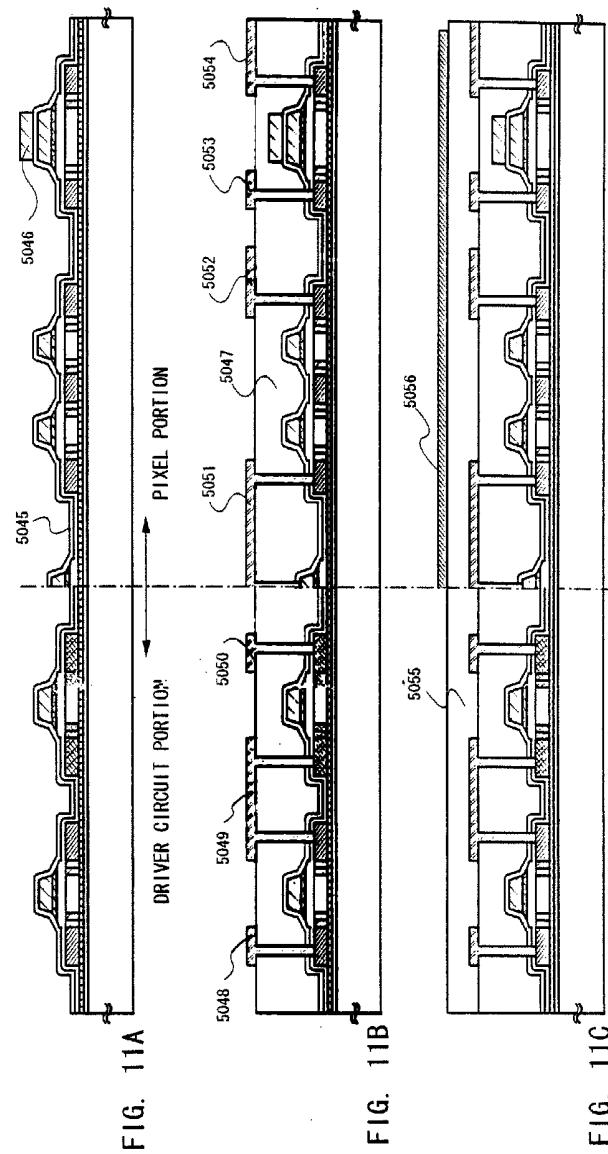


FIG. 8







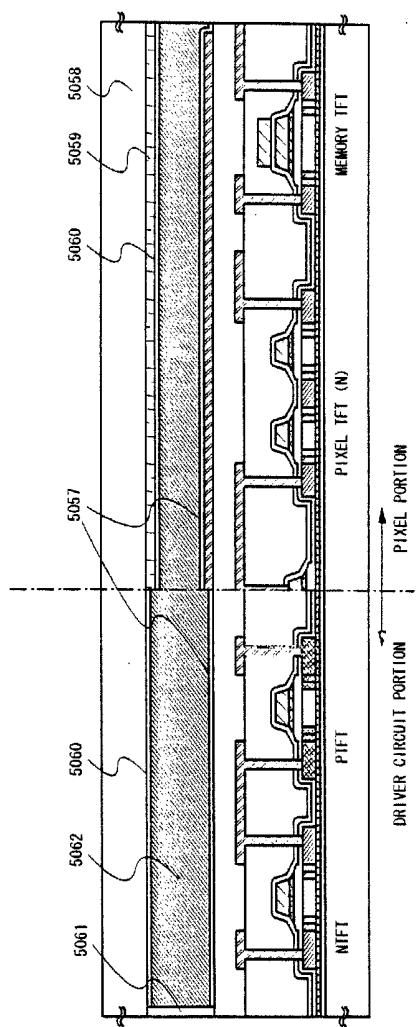


FIG. 12

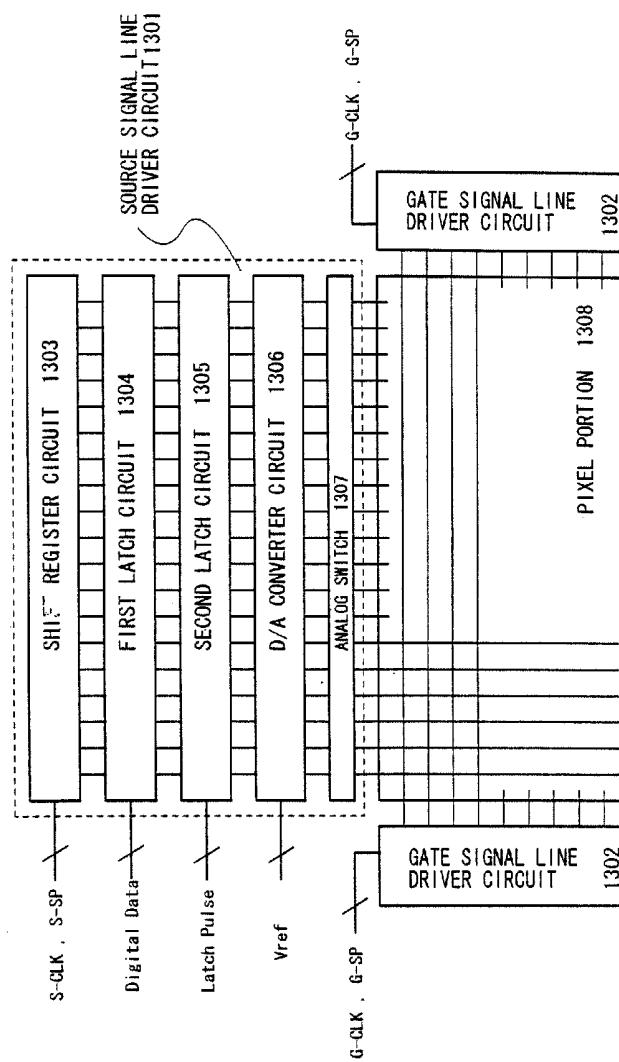


FIG. 13

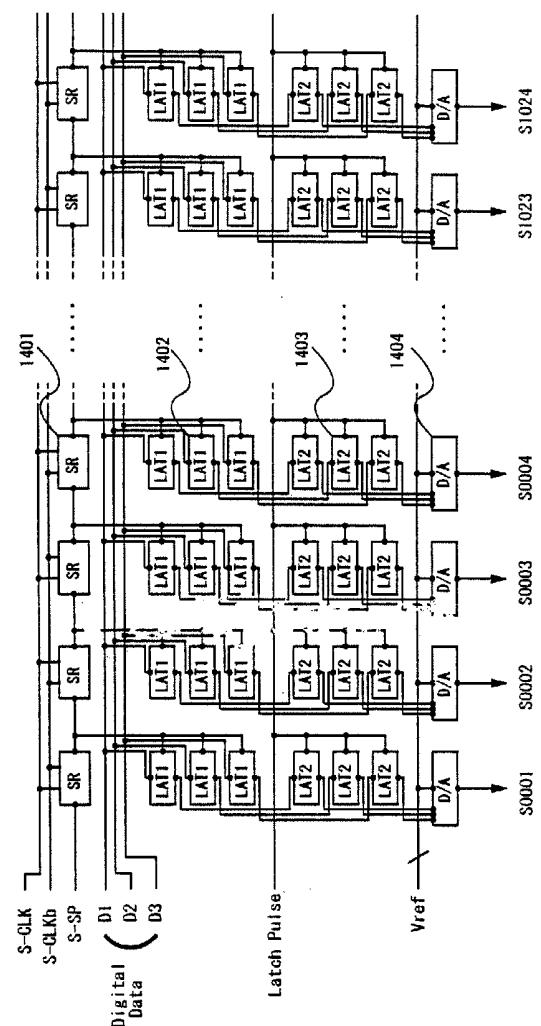
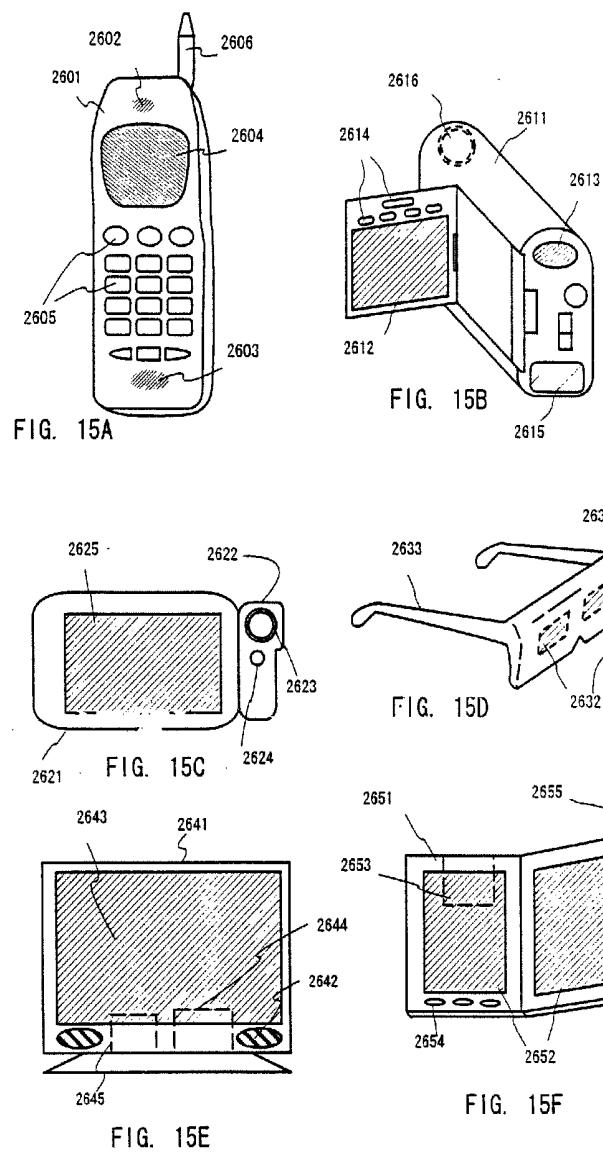


FIG. 14



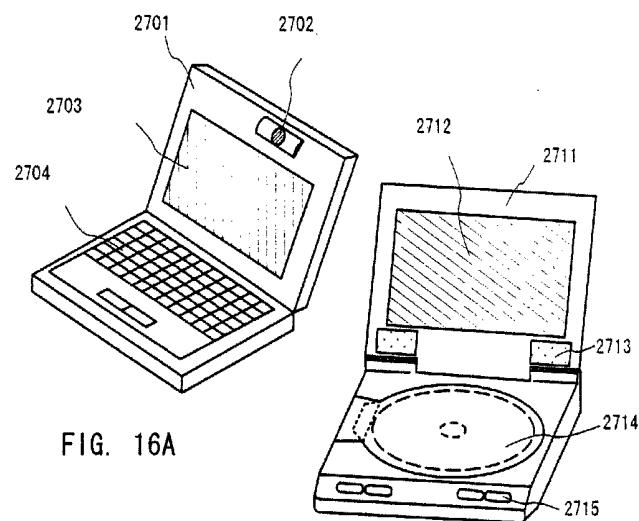


FIG. 16B

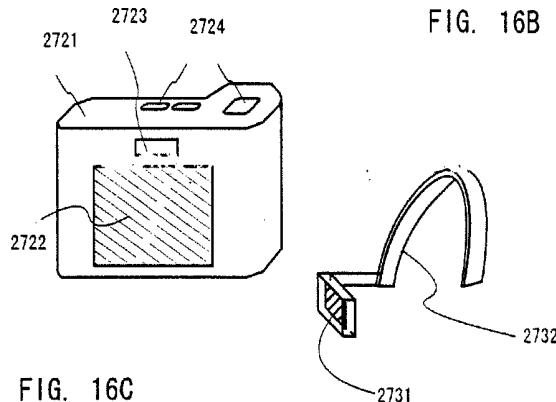


FIG. 16C

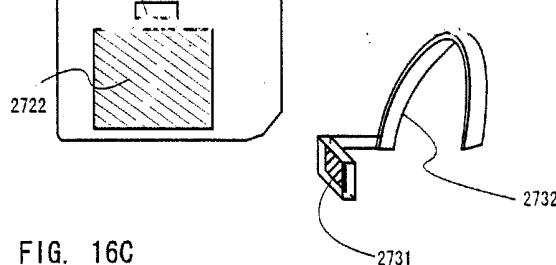
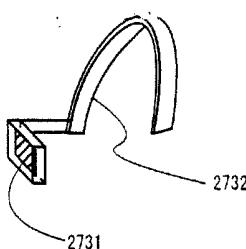


FIG. 16D



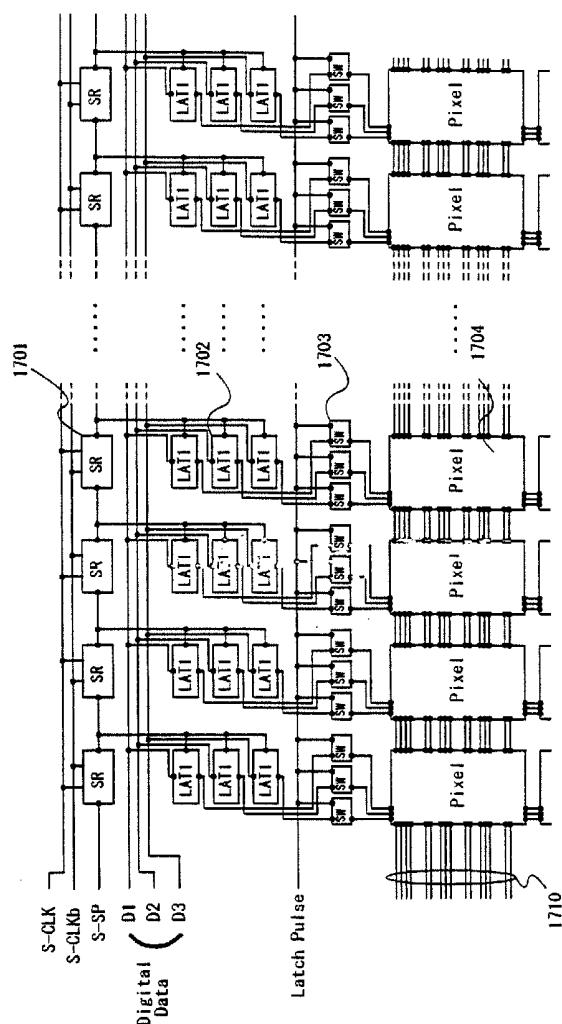


FIG. 17

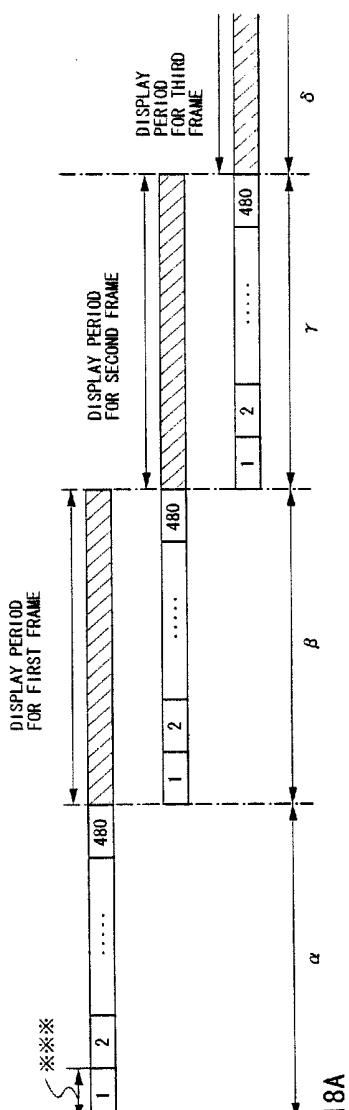


FIG. 18A

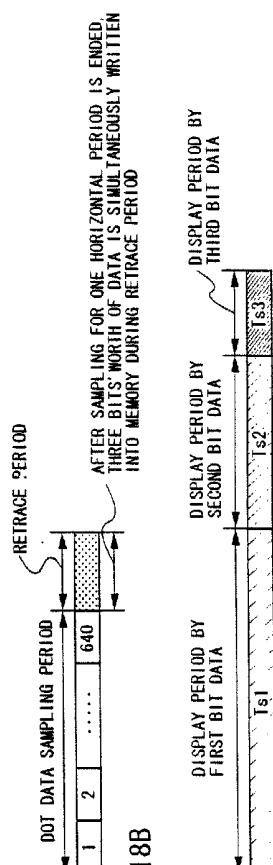


FIG. 18B

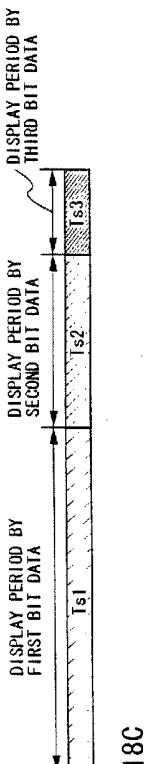
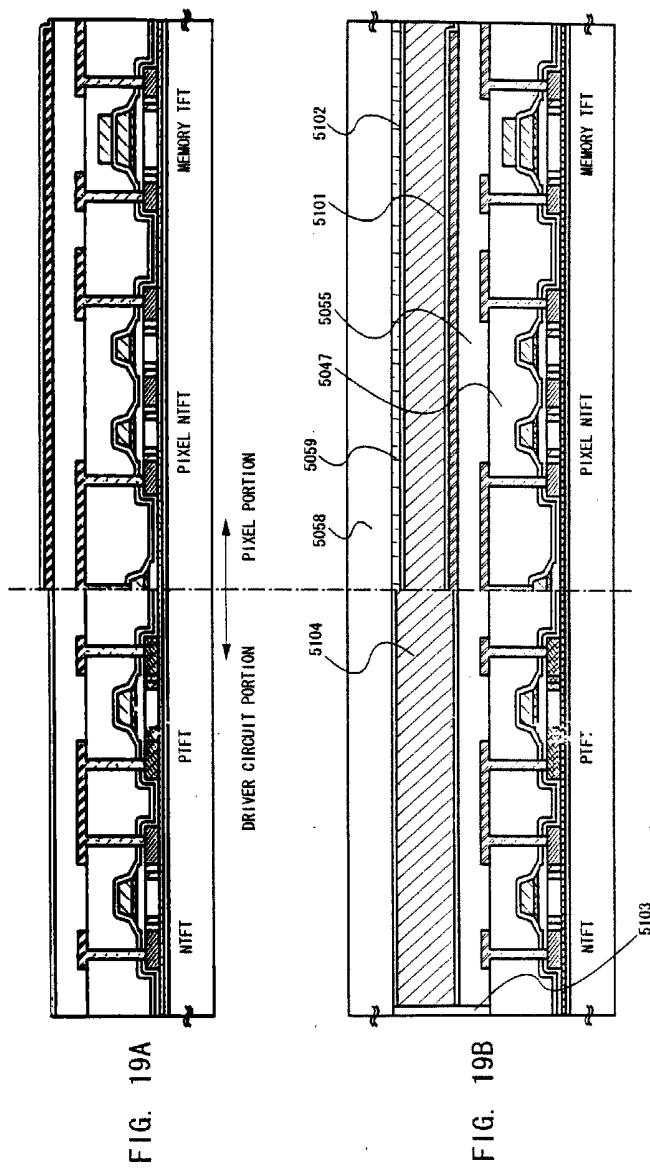


FIG. 18C



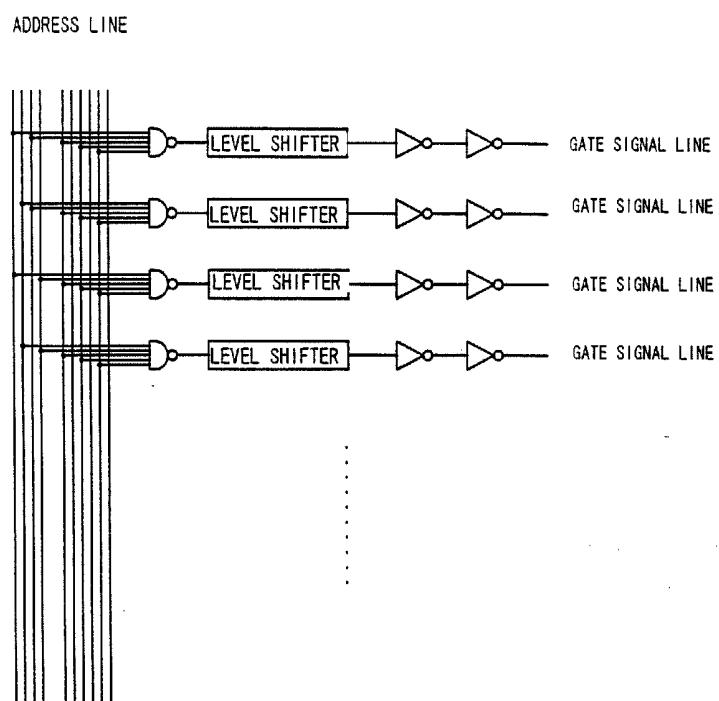


FIG. 20

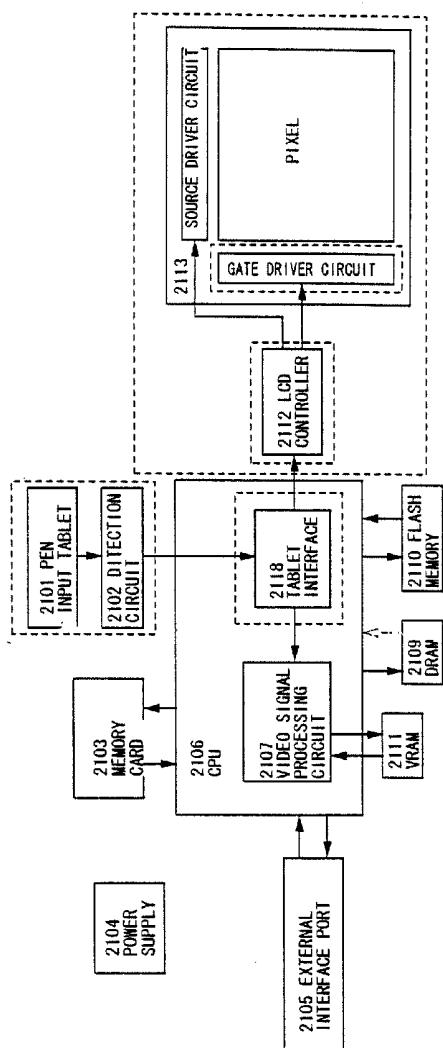


FIG. 21

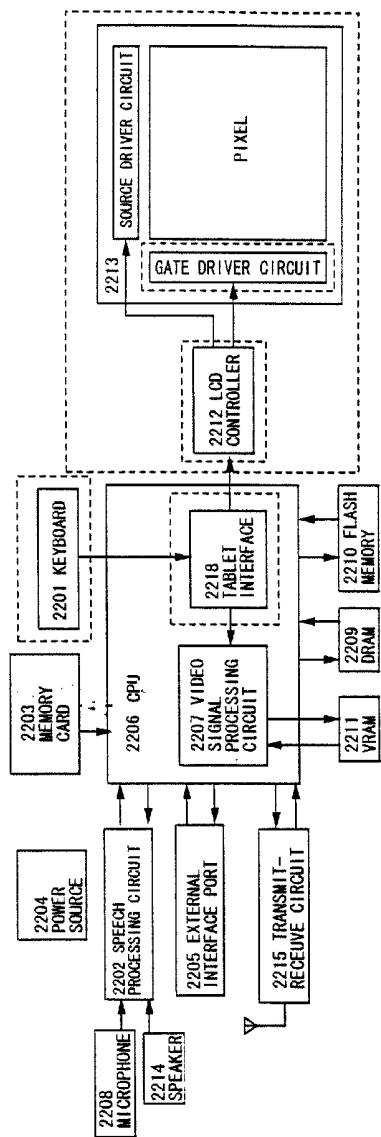


FIG. 22

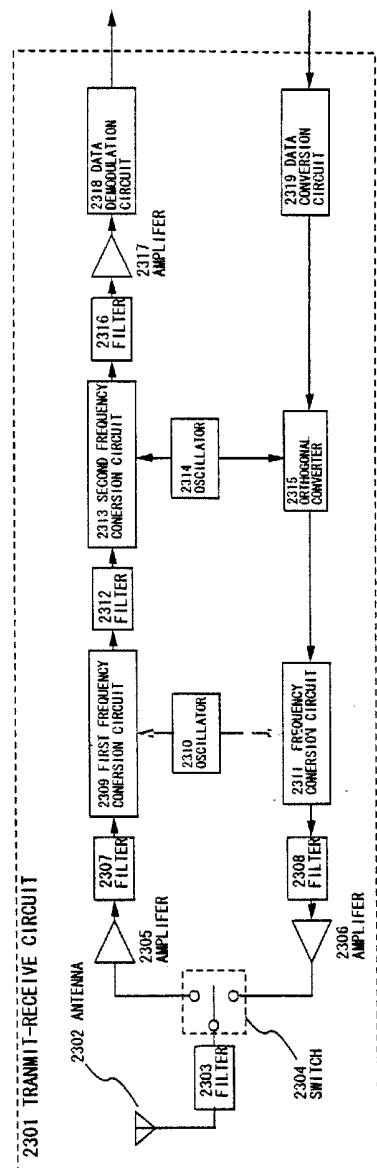


FIG. 23

## LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF DRIVING THE SAME

### CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. application Ser. No. 12/899,070, filed Oct. 6, 2010, now allowed, which is a continuation of U.S. application Ser. No. 11/675,119, filed Feb. 15, 2007, now U.S. Pat. No. 7,812,806, which is a continuation of U.S. application Ser. No. 09/930,956, filed Aug. 17, 2001, now U.S. Pat. No. 7,180,496, which claims the benefit of a foreign priority application filed in Japan as Serial No. 2000-249083 on Aug. 18, 2000, all of which are incorporated by reference.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

[0002] The present invention relates to a driver circuit of a semiconductor display device (hereinafter referred to as display device) and a display device using a driver circuit, specifically to a driver circuit of an active matrix display device having thin film transistors that are formed on an insulator and an active matrix display device using a driver circuit. More specifically, the invention relates to a driver circuit of an active matrix liquid crystal display device that employs a digital video signal as an image source and an active matrix liquid crystal display device using a driver circuit.

[0003] In recent years, display devices with a semiconductor thin film formed on an insulator such as a glass substrate have gained great popularity, especially, active matrix display devices using a thin film transistor (hereinafter referred to as TFT). Any of these active matrix display devices using a TFT has several hundred thousands to several million TFTs and controls electric charge of respective pixels to display an image.

[0004] A technique that is being developed lately relates to a polysilicon TFT for simultaneously forming a pixel TFT and a driver circuit TFT. The pixel TFT is a TFT constituting a pixel and the driver circuit TFT is a TFT constituting a driver circuit that is provided in the periphery of a pixel portion. The technique is a great contribution to reduction in size and reduction in power consumption of the display devices. Owing to the development of this technique, liquid crystal display devices are becoming indispensable devices for, e.g., display units of mobile machines, which lately find their application in increasingly larger fields.

[0005] FIG. 13 shows an example of a schematic diagram of a liquid crystal display device driven by a digital method. A pixel portion 1308 is placed in the center. Above the pixel portion, a source signal line driver circuit 1301 is arranged to control source signal lines. The source signal line driver circuit 1301 has first latch circuits 1304, second latch circuits 1305, D/A converter circuits 1306, analog switches 1307, etc. Gate signal line driver circuits 1302 for controlling gate signal lines are arranged to the left and right of the pixel portion. Although the gate signal line driver circuits 1302 are provided on both sides of the pixel portion in FIG. 13, only one gate signal line driver circuit may be provided to the left or right of the pixel portion. However, it is desirable to place the gate signal line driver circuit on each side of the pixel portion from the viewpoint of driving efficiency and driving reliability.

[0006] The source signal line driver circuit 1301 has a structure as the one shown in FIG. 14. The driver circuit shown in FIG. 14 as an example is a source signal line driver circuit with a horizontal resolution of 1024 pixels for 3 bit digital gray scale display. The driver circuit includes shift register circuits (SR) 1401, first latch circuits (LAT1) 1402, second latch circuits (LAT2) 1403, D/A converter circuits (or D/A converters: D/A) 1404, etc. Though not shown in FIG. 14, the driver circuit may have a buffer circuit, a level shifter circuit and the like if necessary.

[0007] Referring to FIGS. 13 and 14, the operation of the device will be explained briefly. First, clock signals (S-CLK, S-CLKb) and start pulses (S-SP) are inputted to shift register circuits 1303 (denoted by SR in FIG. 14) and pulses are outputted sequentially. The pulses are then inputted to the first latch circuits 1304 (denoted by LAT1 in FIG. 14) so that digital video signals (digital data) also inputted to the first latch circuits 1304 are held therein respectively. Here, D1 is the most significant bit (MSB) whereas D3 is the least significant bit (LSB). When the first latch circuits 1304 complete holding digital video signals corresponding to one horizontal period, the digital video signals held in the first latch circuits 1304 are transferred to the second latch circuits 1305 (denoted by LAT2 in FIG. 14) all at once in response to input of latch signals (latch pulses) during the retrace period.

[0008] Thereafter, the shift register circuits 1303 again operate to start holding of digital video signals corresponding to the next one horizontal period. At the same time, the digital video signals held in the second latch circuits 1305 are converted into analog video signals by the D/A converter circuits 1306 (denoted by D/A in FIG. 14). The analog video signals converted from the digital video signals are written in pixels through source signal lines. An image is displayed by repeating this operation.

[0009] In a general active matrix liquid crystal display device, screen display is updated about sixty times for every second in order to display animation smoothly. In other words, it is necessary to supply digital video signals for every new frame and the signals have to be written in pixels each time. Even when the image to be displayed is a still image; the same digital video signals have to be kept supplied for every new frame and a driver circuit has to process the same digital video signals repeatedly and continuously.

[0010] An alternative method is to write digital video signals of the still image in an external memory circuit once and then supply the digital video signals from the external memory circuit to the liquid crystal display device each time a new frame is started. However, the alternative method is no different from the above method in that the external memory circuit and the driver circuit of the display device are required continuing to operate.

[0011] Reduction in power consumption is greatly demanded particularly in mobile machines. Despite the fact that mobile machines are used mostly in a still image mode, external circuits and driver circuits of the mobile machines continue to operate even during still image display as described above. Therefore, reducing power consumption is hindered.

### SUMMARY OF THE INVENTION

[0012] The present invention has been made in view of the above problems, and an object of the present invention is therefore to reduce power consumption in an external circuit,

a signal line driver circuit, and the like while a still image is displayed by employing a novel circuit.

[0013] In order to attain the object above, the present invention uses the following measures.

[0014] A plurality of memory circuits are provided in each pixel so that digital video signals are stored for each pixel. In the case of displaying a still image, information to be written into a pixel is the same. Therefore, once signals are written, the still image can be continuously displayed by reading out the signals stored in the memory circuits instead of inputting the signals each time a new frame is started. This means that, when a still image is to be displayed, an external circuit, a source signal line driver circuit, and the like can stop their operation once they finish processing signals corresponding to at least one frame.

[0015] Furthermore, some of the memory circuits arranged in each pixel are non-volatile and digital video signals stored in the non-volatile memory circuits once can be kept stored after power supply to the display device is shut off. Accordingly, when the display device is turned on again, there is no need to newly sample the digital video signals but the digital signals are read out of the non-volatile memory circuits to display a still image. This can lead to great reduction in power consumption.

[0016] A liquid crystal display device according to a first aspect of the present invention is characterized in that:

[0017] the liquid crystal display device comprises: a plurality of pixels, wherein the plural pixels each comprises a plurality of memory circuits and a plurality of non-volatile memory circuits.

[0018] A liquid crystal display device according to a second aspect of the present invention is characterized in that:

[0019] the liquid crystal display device comprises: a plurality of pixels, wherein the plural pixels each comprises:

[0020]  $n \times m$  memory circuits for storing  $m$  ( $m$  is a natural number and satisfies  $1 \leq m$ ) frames of  $n$  ( $n$  is a natural number and satisfies  $2 \leq n$ ) bit digital video signals; and

[0021]  $n \times k$  non-volatile memory circuits for storing  $k$  ( $k$  is a natural number and satisfies  $1 \leq k$ ) of the  $n$  bit digital video signals.

[0022] A liquid crystal display device according to a third aspect of the present invention is characterized in that:

[0023] the liquid crystal display device comprises: a plurality of pixels, the plural pixels each comprising:

[0024] a source signal line;

[0025]  $n$  ( $n$  is a natural number and satisfies  $2 \leq n$ ) writing gate signal lines;

[0026]  $n$  reading gate signal lines;

[0027]  $n$  writing transistors;

[0028]  $n$  reading transistors;

[0029]  $n \times m$  memory circuits for storing  $m$  ( $m$  is a natural number and satisfies  $1 \leq m$ ) frames of  $n$  bit digital video signals;

[0030]  $n \times k$  non-volatile memory circuits for storing  $k$  ( $k$  is a natural number and satisfies  $1 \leq k$ ) of the  $n$  bit digital video signals;

[0031]  $2n$  memory circuit selecting units;

[0032]  $2n$  non-volatile memory circuit selecting units; and

[0033] a liquid crystal element,

[0034] wherein each gate electrode of the  $n$  writing transistors is electrically connected to one of the  $n$  writing gate signal lines, with no two gate electrodes sharing the same writing gate signal line,

[0035] wherein each input electrode of the  $n$  writing transistors is electrically connected to the source signal line,

[0036] wherein each output electrode of the  $n$  writing transistors is electrically connected to one of  $m$  circuits out of the  $n \times m$  memory circuits through one of  $n$  units out of the  $2n$  memory circuit selecting units, each memory circuit selecting unit making selection for no more than one output electrode,

[0037] wherein each output electrode of the  $n$  writing transistors is electrically connected to one of  $k$  circuits out of the  $n \times k$  non-volatile memory circuits through one of  $n$  units out of the  $2n$  non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one output electrode,

[0038] wherein each gate electrode of the  $n$  reading transistors is electrically connected to one of the  $n$  reading gate signal lines, with no two gate electrodes sharing the same reading gate signal line,

[0039] wherein each input electrode of the  $n$  reading transistors is electrically connected to one of  $m$  circuits out of the  $n \times m$  memory circuits through one of  $n$  units out of the  $2n$  memory circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode,

[0040] wherein each input electrode of the  $n$  reading transistors is electrically connected to one of  $k$  circuits out of the  $n \times k$  non-volatile memory circuits through one of  $n$  units of the  $2n$  non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode, and

[0041] wherein each output electrode of the  $n$  reading transistors is electrically connected to one of electrodes of the liquid crystal element.

[0042] A liquid crystal display device according to a fourth aspect of the present invention is characterized in that:

[0043] the liquid crystal display device comprises: a plurality of pixels, the plural pixels each comprising:

[0044]  $n$  ( $n$  is a natural number and satisfies  $2 \leq n$ ) source signal lines;

[0045] a writing gate signal line;

[0046]  $n$  reading gate signal lines;

[0047]  $n$  writing transistors;

[0048]  $n$  reading transistors;

[0049]  $n \times m$  memory circuits for storing  $m$  ( $m$  is a natural number and satisfies  $1 \leq m$ ) frames of  $n$  bit digital video signals;

[0050]  $n \times k$  non-volatile memory circuits for storing  $k$  ( $k$  is a natural number and satisfies  $1 \leq k$ ) of the  $n$  bit digital video signals;

[0051]  $2n$  memory circuit selecting units;

[0052]  $2n$  non-volatile memory circuit selecting units; and

[0053] a liquid crystal element,

[0054] wherein each gate electrode of the  $n$  writing transistors is electrically connected to the writing gate signal line,

[0055] wherein each input electrode of the  $n$  writing transistors is electrically connected to one of the  $n$  source signal lines, with no two input electrodes sharing the same source signal line,

[0056] wherein each output electrode of the  $n$  writing transistors is electrically connected to one of  $m$  circuits out of the  $n \times m$  memory circuits through one of  $n$  units out of the  $2n$  memory circuit selecting units, each memory circuit selecting unit making selection for no more than one output electrode,

[0057] wherein each output electrode of the  $n$  writing transistors is electrically connected to one of  $k$  circuits out of the  $n \times k$  non-volatile memory circuits through one of  $n$  units out

of the  $2n$  non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one output electrode,

[0058] is wherein each gate electrode of the  $n$  reading transistors is electrically connected to one of the  $n$  reading gate signal lines, with no two gate electrodes sharing the same reading gate signal line,

[0059] wherein each input electrode of the  $n$  reading transistors is electrically connected to one of  $m$  circuits out of the  $n \times m$  memory circuits through one of  $n$  units out of the  $2n$  memory circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode,

[0060] wherein each input electrode of the  $n$  reading transistors is electrically connected to one of  $k$  circuits out of the  $n \times k$  non-volatile memory circuits through one of  $n$  units out of the  $2n$  non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one input electrode, and

[0061] wherein each output electrode of the  $n$  reading transistors is electrically connected to one of electrodes of the liquid crystal element.

[0062] A liquid crystal display device according to a fifth aspect of the present invention is characterized in that:

[0063] wherein one of the  $m$  memory circuits is selected by one of the memory circuit selecting units, or one of the  $k$  non-volatile memory circuits is selected by one of the non-volatile memory circuit selecting unit, to communicate the selected memory circuit or non-volatile memory circuit with the output electrode of its associated writing transistor, thereby writing the digital video signals in the selected memory circuit, or

[0064] wherein one of the  $m$  memory circuits is selected by one of the memory circuit selecting units, or one of the  $k$  non-volatile memory circuits is selected by one of the non-volatile memory circuit selecting unit, to communicate the selected memory circuit or non-volatile memory circuit with the input electrode of its associated reading transistor, thereby reading the digital video signals stored in the selected memory circuit.

[0065] A liquid crystal display device according to a sixth aspect of the present invention further to the third aspect is characterized in that:

[0066] the display device further comprising:

[0067] shift registers for outputting sampling pulses sequentially in response to clock signals and start pulses;

[0068] first latch circuits for holding  $n$  ( $n$  is a natural number and satisfies  $2 \leq n$ ) bit digital video signals in response to the sampling pulses;

[0069] second latch circuits for receiving the  $n$  bit digital video signals that have been held in the first latch circuits; and

[0070] bit selecting circuits for selecting the  $n$  bit digital video signals transferred to the second latch circuits one bit by one bit to output the signals to the source signal line.

[0071] A liquid crystal display device according to a seventh aspect of the present invention further to the fourth aspect is characterized in that:

[0072] the display device further comprising:

[0073] shift registers for outputting sampling pulses sequentially in response to clock signals and start pulses;

[0074] first latch circuits for holding 1 bit digital video signal out of  $n$  ( $n$  is a natural number and satisfies  $2 \leq n$ ) bit digital video signals in response to the sampling pulses; and

[0075] second latch circuits for receiving the 1 bit digital video signal that has been held in the first latch circuits to output the 1 bit digital video signal to the source signal lines.

[0076] A liquid crystal display device according to a eighth aspect of the present invention further to the fourth aspect is characterized in that:

[0077] the display device further comprising:

[0078] shift registers for outputting sampling pulses sequentially in response to clock signals and start pulses;

[0079] latch circuits for holding 1 bit digital video signal in response to the sampling pulses; and

[0080] bit selecting circuits for selecting one of the source signal lines in order to output the 1 bit digital video signal that has been held in the latch circuits to the selected source signal line.

[0081] A liquid crystal display device according to a ninth aspect of the present invention is characterized in that the memory circuits are static random access memories (SRAM).

[0082] A liquid crystal display device according to a tenth aspect of the present intention is characterized in that the memory circuits are ferroelectric random access memories (FeRAM).

[0083] A liquid crystal display device according to a eleventh aspect of the present invention is characterized in that the memory circuits are dynamic random access memories (DRAM).

[0084] A liquid crystal display device according to a twelfth aspect of the present invention is characterized in that the non-volatile memory circuits are non-volatile electrically erasable programmable read only memories (EEPROM).

[0085] A liquid crystal display device according to a thirteenth aspect of the present invention is characterized in that the memory circuits are formed on a glass substrate.

[0086] A liquid crystal display device according to a fourteenth aspect of the present invention is characterized in that the memory circuits are formed on a plastic substrate.

[0087] A liquid crystal display device according to a fifteenth aspect of the present invention is characterized in that the memory circuits are formed on a stainless steel substrate.

[0088] A liquid crystal display device according to a sixteenth aspect of the present invention is characterized in that the memory circuits are formed on a single crystal wafer.

[0089] According to a seventeenth aspect of the present invention, a method of driving a liquid crystal display device using  $n$  ( $n$  is a natural number and satisfies  $2 \leq n$ ) bit digital video signals to display an image, the liquid crystal display device including a source signal line driving circuit, a gate signal line driving circuit, and a plurality of pixels is characterized in that:

[0090] wherein shift registers in the source signal line driving circuit output sampling pulses, which are inputted to latch circuits, which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line,

[0091] wherein gate signal line selecting pulses are outputted in the gate signal line driving circuit to select a gate signal line, and

[0092] wherein one of the following (a) through (e) is conducted in pixels in the row of the selected gate signal line out of the plural pixels:

[0093] (a) the  $n$  bit digital video signals inputted from the source signal line are written in memory circuits;

[0094] (b) the  $n$  bit digital video signals stored in the memory circuits are read;

[0095] (c) the n bit digital video signals inputted from the source signal line or the n bit digital video signals stored in the memory circuits are written in non-volatile memory circuits;

[0096] (d) the n bit digital video signals stored in the non-volatile memory circuits are read; and

[0097] (e) the n bit digital video signals stored in the non-volatile memory circuits are written in the memory circuits.

[0098] According to an eighteenth aspect of the present invention, a method of driving a liquid crystal display device using n (n is a natural number and satisfies  $2 \leq n$ ) bit digital video signals to display an image, the liquid crystal display device including a source signal line driving circuit, a gate signal line driving circuit, and a plurality of pixels is characterized in that:

[0099] wherein shift registers in the source signal line driving circuit output sampling pulses, which are inputted to latch circuits, which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line,

[0100] wherein gate signal line selecting pulses are outputted in the gate signal line driving circuit to select gate signal lines in order from the first row, and

[0101] wherein the n bit digital video signals are written in or read out the plural pixels in order from the first row.

[0102] According to a nineteenth aspect of the present invention, a method of driving a liquid crystal display device using n (n is a natural number and satisfies  $2 \leq n$ ) bit digital video signals to display an image, the liquid crystal display device including a source signal line driving circuit, a gate signal line driving circuit, and a plurality of pixels is characterized in that:

[0103] wherein shift registers in the source signal line driving circuit output sampling pulses, which are inputted to latch circuits, which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line,

[0104] wherein the gate signal line driving circuit selects a gate signal line by outputting a gate signal line selecting pulse to an arbitrarily specified row of gate signal line, and

[0105] wherein the n bit digital video signals are written in or read out pixels in the arbitrarily selected row of gate signal line out of the plural pixels.

[0106] According to a twentieth aspect of the present invention, wherein, during a still image display period, the n bit digital video signals stored in the memory circuits are repeatedly read to display a still image, so that the source signal line driving circuit can stop its operation.

[0107] According to a twenty-first aspect of the present invention, an electronic device comprising a liquid crystal display device according to any one of first through sixteenth aspects.

[0108] According to a twenty-second aspect of the present invention, an electronic device employing a method of driving a liquid crystal display device according to any one of seventeenth through twentieth aspects.

[0109] According to a twenty-third aspect of the present invention, an electronic device according to twenty-first or twenty-second aspect, wherein the electronic device is one of a television set, a personal computer, a portable terminal, a video camera, and a head mounted display.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0110] In the accompanying drawings:

[0111] FIG. 1 is a circuit diagram of a pixel according to the present invention, the pixel having therein a plurality of memory circuits and a plurality of non-volatile memory circuits;

[0112] FIG. 2 is a diagram showing an example of the circuit structure of a source signal line driver circuit for displaying an image using a pixel of the present invention;

[0113] FIGS. 3A to 3C are timing charts for displaying an image using a pixel of the present invention;

[0114] FIG. 4 is a detailed circuit diagram of a pixel according to the present invention, the pixel having therein a plurality of memory circuits and a plurality of non-volatile memory circuits;

[0115] FIG. 5 is a diagram showing an example of the circuit structure of a source signal line driver circuit having no second latch circuit;

[0116] FIG. 6 is a detailed circuit diagram of a pixel to which the present invention is applied, the pixel being driven by the source signal line driver circuit of FIG. 5;

[0117] FIGS. 7A to 7C are timing charts for displaying an image using the circuits shown in FIGS. 5 and 6;

[0118] FIG. 8 is a detailed circuit diagram of a pixel of the present invention when the memory circuits are dynamic random access memories;

[0119] FIGS. 9A to 9C are diagrams exemplary showing a process of manufacturing a liquid crystal display device that has a pixel of the present invention;

[0120] FIGS. 10A to 10C are diagrams exemplary showing a process of manufacturing a liquid crystal display device that has a pixel of the present invention;

[0121] FIGS. 11A to 11C are diagrams exemplary showing a process of manufacturing a liquid crystal display device that has a pixel of the present invention;

[0122] FIG. 12 is a diagram exemplary showing a process of manufacturing a liquid crystal display device that has a pixel of the present invention;

[0123] FIG. 13 is a diagram showing in a simplified manner the entire circuit structure of a conventional liquid crystal display device;

[0124] FIG. 14 is a diagram showing an example of the circuit structure of a source signal line driver circuit in a conventional liquid crystal display device;

[0125] FIGS. 15A to 15F are diagrams showing examples of an electronic device to which a display device having a pixel of the present invention can be applied;

[0126] FIGS. 16A to 16D are diagrams showing examples of an electronic device to which a display device having a pixel of the present invention can be applied;

[0127] FIG. 17 is a diagram showing an example of the circuit structure of a source signal line driver circuit having no second latch circuit;

[0128] FIGS. 18A to 18C are timing charts for displaying an image using the circuit shown in FIG. 17;

[0129] FIGS. 19A and 19B are diagrams showing an example of manufacturing a liquid crystal display device having a pixel of the present invention;

[0130] FIG. 20 is a diagram showing an example of a gate signal line driver circuit using a decoder;

[0131] FIG. 21 is a block diagram of a portable information terminal employing the present invention;

[0132] FIG. 22 is a block diagram of a cellular phone employing the present invention; and

[0133] FIG. 23 is a block diagram of a transmission/reception unit of the cellular phone.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

##### Embodiment Mode

[0134] FIG. 2 shows the structure of a source signal line driver circuit and the structure of some of pixels in a liquid crystal display device that employs pixels having memory circuits. The circuit is capable of handling 3 bit digital gray scale signals, and is composed of shift register circuits 201, first latch circuits 202, second latch circuits 203, bit signal selecting switches 204, and pixels 205. Denoted by 210 are signal lines to which signals are inputted from a gate signal line driver circuit, or directly from the external, and descriptions of the signal lines will be found later along with explanations of the pixels.

[0135] FIG. 1 shows a detailed circuit structure of one of the pixels 205 in FIG. 2. The pixel is for 3 bit digital gray scale, and is composed of a liquid crystal element (LC), a capacitor storage (Cs), volatile memory circuits (A1 to A3 and B1 to B3), non-volatile memory circuits (C1 to C3), etc. Denoted by 101 is a source signal line. 102 to 104 represent writing gate signal lines, 105 to 107, reading gate signal lines, 108 to 110, writing TFTs, 111 to 113, reading TFTs, and 114 to 125, memory circuit selecting units.

[0136] The present invention is characterized in that the memory circuits in each pixel include non-volatile memory circuits (denoted by C1 to C3 in FIG. 1) for storing at least one frame of n bit digital video signals. The rest of the memory circuits here are referred to as volatile memory circuits on purpose to distinguish them from the non-volatile memory circuits. However, the memory circuits A1 to A3 and B1 to B3 may not always be volatile memory circuits but may be non-volatile ones. The memory circuits A1 to A3 and B1 to B3 in this embodiment mode are volatile memory circuits such as SRAM and DRAM because both writing and reading have to be done in one frame period and the writing time and the reading time need to be short enough.

[0137] FIGS. 3A to 3C show simplified operation timing in the display device shown in FIG. 1 in accordance with the present invention. The display device is for 3 bit digital gray scales and has a VGA level resolution. A method of driving this display device will be described with reference to FIGS. 1 to 3C. The reference symbols used in this description are the same as those in FIGS. 1 to 3C.

[0138] Reference is made to FIG. 2 and FIGS. 3A and 3B. In FIG. 3A, frame periods are respectively denoted by  $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $\delta$ . The operation of the circuit in the frame period  $\alpha$  is described first.

[0139] Similar to the conventional driver circuit of digital driving method, clock signals (S-CLK, S-CLKb) and start pulses (S-SP) are inputted to the shift register circuits 201 and sampling pulses are outputted sequentially. The sampling pulses are then inputted to the first latch circuits 202 (LAT1) so that digital video signals (digital data) also inputted to the first latch circuits 202 are held therein respectively. This period is referred to as dot data sampling period in this specification. The dot data sampling period for data corresponding to one horizontal period stretches from a period 1 to a period 480 in FIG. 3A. The digital video signals are 3 bit signals, and D1 is the most significant bit (MSB) whereas D3 is the least significant bit (LSB). When the first latch circuits 202 com-

plete holding digital video signals corresponding to one horizontal period, the digital video signals held in the first latch circuits 202 are transferred to the second latch circuits 203 (LAT2) all at once in response to input of latch signals (latch pulses) during the retrace period.

[0140] Subsequently, the first latch circuits operate to hold digital video signals corresponding to the next horizontal period in response to sampling pulses again outputted from the shift register circuits 201.

[0141] On the other hand, the digital video signals transferred to the second latch circuits 203 are written in the volatile memory circuits arranged in each pixel. As shown in FIG. 3B, the dot data sampling period of the next column is divided into three, namely, a period I, a period II, and a period III, to output the digital video signals held in the second latch circuits to the source signal line. At this point, the bit signal selecting switches 204 make selective connection to output the signals of the respective bits to the source signal line in order.

[0142] In the period I, pulses are inputted to the writing gate signal line 102 to turn the TFT 108 conductive and the memory circuit selecting unit 114 selects the volatile memory circuit A1 so that digital video signals are written in the volatile memory circuit A1. Subsequently, in the period II, pulses are inputted to the writing gate signal line 103 to turn the TFT 109 conductive and the memory circuit selecting unit 115 selects the volatile memory circuit A2 so that digital video signals are written in the volatile memory circuit A2. Lastly, in the period III, pulses are inputted to the writing gate signal line 104 to turn the TFT 110 conductive and the memory circuit selecting unit 116 selects the volatile memory circuit A3 so that digital video signals are written in the volatile memory circuit A3.

[0143] The above steps complete processing of digital video signals corresponding to one horizontal period. The periods in FIG. 3B correspond to the period indicated by \* in FIG. 3A. The above operation is repeated until the last stage is processed, thereby completing writing digital video signals of one frame in the volatile memory circuits A1 to A3.

[0144] In the display device of the present invention, 3 bit digital gray scales are obtained through a time gray scale method. Unlike the usual gray scale method in which the luminance is controlled by the level of voltage applied to pixels, the time gray scale method applies only two levels of voltage to pixels to render the pixels to an ON state and an OFF state (the ON state corresponds to white and the OFF state corresponds to black on the screen) and gray scales are created utilizing difference in display time. When n bit gray scale display is to be obtained by the time gray scale method, the display period is divided into n periods and the ratio of the periods is set in accordance with power of 2, as in  $2^{n-1} : 2^{n-2} : \dots : 2^0$ . The length of the display period of a pixel is varied depending on in which period the pixel is brought into an ON state, whereby gray scale display is attained. A pixel being in an ON state here means that a voltage is applied between pixel electrodes whereas a pixel being in an OFF state means that a voltage is not applied to the pixel.

[0145] If the display period is divided into periods in accordance with other rules than power of 2, it is still possible to obtain gray scale display.

[0146] Based on the above description, the operation of the circuit in the frame period  $\beta$  will be explained. When writing in the volatile memory circuits in the last stage is finished, the first frame is displayed. FIG. 3C is a diagram illustrating a 3

bit time gray scale method. Currently, digital video signals are assorted by their bits into three groups and the groups are respectively stored in the volatile memory circuits A1 to A3. Ts1 denotes a period of display by first bit data, Ts2 denotes a period of display by second bit data, and Ts3 denotes a period of display by third bit data. The lengths of these display periods are set to satisfy  $Ts1:Ts2:Ts3=4:2:1$ .

[0147] Since the signals here are 3 bit signals, the luminance obtained ranges from 0 to 7, namely, 8 levels in total. When a pixel is not brought into an ON state in any of the periods Ts1 to Ts3, the luminance is 0. When a pixel is in an ON state throughout the entire periods, the luminance is 7. If a pixel is to have the fifth level of luminance, the pixel is brought into ON state in Ts1 and Ts3.

[0148] Specific explanations will be given referring to the drawings. In the period Ts1, pulses are inputted to the reading gate signal line 105 to turn the TFT 111 conductive and the memory circuit selecting unit 117 selects the volatile memory circuit A1 so that the pixel is driven in accordance with the digital video signals stored in the volatile memory circuit A1. Subsequently, in Ts2, pulses are inputted to the reading gate signal line 106 to turn the TFT 112 conductive and the memory circuit selecting unit 118 selects the volatile memory circuit A2 so that the pixel is driven in accordance with the digital video signals stored in the volatile memory circuit A2. Lastly, in Ts3, pulses are inputted to the reading gate signal line 107 to turn the TFT 113 conductive and the memory circuit selecting unit 119 selects the volatile memory circuit A3 so that a voltage is applied to the pixel in accordance with the digital video signals stored in the volatile memory circuit A3.

[0149] When the display device is a liquid crystal display device, there are a normally white mode and a normally black mode. In both modes, white and black are inverted when a pixel switches between an ON state and an OFF state. Accordingly, the luminance may be reverse to what is described in the above.

[0150] Data corresponding to one frame period are displayed as above. Meanwhile, the driver circuit is processing digital video signals of the next frame period. The procedure is the same as the one described above up through transferring the digital video signals to the second latch circuits. In the subsequent volatile memory circuit writing period, the other volatile memory circuits are used. However, if the number of volatile memory circuits in the pixel is not large enough for more than one frame, data of the next frame are overwritten in the volatile memory circuits in which data of the previous frame have already been written.

[0151] In the period I, pulses are inputted to the writing gate signal line 102 to turn the TFT 108 conductive and the memory circuit selecting unit 114 selects the volatile memory circuit B1 so that digital video signals are written in the volatile memory circuit B1. Subsequently, in the period II, pulses are inputted to the writing gate signal line 103 to turn the TFT 109 conductive and the memory circuit selecting unit 115 selects the volatile memory circuit B2 so that digital video signals are written in the volatile memory circuit B2. Lastly, in the period III, pulses are inputted to the writing gate signal line 104 to turn the TFT 110 conductive and the memory circuit selecting unit 116 selects the volatile memory circuit B3 so that digital video signals are written in the volatile memory circuit B3.

[0152] Then the frame period  $\gamma$  is started and the second frame is displayed in accordance with the digital video sig-

nals stored in the volatile memory circuits B1 to B3. At the same time, processing of digital video signals of the next frame period is commenced. The digital video signals of the next frame period are stored again in the volatile memory circuits A1 to A3 that have finished their operations related to display of the first frame period.

[0153] Thereafter, the digital video signals stored in the volatile memory circuits A1 to A3 are displayed in the frame period  $\delta$ , and digital video signals of the next frame period simultaneously begin to receive processing. The digital video signals of the next frame period are stored again in the volatile memory circuits B1 to B3 that have finished their operations related to display of the second frame period.

[0154] Writing digital video signals in the non-volatile memory circuits C1 to C3 usually takes much longer time than writing digital video signals in volatile memory circuits such as SRAM. Therefore, desirable procedure is to store digital video signals in the volatile memory circuits A1 to A3 or B1 to B3 and then write the stored signals in the non-volatile memory circuits C1 to C3. In FIG. 1, writing in the volatile memory circuits A1 to A3 or B1 to B3 is completed before the reading TFTs 111 to 113 are turned ON to display an image. When data is to be written in the non-volatile memory circuits, the reading TFTs 111 to 113 are turned OFF and the memory circuit selecting units 120-122 respectively select the non-volatile memory circuits C1 to C3. No image is displayed on the screen in this writing period but the writing time is about several ms to 100 ms, hardly causing a problem.

[0155] Upon turning the display device on, an image is displayed by reading the digital video signals stored in the non-volatile memory circuits C1 to C3. In this case also, it is desirable to write data in the volatile memory circuits A1 to A3 or B1 to B3 once and read the stored data from the volatile memory circuits A1 to A3 or B1 to B3 in the subsequent frame periods.

[0156] The above operations are repeated to display an image continuously. If the image to be displayed is a still image, digital video signals are stored in the volatile memory circuits A1 to A3 in the first operation. Once the digital video signals are stored, the digital video signals stored in the volatile memory circuits A1 to A3 are repeatedly read out for every new frame period. Thus driving of an external circuit, the source signal line driver circuit, and the like can be stopped while the still image is displayed.

[0157] Furthermore, digital video signals can be kept stored after power supply to the liquid crystal display device is shut off by writing digital video signals in the non-volatile memory circuits C1 to C3 provided in the pixel. Accordingly, when the display device is turned on again, a still image can be displayed without newly sampling the digital video signals.

[0158] Moreover, the gate signal lines can be used one by one, as opposed to driving all of them at once, in writing digital video signals in the memory circuits or reading digital video signals out of the memory circuits. In other words, partial rewriting of a screen is possible by operating the source signal line driver circuit and the gate signal line driver circuit for only a short period of time, thereby increasing display manner options. In this case, it is desirable to use a decoder as the gate signal line driver circuit. A decoder appropriate to use is a circuit disclosed in Japanese Patent Application Laid-open No. Hei 8-101609. An example of the decoder is shown in FIG. 20. The source signal line driver circuit may also include a decoder to rewrite a part of a screen.

[0159] In this embodiment mode, one pixel has volatile memory circuits A1 to A3 and B1 to B3 in order to store 3 bit digital video signals corresponding to two frames. However, the number of memory circuits according to the present invention is not limited thereto. For example, when n bit digital video signals corresponding to m frames are to be stored, one pixel has  $n \times m$  volatile memory circuits.

[0160] Similarly, the number of non-volatile memory circuits according to the present invention is not limited by this embodiment mode in which the non-volatile memory circuits C1 to C3 are provided in one pixel in order to store 3 bit digital video signals of one frame. If n bit digital video signals of k frames are to be kept stored after power supply is shut off,  $n \times k$  non-volatile memory circuits are placed in each pixel.

[0161] The memory circuits provided in the pixels store digital video signals in the manner described above, so that the digital video signals stored in the memory circuits can be used repeatedly for every new frame period when a still image is displayed. This makes it possible to continuously display a still image without driving an external circuit, the source signal line driver circuit, and other circuits. Accordingly, the invention greatly contributes to reduction of power consumption in liquid crystal display devices.

[0162] The source signal line driver circuit may not necessarily be formed on an insulator integrally, considering arrangement of the latch circuits that increase in number in accordance with the bit number. A part of, or the entirety of, the source signal line driver circuit may be external to the insulator.

[0163] Although the source signal line driver circuit in this embodiment mode is provided with a number of latch circuits in accordance with the bit number, the source signal line driver circuit can operate also when the latch circuits are provided in a number necessary for only one bit data processing. In this case, digital video signals of from significant bit to less significant bit are inputted to the latch circuits in series.

[0164] Embodiments of the present invention will be described below.

### Embodiment 1

[0165] This embodiment gives descriptions on the memory circuit selecting units in the circuit shown in Embodiment Mode, regarding its specific structure (arrangement of transistors and other components) and its operation.

[0166] FIG. 4 shows a pixel similar to the one shown in FIG. 1, but circuits constituting the memory circuit selecting units and the peripheral circuits thereof are shown here. In FIG. 4, volatile memory circuits A1 to A3 and B1 to B3 are respectively connected to writing selecting TFTs 420, 422, 424, 426, 428, and 430, and to reading selecting TFTs 421, 423, 425, 427, 429, and 431. The volatile memory circuits are respectively controlled by memory circuit selecting signal lines 414 to 419. Non-volatile memory circuits C1 to C3 are connected to writing selecting TFTs 435, 437, and 439, respectively, and are connected to reading selecting TFTs 436, 438, and 440, respectively. The non-volatile memory circuits are respectively controlled by memory circuit selecting signal lines 432 to 434 and 441 to 443. The pixel shown in this embodiment stores 3 bit digital video signals corresponding to two frames in the volatile memory circuits A1 to A3 and B1 to B3, and stores 3 bit digital video signals corresponding to one frame in the non-volatile memory circuits C1 to C3.

[0167] The circuit of this embodiment, shown in FIG. 4, may be driven in accordance with the timing charts described

in Embodiment Mode with reference to FIGS. 3A to 3C. The operation of the circuit, plus a method of actually driving the memory circuit selecting units, will be described referring to FIGS. 3A to 3C and FIG. 4. The description adopts the reference symbols used in FIGS. 3A to 3C and FIG. 4.

[0168] Reference is made to FIGS. 3A and 3B. In FIG. 3A, frame periods are respectively denoted by  $\alpha$ ,  $\beta$ ,  $\gamma$ , and  $\delta$ . The operation of the circuit in the frame period  $\alpha$  is described first.

[0169] Shift register circuits, first latch circuits, and second latch circuits are driven the same way as Embodiment Mode, so see the descriptions of Embodiment Mode.

[0170] First, pulses are inputted to the memory circuit selecting signal lines 414 to 416 to turn the writing selecting TFTs 420, 424, and 428 ON, thereby readying the volatile memory circuits A1 to A3 for writing in. In the period I, pulses are inputted to a writing gate signal line 402 to turn a writing TFT 408 conductive and digital video signals are written in the volatile memory circuit A1. Subsequently, in the period II, pulses are inputted to a writing gate signal line 403 to turn a writing TFT 409 conductive and digital video signals are written in the volatile memory circuit A2. Lastly, in the period III, pulses are inputted to a writing gate signal line 404 to turn a writing TFT 410 conductive and digital video signals are written in the volatile memory circuit A3.

[0171] The above steps complete processing of digital video signals corresponding to one horizontal period. The periods in FIG. 3B correspond to the period indicated by \* in FIG. 3A. The above operation is repeated until the last stage is processed, thereby completing writing digital video signals of one frame in the volatile memory circuits A1 to A3.

[0172] Subsequently, the operation of the circuit in the frame period  $\beta$  will be explained. When writing in the volatile memory circuits in the last stage is finished, the first frame is displayed. FIG. 3C is a diagram illustrating a 3 bit time gray scale method. Currently, digital video signals are assorted by their bits into three groups and the groups are respectively stored in the volatile memory circuits A1 to A3.  $T_s$  denotes a period of display by first bit data,  $T_{s2}$  denotes a period of display by second bit data, and  $T_{s3}$  denotes a period of display by third bit data. The lengths of these display periods are set to satisfy  $T_{s1}:T_{s2}:T_{s3}=4:2:1$ .

[0173] If the display period is divided into periods in accordance with other rules than power of 2, it is still possible to obtain gray scale display.

[0174] Since the signals here are 3 bit signals, the luminance obtained ranges from 0 to 7, namely, 8 levels in total. When a pixel is not brought into an ON state in any of the periods  $T_{s1}$  to  $T_{s3}$ , the luminance is 0. When a pixel is in an ON state throughout the entire periods, the luminance is 7. If a pixel is to have the fifth level of luminance, the pixel is brought into ON state in  $T_{s1}$  and  $T_{s3}$ .

[0175] Specific explanations will be given referring to the drawings. When moving on to the display period after the operation of writing data in the volatile memory circuits is finished, supply of pulses to the memory circuit selecting signal lines 414 to 416 are cut to turn the writing selecting TFTs 420, 424, and 428 unconductive. At the same time, pulses are inputted to the memory circuit selecting signal lines 417 to 419 to turn the reading selecting TFTs 421, 425, and 429 conductive, thereby readying the volatile memory circuits A1 to A3 for reading. In the period  $T_{s1}$ , pulses are inputted to a reading gate signal line 405 to turn a reading TFT 411 conductive so that the pixel is driven in accordance with the digital video signals stored in the volatile memory circuit

A1. Subsequently, in Ts2, pulses are inputted to a reading gate signal line 406 to turn a reading TFT 412 conductive so that the pixel is driven in accordance with the digital video signals stored in the volatile memory circuit A2. Lastly, in Ts3, pulses are inputted to a reading gate signal line 407 to turn a reading TFT 413 conductive so that a voltage is applied to the pixel in accordance with the digital video signals stored in the volatile memory circuit A3.

[0176] Data corresponding to one frame period are displayed as above. Meanwhile, the driver circuit is processing digital video signals of the next frame period. The procedure is the same as the one described above up through transferring the digital video signals to the second latch circuits. In the subsequent memory circuit writing period, the volatile memory circuits B1 to B3 are used.

[0177] During the period in which signals are written in the volatile memory circuits A1 to A3, the writing selecting TFTs 420, 424, and 428 are turned conductive to make the volatile memory circuits A1 to A3 writeable and, at the same time, the reading selecting TFTs 423, 427, and 431 are turned conductive to make the volatile memory circuits B1 to B3 readable. On the other hand, during the period in which signals are written in the volatile memory circuits B1 to B3, the writing selecting TFTs 422, 426, and 430 are turned conductive to make the volatile memory circuits B1 to B3 writeable and, at the same time, the reading selecting TFTs 421, 425, and 429 are turned conductive to make the volatile memory circuits A1 to A3 readable. To summarize, the volatile memory circuits A1 to A3 and B1 to B3 in the pixel of this embodiment alternately switches between writing and reading over every new frame period.

[0178] In the period I, pulses are inputted to the writing gate signal line 402 to turn the writing TFT 408 conductive so that digital video signals are written in the volatile memory circuit B1. Subsequently, in the period II, pulses are inputted to the writing gate signal line 403 to turn the writing TFT 409 conductive so that digital video signals are written in the volatile memory circuit B2. Lastly, in the period III, pulses are inputted to the writing gate signal line 404 to turn the writing TFT 410 conductive so that digital video signals are written in the volatile memory circuit B3.

[0179] Then the frame period  $\gamma$  is started and the second frame is displayed in accordance with the digital video signals stored in the volatile memory circuits B1 to B3. At the same time, processing of digital video signals of the next frame period is commenced. The digital video signals of the next frame period are stored again in the volatile memory circuits A1 to A3 that have finished their operations related to display of the first frame period.

[0180] Thereafter, the digital video signals stored in the volatile memory circuits A1 to A3 are displayed in the frame period  $\delta$ , and digital video signals of the next frame period simultaneously begin to receive processing. The digital video signals of the next frame period are stored again in the volatile memory circuits B1 to B3 that have finished their operations related to display of the second frame period.

[0181] The operation of writing digital video signals in the non-volatile memory circuits C1 to C3 and the operation of reading digital video signals out of the non-volatile memory circuits C1 to C3 are the same as Embodiment Mode.

[0182] The procedure above is repeated to display an image. When the image to be displayed is a still image, the source signal line driver circuit stops its operation after digital video signals of some frame are written in the memory cir-

cuits, and the image is displayed by reading the same signals stored in the memory circuits each time a new frame is started. In this way, power consumption during still image display can be reduced greatly. Moreover, by storing the digital video signals using the non-volatile memory circuits, the digital video signals of the still image are kept stored after power supply to the display device is shut off and hence the still image can be displayed next time the display device is turned on.

## Embodiment 2

[0183] This embodiment gives a description on a case where signals are written in volatile memory circuits of a pixel portion by dot-sequential system to eliminate the need for a second latch circuit of a source signal line driver circuit.

[0184] FIG. 5 shows the structure of a source signal line driver circuit and the structure of some of pixels in a liquid crystal display device that employs pixels having memory circuits. The circuit is capable of handling 3 bit digital video signals, and is composed of shift register circuits 501, latch circuits 502, and pixels 503. Denoted by 510 are signal lines to which signals are inputted from a gate signal line driver circuit or directly from the external, and descriptions of the signal lines will be found later along with explanations of the pixels.

[0185] FIG. 6 shows a detailed circuit structure of one of the pixels 503 in FIG. 5. As in Embodiment 1, the pixel is for 3 bit digital gray scales, and is composed of a liquid crystal element (LC), volatile memory circuits (A1 to A3 and B1 to B3), non-volatile memory circuits (C1 to C3), etc. Denoted by 601 is a first bit (MSB) signal source signal line, 602, a second bit signal source signal line, and 603, a third bit (LSB) signal source signal line. Reference symbol 604 represents a writing gate signal line, 605 to 607, reading gate signal lines, 608 to 610, writing TFTs, and 611 to 613, reading TFTs. Memory circuit selecting units include writing selecting TFTs 620, 622, 624, 626, 628, and 630, reading selecting TFTs 621, 623, 625, 627, 629, and 631, and other circuits. 632 to 634 and 641 to 643 denote memory circuit selecting signal lines. Memory circuit selecting units for the non-volatile memory circuits C1 to C3 include writing selecting TFTs 636, 638, and 640, reading selecting TFTs 635, 637, and 639, and other circuits.

[0186] FIGS. 7A to 7C are timing charts regarding driving of the circuit of this embodiment. The description will be given with reference to FIG. 5, FIG. 6, and FIGS. 7A to 7C.

[0187] The operation of the shift register circuits 501 and the latch circuits (LAT1) 502 is the same as Embodiment Mode and Embodiment 1. As shown in FIG. 7B, writing in the volatile memory circuits in the pixel is started immediately after the latch operation for the first stage is finished. Pulses are inputted to the writing gate signal line 604 to turn the writing TFTs 608 to 610 conductive and the memory circuit selecting signal lines 614 to 616 also receive pulses to turn the writing selecting TFTs 620, 624, 628 conductive. The volatile memory circuits A1 to A3 are thus readied for writing. The digital video signals grouped by their bits and held in the latch circuits 502 in groups are simultaneously written in the volatile memory circuits through the three source signal lines 601 to 603.

[0188] While the digital video signals held in the latch circuits are written in the volatile memory circuits in the first stage, sampling pulses are newly outputted and, in response,

digital video signals for the next stage are held in the latch circuits. Signals are thus sequentially written in the volatile memory circuits.

[0189] The operation above is conducted in one horizontal period (corresponding to the period indicated by \*\* in FIG. 7A) and the same operation is repeated for all the columns to complete writing digital video signals of one frame in the volatile memory circuits in the frame period  $\alpha$ . Then a display period for the first frame, namely, the frame period  $\beta$ , is started. Supply of pulses to the writing gate signal line 604 is cut and supply of pulses to the memory circuit selecting signal lines 614 to 616 is also stopped to turn the writing selecting TFTs 620, 624, and 628 unconductive. Instead, pulses are inputted to the memory circuit selecting signal lines 617 to 619 to turn the reading selecting TFTs 621, 625, and 629 conductive, thereby readying the volatile memory circuits A1 to A3 for reading.

[0190] The time gray scale method described in Embodiment 1 is then applied as shown in FIG. 7C. In the display period  $Ts_1$ , pulses are inputted to a reading gate signal line 605 to turn a reading TFT 611 conductive so that the digital video signals stored in the volatile memory circuit A1 are read out for display. Subsequently, in  $Ts_2$ , pulses are inputted to a reading gate signal line 606 to turn a reading TFT 612 conductive so that the digital video signals stored in the volatile memory circuit A2 are read out for display. Similarly, in  $Ts_3$ , pulses are inputted to a reading gate signal line 607 to turn a reading TFT 613 conductive so that the digital video signals stored in the volatile memory circuit A3 are read out for display.

[0191] Thus a display period for the first frame is completed. In the frame period  $\beta$ , digital video signals of the next frame are beginning to be processed at the same time. The procedure is the same as the one described above up through holding the digital video signals in the latch circuits 502. In the subsequent volatile memory circuit writing period, the volatile memory circuits B1 to B3 are used.

[0192] During the period in which signals are written in the volatile memory circuits A1 to A3, the writing selecting TFTs 620, 624, and 628 are turned conductive to make the volatile memory circuits A1 to A3 writeable and, at the same time, the reading selecting TFTs 623, 627, and 631 are turned conductive to make the volatile memory circuits B1 to B3 readable. On the other hand, during the period in which signals are written in the volatile memory circuits B1 to B3, the writing selecting TFTs 622, 626, and 630 are turned conductive to make the volatile memory circuits B1 to B3 writeable and, at the same time, the reading selecting TFTs 621, 625, and 629 are turned conductive to make the volatile memory circuits A1 to A3 readable. To summarize, the volatile memory circuits A1 to A3 and B1, to B3 in the pixel of this embodiment alternately switches between writing and reading over every new frame period.

[0193] The operation of writing in the volatile memory circuits B1 to B3 and the operation of reading out of the volatile memory circuits B1 to B3 are the same as the volatile memory circuits A1 to A3. When writing signals in the volatile memory circuits B1 to B3 is finished, the frame period  $\gamma$  is started to move on to the display period for the second frame. Concurrently, digital video signals of the next frame period is processed in the frame period  $\gamma$ . The procedure is the same as the one described above up through holding the digital video signals in the latch circuits 502. In the subse-

quent volatile memory circuit writing period, the volatile memory circuits A1 to A3 are again used.

[0194] Thereafter, the digital video signals stored in the volatile memory circuits A1 to A3 are displayed in the frame period  $\delta$ , and digital video signals of the next frame period simultaneously begin to receive processing. The digital video signals of the next frame period are stored again in the volatile memory circuits B1 to B3 that have finished their operations related to display of the second frame period.

[0195] The operation of writing digital video signals in the non-volatile memory circuits C1 to C3 and the operation of reading digital video signals out of the non-volatile memory circuits C1 to C3 are the same as Embodiment Mode.

[0196] The procedure above is repeated to display an image. When the image to be displayed is a still image, the source signal line driver circuit stops its operation after digital video signals of some frame are written in the memory circuits, and the image is displayed by reading the same signals stored in the memory circuits each time a new frame period is started. In the case where a still image is displayed after power supply to the display device is shut off once and then the display device is turned on, digital video signals stored in the non-volatile memory circuits C1 to C3 are read to display the still image. In this way, power consumption during still image display can be reduced greatly. Furthermore, the number of latch circuits is reduced to half the number of latch circuits in Embodiment 1. This embodiment is therefore space-saving in arrangement of the circuits, and can contribute to overall size reduction of the display device.

### Embodiment 3

[0197] This embodiment describes an example of a liquid crystal display device to which the circuit structure of the liquid crystal display device shown in Embodiment 2 and having no second latch circuit is applied, and which employs dot-sequential driving to write signals in memory circuits in each pixel.

[0198] FIG. 17 shows an example of the circuit structure for a source signal line driver circuit of a liquid crystal display device according to this embodiment. The circuit is capable of handling 3 bit digital gray scale signals, and is composed of shift register circuits 1701, latch circuits 1702, switching circuits 1703, and pixels 1704. Denoted by 1710 are signal lines to which signals are supplied from a gate signal line driver circuit, or directly from the external. The circuit structure of the pixels is the same as Embodiment 2, and hence FIG. 6 can be referred to as it is.

[0199] FIGS. 18A to 18C are timing charts regarding driving of the circuit of this embodiment. The description will be given with reference to FIG. 6, FIG. 17 and FIGS. 18A to 18C.

[0200] The operations from outputting sampling pulses from the shift register circuits 1701 through holding digital video signals in the latch circuits 1702 in response to the sampling pulses are the same as Embodiments 1 and 2. In this embodiment, the switching circuits 1703 are placed between the latch circuits 1702 and the volatile memory circuits in the pixels 1704. Therefore writing in the volatile memory circuits does not start immediately after completing holding the digital video signals in the latch circuits. The switching circuits 1703 are kept closed until the dot data sampling period is ended, and the latch circuits continue to hold the digital video signals as long as the switching circuits are closed.

[0201] As shown in FIG. 18B, the switching circuits 1703 are opened all at once upon receiving input of latch signals (latch pulses) during the retrace period that follows completion of holding digital video signals corresponding to one horizontal period. Then the digital video signals held in the latch circuits 1702 are simultaneously written in the volatile memory circuits in the pixels 1704. The operation in the pixels 1704 during this writing operation, and the operation in the pixels 1704 during reading operation for display in the next frame period are the same as Embodiment 2, and hence explanations thereof are omitted here. Also, how and when to write data in non-volatile memory circuits is the same as Embodiment 2, and hence explanations thereof will not be repeated.

[0202] In this way, driving in accordance with dot-sequential system can easily be made also when a source signal line driver circuit has no second latch circuit.

#### Embodiment 4

[0203] In Embodiment 4, a method of manufacturing TFTs of a pixel portion, a driver circuit portion (source signal line driver circuit, gate signal line driver circuit and pixel selection signal line driven circuit) formed in the periphery thereof in an active EL display device of the present invention simultaneously and a non-volatile storage circuit at the same time is explained. Note that a CMOS circuit which is a base unit is illustrated as the driver circuit portion to make a brief explanation.

[0204] First, as shown in FIG. 9A, a base film 5002 made from an insulating film such as a silicon oxide film, a silicon nitride film, or a silicon nitride oxide film is formed on a substrate 5001 made from glass such as barium borosilicate glass or aluminum borosilicate glass, typically Corning Corp. #7059 glass or #1737 glass. For example, a silicon nitride oxide film 5002a made from SiH<sub>4</sub>, NH<sub>3</sub>, and N<sub>2</sub>O by plasma CVD is formed with a thickness of 10 to 200 nm (preferably from 50 to 100 nm), and a hydrogenized silicon nitride oxide film 5002b with a thickness of 50 to 200 nm (preferably between 100 and 150 nm), made from SiH<sub>4</sub> and N<sub>2</sub>O, is similarly formed and laminated. The base film 5002 is shown as a two layer structure in Embodiment 4, but it may also be formed as a single layer of the above insulating films, and it may also be formed having a lamination structure in which two layers or more are laminated.

[0205] Island shape semiconductor layers 5003 to 5006 are formed by a crystalline semiconductor film manufactured using a laser crystallization method of a semiconductor film having an amorphous structure, or using a known thermal crystallization method. The thickness of the island-shape semiconductor layers 5003 to 5006 is formed to a thickness of 25 to 80 nm (preferably between 30 and 60 nm). There are no limitations in the crystalline semiconductor film material, but it is preferable to form the film from a silicon or a silicon germanium (SiGe) alloy.

[0206] A laser such as a pulse emission type or continuous emission type excimer laser, a YAG laser, and a YVO<sub>4</sub> laser can be used in the laser crystallization method to manufacture a crystalline semiconductor film. A method of condensing laser light emitted from a laser oscillator into a linear shape by an optical system and then irradiating the light to the semiconductor film may be used when these types of lasers are used. The crystallization conditions may be suitably selected by the operator, but when using the excimer laser, the pulse emission frequency is set to 30 Hz, and the laser energy

density is set from 100 to 400 mJ/cm<sup>2</sup> (typically between 200 and 300 mJ/cm<sup>2</sup>). Further, the second harmonic is utilized when using the YAG laser, the pulse emission frequency is set from 1 to 10 KHz, and the laser energy density may be set from 300 to 600 mJ/cm<sup>2</sup> (typically between 350 and 500 mJ/cm<sup>2</sup>). The laser light collected into a linear shape with a width of 100 to 1000 μm, for example 400 μm, is then irradiated over the entire surface of the substrate. This is performed with an overlap ratio of 80 to 98% for the linear shape laser light.

[0207] A gate insulating film 5007 is formed covering the semiconductor layers 5003 to 5006. A gate insulating film 5007 is formed by an insulating film containing silicon with a thickness of 40 to 150 nm by plasma CVD or sputtering. A 120 nm thick silicon nitride oxide film is formed in Embodiment 4. The gate insulating film is not limited to this type of silicon nitride oxide film, of course, and other insulating films containing silicon may also be used, in a single layer or in a lamination structure. For example, when using a silicon oxide film, it can be formed by plasma CVD with a mixture of TEOS (tetraethyl orthosilicate) and O<sub>2</sub>, at a reaction pressure of 40 Pa, with the substrate temperature set from 300 to 400° C., and by discharging at a high frequency (13.56 MHz) electric power density of 0.5 to 0.8 W/cm<sup>2</sup>. Good characteristics as a gate insulating film can be obtained by subsequently performing thermal annealing, at between 400 and 500° C., of the silicon oxide film thus manufactured.

[0208] A first conductive film 5008 and a second conductive film 5009 are then formed on the gate insulating film 5007 in order to form gate electrodes. The first conductive film 5008 is formed from Ta (tantalum) with a thickness of 50 to 100 nm, and the second conductive film 5009 is formed from W (tungsten) having a thickness of 100 to 300 nm, in Embodiment 4.

[0209] The Ta film is formed by sputtering of a Ta target by Ar. If appropriate amounts of Xe and Kr are added to Ar at the time of sputtering, the internal stress of the Ta film is relaxed, and film peeling can be prevented. The resistivity of an α phase Ta film is on the order of 20 μΩcm, and it can be used in the gate electrode, but the resistivity of a β phase Ta film is on the order of 180 μΩcm and it is unsuitable for the gate electrode. An α phase Ta film can easily be obtained if a tantalum nitride film, which possesses a crystal structure near that of α phase Ta, is formed with a thickness of about 10 to 50 nm as a base for Ta in order to form α phase Ta.

[0210] The W film is formed by sputtering with a W target, which can also be formed by thermal CVD using tungsten hexafluoride (WF<sub>6</sub>). Whichever is used, it is necessary to be able to make the film become low resistance in order to use it as the gate electrode, and it is preferable that the resistivity of the W film be made equal to or less than 20 μΩcm. The resistivity can be lowered by enlarging the crystal grains of the W film, but for cases in which there are many impurity elements such as oxygen in the W film, crystallization is inhibited, and the film becomes high resistance. A W target having a purity of 99.9999% is thus used in sputtering. In addition, by forming the W film while taking sufficient care that no impurities from within the gas phase are introduced at the time of film formation, a resistivity of 9 to 20 μΩcm can be achieved.

[0211] Note that, although the first conductive film 5008 is Ta and the second conductive film 5009 is W in Embodiment 4, the conductive films are not limited to these, and both may also be formed from an element selected from the group

consisting of Ta, W, Ti, Mo, Al, and Cu, or from an alloy material having one of these elements as its main component, or from a chemical compound of these elements. Further, a semiconductor film, typically a polysilicon film into which an impurity element such as phosphorous is doped, may also be used. Examples of preferable combinations other than that used in Embodiment 4 include: forming the first conductive film **5008** by tantalum nitride (TaN) and combining it with the second conductive film **5009** formed from W; forming the first conductive film **5008** by tantalum nitride (TaN) and combining it with the second conductive film **5009** formed from Al; and forming the first conductive film **5008** by tantalum nitride (TaN) and combining it with the second conductive film **5009** formed from Cu.

[0212] Then, a mask **5010** is formed from resist, and a first etching process is performed in order to form electrodes and wirings. An ICP (inductively coupled plasma) etching method is used in Embodiment 4. A gas mixture of  $\text{CF}_4$  and  $\text{Cl}_2$  is used as an etching gas, and a plasma is generated by applying a 500 W RF electric power (13.56 MHz) to a coil shape electrode at a pressure of 1 Pa. A 100 W RF electric power (13.56 MHz) is also applied to the substrate side (test piece stage), effectively applying a negative self-bias voltage. The W film and the Ta film are both etched on the same order when  $\text{CF}_4$  and  $\text{Cl}_2$  are combined.

[0213] The edge portions of the first conductive layer and the second conductive layer are made into a tapered shape in accordance with the effect of the bias voltage applied to the substrate side under the above etching conditions by using a suitable resist mask shape. The angle of the tapered portions is from 15 to 45°. The etching time may be increased by approximately 10 to 20% in order to perform etching without any residue remaining on the gate insulating film. The selectivity of a silicon nitride oxide film with respect to a W film is from 2 to 4 (typically 3), and therefore approximately 20 to 50 nm of the exposed surface of the silicon nitride oxide film is etched by this over-etching process. In this way, the first shape conductive layers **5011** to **5016** are thus formed from the first conductive layers and the second conductive layers (the first conductive layers **5011a** to **5016a** and the second conductive layers **5011b** to **5016b**) in accordance with the first etching process. At this time, regions of the gate insulating film **5007** not covered by first shape conductive layers **5011** to **5016** are made thinner by about 20 to 50 nm. (FIG. 9B)

[0214] A first doping process is then performed, and an impurity element which imparts n-type conductivity is added. The doping can be carried out by ion doping or ion implantation. Ion doping is performed under conditions of a dose amount from  $1 \times 10^{13}$  to  $5 \times 10^{14}$  atoms/cm<sup>2</sup> and an acceleration voltage of 60 to 100 keV. An element in periodic table group 15, typically phosphorous (P) or arsenic (As) is used as the impurity element which imparts n-type conductivity, and phosphorous (P) is used here. The conductive layers **5011** to **5016** become masks with respect to the n-type conductivity imparting impurity element in this case, and the first impurity regions **5017** to **5020** are formed in a self-aligning manner. The impurity element which imparts n-type conductivity is added to the first impurity regions **5017** to **5020** at a concentration in the range of  $1 \times 10^{20}$  to  $1 \times 10^{21}$  atoms/cm<sup>3</sup>. (FIG. 9B)

[0215] Next, as shown in FIG. 9C, a second etching process is performed without removing the resist mask. The etching gas of the mixture of  $\text{CF}_4$ ,  $\text{Cl}_2$  and  $\text{O}_2$  is used, and the W film is selectively etched. At this point, second shape conductive layers **5021** to **5026** (first conductive layers **5021a** to **5026a**

and second conductive layers **5021b** to **5026b**) are formed by the second etching process. Regions of the gate insulating film **5007**, which are not covered with the second shape conductive layers **5021** to **5026** are made thinner by about 20 to 50 nm by etching.

[0216] An etching reaction of the W film or the Ta film by the mixture gas of  $\text{CF}_4$  and  $\text{Cl}_2$  can be guessed from a generated radical or ion species and the vapor pressure of a reaction product. When the vapor pressures of fluoride and chloride of W and Ta are compared with each other, the vapor pressure of  $\text{WF}_6$  of fluoride of W is extremely high, and other  $\text{WCl}_5$ ,  $\text{TaF}_5$ , and  $\text{TaCl}_5$  have almost equal vapor pressures. Thus, in the mixture gas of  $\text{CF}_4$  and  $\text{Cl}_2$ , both the W film and the Ta film are etched. However, when a suitable amount of  $\text{O}_2$  is added to this mixture gas,  $\text{CF}_4$  and  $\text{O}_2$  react with each other to form CO and F, and a large number of F radicals or F ions are generated. As a result, an etching rate of the W film having the high vapor pressure of fluoride is increased. On the other hand, with respect to Ta, even if F is increased, an increase of the etching rate is relatively small. Besides, since Ta is easily oxidized as compared with W, the surface of Ta is oxidized by addition of  $\text{O}_2$ . Since the oxide of Ta does not react with fluorine or chlorine, the etching rate of the Ta film is further decreased. Accordingly, it becomes possible to make a difference between the etching rates of the W film and the Ta film, and it becomes possible to make the etching rate of the W film higher than that of the Ta film.

[0217] Then, as shown in FIG. 10A, a second doping process is performed. In this case, a dosage is made lower than that of the first doping process and under the condition of a high acceleration voltage, an impurity element for imparting the n-type conductivity is doped. For example, the process is carried out with an acceleration voltage set to 70 to 120 keV and at a dosage of  $1 \times 10^{13}$  atoms/cm<sup>2</sup>, so that new impurity regions are formed inside of the first impurity regions formed into the island-shape semiconductor layers in FIG. 10B. Doping is carried out such that the second shape conductive layers **5021** to **5026** are used as masks to the impurity element and the impurity element is added also to the regions under the first conductive layers **5021a** to **5026a**. In this way, second impurity regions **5027** to **5031** are formed. The concentration of phosphorous (P) added to the third impurity regions **5027** to **5031** has a gentle concentration gradient in accordance with the thickness of tapered portions of the first conductive layers **5021a** to **5026a**. Note that in the semiconductor layer that overlap with the tapered portions of the first conductive layers **5021a** to **5026a**, the impurity concentration slightly falls from the end portions of the tapered portions of the first conductive layers **5021a** to **5026a** toward the inner portions, but the concentration keeps almost the same level.

[0218] As shown in FIG. 10B, a third etching process is performed using the etching gas of  $\text{CHF}_3$ , and a reactive ion etching (RIE method) is used. By the third etching process, the tapered portion of the first conductive layers **5021a** to **5026a** are partly etched to contract the overlapping region of the first conductive layers with a semiconductor layer. Third shape conductive layers **5037** to **5040** (first conductive layers **5032a** to **5037a** and second conductive layers **5032b** to **5037b**) are formed by the third etching process. Regions of the gate insulating film **5007**, which are not covered with the third shape conductive layers **5032** to **5037** are made thinner by about 20 to 50 nm by etching.

[0219] By the third etching process, second impurity regions **5027a** to **5031a** that overlap with the first conductive

layers **5032a** to **5037a** and third impurity regions **5027b** to **5031b** between the first impurity region and the third impurity region, are formed in the second impurity regions **5027** to **5031**.

[0220] Fourth impurity regions **5039** to **5044** having a conductivity type which is the opposite of the first conductive type, are then formed as shown in FIG. 10C in the island shape semiconductor layer **5004** which forms p-channel TFTs. The third shape conductive layer **5033b** is used as a mask with respect to the impurity element, and the impurity regions are formed in a self-aligning manner. The island shape semiconductor layers **5003** and **5005**, which form n-channel TFTs, are covered over their entire surface areas by resist masks **5038**. Phosphorous is added in differing concentration to the impurity regions **5039** to **5044**, and ion doping is performed here using diborane ( $B_2H_6$ ), so that the impurity concentration in the regions becomes from  $2 \times 10^{20}$  to  $2 \times 10^{21}$  atoms/cm<sup>3</sup>.

[0221] Impurity regions are formed in the respective island shape semiconductor layers by the above processes. The third shape conductive layers **5032**, **5033**, **5035** and **5036** overlapping the island shape semiconductor layers function as gate electrodes. Reference numeral **5037** functions as floating gate electrode of the memory cell. Also reference numeral **5034** functions island shape source signal line. (FIG. 10C)

[0222] After removing the resist mask **5038**, the second gate insulating film is formed as shown in FIG. 11A. A thickness of the second gate insulating film **5045** may be 10 to 250 nm. It can be using known gas phase method (plasma CVD or sputtering and so on) as a method of film formation. Not that SiNO film is formed by plasma CVD having a thickness of 70 nm, in Embodiment 4.

[0223] A process of activating the impurity elements added to the respective island shape semiconductor layers is then performed with the aim of controlling conductivity type. Thermal annealing using an annealing furnace is performed for this process. In addition, laser annealing and rapid thermal annealing (RTA) can also be applied. Thermal annealing is performed with an oxygen concentration equal to or less than 1 ppm, preferably equal to or less than 0.1 ppm, in a nitrogen atmosphere at 400 to 700°C., typically between 500 and 600°C. Heat treatment is performed for 4 hours at 500°C. in Embodiment 4. However, for cases in which the wiring material used in the third shape conductive layers **5037** to **5040** is weak with respect to heat, it is preferable to perform activation after forming an interlayer insulating film (having silicon as its main constituent) in order to protect the wirings and the like.

[0224] In addition, heat treatment is performed for 1 to 12 hours at 300 to 450°C. in an atmosphere containing between 3 and 100% hydrogen, performing hydrogenation of the island shape semiconductor layers. This process is one of terminating dangling bonds in the island shape semiconductor layers by hydrogen which is thermally excited. Plasma hydrogenation (using hydrogen excited by a plasma) may also be performed as another means of hydrogenation.

[0225] Thereafter, a conductive film with a thickness of 200 to 400 nm is formed and patterned to form a control gate electrode **5046**. The control gate electrode **5046** is formed such that it partially or entirely overlaps a floating gate electrode **5037** with the second gate insulating film **5045** sandwiched therebetween (FIG. 11A).

[0226] A first interlayer insulating film **5047** is formed from a silicon oxynitride film having a thickness of 100 to 200 nm. Formed next are source wiring lines **5048** and **5050**

contacting the source region of the island-like semiconductor layer in the driver circuit portion, and a drain wiring line **5049** contacting the drain region thereof. In the pixel portion, connector electrodes **5051** and **5052** are formed. At the same time, connector electrodes **5053** and **5054** are formed in the memory cell portion. The connector electrode **5051** forms an electrical connection between the source signal line **5034** and the pixel TFT (FIG. 11B).

[0227] A second interlayer insulating film **5055** is formed thereon from an organic insulating material, and a pixel electrode **5056** is formed next. When the display device to be manufactured is a reflective liquid crystal display device as the one shown in this embodiment, the pixel electrode **5056** is desirably formed of a material having high reflectance, such as a film mainly containing Al or Ag or a laminate of a Al film and a Ag film.

[0228] In the manner described above, a driver circuit portion having an n-channel TFT and a p-channel TFT can be formed on the same substrate on which a pixel portion having a pixel TFT and volatile memory circuits is formed as shown in FIG. 11C. A substrate such as this is called an active matrix substrate in this specification.

[0229] After the active matrix substrate in the state of FIG. 11C is obtained an oriented film **5057** is formed on the active matrix substrate and subjected to rubbing treatment as shown in FIG. 12A.

[0230] An opposite substrate **5058** is prepared. On the opposite substrate **5058**, an opposite electrode **5059** is formed by patterning and an oriented film **5060** is formed and subjected to rubbing treatment. The opposite electrode is formed of an ITO film or like other transparent conductive materials.

[0231] A spacer (not shown) is formed on the active matrix substrate or the opposite substrate. The spacer may be spherical beads sprayed to the substrate. Alternatively, a photosensitive resin is patterned into dots or stripes in a display region. The spacer prevents orientation defect of a liquid crystal material.

[0232] A desirable cell gap for the reflective liquid crystal display device of this embodiment is 0.5 to 1.5 μm, considering retardation. In this embodiment, the cell gap in the pixel portion is set to 1.0 μm.

[0233] The active matrix substrate on which the pixel portion and the driver circuit portion are formed is then bonded to the opposite substrate using a seal **5061**. The seal **5061** has a filler mixed therein, and the filler, together with the spacer, keeps the distance uniform between the two substrates when they are bonded. A liquid crystal material **5062** is injected between the substrates, and then the substrates are completely sealed by an end sealing material (not shown). The liquid crystal material **5062** may be a known liquid crystal material. Thus completed is an active matrix liquid crystal display device shown in FIG. 12A.

[0234] The TFTs have a top gate structure in the active matrix liquid crystal display device manufactured by the above process. However, this embodiment can readily be applied to cases in which TFTs have a bottom gate structure or other structures.

[0235] Although a glass substrate is used in this embodiment the substrate is not limited to the glass substrate. This embodiment can be carried out also with a plastic substrate, a stainless steel substrate, a single crystal wafer, and the like.

[0236] The description given in this embodiment takes a reflective liquid crystal display device as an example. However, with a pixel electrode structured differently, the present

invention can readily be applied to a transmissive liquid crystal display device and to a semi-transmissive display device in which half the pixels have reflective electrodes and the rest of the pixels have transparent electrodes.

#### Embodiment 5

[0237] The display device of the present invention employs the time gray scale method to obtain gray scale display. Accordingly, if pixels have liquid crystal elements, a quicker response is required than the usual analog gray scale method and it is desirable to use a ferroelectric liquid crystal (FLC). This embodiment describes an example of fabricating a substrate suitable for a liquid crystal element made of a ferroelectric liquid crystal through the display device manufacture process introduced in Embodiment 4.

[0238] An active matrix substrate shown in FIG. 19A (corresponding to FIG. 11C) is fabricated in accordance with Embodiment 4.

[0239] An opposite substrate 5058 is prepared. On the opposite substrate 5058, an opposite electrode 5059 is formed by patterning. The opposite electrode is formed of an ITO film or like other transparent conductive materials.

[0240] Oriented films 5101 and 5102 are formed on the active matrix substrate and the opposite substrate, respectively. An oriented film RN 1286, a product of Nissan Chemical Industries, LTD., is formed and pre-baked at 90° C. for five minutes before post-baking it at 250° C. for an hour. The thickness of the film after post-baking is 40 nm. The oriented film is formed by flexographic printing or spinner application. The RN 1286 adheres poorly to a seal, and hence the oriented film is removed from the positions where the seal is to be placed. Also, the oriented film is not formed on a contact pad for electrically connecting the active matrix substrate with the opposite substrate and on a lead wire for connecting a flexible printed circuit (FPC).

[0241] The oriented films 5101 and 5102 are subjected to rubbing treatment. In the rubbing treatment, the rubbing directions are set to be parallel to each other when the opposite substrate 5058 is bonded to the active matrix substrate. Rubbing cloth used in the rubbing treatment is YA-20R, a product of Yoshikawa Chemical. A rubbing apparatus produced by Joyo Engineering, Co., LTD, is used to subject the oriented films to rubbing once with the depression amount set to 0.25 mm, the roll rpm to 100 rpm, and the stage rate to 10 mm/sec. The diameter of the rubbing roll is 130 mm. After the rubbing, the oriented films are washed by running water over the substrate surfaces.

[0242] A seal 5103 is formed next. The seal is patterned into a shape having one liquid crystal material inlet so that the liquid crystal material can be injected in vacuum.

[0243] The seal is formed on the opposite substrate using a seal dispenser produced by Hitach Chemical Co., Ltd. The seal used is XN-21S, a product of Mitsui Chemicals, Inc. The seal is subjected to test baking at 90° C. for thirty minutes and then gradually cooled for the following fifteen minutes.

[0244] It is a known fact that the seal XN-21S can provide a cell gap of merely 2.3 to 2.6  $\mu\text{m}$  even after subjected to thermal pressing. Then, in order to obtain a cell gap of 1.0  $\mu\text{m}$ , the seal is arranged in a region where the laminate is thinner than the pixel portion by 1.5  $\mu\text{m}$  or more. In this embodiment, the seal 5103 is placed in a region where a first interlayer insulating film 5047 and a second interlayer insulating film 5055 are removed by etching.

[0245] A conductive spacer (not shown) is formed at the same time the seal is formed.

[0246] The spacer (not shown) is formed on the active matrix substrate or the opposite substrate. The spacer may be spherical beads sprayed to the substrate. Alternatively, a photosensitive resin is patterned into dots or stripes in a display region. The spacer prevents orientation defect of a liquid crystal material.

[0247] A desirable cell gap for a reflective liquid crystal display device is 0.5 to 1.5  $\mu\text{m}$ , considering retardation. In this embodiment, the cell gap in the pixel portion is set to 1.0  $\mu\text{m}$ .

[0248] After that, with a bonding apparatus by Newton Corporation, the active matrix substrate and the opposite substrate are bonded to each other by aligning markers on the substrates.

[0249] The seal is then thermally cured in a clean oven at 160° C. for three hours while applying a pressure of 0.3 to 1.0 kgf/cm<sup>2</sup> to the entire surfaces of the substrates in the direction perpendicular to the substrate plane. The opposite substrate and the active matrix substrate are thus bonded.

[0250] A pair of substrates consisting of the bonded opposite substrate and active matrix substrate are cut into pieces.

[0251] A liquid crystal material 5104 is a bistable ferroelectric liquid crystal or a tristable ferroelectric liquid crystal.

[0252] The liquid crystal material is heated until it reaches the isotropic phase and then injected. Thereafter, the liquid crystal material is gradually cooled at 0.1° C. per minute to room temperature (FIG. 19B).

[0253] A UV-curable resin (not shown) as an end-sealing material is applied by a small-sized dispenser so as to cover the liquid crystal material inlet.

[0254] The flexible printed board (not shown) is then bonded using an anisotropic conductive film (not shown) to complete an active matrix liquid crystal display device.

[0255] If a pixel electrode on the active matrix substrate is formed of a transparent conductive film, a transmissive liquid crystal display device can also be formed by the manufacture process of this embodiment. A desirable cell gap for the transmissive liquid crystal display device is 1.0 to 2.5  $\mu\text{m}$ , considering retardation and avoiding the helical structure of the ferroelectric liquid crystal.

#### Embodiment 6

[0256] Static random access memories (SRAM) are used for the volatile memory circuits in the pixel portions of the liquid crystal display devices according to Embodiments 1 through 3 of the present invention. However, the volatile memory circuits are not limited to SRAM. Dynamic random access memories (DRAM) can be given as other volatile memory circuits employable by a pixel portion in a liquid crystal display device of the present invention. This embodiment shows an example of using various memory circuits.

[0257] FIG. 8 shows the case in which DRAM is used for volatile memory circuits A1 to A3 and B1 to B3 arranged in a pixel. The basic structure thereof is the same as the circuits shown in Embodiment 1. The DRAM used for the volatile memory circuits A1 to A3 and B1 to B3 may have a general structure. In this embodiment, a relatively simple structure comprised of an inverter and a capacitor storage as shown in FIG. 8 is used.

[0258] The operation of a source signal line driver circuit is the same as Embodiment 1. Unlike SRAM, DRAM requires rewriting for once in a while (the rewriting operation is hereinafter referred to as refresh), and therefore is connected to

refresh TFTs **801** to **803**. Refresh is achieved by turning the refresh TFTs **801** to **803** conductive at some point in a still image display period (the period during which digital video signals stored in the volatile memory circuits are repeatedly read out to display a still image), so that electric charges in a pixel portion is returned to the volatile memory circuit side.

[0259] Still another format of memory circuits that can be used to constitute a pixel portion in a liquid crystal display device of the present invention is, though not shown in the drawing, ferroelectric random access memory (FeRAM). FeRAM is a non-volatile memory and having the same level of writing speed as SRAM and DRAM. Characteristics of FeRAM, including low writing voltage, can be utilized to further reduce power consumption of the liquid crystal display device of the present invention. Flash memories may also be used to constitute the memory circuits of the present invention.

#### Embodiment 7

[0260] An active matrix semiconductor display device made from a driver circuit of the present invention has various uses. In the present embodiment, a description will be given on a semiconductor device incorporating an active matrix semiconductor display device made from a driver circuit of the present invention.

[0261] The following can be given as examples of these semiconductor devices: a portable information terminal (such as an electronic book, a mobile computer, and a portable telephone), a video camera, a digital camera, a personal computer and a television. Examples of those are shown in FIGS. 15 and 16.

[0262] FIG. 15A is a portable telephone, and is composed of a main body **2601**, an audio output portion **2602**, an audio input portion **2603**, a display portion **2604**, operation switches **2605**, and an antenna **2606**. The present invention can be applied to the display portion **2604**.

[0263] FIG. 15B is a video camera, and is composed of a main body **2611**, a display portion **2612**, an audio input portion **2613**, operation switches **2614**, a battery **2615**, and an image receiving portion **2616**. The present invention can be applied to the display portion **2612**.

[0264] FIG. 15C is a mobile computer or a portable type information terminal, and is composed of a main body **2621**, a camera portion **2622**, an image receiving portion **2623**, operation switches **2624**, and a display portion **2625**. The present invention can be applied to the display portion **2625**.

[0265] FIG. 15D is a head mount display, and is composed of a main body **2631**, a display portion **2632**, and an arm portion **2633**. The present invention can be applied to the display portion **2632**.

[0266] FIG. 15E is a television, and is composed of a main body **2641**, speakers **2642**, a display portion **2643**, a receiving device **2644**, and an amplification device **2645**. The present invention can be applied to the display portion **2643**.

[0267] FIG. 15F is a portable electronic book, and is composed of a main body **2651**, a display device **2652**, a memory medium **2653**, an operation switch **2654** and an antenna **2655**. The book is used to display data stored in a mini-disk (MD) or a DVD (Digital Versatile Disk), or a data received with the antenna. The present invention can be applied to the display portion **2652**.

[0268] FIG. 16A is a personal computer, and is composed of a main body **2701**, an image inputting portion **2702**, a

display device **2703** and a keyboard **2704**. The present invention can be applied to the display portion **2703**.

[0269] FIG. 16B is a player that employs a recording medium in which programs are recorded, and is composed of a main body **2711**, a display portion **2712**, a speaker portion **2713**, a recording medium **2714**, and an operation switch **2715**. Note that this player uses a DVD (Digital Versatile Disc), CD and the like as the recording medium to appreciate music and films, play games, and connect to the Internet. The present invention can be applied to the display portion **2612**.

[0270] FIG. 16C is a digital camera comprising a main body **2721**, a display portion **2722**, an eye piece **2723**, operation switches **2724**, and an image receiving portion (not shown). The present invention can be applied to the display portion **2722**.

[0271] FIG. 16D is ahead mount display comprising a display portion **2731**, and a band portion **2732**. The present invention can be applied to the display portion **2731**.

#### Embodiment 8

[0272] FIG. 21 shows an example of applying the present invention to a portable information terminal. In this example, a video signal processing circuit **2107** of a CPU **2106**, VRAM **2111** and some other circuits stop their functions during a still image is displayed to reduce power consumption. In FIG. 21, parts which operate are indicated by dotted lines. A controller **2112** may be mounted to a display device **2113** by COG or incorporated in the display device. FIGS. 22 and 23 show an example of applying the present invention to a cellular phone. Similar to the case shown in FIG. 21, some functions can be stopped during still image display to reduce power consumption.

[0273] A plurality of memory circuits arranged in each pixel are used to store digital video signals, so that the digital video signals stored in the memory circuits can be repeatedly used for every new frame period to display a still image continuously. Thus an external circuit, a source signal line driver circuit, and other circuits can stop their operations during the still image is displayed. Furthermore, non-volatile memory circuits arranged in each pixel are used to hold digital video signals, making it possible to keep the digital video signals stored after power supply is shut off. Accordingly, the invention can greatly contribute to overall power consumption reduction of a liquid crystal display device.

1. (canceled)
2. A display device comprising:
  - a first gate signal line;
  - a second gate signal line;
  - a source signal line; and
  - a pixel comprising:
    - a first transistor electrically connected to the first gate signal line and the source signal line;
    - a second transistor electrically connected to the second gate signal line and the source signal line;
    - a first memory circuit electrically connected to the first transistor, the first memory circuit being configured to hold a first bit signal;
    - a second memory circuit electrically connected to the second transistor, the second memory circuit being configured to hold a second bit signal,

wherein one of a source and a drain of the first transistor is directly connected to the source signal line,

wherein one of a source and a drain of the second transistor is directly connected to the source signal line,

wherein the pixel is configured to express light gradation using the first bit signal and the second bit signal.

**3. A display device comprising:**

a gate signal line;  
a first source signal line;  
a second source signal line; and  
a pixel comprising:

a first transistor electrically connected to the gate signal line and the first source signal line;

a second transistor electrically connected to the gate signal line and the second source signal line;

a first memory circuit electrically connected to the first transistor, the first memory circuit being configured to hold a first bit signal; and

a second memory circuit electrically connected to the second transistor, the second memory circuit being configured to hold a second bit signal,

wherein one of a source and a drain of the first transistor is directly connected to the first source signal line,

wherein one of a source and a drain of the second transistor is directly connected to the second source signal line,

wherein the pixel is configured to express light gradation using the first bit signal and the second bit signal.

**4. A display device comprising:**

a first gate signal line;

a second gate signal line;

a source signal line; and

a pixel comprising:

a first transistor electrically connected to the first gate signal line and the source signal line;

a second transistor electrically connected to the second gate signal line and the source signal line;

a first memory circuit electrically connected to the first transistor, the first memory circuit being configured to hold a first bit signal;

a second memory circuit electrically connected to the second transistor, the second memory circuit being configured to hold a second bit signal;

a third transistor electrically connected to the first memory circuit; and

a fourth transistor electrically connected to the second memory circuit,

wherein one of a source and a drain of the first transistor is directly connected to the source signal line,

wherein one of a source and a drain of the second transistor is directly connected to the source signal line, and

wherein the pixel is configured to express gradation using the first bit signal and the second bit signal.

**5. The display device according to claim 2, wherein each of the first and second memory circuits is a memory circuit selected from the group consisting of a static memory circuit, a ferroelectric memory circuit and a dynamic memory circuit.**

**6. The display device according to claim 3, wherein each of the first and second memory circuits is a memory circuit selected from the group consisting of a static memory circuit, a ferroelectric memory circuit and a dynamic memory circuit.**

**7. The display device according to claim 4, wherein each of the first and second memory circuits is a memory circuit selected from the group consisting of a static memory circuit, a ferroelectric memory circuit and a dynamic memory circuit.**

**8. The display device according to claim 2, further comprising a driver circuit configured to control the pixel,**

wherein the driver circuit comprises a driver circuit transistor and the first memory circuit comprises a memory transistor,

wherein the driver circuit transistor, the memory transistor and the first transistor are thin film transistors formed on a same substrate.

**9. The display device according to claim 3, further comprising a driver circuit configured to control the pixel,**

wherein the driver circuit comprises a driver circuit transistor and the first memory circuit comprises a memory transistor,

wherein the driver circuit transistor, the memory transistor and the first transistor are thin film transistors formed on a same substrate.

**10. The display device according to claim 4, further comprising a driver circuit configured to control the pixel,**

wherein the driver circuit comprises a driver circuit transistor and the first memory circuit comprises a memory transistor,

wherein the driver circuit transistor, the memory transistor and the first transistor are thin film transistors formed on a same substrate.

**11. The display device according to claim 2, further comprising a driver circuit configured to control the pixel,**

wherein the driver circuit comprises a driver circuit transistor and the first memory circuit comprises a memory transistor,

wherein the driver circuit transistor, the memory transistor and the first transistor are thin film transistors formed on a same semiconductor layer.

**12. The display device according to claim 3, further comprising a driver circuit configured to control the pixel,**

wherein the driver circuit comprises a driver circuit transistor and the first memory circuit comprises a memory transistor,

wherein the driver circuit transistor, the memory transistor and the first transistor are thin film transistors formed on a same semiconductor layer.

**13. The display device according to claim 4, further comprising a driver circuit configured to control the pixel,**

wherein the driver circuit comprises a driver circuit transistor and the first memory circuit comprises a memory transistor,

wherein the driver circuit transistor, the memory transistor and the first transistor are thin film transistors formed on a same semiconductor layer.

**14. The display device according to claim 2, wherein the first and second memory circuits are formed over a substrate selected from the group consisting of a glass substrate, a plastic substrate, a stainless substrate and a single crystal wafer.**

**15. The display device according to claim 3, wherein the first and second memory circuits are formed over a substrate selected from the group consisting of a glass substrate, a plastic substrate, a stainless substrate and a single crystal wafer.**

**16. The display device according to claim 4, wherein the first and second memory circuits are formed over a substrate selected from the group consisting of a glass substrate, a plastic substrate, a stainless substrate and a single crystal wafer.**

**17. The display device according to claim 2, wherein the display device is applied to a portable information apparatus**

selected from the group consisting of a portable telephone, a personal computer, a navigation system, a PDA, and an electronic book.

**18.** The display device according to claim **3**, wherein the display device is applied to a portable information apparatus selected from the group consisting of a portable telephone, a personal computer, a navigation system, a PDA, and an electronic book.

**19.** The display device according to claim **4**, wherein the display device is applied to a portable information apparatus selected from the group consisting of a portable telephone, a personal computer, a navigation system, a PDA, and an electronic book.

\* \* \* \* \*

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#### 摘要(译)

通过使用具有新颖电路结构的驱动电路和像素来提供具有低功耗的液晶显示装置。在使用n ( n是自然数且满足n≥2 ) 位数字视频信号以显示图像的液晶显示装置中，n×m ( m是自然数 ) 存储电路和n×k ( k是自然的 ) 在每个像素中提供非易失性存储电路，从而给予该装置在存储电路中存储n帧数字视频信号的功能和在非易失性存储电路中存储k帧数字视频信号的功能。一旦存储在存储器电路中，就针对每个新帧重复读出数字视频信号以显示静止图像，从而可以在静止图像显示期间停止源信号线驱动电路的驱动。此外，存储在非易失性存储电路中的数字视频信号在电源关闭后保持存储，因此下次显示装置开启时可立即显示存储数据的图像。

