



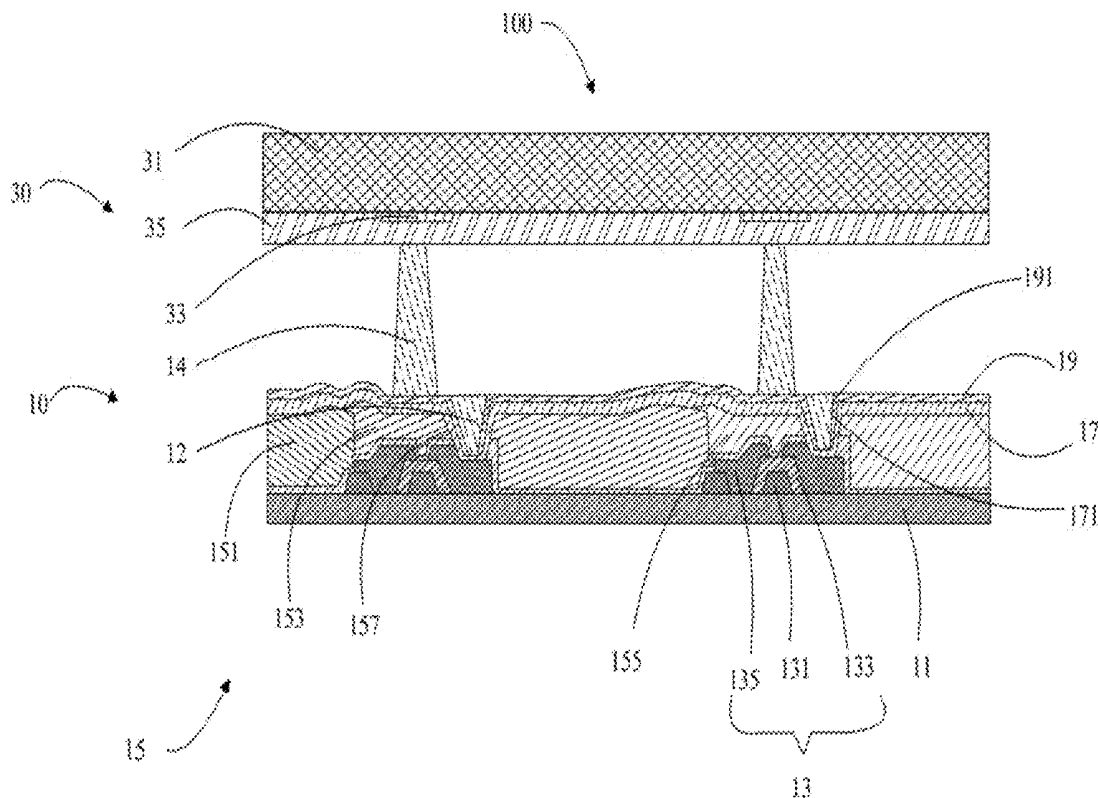
US 20180188626A1

(19) **United States**(12) **Patent Application Publication**
Chien(10) **Pub. No.: US 2018/0188626 A1**(43) **Pub. Date: Jul. 5, 2018**(54) **DISPLAY PANEL, METHOD OF
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DISPLAY USING THE SAME**(71) Applicants: **HKC Corporation Limited**, Shenzhen
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078052, filed on Mar. 24, 2017.(30) **Foreign Application Priority Data**

Dec. 29, 2016 (CN) 201611250653.0

Publication Classification(51) **Int. Cl.**
G02F 1/1362 (2006.01)
G02F 1/1368 (2006.01)
H01L 27/12 (2006.01)**H01L 21/027** (2006.01)**G02F 1/1339** (2006.01)(52) **U.S. Cl.**CPC **G02F 1/136286** (2013.01); **G02F 1/1368**
(2013.01); **H01L 27/127** (2013.01); **H01L**
27/1288 (2013.01); **H01L 27/1222** (2013.01);
H01L 29/66765 (2013.01); **H01L 27/124**
(2013.01); **G02F 1/13394** (2013.01); **G02F**
2202/02 (2013.01); **G02F 2202/103** (2013.01);
G02F 2001/136295 (2013.01); **H01L 21/0274**
(2013.01)(57) **ABSTRACT**

A display panel is disclosed that includes a first substrate, a second substrate, and a liquid crystal layer sandwiched between the second substrate and the first substrate. The first substrate includes a first base, a switch array layer disposed on the first base, a filter layer covering the first base and the switch array layer, and a passivation layer and a first conductive layer disposed in succession on the filter layer. The filter layer has a first through hole. The first conductive layer is coupled through the first through hole of the filter layer to the switch array layer. The first conductive layer is defined with at least one recess which may be filled with a filler. There are also disclosed a method of manufacturing the display panel and a display to which the display panel is applied.



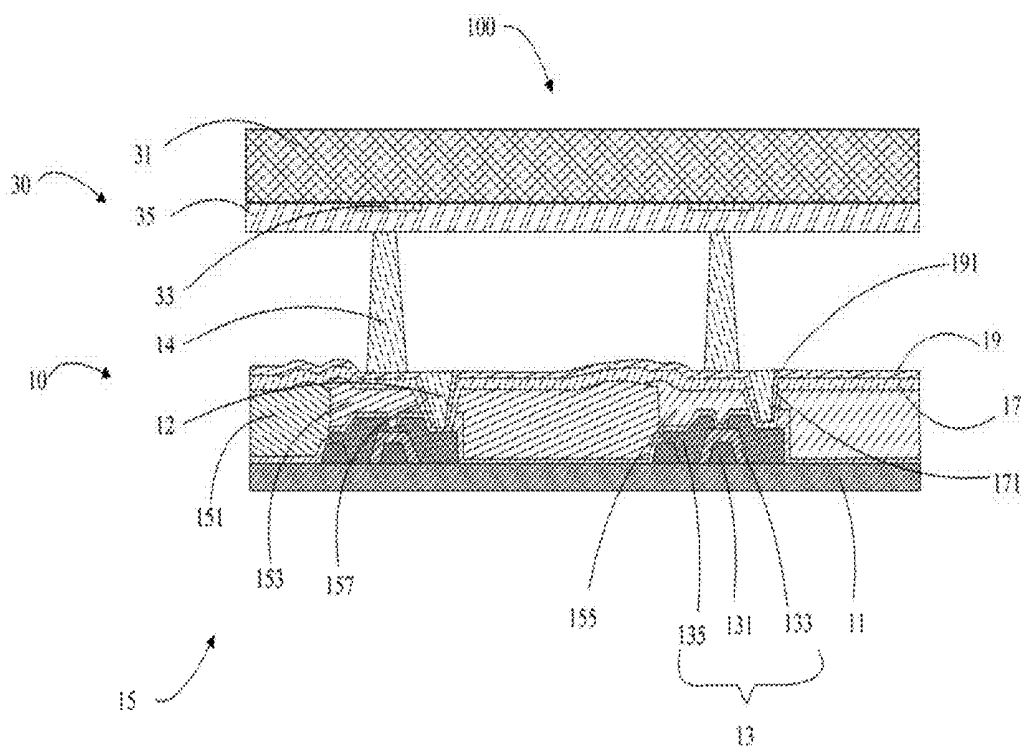


FIG. 1

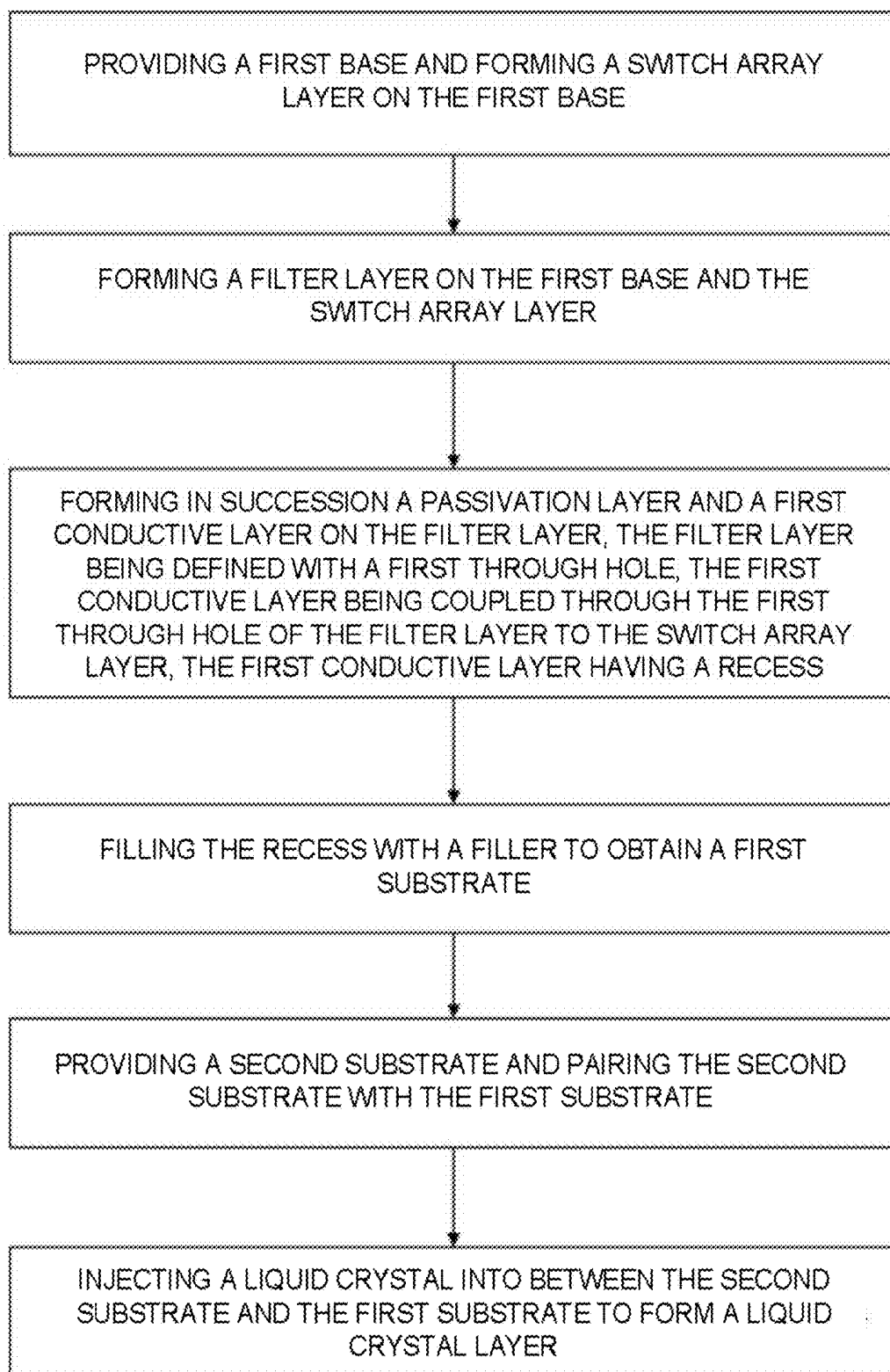


FIG. 2

DISPLAY PANEL, METHOD OF MANUFACTURING THE SAME, AND DISPLAY USING THE SAME

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of PCT/CN2017/078052 filed on Mar. 24, 2017, entitled “DISPLAY PANEL, METHOD OF MANUFACTURING THE SAME, AND DISPLAY USING THE SAME”, and the entire contents of which is hereby incorporated by reference.

BACKGROUND OF THE DISCLOSURE

1. Field of the Disclosure

[0002] The present disclosure relates generally to display technologies, and more particularly to a display panel, a method of manufacturing the same, and a display using the same.

2. Description of the Prior Art

[0003] A display panel generally includes a first substrate, a second substrate, and a liquid crystal layer sandwiched between the first substrate and the second substrate. A pixel electrode of the first substrate may be defined with a concave portion and so the pixel electrode can be coupled through concave portion to a source electrode and a drain electrode. However, when liquid crystal is injected into between the first substrate and the second substrate, the liquid crystal may flow into the concave portion, resulting in a poor diffusion of the liquid crystal, thereby affecting the quality of the display panel.

SUMMARY OF THE DISCLOSURE

[0004] In view of the above problems, the present disclosure provides a display panel in order to solve to a certain degree the problem of poor quality of the display panel in the prior art.

[0005] To solve the above problems, the present disclosure provides a display panel that includes a first substrate, a second substrate, and a liquid crystal layer sandwiched between the second substrate and the first substrate. The first substrate may include a first base, a switch array layer disposed on the first base, a filter layer covering the first base and the switch array layer, and a passivation layer and a first conductive layer provided in succession on the surface of the filter layer. The filter layer may have a first through hole. The first conductive layer may be coupled through the first through hole of the filter layer to the switch array layer. The first conductive layer may be defined with at least one recess which may be filled with a filler.

[0006] The recess may have a depth of 1 to 2 μm , and the filler may have a height of 1 to 2 μm .

[0007] The filler may be of polyimide or polymethyl methacrylate.

[0008] The filter layer may be defined with at least one first through hole, and a part of the passivation layer may be accommodated within the first through hole. The partial passivation layer may be defined with at least one second through hole, and a part of the first conductive layer may be received within the second through hole. The first conductive layer may be coupled through the first through hole of the filter layer and the second through hole to the switch

array layer, and the recess may be defined in the partial first conductive layer that is received within the second through hole.

[0009] The filter layer may include a plurality of color resist elements connected in series, and every two adjacent color resist elements may overlap.

[0010] The switch array layer may include a first metal layer disposed on the first base, an intermediate layer provided on the first metal layer and the first base, and a second metal layer disposed on the intermediate layer, the first metal layer, and the first base. The first conductive layer may be coupled to the second metal layer.

[0011] The first metal layer may be a first metal composite layer, being a molybdenum-aluminum metal composite layer, a molybdenum-aluminum alloy composite layer, a titanium-aluminum metal composite layer, or a copper-molybdenum metal composite layer.

[0012] The second metal layer may be a second metal composite layer, being a molybdenum-aluminum-molybdenum metal composite layer, a titanium-aluminum-titanium composite layer, or a copper-molybdenum metal composite layer.

[0013] The intermediate layer may include an insulating layer and an amorphous silicon layer that are disposed in succession on the surface of the first metal layer and the surface of the first base.

[0014] A protective layer may be formed between the filter layer and the second metal layer. Both the protective layer and the passivation layer may be of monosilicon mononitride or trisilicon tetranitride (also abbreviated as silicon nitride).

[0015] The second substrate may include a second base, a matrix layer disposed on the second base, and a second conductive layer provided on the second base and the matrix layer.

[0016] Both the first conductive layer and the second conductive layer may be translucent or transparent conductive metal layers.

[0017] The translucent or transparent conductive metal layer is made of indium oxide, tin oxide, zinc oxide, cadmium oxide, cadmium-indium oxide, tin-cadmium oxide, zinc-tin oxide, a mixture of indium oxide and zinc oxide, or tin-doped indium trioxide.

[0018] The display panel may further include multiple spacer columns connected between the first conductive layer and the second conductive layer.

[0019] The spacer columns may be of polyimide or polymethyl methacrylate.

[0020] There is also provided a method of manufacturing a display panel, the method comprising:

[0021] providing a first base and forming a switch array layer on the first base;

[0022] forming a filter layer on the first base and the switch array layer, the filter layer being defined with a first through hole;

[0023] forming in succession a passivation layer and a first conductive layer on the filter layer, the first conductive layer being coupled through the first through hole of the filter layer to the switch array layer and being defined with a recess;

[0024] filling the recess with a filler to obtain a first substrate;

[0025] providing a second substrate and pairing the second substrate with the first substrate; and

[0026] injecting a liquid crystal into between the second substrate and the first substrate to form a liquid crystal layer.

[0027] The preparation of the filter layer may comprise:

[0028] providing a photoresist;

[0029] coating the first base and the switch array layer with the photoresist to form a photoresist film;

[0030] performing photolithography with the photoresist film to form a plurality of color resist elements, every two adjacent color resist elements overlapping and the filter layer being defined with at least one first through hole.

[0031] Filling the recess with the filler may comprise:

[0032] filling the recess with an organic solvent and coating the surface of the first conductive layer with an organic material to form an organic layer; and

[0033] performing photolithography with the organic layer to form a plurality of spacer columns and at least one filler, the plurality of spacer columns being connected between the first conductive layer and the second substrate, the recess being filled with the filler.

[0034] The preparation of the second substrate may include:

[0035] providing a second base;

[0036] disposing a matrix layer on the second base; and

[0037] plating a second conductive layer on the surface of the second base and the surface of the matrix layer.

[0038] There is further provided a display that includes the display panel. The display panel may include a first substrate, a second substrate, and a liquid crystal layer sandwiched between the second substrate and the first substrate. The first substrate may include a first base, a switch array layer disposed on the first base, a filter layer covering the first base and the switch array layer, and a passivation layer and a first conductive layer provided in succession on the surface of the filter layer. The filter layer may have a first through hole. The first conductive layer may be coupled through the first through hole of the filter layer to the switch array layer. The first conductive layer may be defined with at least one recess which may be filled with a filler.

[0039] Advantages of the present disclosure may follow: according to the present disclosure the filter layer is defined with a first through hole and the first conductive layer is coupled through the first through hole of the filter layer to the switch array layer, while the first conductive layer is provided with at least one recess which is filled with a filler. Since the recess is filled with the filler, the liquid crystal would not flow into the recess when rejected into between the first substrate and the second substrate. Therefore, the liquid crystal can be uniformly distributed between the first substrate and the second substrate, so that the resulting display panel can have a superior quality.

BRIEF DESCRIPTION OF THE DRAWINGS

[0040] In order to more clearly illustrate the embodiments of the present disclosure or the prior art solutions, a brief description of the accompanying drawings for use in the illustration of the embodiments herein or the prior art are provided below. It is obvious that the drawings described below depict merely some embodiments of the disclosure and those of ordinary skill in the art can obtain other drawings based on the arrangements shown in these drawings without making inventive efforts.

[0041] FIG. 1 shows a schematic view of a display panel according to an embodiment of the present disclosure.

[0042] FIG. 2 shows a flowchart illustrating a method of manufacturing a display panel according to an embodiment of the present disclosure.

Description of Reference Numerals:	
Reference Numeral	Name
100	Display panel
10	First substrate
11	First base
12	Filler
13	Switch array layer
131	First metal layer
133	Intermediate layer
135	Second metal layer
14	Spacer column
15	Filter layer
151	First color resist element
153	Second color resist element
155	Third color resist element
157	First through hole
17	Passivation layer
171	Second through hole
19	First conductive layer
191	Recess
30	Second substrate
31	Second base
33	Matrix layer
35	Second conductive layer

[0043] The foregoing objects, features and advantages of the present disclosure will be described in further detail with reference to the accompanying drawings.

DETAILED DESCRIPTION

[0044] Embodiments of the present disclosure will now be described in such definite and comprehensive details with reference to the accompanying drawings of the disclosure. It is obvious that the embodiments described herein constitute merely part but not all of the embodiments of the disclosure. Therefore all other embodiments obtained by those of ordinary skill in the art based on the embodiments of the present disclosure without making inventive efforts shall all fall in the scope of the disclosure.

[0045] It should be noted that in the embodiments herein all directional indications, e.g., up, down, left, right, front, back, . . . , are only intended to illustrate the relative positional relationships or motions among various components under a certain posture or arrangement (as shown in the drawings), thus a directional indication would vary accordingly should the particular posture change.

[0046] In addition, references to “first,” “second,” and the like herein are for illustration purposes only, and are not to be construed as indicating or implying their relative importance or implicitly indicating the number of technical features involved. Thus, a feature that is defined by “first,” or “second,” and the like may include at least one such feature, either explicitly or implicitly. Furthermore, solutions of

various embodiments can be combined with one another. However, any such combinations should be predicated on the achievability by those of ordinary skill in the art. Hence, any combinations of solutions should be considered to be absent nor within the claimed scope of the disclosure should such combinations end up in contradiction or unachievability.

[0047] Referring to FIG. 1, there is provided a display panel 100.

[0048] The display panel 100 may include a first substrate 10, a second substrate 30, and a liquid crystal layer sandwiched between the second substrate 30 and the first substrate 10. The first substrate 10 may include a first base 11, a switch array layer 13 disposed on the first base 11, a filter layer 15 covering the first base 11 and the switch array layer 13, and a passivation layer 17 and a first conductive layer 19 disposed in succession on the surface of the filter layer 15. The filter layer 15 may have a first through hole 157. The first conductive layer 19 may be coupled through the first through hole 157 of the filter layer 15 to the switch array layer 13. The first conductive layer 19 may be defined with at least one recess 191 which may be filled with a filler 12.

[0049] In the present embodiment, the number of the recesses 191 can be, e.g., 2, in order to correspond to two switch array layers 13.

[0050] That is, the filter layer 15 may be defined with a first through hole 157, and the first conductive layer 19 may be coupled through the first through hole 157 of the filter layer 15 to the switch array layer 13. The first conductive layer 19 may be provided with at least one recess 191, inside which may be filled via a filler 12. Since the recess 191 is filled with the filler 12, the liquid crystal would not flow into the recess 191 when rejected into between the first substrate 10 and the second substrate 30. Therefore, the liquid crystal can be uniformly distributed between the first substrate 10 and the second substrate 30, thereby the resulting display panel 100 can have a superior quality.

[0051] The recess 191 may have a depth of 1 to 2 μm , and the filler 12 may have a height of 1 to 2 μm .

[0052] That is, the recess 191 may have a depth of 12 μm while the filler 12 may have a height of 1-2 μm , the recess 191 being filled with the filler 12. Furthermore, the surface of the filler 12 near the second substrate 30 may be flush with the surface of the first conductive layer 19. Therefore, when the liquid crystal is injected into between the first substrate 10 and the second substrate 30, the liquid crystal would not flow into the recess 191, because the recess 191 is filled with the filler 12 and the surface of the filler 12 near the second substrate 30 is level with the surface of the first conductive layer 19, and so the liquid crystal can be evenly distributed between the first substrate 10 and the second substrate 30, enabling the resulting display panel 100 with a superior quality.

[0053] The filler 12 may be of a polyimide material or a polymethyl methacrylate material.

[0054] In other words, the filler 12 may be made of a polyimide material or a polymethyl methacrylate material, so that the recess 191 can be sealed by the filler 12, and thus the liquid crystal can be prevented from flowing into the recess 191.

[0055] The filter layer 15 may be provided with at least one first through hole 157, and a part of the passivation layer 17 may be accommodated inside the first through hole 157. The partial passivation layer 17 may be defined with at least

one second through hole 171, and a part of the first conductive layer 19 may be accommodated within the second through hole 171, where the recess 191 may be defined in the part of the first conductive layer 19 that is received in the second through hole 171.

[0056] The number of the first through holes 157, the second through holes 171, and the recesses 191 can be determined according to actual production requirements. In the present embodiment, the number of the first through holes 157, the number of the second through holes 171, and the number of the recesses 191 can all be two.

[0057] That is, a part of the passivation layer 17 may be accommodated inside the first through hole 157 of the filter layer 15, in turn a part of the first conductive layer 19 may be held inside the second through hole 171. The recess 191 may be defined in the part of the first conductive layer 19 that is received within the second through hole 171. The first through hole 157, the second through hole 171, and the recess 191 can be connected with each other, so that the first conductive layer 19 can be coupled through the first through hole 157 and the second through hole 171 to the second metal layer 135.

[0058] The filter layer 15 may include a plurality of color resist elements connected in series, and every two adjacent color resist elements may overlap.

[0059] The filter layer 15 may be a color filter, including a first color resist element 131 (red resist), a second color resist element 133 (green resist), and a third color resist element 135 (blue resist).

[0060] Among the multiple color resist elements sequentially connected according to the solution of the present disclosure, every two adjacent color resist elements may overlap, thereby providing a superior color display with the display panel 100.

[0061] The switch array layer 13 may include a first metal layer 131 disposed on the first base 11, an intermediate layer 133 provided on the first metal layer 131 and the first base 11, and a second metal layer 135 disposed on the intermediate layer and the first base 11. The first conductive layer 19 may be coupled to the second metal layer 135.

[0062] The first metal layer 131 may form a gate, a gate line, and a common electrode.

[0063] The second metal layer 135 may form a source and a drain.

[0064] The intermediate layer 133 may include an insulating layer and an amorphous silicon layer that are disposed in succession on the surface of the first metal layer 131 and the surface of the first base 11. The insulating layer may be a silicon nitride (SiN_x) layer or a gate-silicon nitride (G-SiN_x) layer, x being 1 or $\frac{3}{4}$. The amorphous silicon layer may include an amorphous silicon ($\alpha\text{-Si}$) layer and an N-type amorphous silicon ($\text{N}+\alpha\text{-Si}$) layer deposited on the amorphous silicon layer.

[0065] That is, the switch array layer 13 may include a first metal layer 131, an intermediate layer 133, and a second metal layer 135 plated on the intermediate layer and the first base 11, so that the display panel 100 can operate properly.

[0066] The first metal layer 131 may be a first metal composite layer, being a molybdenum-aluminum metal composite layer, a molybdenum-aluminum alloy composite layer, a titanium-aluminum metal composite layer, or a copper-molybdenum metal composite layer.

[0067] That is, the first metal layer 131 is a composite metal layer, so that the first metal layer 131 can have a superior electrical conductivity.

[0068] The second metal layer 135 maybe a second metal composite layer, being a molybdenum-aluminum-molybdenum metal composite layer, a titanium-aluminum-titanium composite layer, or a copper-molybdenum metal composite layer.

[0069] That is, the second metal layer 135 is a composite metal layer, so that the second metal layer 135 can have a superior electrical conductivity.

[0070] Further a protective layer may be formed between the filter layer 15 and the second metal layer 135. Both the protective layer and the passivation layer 17 may be of monosilicon mononitride or trisilicontetranitride (also abbreviated as silicon nitride), namely SiN_x , with x being 1 or $\frac{3}{4}$.

[0071] Said differently, the protective layer is further formed between the filter layer 15 and the second metal layer 135 in order to protect the second metal layer 135. The passivation layer 17 can insulate the filter layer 15 from the first conductive layer 19.

[0072] The second substrate 30 may include a second base 31, a matrix layer 33 disposed on the second base 31, and a second conductive layer 35 plated on the second base 31 and the matrix layer 33.

[0073] The matrix layer 33 may be a black matrix layer.

[0074] To put it another way, the second substrate 30 may include a second base 31, a matrix layer 33, and a second conductive layer 35, so that the display panel 100 can operate properly.

[0075] Both the first conductive layer 19 and the second conductive layer 35 may be translucent or transparent conductive metal layers.

[0076] The translucent or transparent conductive metal layer is made of the materials as follows: indium oxide (In_2O_3), tin oxide (SnO_2), zinc oxide (ZnO), cadmium oxide (CdO), cadmium-indium oxide (CdIn_2O_4), cadmium-tin oxide (Cd_2SnO_4), zin-tin oxide (Zn_2SnO_4), a mixture of indium oxide and zinc oxide ($\text{In}_2\text{O}_3\text{—ZnO}$), or tin-doped indium oxide ($\text{In}_2\text{O}_3\text{:Sn}$), etc.

[0077] The first conductive layer 19 may have a depth of $0.03\text{--}0.05\text{ }\mu\text{m}$.

[0078] According to the solution of the present disclosure, the first conductive layer 19 and the second conductive layer 35 are both translucent or transparent conductive metal layers, so that the display panel can provide superior display effects.

[0079] The display panel 100 may further include multiple spacer columns 14 connected between the first conductive layer 19 and the second conductive layer 35.

[0080] Thus, multiple spacer columns 14 may be disposed between the first conductive layer 19 and the second conductive layer 35, so that the first conductive layer 19 and the second conductive layer 35 can form a proper gap therebetween.

[0081] Note, the display panel 100 can be enabled with an in-plane switching mode (IPS mode) or a vertical alignment mode (VA mode).

[0082] Referring now to FIG. 2, there is also provided a method of manufacturing a display panel, the method comprising:

[0083] providing a first base 11 and forming a switch array layer 13 on the first base 11;

[0084] forming a filter layer 15 on the first base 11 and the switch array layer 13;

[0085] forming in succession a passivation layer 17 and a first conductive layer 19 on the filter layer 15, the filter layer 15 being defined with a first through hole 157, the first conductive layer 19 being coupled through the first through hole 157 of the filter layer 15 to the switch array layer 13 and being defined with a recess 191;

[0086] filling the recess 191 with a filler 12 to obtain a first substrate 10;

[0087] providing a second substrate 30 and pairing the second substrate 30 with the first substrate 10; and

[0088] injecting a liquid crystal into between the second substrate 30 and the first substrate 10 to form a liquid crystal layer.

[0089] In the present embodiment, the filter layer 15 may be defined with two through holes 157, while there also are defined two recesses 191.

[0090] That is, the first conductive layer 19 may be provided with at least one recess 191, inside which maybe filled a filler 12. Since the recess 191 is filled with the filler 12, the liquid crystal would not flow into the recess 191 when rejected into between the first substrate 10 and the second substrate 30. Therefore, the liquid crystal can be uniformly distributed between the first substrate 10 and the second substrate 30, so that the resulting display panel 100 can have a superior quality.

[0091] The preparation of the switch array layer 13 may include:

[0092] plating a first metal layer 131 on the first base 11 and performing a first photolithography with the first metal layer 131 to remove a part of the first metal layer 131, in order to form a gate, a gate line, and a common electrode;

[0093] depositing in turn an insulating layer and a semiconductive silicon layer on the remained first metal layer 131 and on the first base 11;

[0094] plating a second metal layer 135 on the remained insulating layer and the remained semiconductive silicon layer; and

[0095] performing a second photolithography with the insulating layer, the semiconductive silicon layer, and the second metal layer 135, in order to remove a part of the insulating layer and semiconductive silicon layer and a part of the second metal layer 135 to form a source and a drain.

[0096] The intermediate layer 133 may include an insulating layer and an amorphous silicon layer that are coated in succession on the surface of the first metal layer 131 and the surface of the first base 11. The insulating layer may be a silicon nitride (SiN_x) layer or a gate-silicon nitride (G-SiN_x) layer. The amorphous silicon layer may include an amorphous silicon ($\alpha\text{-Si}$) layer and an N-type amorphous silicon ($\text{N}+\alpha\text{-Si}$) layer deposited on the amorphous silicon layer.

[0097] That is, the switch array layer 13 may include a first metal layer 131, an intermediate layer 133, and a second metal layer 135 plated on the intermediate layer and the first base 11, so that the display panel 100 can operate properly.

[0098] The preparation of the filter layer 15 may include:

[0099] providing a photoresist;

[0100] coating the first base 11 and the switch array layer 13 with the photoresist to form a photoresist film;

- [0101] performing a third photolithography with the photoresist film to form a plurality of color resist elements, every two adjacent color resist elements overlapping and the filter layer 15 being defined with at least one first through hole 157, the partial passivation layer 17 and partial first conductive layer 19 being received within the first through hole 157.
- [0102] The part of passivation layer 17 received within the first through hole 157 maybe subject to a fourth photolithography in order to form a second through hole 171. The part of the first conductive layer 19 received within the second through hole 171 may receive a fifth photolithography in order to form the recess 191.
- [0103] The filter layer 15 may be a color filter, e.g., but not limited to, a first color resist element 131 (red resist), a second color resist element 133 (green resist), and a third color resist element 135 (blue resist).
- [0104] Among the multiple color resist elements sequentially connected according to the solution of the present disclosure, every two adjacent color resist elements may overlap, thereby providing a superior color display with the display panel 100.
- [0105] Filling the recess 191 with the filler 12 may include:
- [0106] filling the recess 191 with an organic solvent and coating the surface of the first conductive layer 19 with an organic material to form an organic layer; the organic layer may be of a polyimide material or a polymethyl methacrylate material;
- [0107] performing photolithography with the organic layer to form a plurality of spacer columns 14 and at least one filler 12, the plurality of spacer columns 14 being connected between the first conductive layer 19 and the second substrate 30, the recess 191 being filled with the filler 12.
- [0108] The photolithography processing may include:
- [0109] filling the recess 191 with an organic solvent and coating the surface of the first conductive layer 19 with an organic solvent to form an organic layer; the organic layer may be of a polyimide material or a polymethyl methacrylate material.
- [0110] providing a ternary mask including a first mask, a second mask, and a third mask. The first mask may be devoid of light transmittance, i.e., the percentage light transmittance of the first mask is 0%; the percentage transmittance of the second mask is 100%; and the percentage transmittance of the third mask is 10~90%;
- [0111] placing the ternary mask on the organic layer;
- [0112] performing exposure treatment with the organic layer, including: irradiating the ternary mask with ultraviolet light, where the ultraviolet light irradiated onto the first mask does not pass through the first mask so that the ultraviolet light irradiated to the first mask will not shine onto a first portion of the organic layer; the ultraviolet light irradiated to the second mask may pass through the second mask so that it may shine on a second portion of the organic layer; and the ultraviolet light irradiated to the third mask may pass in part through the third mask so that it will shine on a third portion of the organic layer;
- [0113] subjecting the organic layer to a dry etching treatment to remove the unexposed organic layer, so as to form the filler 12 and the spacer column 14.
- [0114] It is understood that the percent light transmittance of the third mask may lie in the range of 10~90% which means the percent transmittance of the ultraviolet light would be in the range of 10~90%. The third mask can

correspond to the recess 191 in position, and so only a part of the ultraviolet light would be able to pass through the third mask and be irradiated onto the organic layer located on the filler 12. That is, the organic material in the filler 12 is not exposed, and so the organic layer on the filler 12 would not be completely exposed. After removal of the unexposed organic layer, the organic material in the filler 12 may not be etched and removed, thus the filler 12 can be formed in this way.

[0115] According to the solution of the present disclosure multiple spacer columns 14 may be disposed between the first conductive layer 19 and the second conductive layer 35, so that a proper gap can be formed between the first conductive layer 19 and the second conductive layer 35. Since the recess 191 is filled with the filler 12, the liquid crystal would not flow into the recess 191. Therefore, the liquid crystal can be uniformly distributed between the first substrate 10 and the second substrate 30, and so the resulting display panel 100 can have a superior quality.

[0116] The preparation of the second substrate 30 may include:

[0117] providing a second base 31;

[0118] disposing a matrix layer 33 on the second base 31; and

[0119] plating a second conductive layer 35 on the surface of the second base 31 and the surface of the matrix layer 33.

[0120] In other words, the second substrate 30 may include a second base 31, a matrix layer 33, and a second conductive layer 35, whereby the display panel 100 can operate properly.

[0121] A protective layer may be formed between the filter layer 15 and the second metal layer 135. Both the protective layer and the passivation layer 17 may be of monosilicon mononitride or trisilicon tetranitride (also abbreviated as silicon nitride), namely SiN_x , with x being 1 or $\frac{3}{4}$.

[0122] According to the solution of the present disclosure, the protective layer is further formed between the filter layer 15 and the second metal layer 135 in order to protect the second metal layer 135. The passivation layer 17 can insulate the filter layer 15 from the first conductive layer 19.

[0123] There is further provided a display that includes the display panel 100. Because the display employs all of the solutions of the above embodiments, at least all of the advantages brought about by the solutions of the above embodiments are present here and are not to be detailed again.

[0124] It should be appreciated that the display also includes other components that perform the display function, such as a horizontal polarizer, a vertical polarizer, etc.

[0125] The foregoing description merely depicts some exemplary embodiments of the present disclosure and therefore is not intended to be limiting the scope of the disclosure. Any equivalent structural transformations made to the disclosure, or any direct or indirect applications of the disclosure on any other related fields based on the concepts of the present disclosure, shall all fall in the scope of the disclosure.

What is claimed is:

1. A display panel, comprising:

a first substrate, comprising:

a first base;

a switch array layer disposed on the first base;

a filter layer covering the first substrate and the switch array layer, the filter layer having a first through hole;

a passivation layer disposed on a surface of the filter layer; and

a first conductive layer disposed on a surface of the passivation layer, the first conductive layer being coupled through the first through hole of the filter layer to the switch array layer, the first conductive layer being defined with at least one recess, the recess being filled with a filler;

a second substrate; and

a liquid crystal layer sandwiched between the second substrate and the first substrate.

2. The display panel according to claim 1, wherein the recess has a depth of 1 μm to 2 μm , and the filler has a height of 1 μm to 2 μm .

3. The display panel according to claim 1, wherein the filler is of polyimide or polymethyl methacrylate.

4. The display panel according to claim 1, wherein the filter layer is defined with at least one of the first through hole and a part of the passivation layer is accommodated within the first through hole, where the part of the passivation layer is defined with at least one second through hole and a part of the first conductive layer is received within the second through hole, the first conductive layer being coupled through the first through hole of the filter layer and the second through hole to the switch array layer, the recess being defined in the part of the first conductive layer that is received within the second through hole.

5. The display panel according to claim 1, wherein the filter layer comprises a plurality of color resist elements connected in series, every two adjacent color resist elements overlapping.

6. The display panel according to claim 1, wherein the switch array layer comprises a first metal layer disposed on the first base, an intermediate layer disposed on the first metal layer and on the first base, and a second metal layer disposed on the intermediate layer and the first metal layer and the first base, the first conductive layer being coupled to the second metal layer.

7. The display panel according to claim 6, wherein the first metal layer is a first metal composite layer, the first metal composite layer being a molybdenum-aluminum metal composite layer, a molybdenum-aluminum alloy composite layer, a titanium-aluminum metal composite layer, or a copper-molybdenum metal composite layer.

8. The display panel according to claim 6, wherein the second metal layer is a second metal composite layer, the second metal composite layer being a molybdenum-aluminum-molybdenum metal composite layer, a titanium-aluminum-titanium metal composite layer, or a copper-molybdenum metal composite layer.

9. The display panel according to claim 6, wherein the intermediate layer comprises an insulating layer and an amorphous silicon layer that are disposed in succession on the first metal layer and the first base.

10. The display panel according to claim 6, further comprising a protective layer formed between the filter layer and the second metal layer, both the protective layer and the passivation layer being of monosilicon mononitride or trisilicon tetranitride.

11. The display panel according to claim 1, wherein the second substrate comprises a second base, a matrix layer disposed on the second base, and a second conductive layer disposed on the second base and on the matrix layer.

12. The display panel according to claim 11, wherein both the first conductive layer and the second conductive layer are translucent or transparent conductive metal layers.

13. The display panel according to claim 12, wherein the translucent or transparent conductive metal layer is made of indium oxide, tin oxide, zinc oxide, cadmium oxide, cadmium-indium oxide, cadmium-tin oxide, zinc-tin oxide, a mixture of indium oxide and zinc oxide, or tin-doped indium oxide.

14. The display panel according to claim 11, further comprising a plurality of spacer columns connected between the first conductive layer and the second conductive layer.

15. The display panel according to claim 14, wherein the spacer columns are of polyimide or polymethyl methacrylate.

16. A method of manufacturing a display panel, the method comprising:

providing a first base and forming a switch array layer on the first base;

forming a filter layer on the first base and on the switch array layer, the filter layer being defined with a first through hole;

forming in succession a passivation layer and a first conductive layer on the filter layer, the first conductive layer being coupled through the first through hole of the filter layer to the switch array layer and being defined with a recess;

filling the recess with a filler to obtain a first substrate;

providing a second substrate and pairing the second substrate with the first substrate; and

injecting a liquid crystal into between the second substrate and the first substrate to form a liquid crystal layer.

17. The method according to claim 16, wherein preparation of the filter layer comprising:

providing a photoresist;

coating the first base and the switch array layer with the photoresist to form a photoresist film; and

performing photolithography with the photoresist film to form a plurality of color resist elements, every two adjacent color resist elements overlapping and the filter layer being defined with at least one of the first through hole.

18. The method according to claim 16, wherein filling the recess with the filler comprising:

filling the recess with an organic solvent and coating a surface of the first conductive layer with an organic material to form an organic layer; and

performing photolithography with the organic layer to form a plurality of spacer columns and at least one filler, the plurality of spacer columns being connected between the first conductive layer and the second substrate, the recess being filled with the filler.

19. The method according to claim 16, wherein preparation of the second substrate comprising:

providing a second base;

disposing a matrix layer on the second base; and

plating a second conductive layer on a surface of the second base and a surface of the matrix layer.

20. A display comprising a display panel, the display panel comprising:

a first substrate, comprising:

a first base;

a switch array layer disposed on the first base;

a filter layer covering the first substrate and the switch array layer, the filter layer having a first through hole;

a passivation layer provided on a surface of the filter layer; and

a first conductive layer provided on a surface of the passivation layer, the first conductive layer being coupled through the first through hole of the filter layer to the switch array layer, the first conductive layer being defined with at least one recess, the recess being filled with a filler;

a second substrate; and

a liquid crystal layer sandwiched between the second substrate and the first substrate.

* * * * *

专利名称(译)	显示面板，其制造方法以及使用该显示面板的显示器		
公开(公告)号	US20180188626A1	公开(公告)日	2018-07-05
申请号	US15/832723	申请日	2017-12-05
[标]申请(专利权)人(译)	惠科股份有限公司 重庆惠科金渝光电科技有限公司		
[标]发明人	CHIEN CHUNGKUANG		
发明人	CHIEN, CHUNGKUANG		
IPC分类号	G02F1/1362 G02F1/1368 H01L27/12 H01L21/027 G02F1/1339		
CPC分类号	G02F1/136286 G02F1/1368 H01L27/127 H01L27/1288 H01L27/1222 H01L21/0274 H01L27/124 G02F1/13394 G02F2202/02 G02F2202/103 G02F2001/136295 H01L29/66765 H01L29/78669 G02F2001/136222 G02F2001/13398 G02F1/1341 G02F1/1362 G02F1/136227 G02F2001/133776		
优先权	201611250653.0 2016-12-29 CN		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种显示面板，包括第一基板，第二基板和夹在第二基板和第一基板之间的液晶层。第一基板包括第一基底，设置在第一基底上的开关阵列层，覆盖第一基底和开关阵列层的滤光层，以及在滤光层上依次设置的钝化层和第一导电层。过滤层具有第一通孔。第一导电层通过滤光层的第一通孔耦合到开关阵列层。第一导电层限定有至少一个凹槽，该凹槽可填充有填料。还公开了一种制造显示面板的方法和应用该显示面板的显示器。

