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ZENG(10) **Pub. No.: US 2018/0182339 A1**(43) **Pub. Date: Jun. 28, 2018**(54) **GOA DRIVER CIRCUIT AND LIQUID
CRYSTAL DISPLAY****Publication Classification**

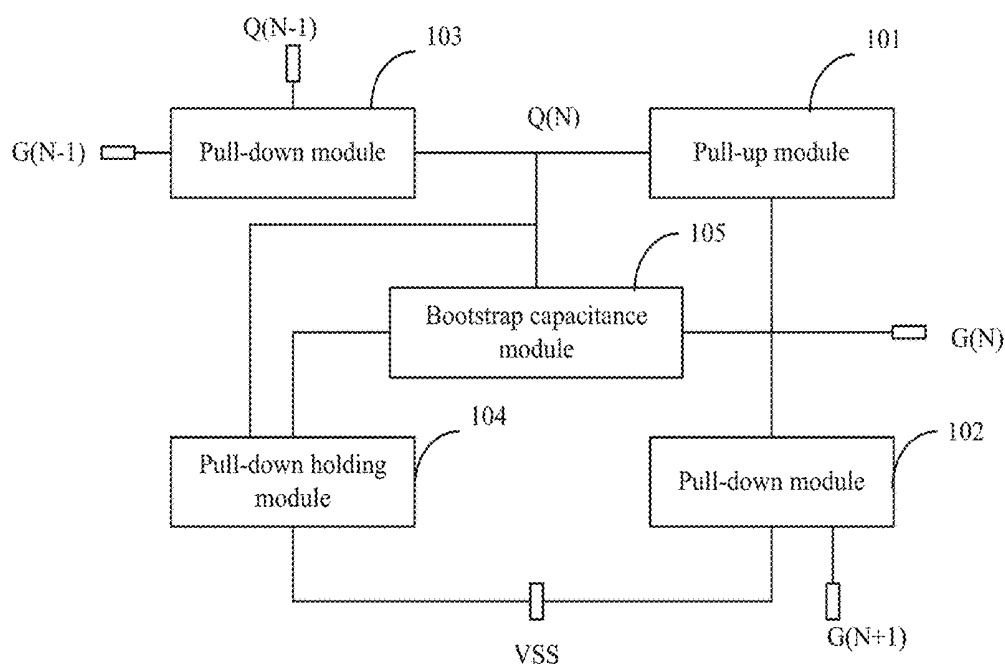
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Technology Co. Ltd., Shenzhen (CN)**(72) Inventor: **Mian ZENG, Shenzhen (CN)**(21) Appl. No.: **15/325,742**(22) PCT Filed: **Dec. 28, 2016**(86) PCT No.: **PCT/CN2016/112540**

§ 371 (c)(1),

(2) Date: **Jan. 12, 2017**(57) **ABSTRACT**

The present disclosure proposes a gate driver on array (GOA) driving circuit and a liquid crystal display. The GOA driving circuit includes cascaded GOA units. An Nth stage GOA unit outputs a gate driving signal to an Nth scan line on a display area. The Nth stage GOA unit includes a pull-up module, a pull-down module, a pull-up controlling module, a pull-down holding module, and a bootstrap capacitance module.



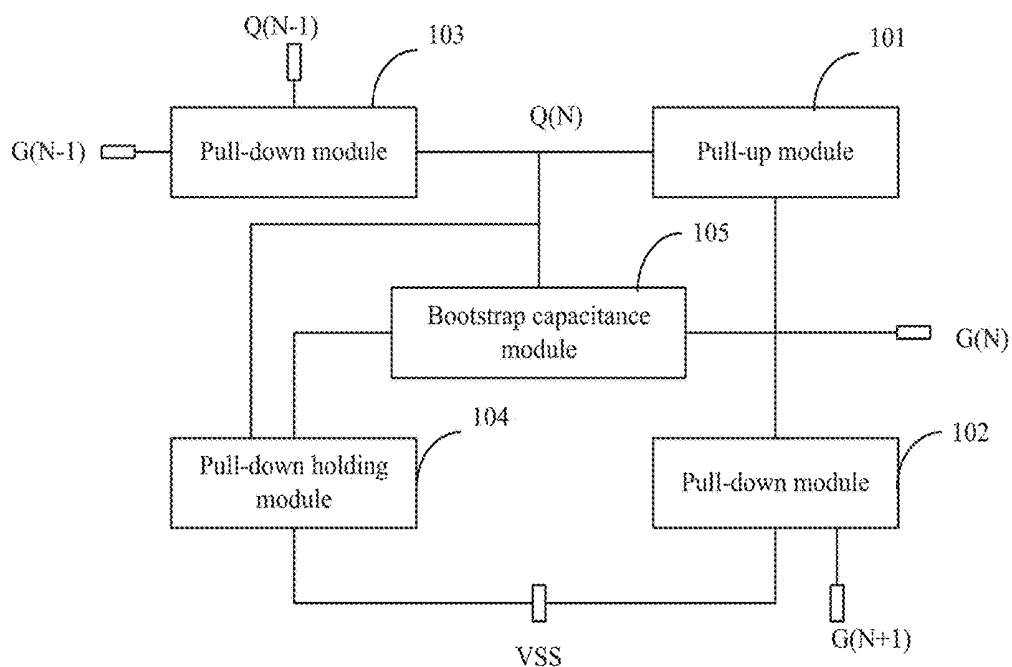


Fig. 1

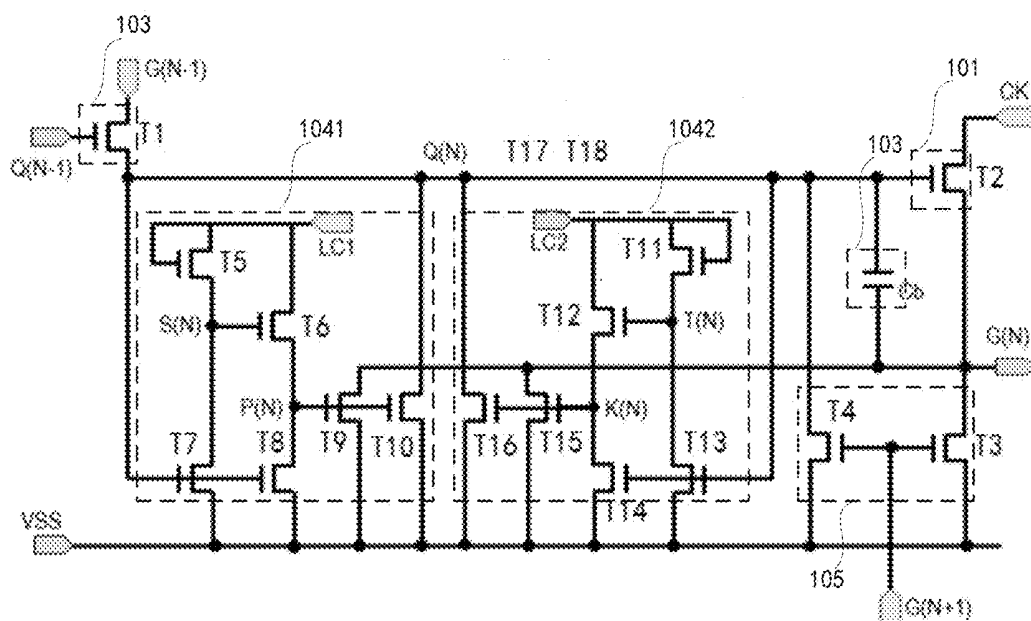


Fig. 2

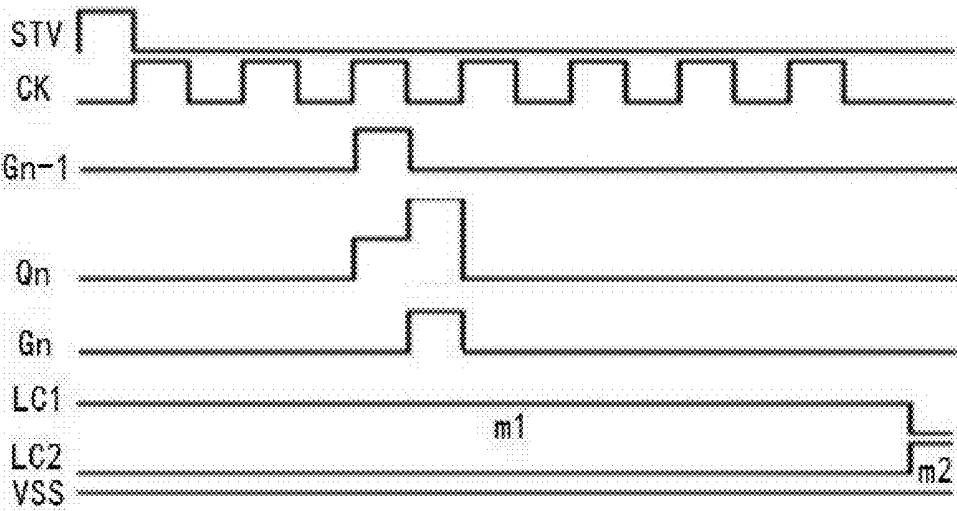


Fig. 3

GOA DRIVER CIRCUIT AND LIQUID CRYSTAL DISPLAY

BACKGROUND

1. Field of the Disclosure

[0001] The present disclosure relates to the field of liquid crystal display, and more particularly, to a gate driver on array (GOA) driver circuit and a liquid crystal display (LCD).

2. Description of the Related Art

[0002] The gate driver on array (GOA) technique is that a gate driver circuit is formed in an array substrate based on the conventional transistor LCD array process. Pixels can be scanned row by row with the GOA technique.

[0003] Conventionally, a clock signal applied to a pull-up module of a current stage GOA unit is transmitted to a pull-up module of a next stage GOA unit via a transferring module of the current stage GOA unit. Not only arranging the transferring module raises a cost of GOA unit, but conducting the clock signal to the pull-up module of the next stage GOA unit via the transferring module of the current stage GOA unit causes limited pulling up ability.

[0004] Therefore, the prior art is defective and needs to be improved and developed.

SUMMARY

[0005] An object of the present disclosure is to propose a gate driver on array (GOA) driver circuit and a liquid crystal display (LCD).

[0006] According to the present disclosure, a gate driver on array (GOA) driving circuit includes a plurality of cascaded GOA units. The Nth stage GOA unit outputs a gate driving signal to an Nth scan line on a display area. The Nth stage GOA unit includes a pull-up module coupled to a Nth gate signal node and the Nth scan line, a pull-down module coupled to the Nth scan line, a pull-up controlling module coupled to the Nth gate signal node, a pull-down holding module coupled to the Nth gate signal node, and a bootstrap capacitance module coupled to the Nth gate signal node and the Nth scan line.

[0007] A control terminal and an input terminal of the pull-up controlling module are coupled to an (N-1)th gate signal node and an (N-1)th scan line, respectively, and a control terminal of the pull-down module is coupled to an (N+1)th scan line.

[0008] Preferably, the pull-up controlling module comprises a first transistor which comprises a drain coupled to the (N-1)th scan line and a source coupled to the Nth gate signal node.

[0009] Preferably, the pull-up module comprises a second transistor which comprises a drain coupled to a high frequency clock signal, a gate coupled to the Nth gate signal node, and a source coupled to the Nth scan line.

[0010] Preferably, the pull-down module comprises:

[0011] a third transistor, comprising a drain coupled to the source of the second transistor and the Nth scan line, a gate coupled to the (N+1)th scan line, and a source coupled to a constant low voltage; and

[0012] a fourth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the (N+1)th scan line, and a source coupled to the constant low voltage.

[0013] Preferably, the pull-down holding module comprises a first pull-down holding circuit, where the first pull-down holding circuit comprises:

[0014] a fifth transistor, comprising a drain coupled to a first low frequency clock signal, a gate coupled to the first low frequency clock signal, and a source;

[0015] a sixth transistor, comprising a drain coupled to the first low frequency clock signal, a gate coupled to the source of the fifth transistor, and a source;

[0016] a seventh transistor, comprising a drain coupled to the source of the fifth transistor and the gate of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0017] an eighth transistor, comprising a drain coupled to the source of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0018] a ninth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage; and

[0019] a tenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage.

[0020] Preferably, the pull-down holding module comprises a second pull-down holding circuit, where the second pull-down holding circuit comprises:

[0021] an eleventh transistor, comprising a drain coupled to a second low frequency clock signal, a gate coupled to the second low frequency clock signal, and a source;

[0022] a twelfth transistor, comprising a drain coupled to the second low frequency clock signal, a gate coupled to the source of the eleventh transistor, and a source;

[0023] a thirteenth transistor, comprising a drain coupled to the source of the eleventh transistor and the gate of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0024] an fourteenth transistor, comprising a drain coupled to the source of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0025] a fifteenth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage; and

[0026] a sixteenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage.

[0027] Preferably, the bootstrap capacitance module comprises a bootstrap capacitor coupled between the Nth gate signal node and the Nth scan line.

[0028] Preferably, the first low frequency clock signal is inverted to the second low frequency clock signal.

[0029] Preferably, the first low frequency clock signal and the second low frequency clock signal are coupled the plurality of GOA units through a common metallic line.

[0030] According to the present disclosure, a gate driver on array (GOA) driving circuit includes a plurality of cascaded GOA units. The Nth stage GOA unit outputs a gate driving signal to an Nth scan line on a display area. The Nth stage GOA unit includes a pull-up module coupled to a Nth gate signal node and the Nth scan line, a pull-down module

coupled to the Nth scan line, a pull-up controlling module coupled to the Nth gate signal node, a pull-down holding module coupled to the Nth gate signal node, and a bootstrap capacitance module coupled to the Nth gate signal node and the Nth scan line.

[0031] A control terminal and an input terminal of the pull-up controlling module are coupled to an (N-1)th gate signal node and an (N-1)th scan line, respectively, and a control terminal of the pull-down module is coupled to an (N+1)th scan line.

[0032] The pull-up controlling module comprises a first transistor which comprises a drain coupled to the (N-1)th scan line and a source coupled to the Nth gate signal node.

[0033] The pull-up module comprises a second transistor which comprises a drain coupled to a high frequency clock signal, a gate coupled to the Nth gate signal node, and a source coupled to the Nth scan line.

[0034] The pull-down module comprises:

[0035] a third transistor, comprising a drain coupled to the source of the second transistor and the Nth scan line, a gate coupled to the (N+1)th scan line, and a source coupled to a constant low voltage; and

[0036] a fourth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the (N+1)th scan line, and a source coupled to the constant low voltage.

[0037] The pull-down holding module comprises a first pull-down holding circuit, where the first pull-down holding circuit comprises:

[0038] a fifth transistor, comprising a drain coupled to a first low frequency clock signal, a gate coupled to the first low frequency clock signal, and a source;

[0039] a sixth transistor, comprising a drain coupled to the first low frequency clock signal, a gate coupled to the source of the fifth transistor, and a source;

[0040] a seventh transistor, comprising a drain coupled to the source of the fifth transistor and the gate of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0041] an eighth transistor, comprising a drain coupled to the source of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0042] a ninth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage; and

[0043] a tenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage.

[0044] The pull-down holding module comprises a second pull-down holding circuit, where the second pull-down holding circuit comprises:

[0045] an eleventh transistor, comprising a drain coupled to a second low frequency clock signal, a gate coupled to the second low frequency clock signal, and a source;

[0046] a twelfth transistor, comprising a drain coupled to the second low frequency clock signal, a gate coupled to the source of the eleventh transistor, and a source;

[0047] a thirteenth transistor, comprising a drain coupled to the source of the eleventh transistor and the gate of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0048] an fourteenth transistor, comprising a drain coupled to the source of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

[0049] a fifteenth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage; and

[0050] a sixteenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage.

[0051] The bootstrap capacitance module comprises a bootstrap capacitor coupled between the Nth gate signal node and the Nth scan line.

[0052] The first low frequency clock signal is inverted to the second low frequency clock signal.

[0053] The first low frequency clock signal and the second low frequency clock signal are coupled the plurality of GOA units through a common metallic line.

[0054] The present disclosure also proposes a liquid crystal display comprising a gate driver on array (GOA) driver circuit as disclosed above.

[0055] The present disclosure proposes a Nth stage GOA unit utilizing a gate signal node Q(N) as a transferring signal without using a transferring module. Furthermore, voltage applied on a gate signal node Q(N-1) is used to trigger the pull-up controlling module of the Nth stage GOA unit. When voltage applied on the gate signal node Q(N-1) is at high voltage level, signal applied on the scan line G(N-1) is transmitted to the gate signal node Q(N), so that the pull-up controlling module receives greater turn-on voltage and enhances pull-up voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0056] FIG. 1 illustrates a block diagram of an Nth GOA driving circuit according to a first embodiment of the present disclosure.

[0057] FIG. 2 illustrates a circuit diagram of the Nth GOA driving circuit shown in FIG. 2.

[0058] FIG. 3 illustrates waveforms of signals applied on the GOA driving circuit according to the embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0059] The following description of every embodiment with reference to the accompanying drawings is used to exemplify a specific embodiment, which may be carried out in the present invention. Directional terms mentioned in the present invention, such as "top", "bottom", "front", "back", "left", "right", "inside", "outside", "side" etc., are only used with reference to the orientation of the accompanying drawings. Therefore, the used directional terms are intended to illustrate, but not to limit, the present invention.

[0060] In the drawings, the components having similar structures are denoted by the same numerals.

[0061] Please refer to FIG. 1. A gate driver on array (GOA) driving circuit includes a plurality of cascaded GOA units. An Nth stage GOA unit outputs a gate driving signal to an Nth scan line on a display area. The Nth stage GOA unit includes a pull-up module 101, a pull-down module

102, a pull-up controlling module **103**, a pull-down holding module **104**, and a bootstrap capacitance module **105**.

[0062] The pull-up module **102** is coupled to a Nth gate signal node $Q(N)$ and the Nth scan line $G(N)$. The pull-down module **102** is coupled to the Nth scan line $G(N)$. The pull-up controlling module **103** is coupled to the Nth gate signal node $Q(N)$. The pull-down holding module **104** is coupled to the Nth gate signal node $Q(N)$. The bootstrap capacitance module **105** is coupled to the Nth gate signal node $Q(N)$ and the Nth scan line $G(N)$. A control terminal and an input terminal of the pull-up controlling module **103** are coupled to an $(N-1)$ th gate signal node $Q(N-1)$ and an $(N-1)$ th scan line $G(N-1)$, respectively. A control terminal of the pull-down module **102** is coupled to an $(N+1)$ th scan line $G(N+1)$. It is noted that a control terminal and an input terminal of the pull-up controlling module **103** of the first GOA unit are coupled to a start signal STV and a driving signal, respectively.

[0063] As illustrated in FIG. 2, the pull-up module **101** includes a second transistor **T2** which comprises a drain coupled to a high frequency clock signal, a gate coupled to the Nth gate signal node $Q(N)$, and a source coupled to the Nth scan line $G(N)$. The pull-up module **101** is used to transmit the high frequency clock signal to a gate driving signal of the Nth scan line $G(N)$.

[0064] The pull-up controlling module **103** includes a first transistor **T3** which comprises a drain coupled to the $(N-1)$ th scan line and a source coupled to the Nth gate signal node $Q(N)$. The pull-up controlling module **103** is used to control a on/off state of the second transistor **T2**.

[0065] The pull-down module **102** includes a third transistor **T3** and a fourth transistor **T4**. The third transistor **T3** includes a drain coupled to the source of the second transistor **T2** and the Nth scan line $G(N)$, a gate coupled to the $(N+1)$ th scan line $G(N+1)$, and a source coupled to a constant low voltage VSS . The fourth transistor **T4** includes a drain coupled to the Nth gate signal node $Q(N)$, a gate coupled to the $(N+1)$ th scan line $G(N+1)$, and a source coupled to the constant low voltage VSS . The pull-down module **102** is used to rapidly pull down the gate driving signal of the Nth scan line to a low voltage level.

[0066] The pull-down holding module **104** includes a first pull-down holding circuit **1041** and a second pull-down holding circuit **1042**.

[0067] The first pull-down holding circuit **1041** includes a fifth transistor **T5**, a sixth transistor **T6**, a seventh transistor **T7**, an eighth transistor **T8**, a ninth transistor **T9**, and a tenth transistor **T10**. The fifth transistor **T5** includes a drain coupled to a first low frequency clock signal $LC1$, a gate coupled to the first low frequency clock signal $LC1$, and a source. The sixth transistor **T6** includes a drain coupled to the first low frequency clock signal $LC1$, a gate coupled to the source of the fifth transistor **T5**, and a source. The seventh transistor **T7** includes a drain coupled to the source of the fifth transistor **T5** and the gate of the sixth transistor **T6**, a gate coupled to the Nth gate signal node $Q(N)$, and a source coupled to the constant low voltage VSS . The eighth transistor **T8** includes a drain coupled to the source of the sixth transistor **T6**, a gate coupled to the Nth gate signal node $Q(N)$, and a source coupled to the constant low voltage VSS . The ninth transistor **T9** includes a drain coupled to the Nth scan line $G(N)$, a gate coupled to the source of the sixth transistor **T6**, and a source coupled to the constant low voltage VSS . The tenth transistor **T10** includes a drain

coupled to the Nth gate signal node $Q(N)$, a gate coupled to the source of the sixth transistor **T6**, and a source coupled to the constant low voltage VSS .

[0068] The second pull-down holding circuit **1042** includes an eleventh transistor **T11**, a twelfth transistor **T12**, a thirteenth transistor **T13**, a fourteenth transistor **T14**, a fifteenth transistor **T15**, and a sixteenth transistor **T16**. The eleventh transistor **T11** includes a drain coupled to a second low frequency clock signal $LC2$, a gate coupled to the second low frequency clock signal $LC2$, and a source. The twelfth transistor **T12** includes a drain coupled to the second low frequency clock signal $LC2$, a gate coupled to the source of the eleventh transistor **T11**, and a source. The thirteenth transistor **T13** includes a drain coupled to the source of the eleventh transistor **T11** and the gate of the twelfth transistor **T12**, a gate coupled to the Nth gate signal node $Q(N)$, and a source coupled to the constant low voltage VSS . The fourteenth transistor **T14** includes a drain coupled to the source of the twelfth transistor **T12**, a gate coupled to the Nth gate signal node $Q(N)$, and a source coupled to the constant low voltage VSS . The fifteenth transistor **T15** includes a drain coupled to the Nth scan line $G(N)$, a gate coupled to the source of the twelfth transistor **T12**, and a source coupled to the constant low voltage VSS . The sixteenth transistor **T16** includes a drain coupled to the Nth gate signal node $Q(N)$, a gate coupled to the source of the twelfth transistor **T12**, and a source coupled to the constant low voltage VSS .

[0069] The bootstrap capacitance module **103** includes a bootstrap capacitor C_b coupled between the Nth gate signal node $Q(N)$ and the Nth scan line $G(N)$.

[0070] The first low frequency clock signal $LC1$ and the second low frequency clock signal $LC2$ are coupled the plurality of GOA units through a common metallic line.

[0071] As illustrated in FIG. 3, the first low frequency clock signal $LC1$ is inverted to the second low frequency clock signal $LC2$. The first pull-down holding circuit **1041** and second pull-down holding circuit **1042** alternatively work according to the first low frequency clock signal $LC1$ and the second low frequency clock signal $LC2$. Therefore, each of the first pull-down holding circuit **1041** and second pull-down holding circuit **1042** does not work continuously, so that voltage stress applied on transistors of the circuits is lowered and enhance reliability of the circuits.

[0072] Specifically, as illustrated in FIG. 3, during a time period $m1$, the first pull-down holding circuit **1041** works in response to a high voltage level of the first low frequency clock signal $LC1$. During a time period $m2$, the second pull-down holding circuit **1042** works in response to a high voltage level of the second low frequency clock signal $LC2$.

[0073] The present disclosure proposes a Nth stage GOA unit utilizing a gate signal node $Q(N)$ as a transferring signal without using a transferring module. Furthermore, voltage applied on a gate signal node $Q(N-1)$ is used to trigger the pull-up controlling module of the Nth stage GOA unit. When voltage applied on the gate signal node $Q(N-1)$ is at high voltage level, signal applied on the scan line $G(N-1)$ is transmitted to the gate signal node $Q(N)$, so that the pull-up controlling module receives greater turn-on voltage and enhances pull-up voltage.

[0074] The present disclosure further proposes a liquid crystal display device using a GOA driving circuit as provided in the above embodiments. As the above, it should be understood that the present disclosure has been described

with reference to certain preferred and alternative embodiments which are intended to be exemplary only and do not limit the full scope of the present disclosure as set forth in the appended claims.

What is claimed is:

1. A gate driver on array (GOA) driving circuit, comprising a plurality of cascaded GOA units, an Nth stage GOA unit outputting a gate driving signal to an Nth scan line on a display area, the Nth stage GOA unit comprising:

- a pull-up module coupled to a Nth gate signal node and the Nth scan line;
- a pull-down module coupled to the Nth scan line;
- a pull-up controlling module coupled to the Nth gate signal node;
- a pull-down holding module coupled to the Nth gate signal node; and
- a bootstrap capacitance module coupled to the Nth gate signal node and the Nth scan line,

wherein a control terminal and an input terminal of the pull-up controlling module are coupled to an (N-1)th gate signal node and an (N-1)th scan line, respectively, and a control terminal of the pull-down module is coupled to an (N+1)th scan line.

2. The GOA driving circuit of claim 1, wherein the pull-up controlling module comprises a first transistor which comprises a drain coupled to the (N-1)th scan line and a source coupled to the Nth gate signal node.

3. The GOA driving circuit of claim 2, wherein the pull-up module comprises a second transistor which comprises a drain coupled to a high frequency clock signal, a gate coupled to the Nth gate signal node, and a source coupled to the Nth scan line.

4. The GOA driving circuit of claim 2, wherein the pull-down module comprises:

- a third transistor, comprising a drain coupled to the source of the second transistor and the Nth scan line, a gate coupled to the (N+1)th scan line, and a source coupled to a constant low voltage; and
- a fourth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the (N+1)th scan line, and a source coupled to the constant low voltage.

5. The GOA driving circuit of claim 2, wherein the pull-down holding module comprises a first pull-down holding circuit, where the first pull-down holding circuit comprises:

- a fifth transistor, comprising a drain coupled to a first low frequency clock signal, a gate coupled to the first low frequency clock signal, and a source;
- a sixth transistor, comprising a drain coupled to the first low frequency clock signal, a gate coupled to the source of the fifth transistor, and a source;
- a seventh transistor, comprising a drain coupled to the source of the fifth transistor and the gate of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;
- an eighth transistor, comprising a drain coupled to the source of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;
- a ninth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage; and

a tenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage.

6. The GOA driving circuit of claim 5, wherein the pull-down holding module comprises a second pull-down holding circuit, where the second pull-down holding circuit comprises:

- an eleventh transistor, comprising a drain coupled to a second low frequency clock signal, a gate coupled to the second low frequency clock signal, and a source;
- a twelfth transistor, comprising a drain coupled to the second low frequency clock signal, a gate coupled to the source of the eleventh transistor, and a source;
- a thirteenth transistor, comprising a drain coupled to the source of the eleventh transistor and the gate of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;
- an fourteenth transistor, comprising a drain coupled to the source of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;
- a fifteenth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage; and
- a sixteenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage.

7. The GOA driving circuit of claim 1, wherein the bootstrap capacitance module comprises a bootstrap capacitor coupled between the Nth gate signal node and the Nth scan line.

8. The GOA driving circuit of claim 6, wherein the first low frequency clock signal is inverted to the second low frequency clock signal.

9. The GOA driving circuit of claim 6, wherein the first low frequency clock signal and the second low frequency clock signal are coupled to the plurality of GOA units through a common metallic line.

10. A gate driver on array (GOA) driving circuit, comprising a plurality of cascaded GOA units, an Nth stage GOA unit outputting a gate driving signal to an Nth scan line on a display area, the Nth stage GOA unit comprising:

- a pull-up module coupled to a Nth gate signal node and the Nth scan line;
 - a pull-down module coupled to the Nth scan line;
 - a pull-up controlling module coupled to the Nth gate signal node;
 - a pull-down holding module coupled to the Nth gate signal node; and
 - a bootstrap capacitance module coupled to the Nth gate signal node and the Nth scan line,
- wherein a control terminal and an input terminal of the pull-up controlling module are coupled to an (N-1)th gate signal node and an (N-1)th scan line, respectively, and a control terminal of the pull-down module is coupled to an (N+1)th scan line,

wherein the pull-up controlling module comprises a first transistor which comprises a drain coupled to the (N-1)th scan line and a source coupled to the Nth gate signal node,

wherein the pull-up module comprises a second transistor which comprises a drain coupled to a high frequency clock signal, a gate coupled to the Nth gate signal node, and a source coupled to the Nth scan line,

wherein the pull-down module comprises:

a third transistor, comprising a drain coupled to the source of the second transistor and the Nth scan line, a gate coupled to the (N+1)th scan line, and a source coupled to a constant low voltage; and

a fourth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the (N+1)th scan line, and a source coupled to the constant low voltage,

wherein the pull-down holding module comprises a first pull-down holding circuit, where the first pull-down holding circuit comprises:

a fifth transistor, comprising a drain coupled to a first low frequency clock signal, a gate coupled to the first low frequency clock signal, and a source;

a sixth transistor, comprising a drain coupled to the first low frequency clock signal, a gate coupled to the source of the fifth transistor, and a source;

a seventh transistor, comprising a drain coupled to the source of the fifth transistor and the gate of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

an eighth transistor, comprising a drain coupled to the source of the sixth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

a ninth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage; and

a tenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the sixth transistor, and a source coupled to the constant low voltage,

wherein the pull-down holding module comprises a second pull-down holding circuit, where the second pull-down holding circuit comprises:

an eleventh transistor, comprising a drain coupled to a second low frequency clock signal, a gate coupled to the second low frequency clock signal, and a source;

a twelfth transistor, comprising a drain coupled to the second low frequency clock signal, a gate coupled to the source of the eleventh transistor, and a source;

a thirteenth transistor, comprising a drain coupled to the source of the eleventh transistor and the gate of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

an fourteenth transistor, comprising a drain coupled to the source of the twelfth transistor, a gate coupled to the Nth gate signal node, and a source coupled to the constant low voltage;

a fifteenth transistor, comprising a drain coupled to the Nth scan line, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage; and

a sixteenth transistor, comprising a drain coupled to the Nth gate signal node, a gate coupled to the source of the twelfth transistor, and a source coupled to the constant low voltage,

wherein the bootstrap capacitance module comprises a bootstrap capacitor coupled between the Nth gate signal node and the Nth scan line,

wherein the first low frequency clock signal is inverted to the second low frequency clock signal, and

wherein the first low frequency clock signal and the second low frequency clock signal are coupled the plurality of GOA units through a common metallic line.

11. A liquid crystal display comprising a gate driver on array (GOA) driver circuit as claimed in claim 1.

12. A liquid crystal display comprising a gate driver on array (GOA) driver circuit as claimed in claim 10.

* * * * *

专利名称(译)	GOA驱动电路和液晶显示器		
公开(公告)号	US20180182339A1	公开(公告)日	2018-06-28
申请号	US15/325742	申请日	2016-12-28
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
申请(专利权)人(译)	深圳中星光电科技有限公司		
当前申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
[标]发明人	ZENG MIAN		
发明人	ZENG, MIAN		
IPC分类号	G09G3/36 G11C19/28		
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优先权	201611071751.8 2016-11-28 CN		
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摘要(译)

本公开提出了一种栅极驱动器阵列 (GOA) 驱动电路和液晶显示器。GOA驱动电路包括级联GOA单元。第N级GOA单元将栅极驱动信号输出到显示区域上的第N条扫描线。第N级GOA单元包括上拉模块，下拉模块，上拉控制模块，下拉保持模块和自举电容模块。

