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G06F 3/044	(2006.01)

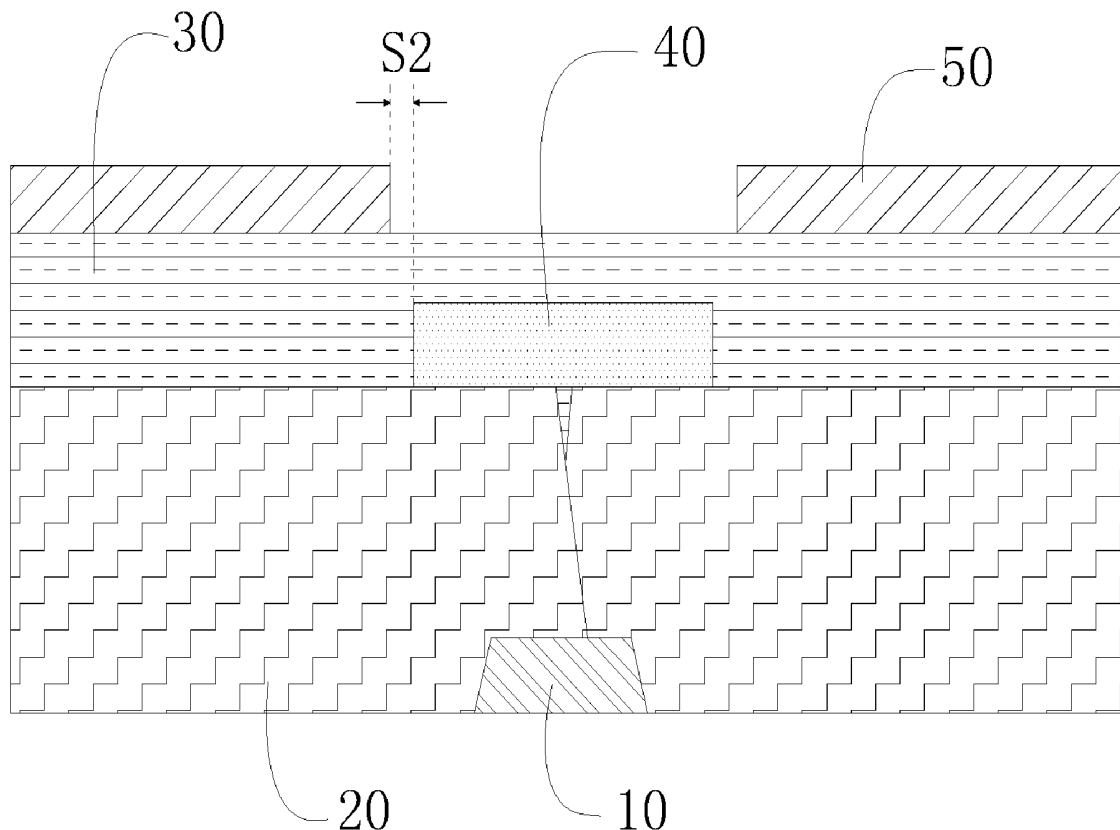
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(57)

ABSTRACT

The present disclosure provides a COA array substrate and a display device. The COA array substrate includes a plurality of gate lines; a plurality of data lines; and a plurality of pixel units. Each of the pixel units includes a pixel electrode and a common electrode. The common electrode includes a lower common electrode and an upper common electrode. The lower common electrode is disposed on one of the data lines, and the upper common electrode is disposed on one of the gate lines. The present disclosure solves a light leakage problem and problems that an aperture ratio and a transmittance are low in a liquid crystal panel.



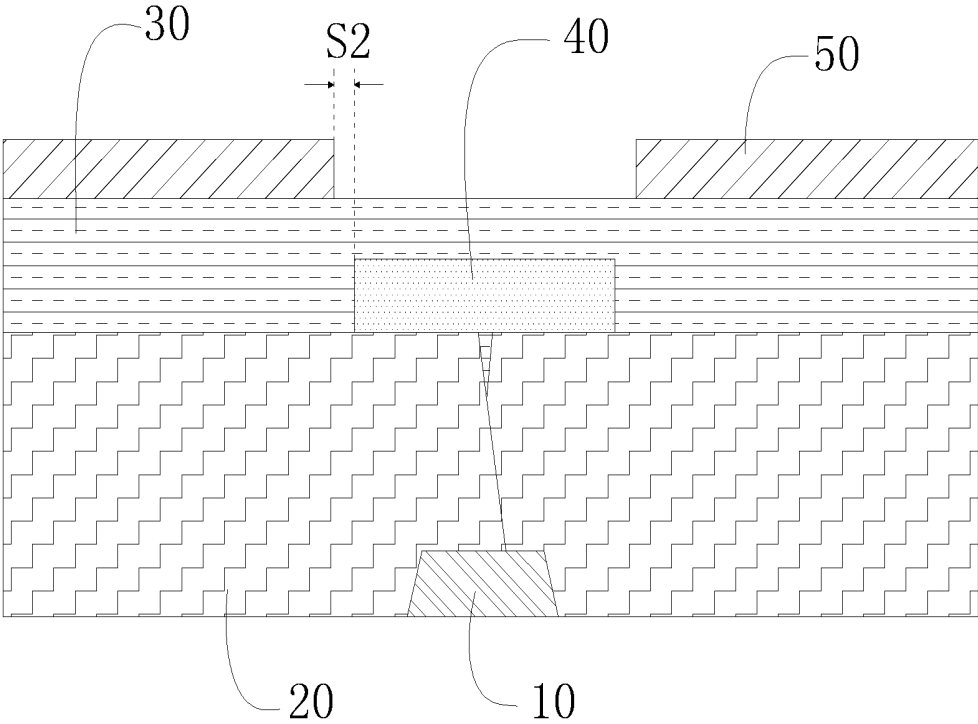


FIG. 1

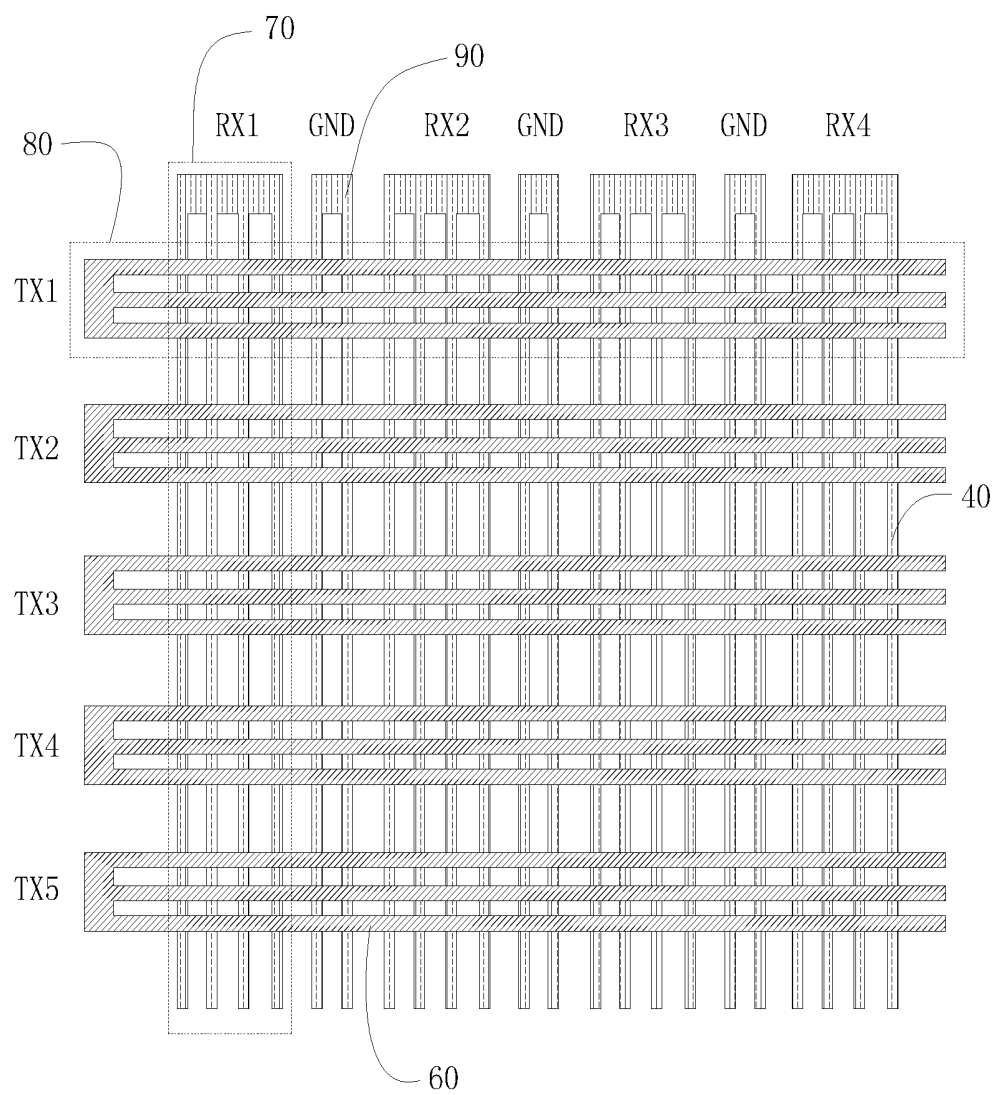


FIG. 2

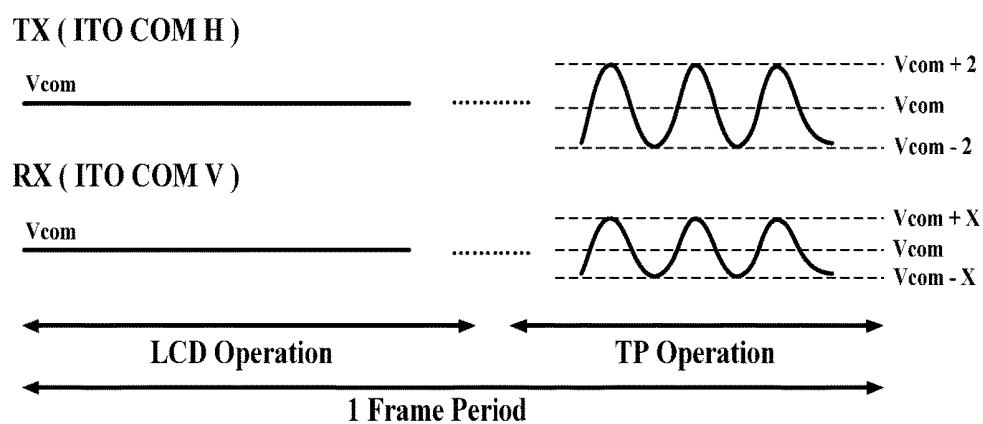


FIG. 3

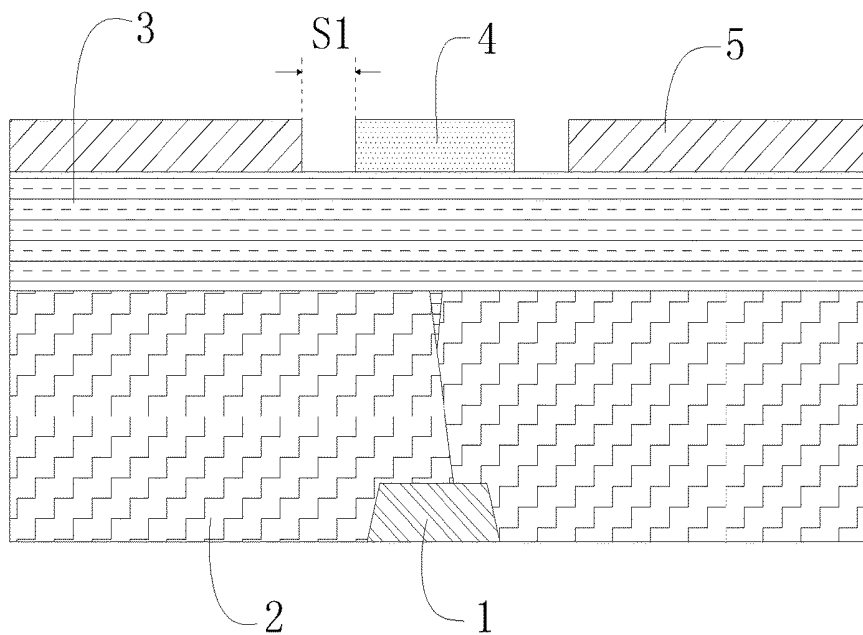


FIG. 4

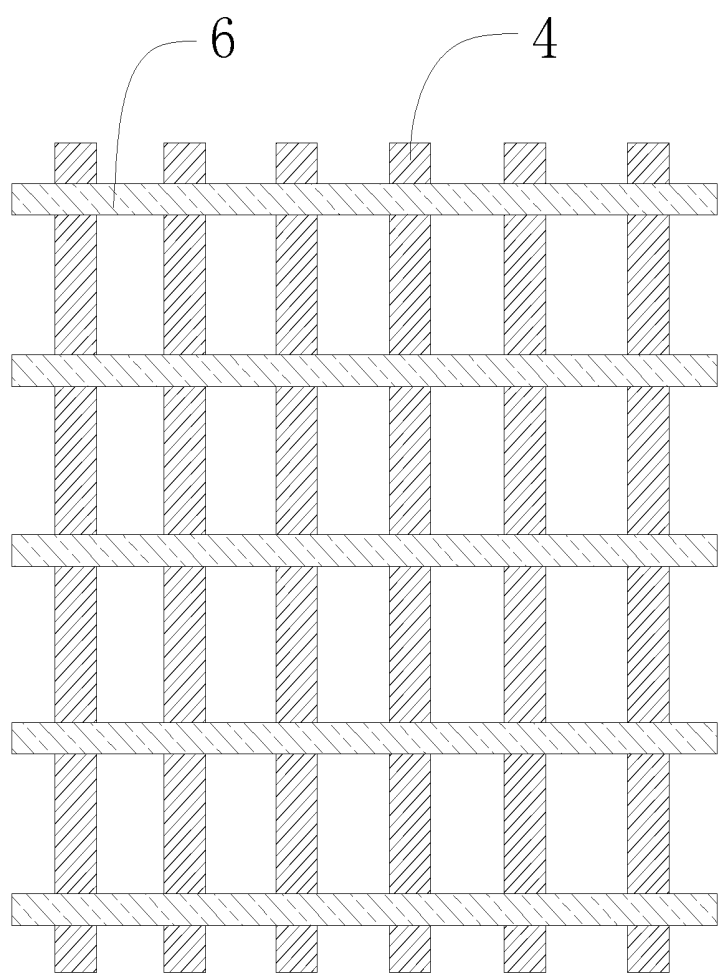


FIG. 5

COA ARRAY SUBSTRATE AND DISPLAY DEVICE

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a liquid crystal display field, and more particularly to a COA array substrate and a display device.

Description of Prior Art

[0002] Flat liquid crystal display devices, such as liquid crystal displays (LCDs), have advantages of high quality, power saving, a thin structure, and a wide application. Accordingly, the liquid crystal display devices are widely utilized in various consumer electronic products, e.g., mobile phones, televisions, personal digital assistants, digital cameras, notebooks, desktop computers, and they become mainstream display devices. Currently, most of the liquid crystal display device on the market are backlight type liquid crystal display devices, and each comprises a thin film transistor liquid crystal display (TFT-LCD) panel and a backlight module. An operating principle of the liquid crystal display panel is to place liquid crystal molecules between two glass substrates which are parallel with each other. Vertical and horizontal fine wirings are disposed between the two glass substrates. Orientations of the liquid crystal molecules are controlled to be changed by providing electricity. An image is generated by refracting light from the backlight module. In-cell capacitance screens, which integrate a touch function with internal units, become increasingly popular because of advantages that the display panels can be thinned and outdoor visibility can be increased. In a traditional panel design and an in-cell design, at least two additional layers are required to include touch sensors manufactured thereon, and thus manufacturing cost is increased. In a traditional pixel design, a black matrix (BM) is utilized to shade light. However, the black matrix is positioned on a color filter (CF) substrate. When a curved display device is bent, a problem that an upper substrate and a lower substrate are misaligned with each other might occur. Accordingly, a risk of light leakage exists, a panel, which is normal in a flat state, has mura phenomenon in a curved state.

[0003] To solve the problem, a DBS (Dali Line BM Less) pixel design is utilized more and more in a curved display panel. In this design, ITO (Indium Tin Oxide) wirings cover data lines. A width of each of the ITO wirings is slightly wider than a width of each of the data lines. The ITO wirings are connected to common electrodes. When the panel is operated normally, an electric field generated by the ITO wirings and the common electrodes can control the liquid crystal molecules not to be oriented, so as to achieve an objective of shading the light. Further, this design has an advantage that the ITO wirings utilized for shading the light are positioned on a TFT substrate (i.e., an array substrate). When the panel is manufactured as a curved display device and the curved display device is bent, positions of the ITO wirings are not changed relative to positions of the data lines. As a result, the problem of the light leakage does not exist.

[0004] FIG. 5 is a DBS pixel design of wirings of common electrodes in a display area in the prior art. FIG. 5 shows a

mesh structure. The wirings of the common electrodes 4 in a vertical direction have a light shading function for data lines. The wirings of the common electrodes 6 in a horizontal direction are connected to the wirings of the common electrodes 4 in the vertical direction to form the mesh structure, so as to ensure stability of a voltage of a common signal.

[0005] FIG. 4 is a cross-sectional view of a DBS pixel including a data line 1 in the prior art. The pixel is manufactured on a COA (color filter on array) substrate on which a color filter is manufactured. A wiring of a common electrode 4 in the vertical direction is positioned above the data line 1, and its width is greater than a width of the data line 1. A pixel electrode 5 includes light transmitting areas at two sides of the data line 1. Since the common electrode 4 in the vertical direction and the pixel electrode 5 are manufactured of the same metal layer, a minimum distance S1 between the common electrode 4 and the pixel electrode 5 is required to prevent a short circuit. Accordingly, an area of the pixel electrode 5 is limited, and an aperture ratio and a transmittance are difficult to be increased.

SUMMARY OF THE INVENTION

[0006] An objective of the present disclosure is to provide a COA array substrate and a display device for solving a light leakage problem that an upper substrate and a lower substrate are misaligned with each other in the prior art when a DBS liquid crystal panel is bent, and solving problems that an aperture ratio and a transmittance of the DBS liquid crystal panel are low.

[0007] A technical scheme of the present disclosure is described as follows.

[0008] A COA array substrate comprises:

[0009] A plurality of gate lines;

[0010] A plurality of data lines intersecting with the gate lines; and

[0011] A plurality of pixel units defined by the gate lines and the data lines, and each of the pixel units comprising a pixel electrode and a common electrode.

[0012] The common electrode includes a lower common electrode and an upper common electrode which are positioned in different layers. The lower common electrode is disposed on one of the data lines and covers the one of the data lines, and the upper common electrode is disposed on one of the gate lines and covers the one of the gate lines.

[0013] The lower common electrode is parallel with the data lines, and the upper common electrode is parallel with the gate lines.

[0014] The upper common electrode is positioned in a same layer as the pixel electrode. A first predetermined horizontal distance is maintained between the upper common electrode and the pixel electrode. The first predetermined horizontal distance prevents a short circuit between the upper common electrode and the pixel electrode.

[0015] Preferably, a second predetermined horizontal distance is maintained between each of vertical extending lines at two sides of the lower common electrode and the pixel electrode. The second predetermined horizontal distance prevents a capacitance from being formed between the lower common electrode and the pixel electrode.

[0016] Preferably, an insulating layer is disposed between the lower common electrode and the upper common electrode. The lower common electrode is covered by the

insulating layer. A color resist layer is disposed between one of the data lines and the lower common electrode.

[0017] Preferably, terminals of at least two of the lower common electrodes are connected together. The at least two of the lower common electrodes are integrally formed as a sensing electrode. Terminals of at least two of the upper common electrodes are connected together. The at least two of the upper common electrodes are integrally formed as a driving electrode. A sensing capacitance is formed in an overlapping part of the sensing electrode and the driving electrode.

[0018] Preferably, a shielding structure is disposed between two adjacent ones of the sensing electrodes for preventing signals from interfering with each other.

[0019] Preferably, the shielding structure is a metal sheet, the metal sheet is positioned in a same layer as the lower common electrode, and the metal sheet and the lower common electrode are made of a same material.

[0020] Preferably, the pixel electrode, the upper common electrode, and the metal sheet are manufactured in a same manufacturing step.

[0021] A COA array substrate comprises:

[0022] A plurality of gate lines;

[0023] A plurality of data lines intersecting with the gate lines; and

[0024] A plurality of pixel units defined by the gate lines and the data lines, and each of the pixel units comprising a pixel electrode and a common electrode.

[0025] The common electrode includes a lower common electrode and an upper common electrode which are positioned in different layers. The lower common electrode is disposed on one of the data lines and covers the one of the data lines. The upper common electrode is disposed on one of the gate lines and covers the one of the gate lines.

[0026] Preferably, the lower common electrode is parallel with the data lines, and the upper common electrode is parallel with the gate lines.

[0027] Preferably, the upper common electrode is positioned in a same layer as the pixel electrode. A first predetermined horizontal distance is maintained between the upper common electrode and the pixel electrode. The first predetermined horizontal distance prevents short circuit between the upper common electrode and the pixel electrode.

[0028] Preferably, a second predetermined horizontal distance is maintained between each of vertical extending lines at two sides of the lower common electrode and the pixel electrode. The second predetermined horizontal distance prevents a capacitance from being formed between the lower common electrode and the pixel electrode.

[0029] Preferably, an insulating layer is disposed between the lower common electrode and the upper common electrode. The lower common electrode is covered by the insulating layer. A color resist layer is disposed between one of the data lines and the lower common electrode.

[0030] Preferably, terminals of at least two of the lower common electrodes are connected together, and the at least two of the lower common electrodes are integrally formed as a sensing electrode. Terminals of at least two of the upper common electrodes are connected together, and the at least two of the upper common electrodes are integrally formed as a driving electrode. A sensing capacitance is formed in an overlapping part of the sensing electrode and the driving electrode.

[0031] Preferably, a shielding structure is disposed between two adjacent ones of the sensing electrodes for preventing signals from interfering with each other.

[0032] Preferably, the shielding structure is a metal sheet. The metal sheet is positioned in a same layer as the lower common electrode. The metal sheet and the lower common electrode are made of a same material.

[0033] Preferably, the pixel electrode, the upper common electrode, and the metal sheet are manufactured in a same manufacturing step.

[0034] A display device comprises any of the above-mentioned COA array substrates.

[0035] Advantageous effects of the present disclosure are described as follows.

[0036] In the COA array substrate of the display device in accordance with the present disclosure, the common electrode is divided into the lower common electrode and the upper common electrode. The lower common electrode is disposed on the data line to cover the data line. The upper common electrode is disposed on the gate line to cover the gate line. Accordingly, a black matrix (BM) utilized for providing a light shading function for the data line and the gate line is not required. Furthermore, the present disclosure can solve a light leakage problem that an upper substrate and a lower substrate are misaligned with each other when a DBS liquid crystal panel is bent. The present disclosure also can solve problems that an aperture ratio and a transmittance of the DBS liquid crystal panel are low.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] FIG. 1 is a cross-sectional view of a display area including a data line in a COA array substrate in accordance with an embodiment of the present disclosure.

[0038] FIG. 2 is a layout diagram of the display area, including the lower common electrode and the top common electrode and excluding the pixel electrode, and an edge area in the COA array substrate in accordance with an embodiment of the present disclosure.

[0039] FIG. 3 is a waveform diagram in accordance with an embodiment of the present disclosure when the lower common electrode and the upper common electrode are operated.

[0040] FIG. 4 is a cross-sectional view of a display area including a data line in a COA array substrate in the prior art.

[0041] FIG. 5 is a layout diagram of a display area, including a lower common electrode and a top common electrode and excluding a pixel electrode, and an edge area in a COA array substrate in the prior art.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0042] The following embodiments are referring to the accompanying drawings for exemplifying specific implementable embodiments of the present invention. Furthermore, directional terms described by the present invention, such as upper, lower, front, back, left, right, inner, outer, side and etc., are only directions by referring to the accompanying drawings, and thus the used directional terms are used to describe and understand the present invention, but the present invention is not limited thereto. In the drawings, structure-like elements are labeled with like reference numerals.

Embodiment 1

[0043] Please refer to FIG. 1. FIG. 1 is a cross-sectional view of a display area including a data line 10 in a COA array substrate in accordance with an embodiment of the present disclosure. It can be seen from FIG. 1 that the COA array substrate in accordance with the present disclosure includes:

[0044] A plurality of gate lines (not shown) configured to input driving signals;

[0045] A plurality of data lines 10 intersecting with the gate lines and configured to input data signals to pixel electrodes 50; and

[0046] A plurality of pixel units defined by the gate lines and the data lines 10, and each of the pixel units including a pixel electrode and a common electrode.

[0047] The common electrode includes a lower common electrode 40 and an upper common electrode 60 which are positioned in different layers. The upper common electrode 60 is positioned on the lower common electrode 40. The lower common electrode 40 is disposed on the data line 10 and covers the data line 10. The upper common electrode 60 is disposed on the gate line and covers the gate line. Furthermore, a width of the lower common electrode 40 is greater than a width of the data line 10. A width of the upper common electrode 60 is greater than a width of the gate line. In summary, an area of each of the data lines 10 is smaller than an area of the corresponding lower common electrode 40. An area of each of the gate lines is smaller than an area of the corresponding upper common electrode 60.

[0048] Herein, the lower common electrode 40 provides a light shading function for the data line 10, and thus it is necessary to dispose a black matrix to shade light. Similarly, the upper common electrode 60 also provides a light shading function for the gate line, and thus it is necessary to dispose a black matrix to shade light.

[0049] In the present embodiment, the lower common electrode 40 is parallel with the data lines 10, and the upper common electrode 60 is parallel with the gate lines 10.

[0050] In the present embodiment, the upper common electrode 60 is positioned in a same layer as the pixel electrode 50, and a first predetermined horizontal distance is maintained between the upper common electrode 60 and the pixel electrode 50. The first predetermined horizontal distance can prevent a short circuit between the upper common electrode 60 and the pixel electrode 50.

[0051] In the present embodiment, a second predetermined horizontal distance S2 is maintained between each of vertical extending lines at two sides of the lower common electrode 40 and the pixel electrode 50. The second predetermined horizontal distance S2 can prevent a capacitance from being formed between the lower common electrode 40 and the pixel electrode 50.

[0052] In the present embodiment, an insulating layer 30 is disposed between the lower common electrode 40 and the upper common electrode 60. The lower common electrode 40 is covered by the insulating layer 30. A color resist layer 20 is disposed between the data line 10 and the lower common electrode 40.

[0053] Please refer to FIG. 2. FIG. 2 is a layout diagram of the display area, including the lower common electrode 40 and the top common electrode 60 and excluding the pixel electrode 50, and an edge area in the COA array substrate in accordance with an embodiment of the present disclosure.

[0054] In the present embodiment, terminals of at least two of the lower common electrodes 40 are connected together. The at least two of the lower common electrodes 40 are integrally formed as a sensing electrode 70 which is represented as RX. Terminals of at least two of the upper common electrodes 60 are connected together. The at least two of the upper common electrodes 60 are integrally formed as a driving electrode 80 which is represented as TX. A sensing capacitance is formed in an overlapping part of the sensing electrode 70 and the driving electrode 80. Herein, an objective of integrally forming the at least two of the lower common electrodes 40 as the sensing electrode 70 is to make the sensing electrode 70 reach a certain width. Similarly, an objective of integrally forming the at least two of the upper common electrodes 60 as the driving electrode 80 is to make the driving electrode 80 reach a certain width. The sensing capacitance is effectively formed only when the width of the sensing electrode 70 and the width of the driving electrode 80 reach a certain width, such as 5-6 millimeters (mm).

[0055] In the present embodiment, a shielding structure 90 is disposed between two adjacent ones of the sensing electrodes 70 for preventing signals from interfering with each other.

[0056] In the present embodiment, preferably, the shielding structure 90 is a metal sheet. The metal sheet is positioned in a same layer as the lower common electrode 40. The metal sheet and the lower common electrode 40 are made of a same material.

[0057] In the present embodiment, the pixel electrode 50, the upper common electrode 60, and the metal sheet are manufactured in a same manufacturing step. Accordingly, manufacturing steps can be simplified, and manufacturing cost can be reduced.

[0058] Please refer to FIG. 3. FIG. 3 is a waveform diagram in accordance with an embodiment of the present disclosure when the lower common electrode 40 and the upper common electrode 60 are operated. It can be seen from FIG. 3 that a frame of a picture (i.e., one frame period in FIG. 3) includes an LCD operation time segment and a touch detection operation time segment. In the LCD operation time segment, waveforms of the lower common electrodes 40 and the upper common electrode 60 are the same as those in a conventional TFT-LCD. Herein, taking a direct current (DC) Vcom signal as an example. In the touch detection operation time segment, a TX signal provides a high-frequency sine wave. A center value of the TX signal is the same as the Vcom signal in the display time segment. An amplitude of the TX signal is 2V. Accordingly, a highest voltage is Vcom+2V, and a lowest voltage is Vcom-2V. A RX signal is set as the Vcom (a direct current voltage). Due to capacitance coupling effect, a sine wave having a smaller amplitude is correspondingly generated in a wiring of the RX signal. Since a frequency of the sine wave is far higher than a frequency of liquid crystal molecules, the sine wave does not have adverse effect on display quality. Please refer to FIG. 2 and FIG. 3. In the display time segment in one frame period, the Vcom signal is inputted to all the signals. In the touch detection time segment, the shielding structure 90 can provide a shielding function when the shielding structure 90 is in a ground (GND) state or the Vcom signal is inputted to the shielding structure 90.

[0059] In the COA array substrate and a display device in accordance with the present disclosure, the common electrode is divided into the lower common electrode 40 and the

upper common electrode 60. The lower common electrode 40 is disposed on the data line 10 to cover the data line 10. The upper common electrode 60 is disposed on the gate line to cover the gate line. Accordingly, a black matrix (BM) utilized for providing a light shading function for the data line and the gate line is not required. Furthermore, the present disclosure can solve a light leakage problem that an upper substrate and a lower substrate are misaligned with each other when a DBS liquid crystal panel is bent. The present disclosure also can solve problems that an aperture ratio and a transmittance of the DBS liquid crystal panel are low.

Embodiment 2

[0060] The present disclosure provides a display device which includes the COA array substrate described in the embodiment 1. The COA array substrate is described in detail in the embodiment 1 and thus is not repeated herein.

[0061] In the COA array substrate of the display device in accordance with the present disclosure, the common electrode is divided into the lower common electrode 40 and the upper common electrode 60. The lower common electrode 40 is disposed on the data line 10 to cover the data line 10. The upper common electrode 60 is disposed on the gate line to cover the gate line. Accordingly, a black matrix (BM) utilized for providing a light shading function for the data line and the gate line is not required. Furthermore, the present disclosure can solve a light leakage problem that an upper substrate and a lower substrate are misaligned with each other when a DBS liquid crystal panel is bent. The present disclosure also can solve problems that an aperture ratio and a transmittance of the DBS liquid crystal panel are low.

[0062] As is understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrative rather than limiting of the present invention. It is intended that they cover various modifications and similar arrangements be included within the spirit and scope of the present invention, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structures.

1. A COA array substrate, comprising:

- a plurality of gate lines;
- a plurality of data lines intersecting with the gate lines; and
- a plurality of pixel units defined by the gate lines and the data lines, and each of the pixel units comprising a pixel electrode and a common electrode,

wherein the common electrode includes a lower common electrode and an upper common electrode which are positioned in different layers, the lower common electrode is disposed on one of the data lines and covers the one of the data lines, and the upper common electrode is disposed on one of the gate lines and covers the one of the gate lines,

wherein the lower common electrode is parallel with the data lines, and the upper common electrode is parallel with the gate lines,

wherein the upper common electrode is positioned in a same layer as the pixel electrode, a first predetermined horizontal distance is maintained between the upper common electrode and the pixel electrode, and the first

predetermined horizontal distance prevents a short circuit between the upper common electrode and the pixel electrode.

2. The COA array substrate of claim 1, wherein a second predetermined horizontal distance is maintained between each of vertical extending lines at two sides of the lower common electrode and the pixel electrode, and the second predetermined horizontal distance prevents a capacitance from being formed between the lower common electrode and the pixel electrode.

3. The COA array substrate of claim 1, wherein an insulating layer is disposed between the lower common electrode and the upper common electrode, the lower common electrode is covered by the insulating layer, and a color resist layer is disposed between one of the data lines and the lower common electrode.

4. The COA array substrate of claim 1, wherein terminals of at least two of the lower common electrodes are connected together, and the at least two of the lower common electrodes are integrally formed as a sensing electrode,

terminals of at least two of the upper common electrodes are connected together, and the at least two of the upper common electrodes are integrally formed as a driving electrode,

a sensing capacitance is formed in an overlapping part of the sensing electrode and the driving electrode.

5. The COA array substrate of claim 4, wherein a shielding structure is disposed between two adjacent ones of the sensing electrodes for preventing signals from interfering with each other.

6. The COA array substrate of claim 5, wherein the shielding structure is a metal sheet, the metal sheet is positioned in a same layer as the lower common electrode, and the metal sheet and the lower common electrode are made of a same material.

7. The COA array substrate of claim 6, wherein the pixel electrode, the upper common electrode, and the metal sheet are manufactured in a same manufacturing step.

8. A COA array substrate, comprising:

- a plurality of gate lines;
- a plurality of data lines intersecting with the gate lines; and
- a plurality of pixel units defined by the gate lines and the data lines, and each of the pixel units comprising a pixel electrode and a common electrode,

wherein the common electrode includes a lower common electrode and an upper common electrode which are positioned in different layers, the lower common electrode is disposed on one of the data lines and covers the one of the data lines, and the upper common electrode is disposed on one of the gate lines and covers the one of the gate lines.

9. The COA array substrate of claim 8, wherein the lower common electrode is parallel with the data lines, and the upper common electrode is parallel with the gate lines.

10. The COA array substrate of claim 8, wherein the upper common electrode is positioned in a same layer as the pixel electrode, a first predetermined horizontal distance is maintained between the upper common electrode and the pixel electrode, and the first predetermined horizontal distance prevents a short circuit between the upper common electrode and the pixel electrode.

11. The COA array substrate of claim 8, wherein a second predetermined horizontal distance is maintained between

each of vertical extending lines at two sides of the lower common electrode and the pixel electrode, and the second predetermined horizontal distance prevents a capacitance from being formed between the lower common electrode and the pixel electrode.

12. The COA array substrate of claim 8, wherein an insulating layer is disposed between the lower common electrode and the upper common electrode, the lower common electrode is covered by the insulating layer, and a color resist layer is disposed between one of the data lines and the lower common electrode.

13. The COA array substrate of claim 8, wherein terminals of at least two of the lower common electrodes are connected together, and the at least two of the lower common electrodes are integrally formed as a sensing electrode, terminals of at least two of the upper common electrodes are connected together, and the at least two of the upper common electrodes are integrally formed as a driving electrode,

a sensing capacitance is formed in an overlapping part of the sensing electrode and the driving electrode.

14. The COA array substrate of claim 13, wherein a shielding structure is disposed between two adjacent ones of the sensing electrodes for preventing signals from interfering with each other.

15. The COA array substrate of claim 14, wherein the shielding structure is a metal sheet, the metal sheet is positioned in a same layer as the lower common electrode, and the metal sheet and the lower common electrode are made of a same material.

16. The COA array substrate of claim 15, wherein the pixel electrode, the upper common electrode, and the metal sheet are manufactured in a same manufacturing step.

17. A display device, comprising the COA array substrate of claim 8.

* * * * *

专利名称(译)	COA阵列基板和显示装置		
公开(公告)号	US20180164647A1	公开(公告)日	2018-06-14
申请号	US15/323975	申请日	2016-12-14
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
当前申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
[标]发明人	DU PENG		
发明人	DU, PENG		
IPC分类号	G02F1/1343 H01L27/12 G02F1/1362 G02F1/1368 G02F1/1333 G06F3/041 G06F3/044		
CPC分类号	G02F1/134336 H01L27/1248 H01L27/1244 G02F1/136286 G02F1/1368 G02F1/136204 G02F1/13338 G02F1/133345 G02F1/133305 G06F3/0412 G06F3/044 G02F2201/121 G02F2201/123 G02F2001/136218 G02F2001/136222 G06F2203/04103 G06F2203/04107 G06F2203/04112 G02F1/134309 G02F1/133512 G02F2201/122 G02F2201/40 G06F3/04166 G06F3/0446 H01L27/124 G06F3/0416		
其他公开文献	US10274793		
外部链接	Espacenet USPTO		

摘要(译)

本公开提供了一种COA阵列基板和显示装置。COA阵列基板包括多条栅极线;多条数据线;和多个像素单元。每个像素单元包括像素电极和公共电极。公共电极包括下公共电极和上公共电极。下公共电极设置在其中一条数据线上,上公共电极设置在其中一条选通线上。本公开解决了漏光问题以及液晶面板中的开口率和透射率低的问题。

