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(54) **TFT ARRAY SUBSTRATE, AND LIQUID CRYSTAL DISPLAY PANEL**

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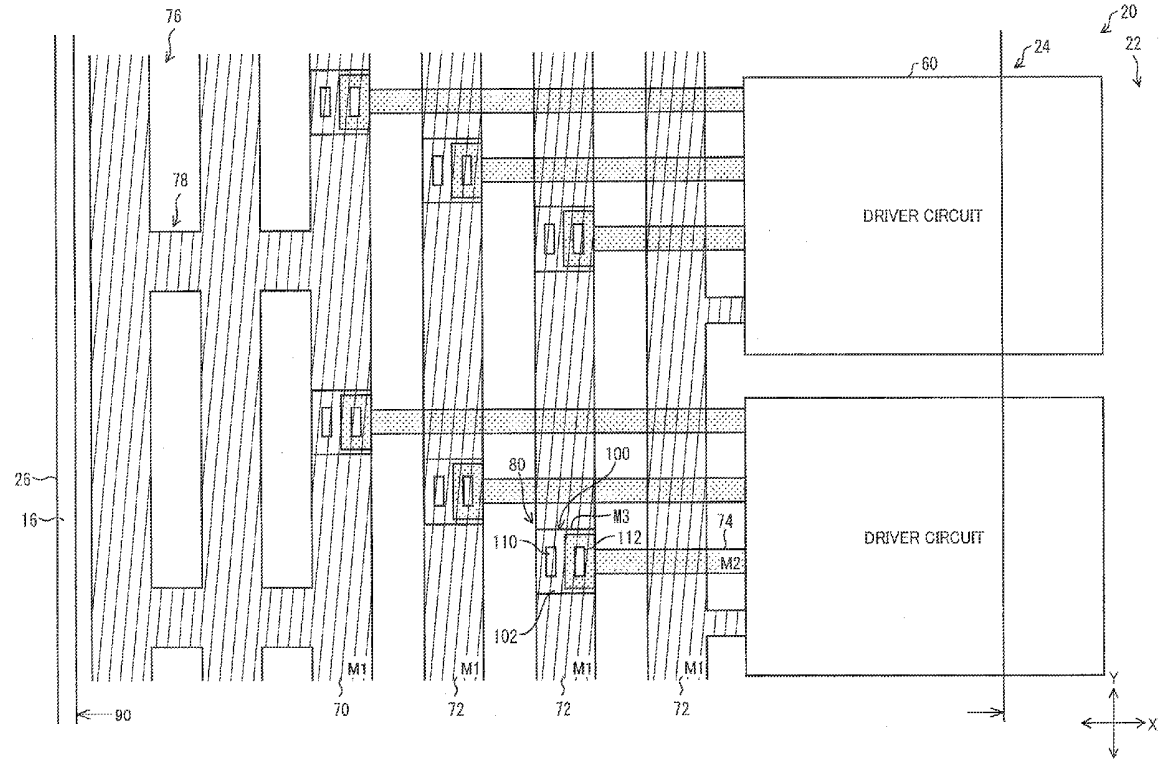
(57) **ABSTRACT**

An embodiment of the present invention provides a TFT array substrate, in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate including: gate bus lines made from a first metal material; source bus lines made from a second metal material; pixel electrodes made from a third metal material; a clock wiring made from the first metal material; a branch wiring made from the second metal material; and a connection conductor made from the third metal material, the connection conductor connecting the clock wiring and the branch wiring at a connection part in a periphery area, the connection part having a branch-wiring via hole, which exposes the branch wiring which is covered with the connection conductor, and overlaps the clock wiring at least partly in a plane view.



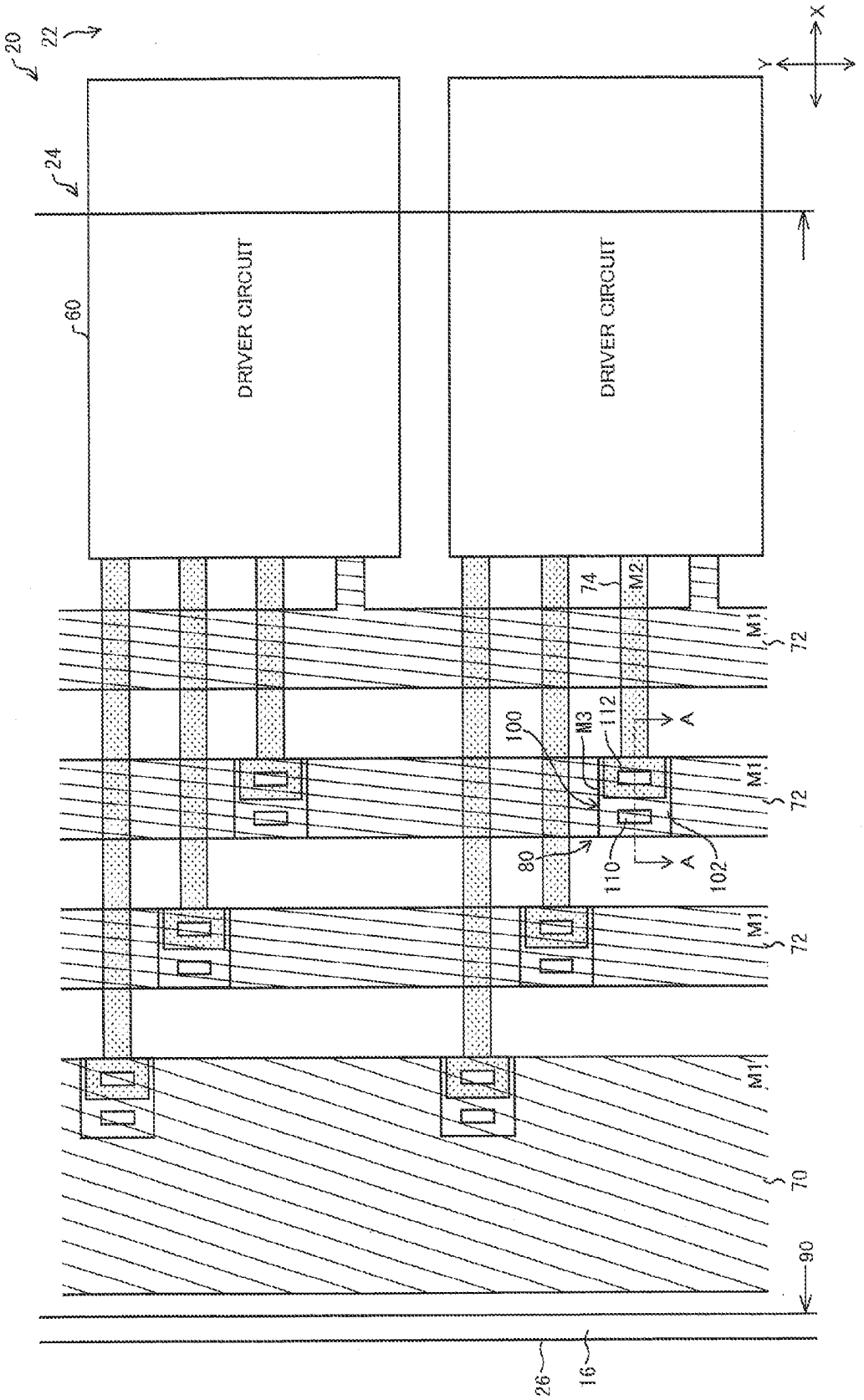
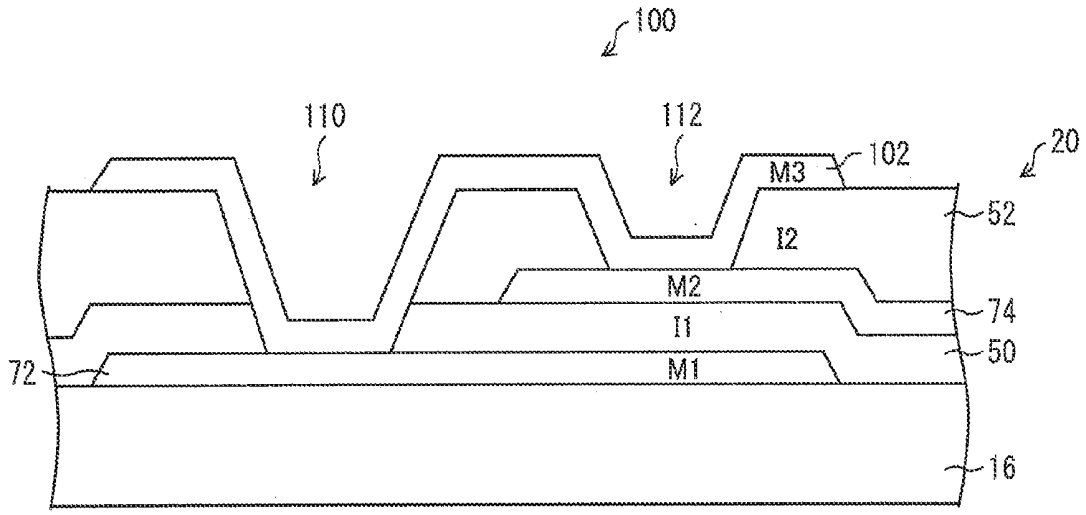

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
74
M2
M1
72
M3
112
100
A
80
110
102
70
90
26
16
X
Y

FIG. 1

FIG. 2



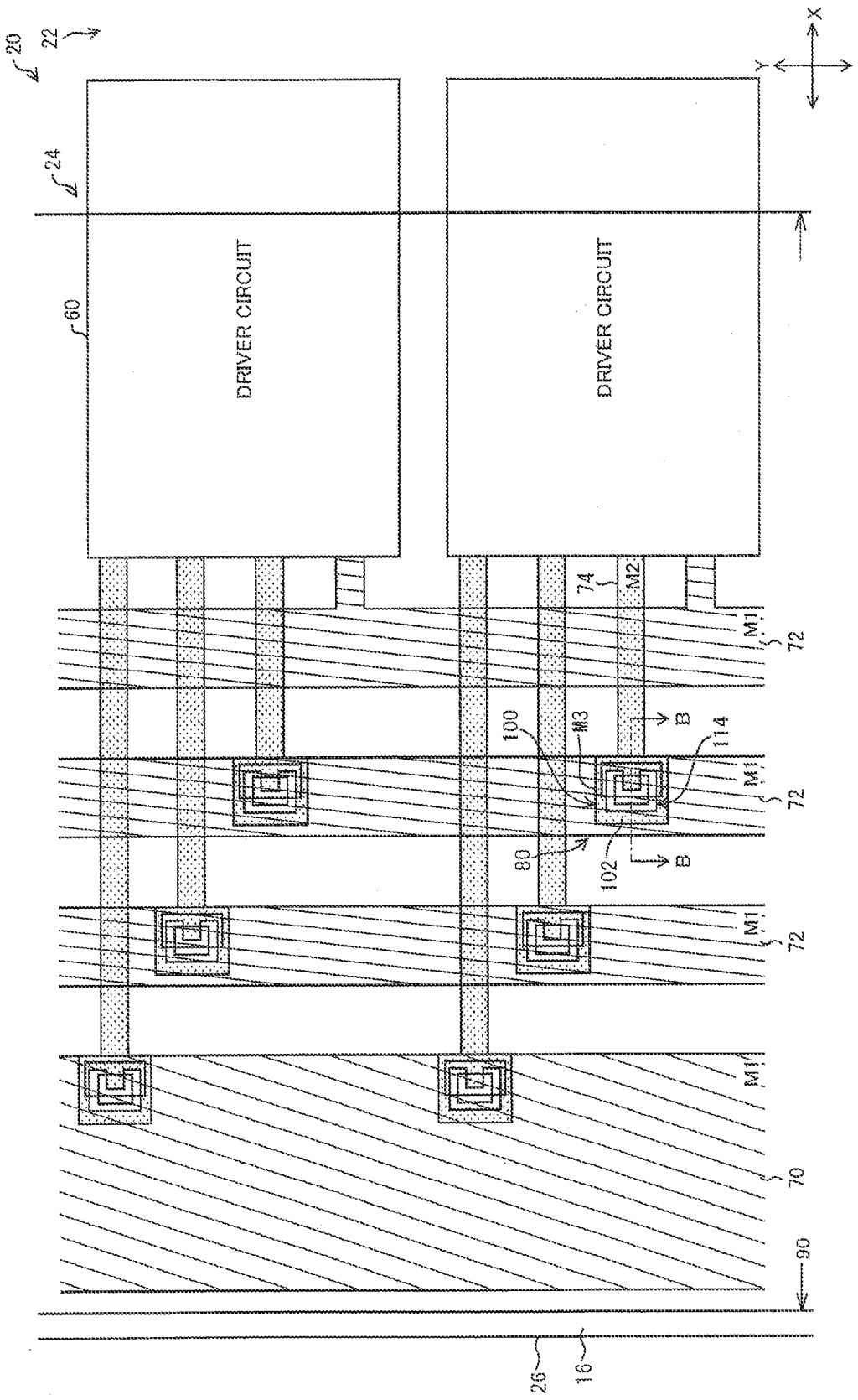
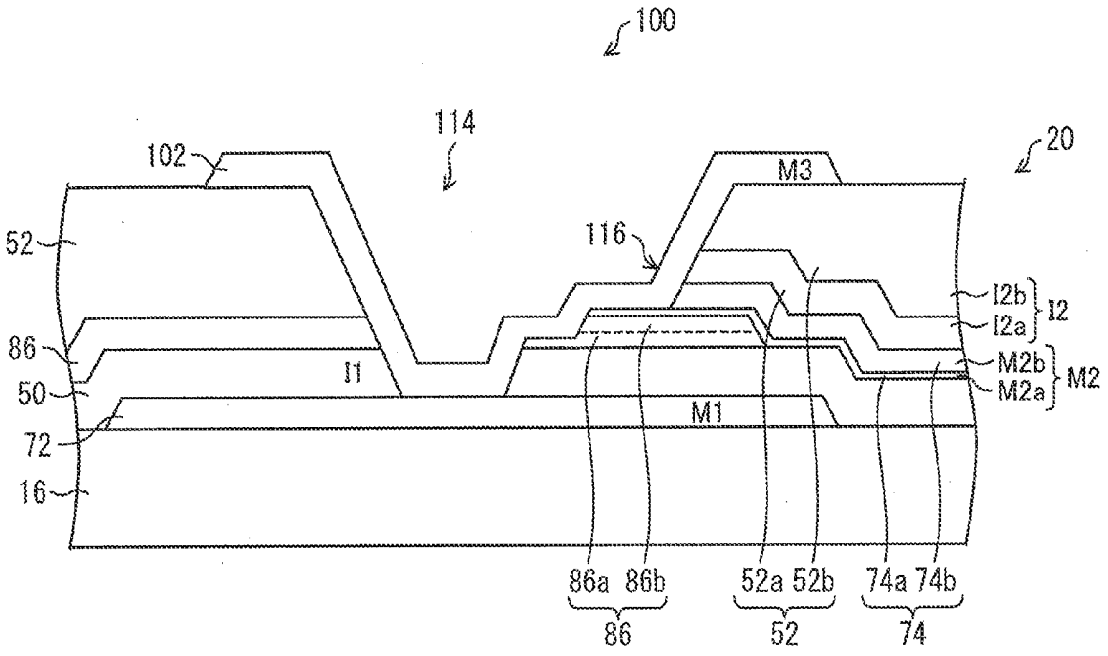

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
100
M3
114
B
80
102
70
90
26
16

FIG. 3

FIG. 4


100
114
102
20
M3
116
52
I2b
I2a
I2
86
I1
M2b
M2a
M2
50
M1
72
16
86a 86b
52a 52b
74a 74b
86
52
74

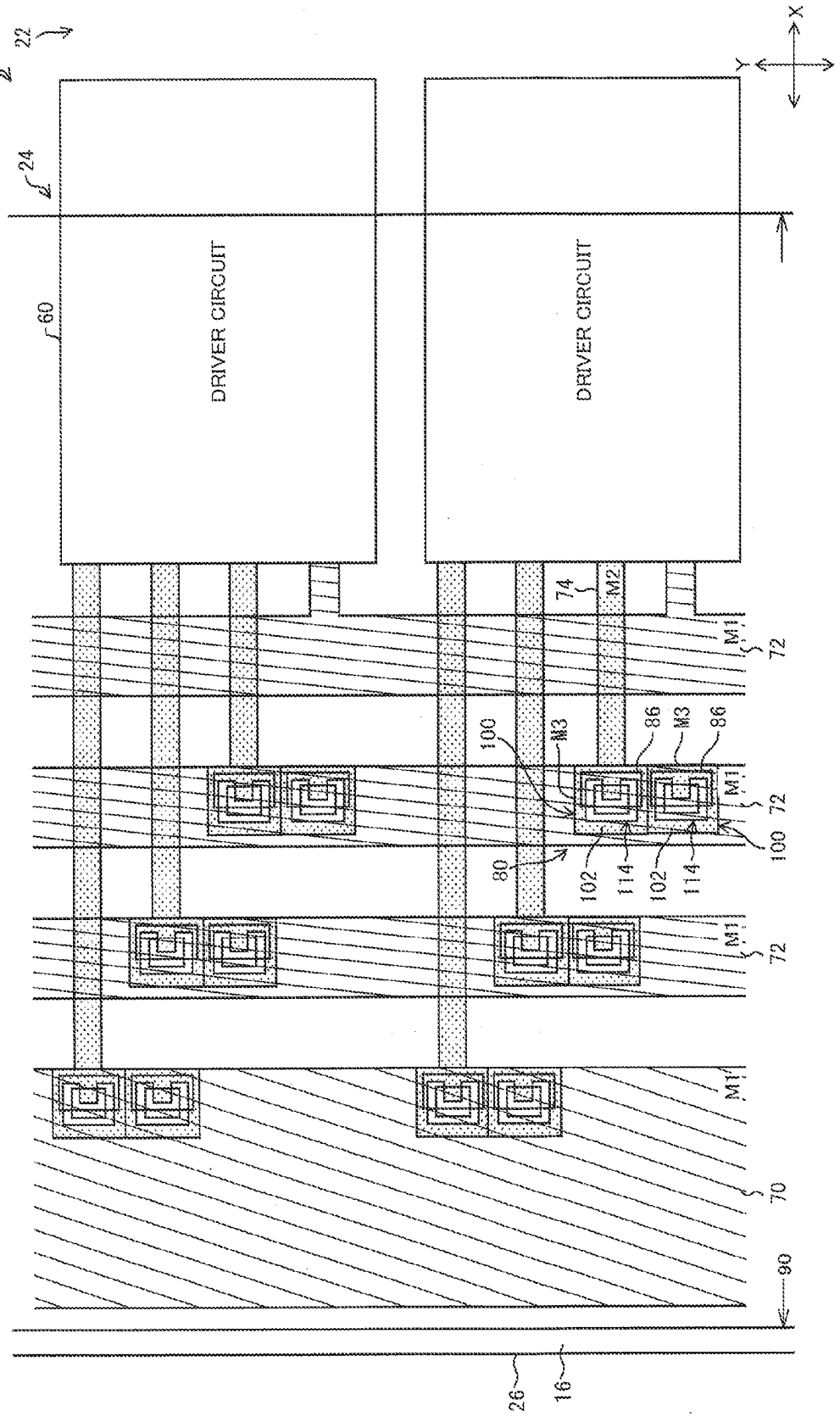

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
74
M2
M1
72
100
M3
86
M3
86
M1
72
100
80
102
114
102
114
M1
72
M1
70
90
26
16
Y
X

FIG. 5

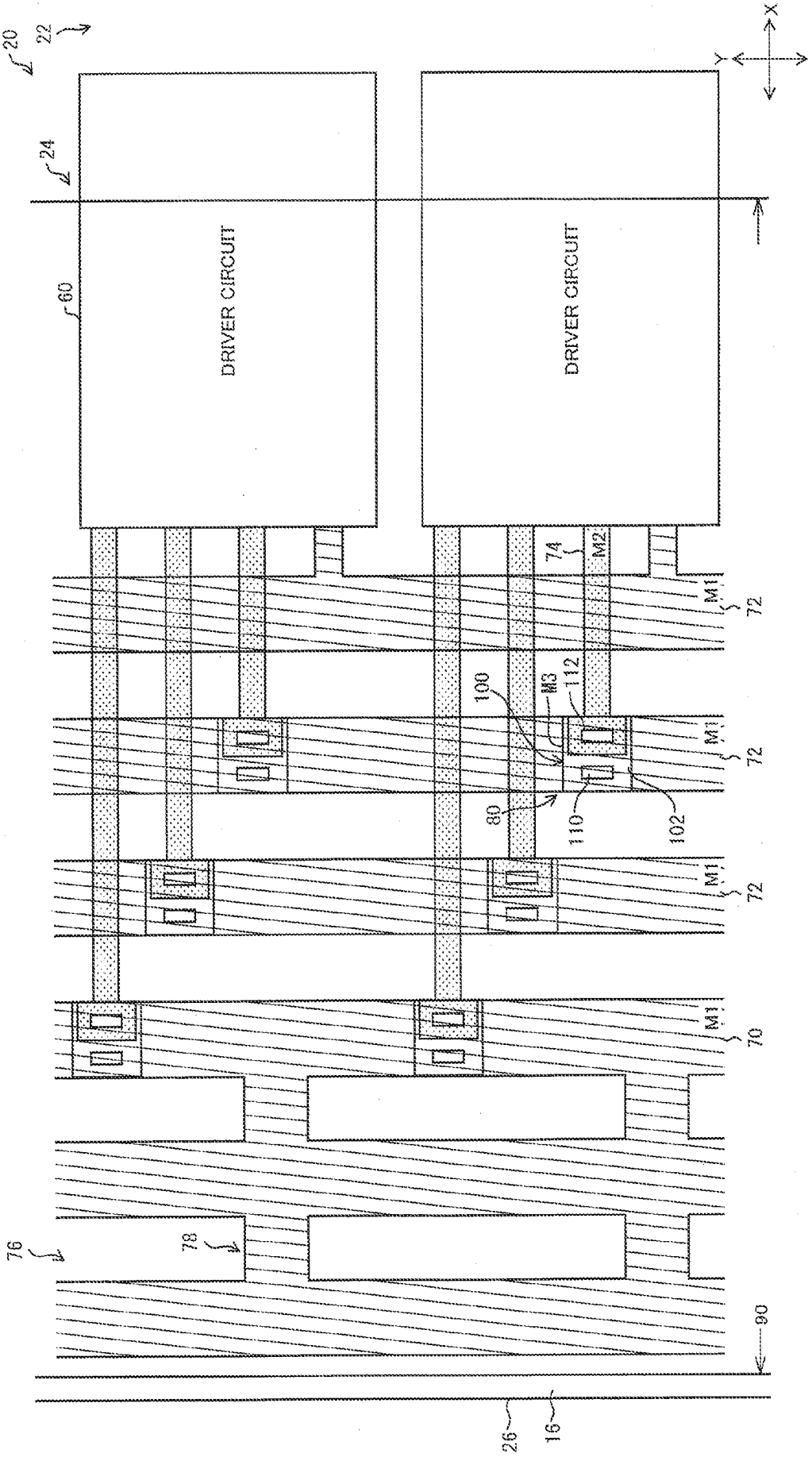

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
74
M2
M1
72
100
M3
112
80
110
102
70
76
78
90
26
16
Y
X

FIG. 6

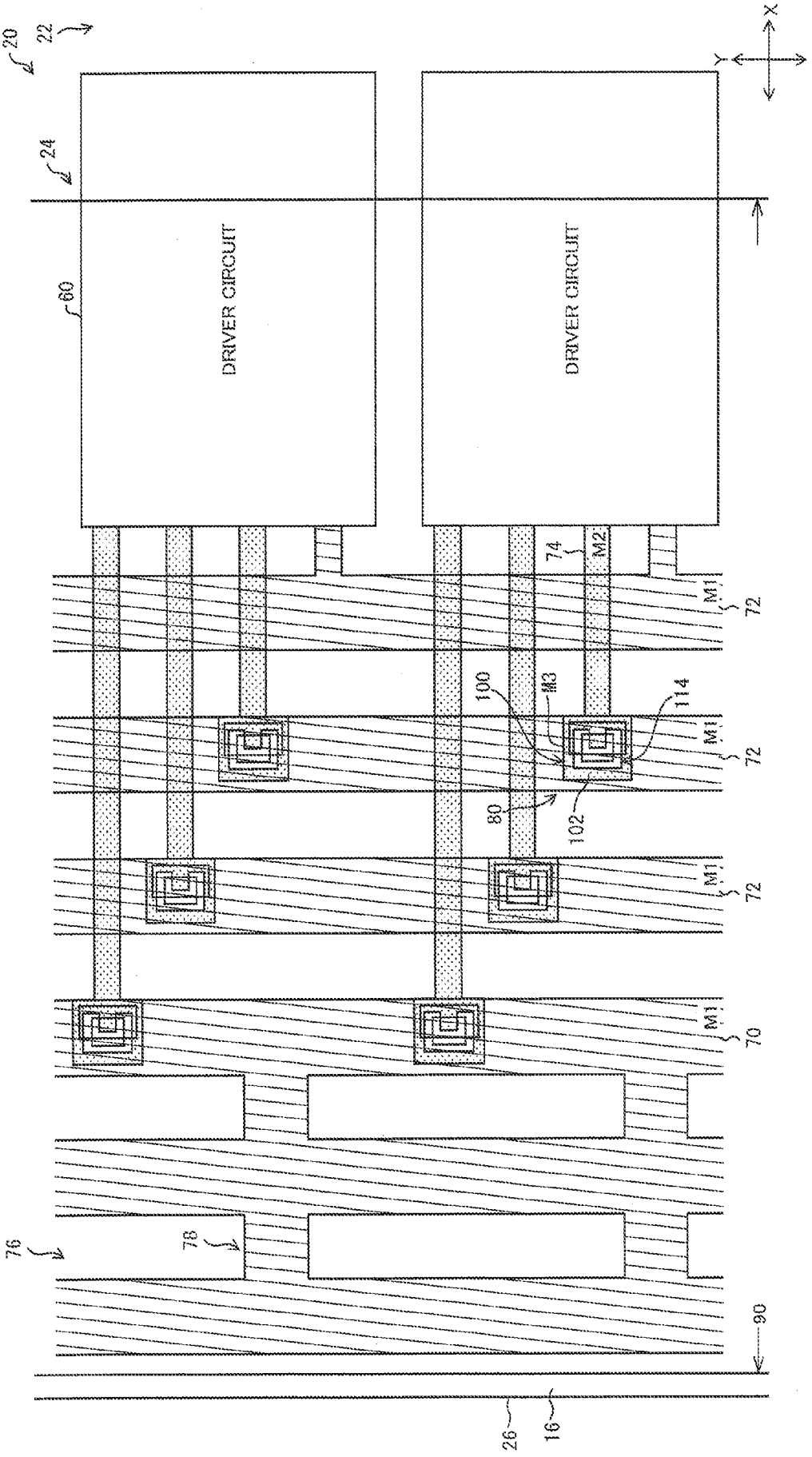

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
74
M2
M1
72
100
M3
114
M1
72
80
102
M1
72
M1
70
76
78
90
26
16
Y
X

FIG. 7

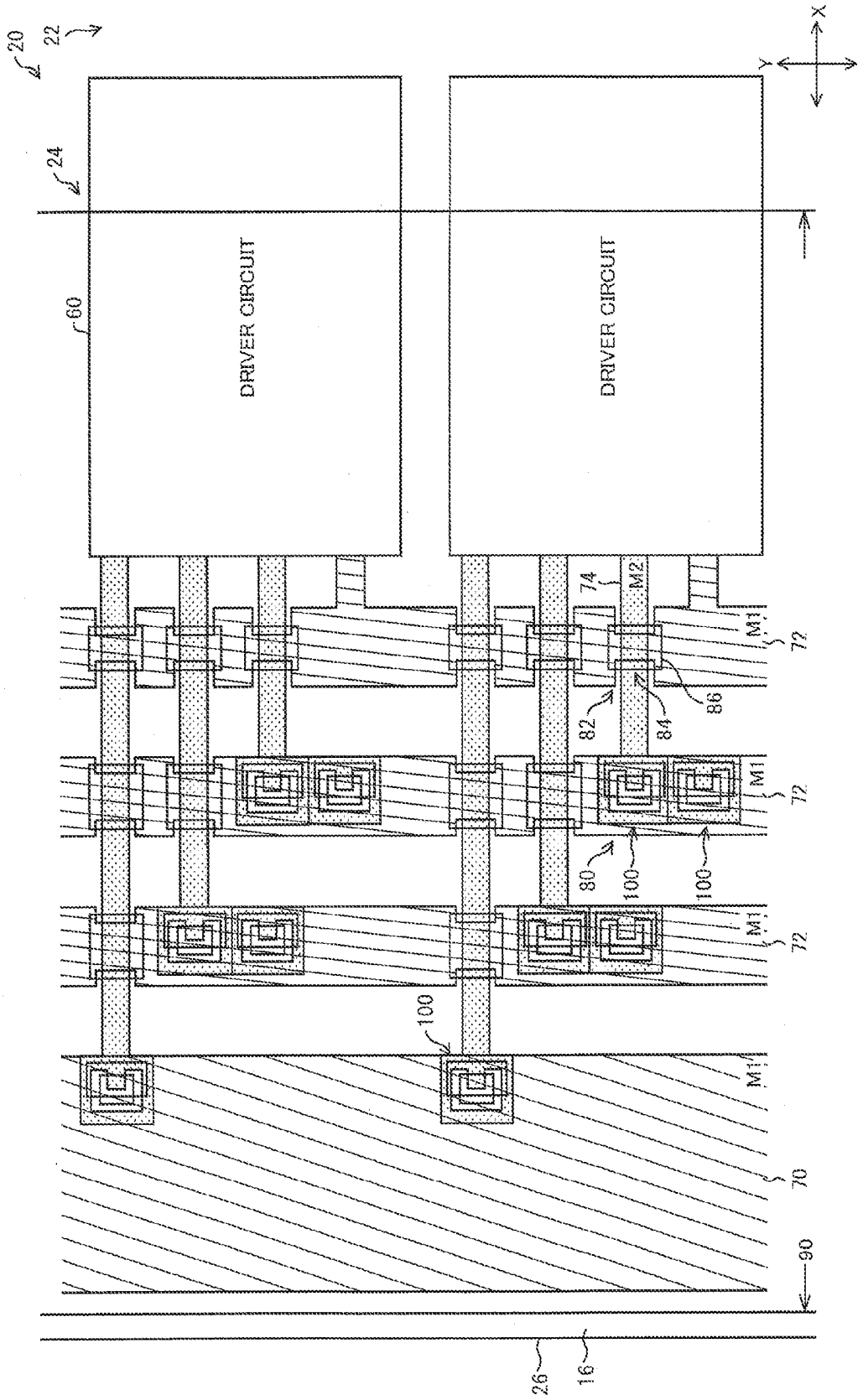

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
X
Y
74
M2
M1
72
82
84
86
80
100
70
90
26
16

FIG. 8

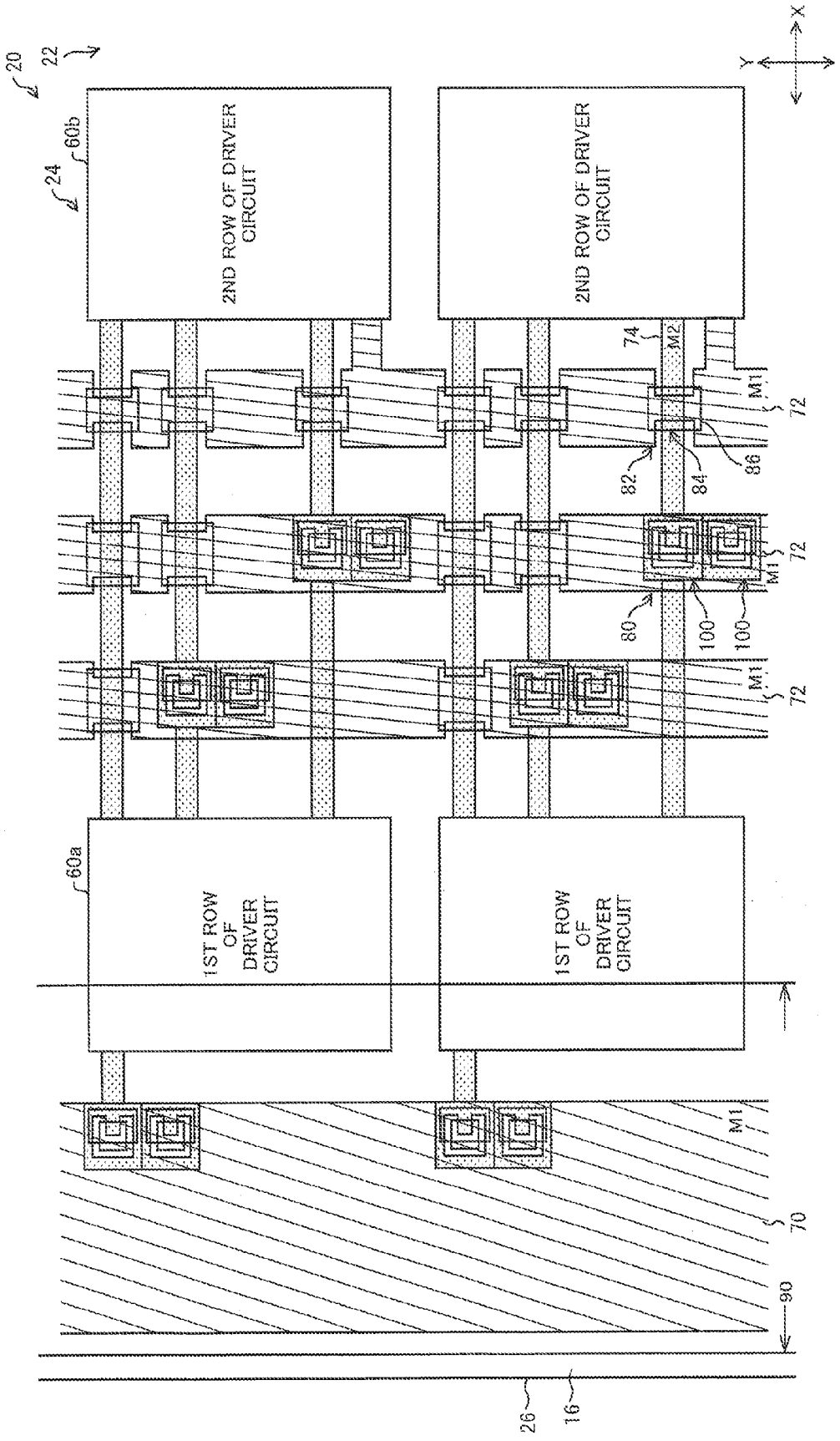

20
22
24
60b
2ND ROW OF DRIVER CIRCUIT
2ND ROW OF DRIVER CIRCUIT
74
M2
M1
72
82
84
86
80
100
100
60a
1ST ROW OF DRIVER CIRCUIT
1ST ROW OF DRIVER CIRCUIT
70
90
26
16
X
Y

FIG. 9

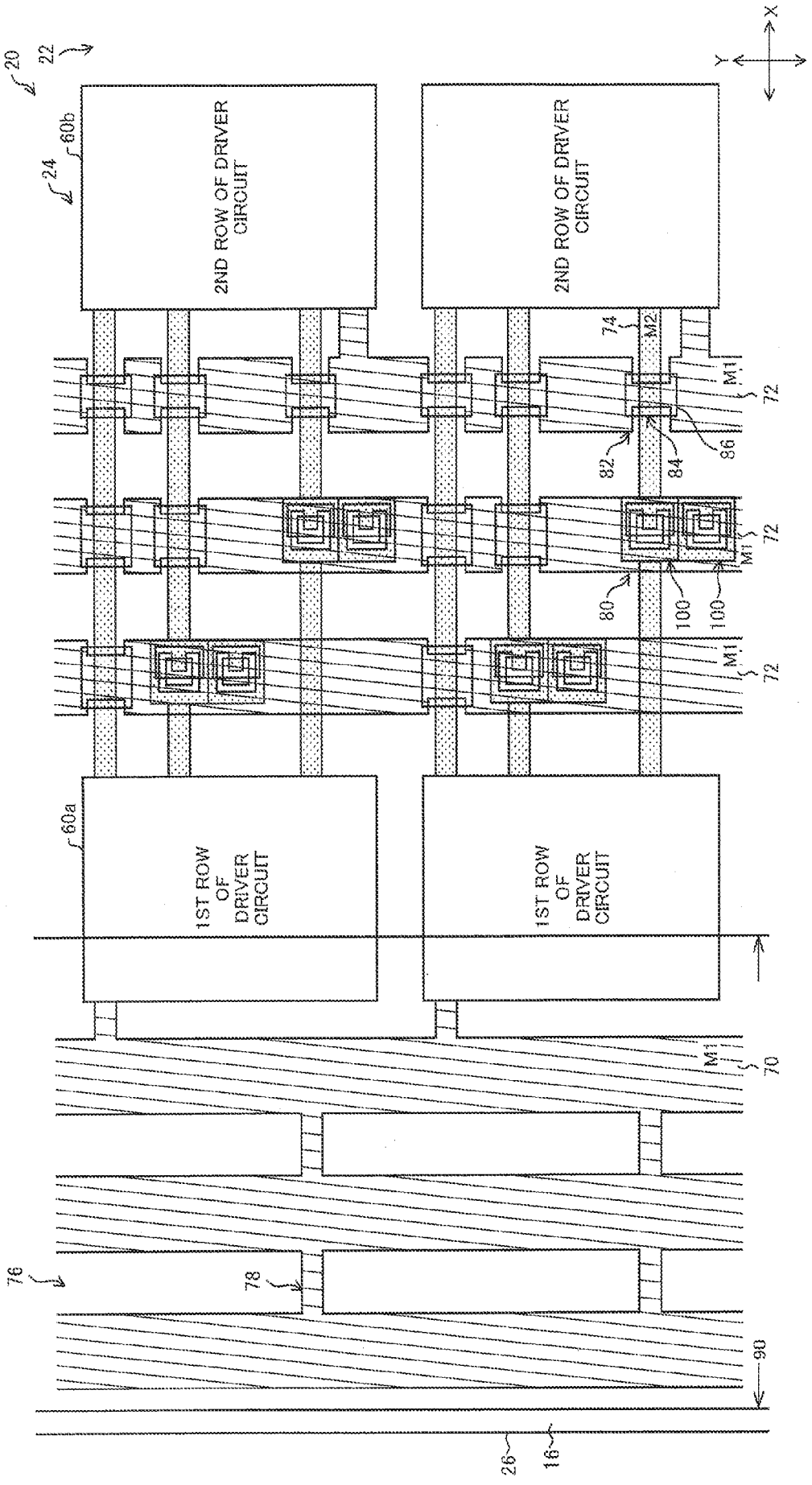

20
22
24
60b
2ND ROW OF DRIVER CIRCUIT
2ND ROW OF DRIVER CIRCUIT
74
M2
M1
72
82
84
86
80
100
100
60a
1ST ROW OF DRIVER CIRCUIT
1ST ROW OF DRIVER CIRCUIT
70
76
78
90
26
16
X
Y

FIG. 10

FIG. 11

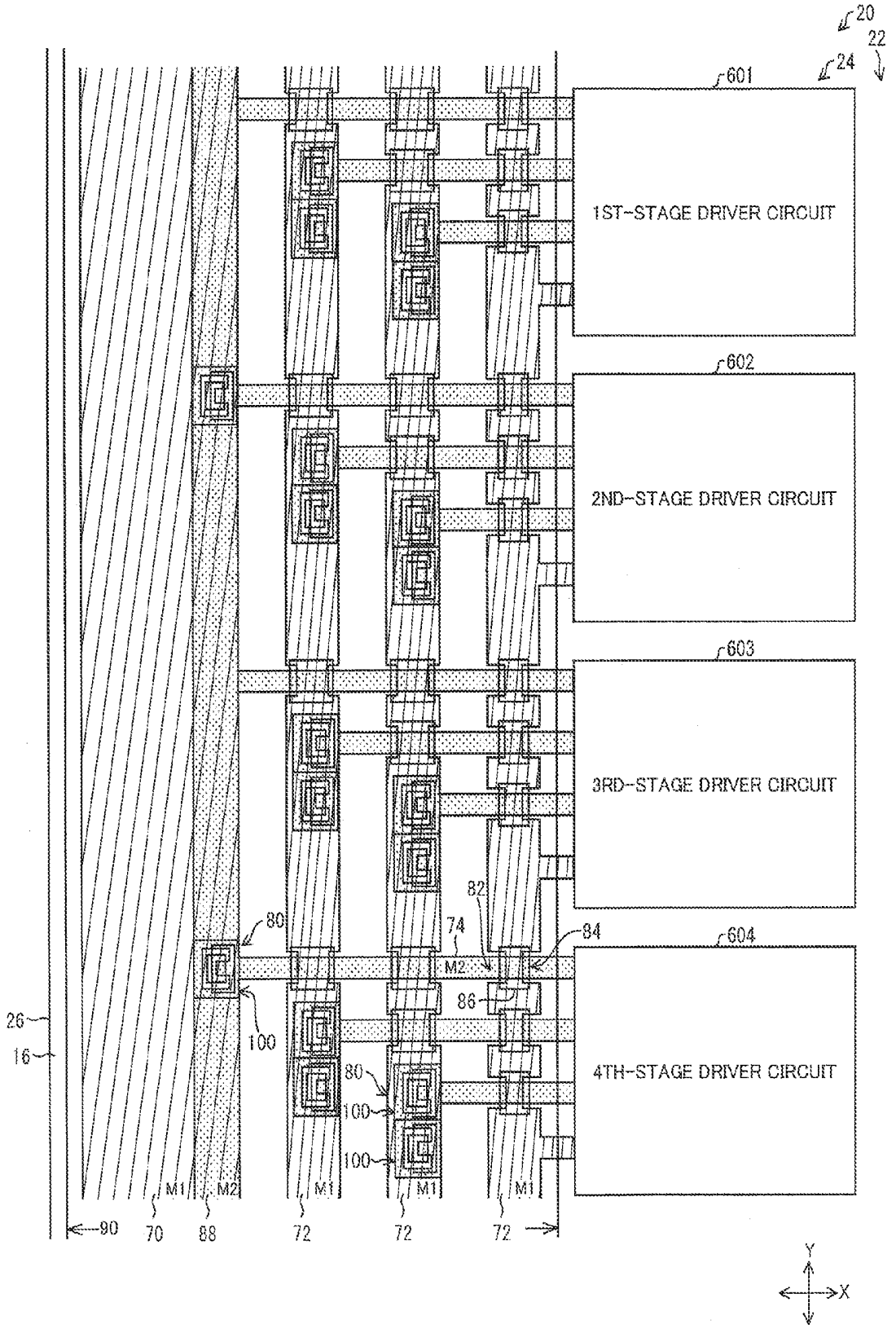
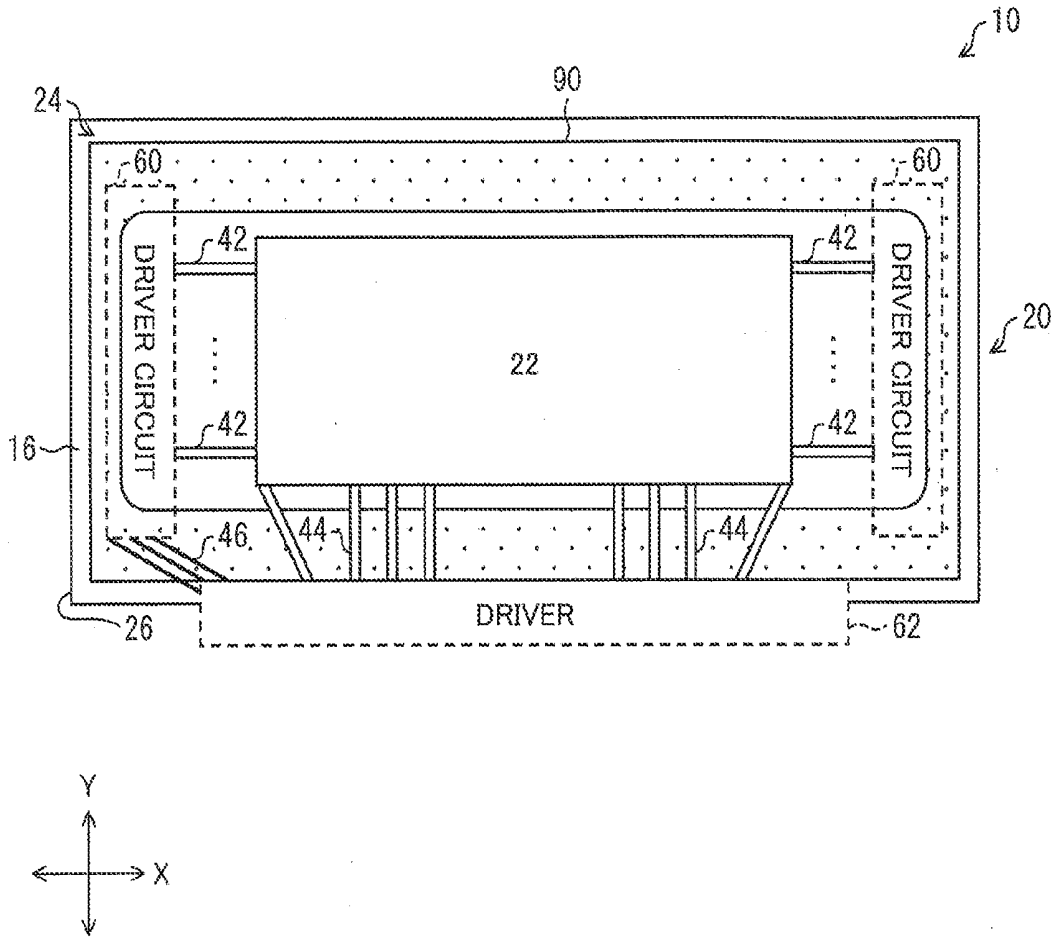

20
22
24
601
1ST-STAGE DRIVER CIRCUIT
602
2ND-STAGE DRIVER CIRCUIT
603
3RD-STAGE DRIVER CIRCUIT
604
4TH-STAGE DRIVER CIRCUIT
26
16
80
74
82
84
M2
86
100
80
100
100
M1
M2
M1
M1
M1
90
70
88
72
72
72
Y
X

FIG. 12


10
90
24
60
60
42
42
DRIVER CIRCUIT
DRIVER CIRCUIT
20
22
16
42
42
46
44
44
DRIVER
26
62
Y
X

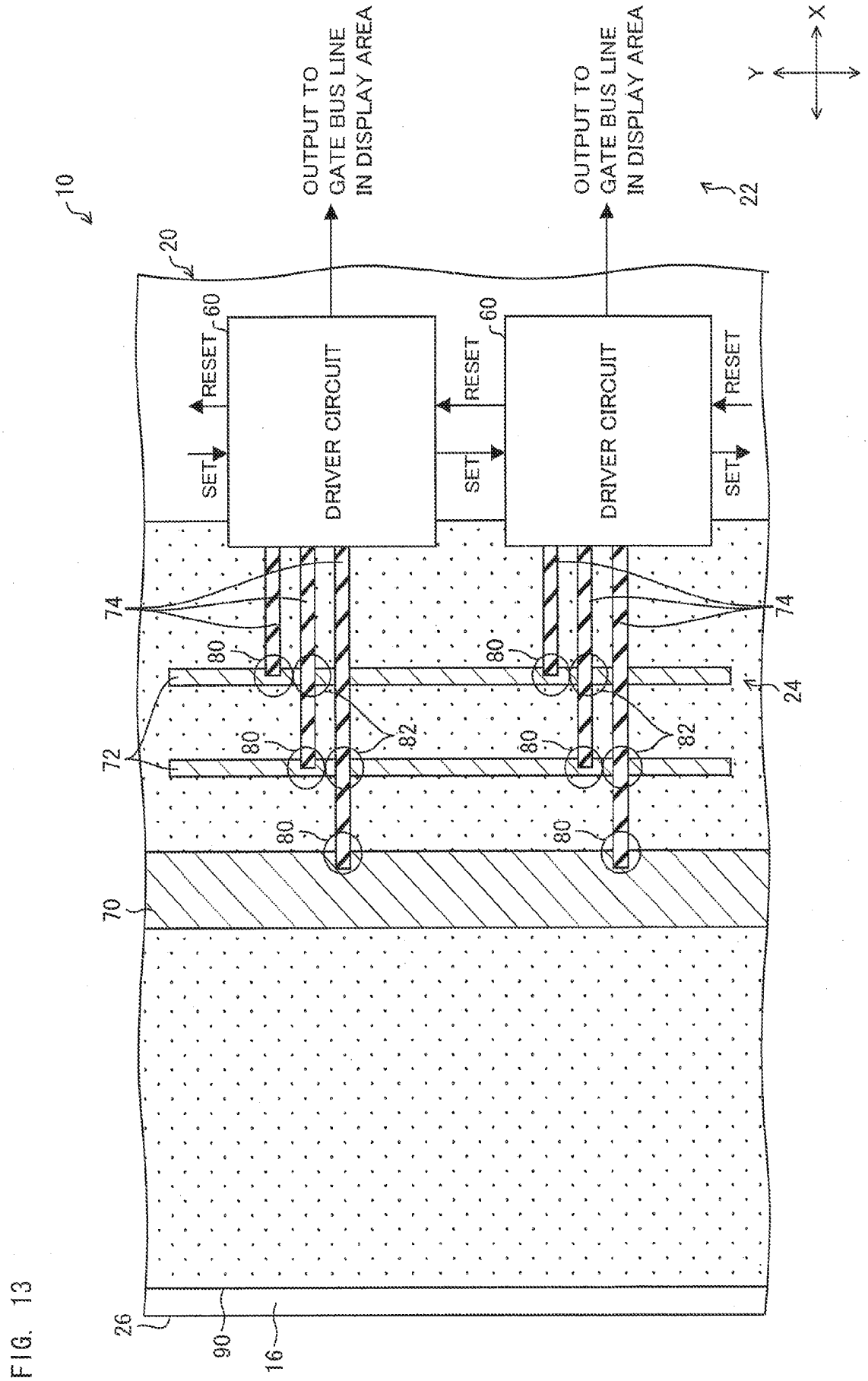
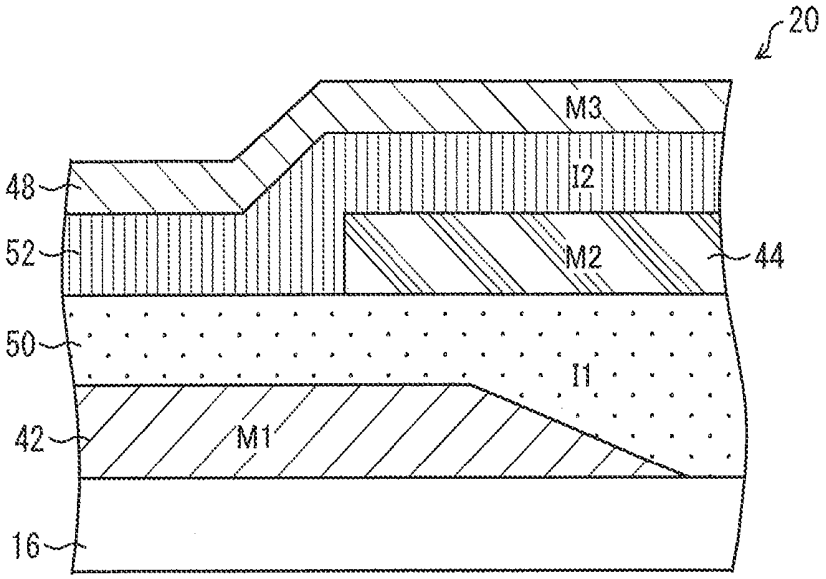

10
20
22
OUTPUT TO GATE BUS LINE IN DISPLAY AREA
OUTPUT TO GATE BUS LINE IN DISPLAY AREA
Y
X
60
RESET
SET
DRIVER CIRCUIT
74
80
82
72
70
24
26
90
16

FIG. 13

FIG. 14



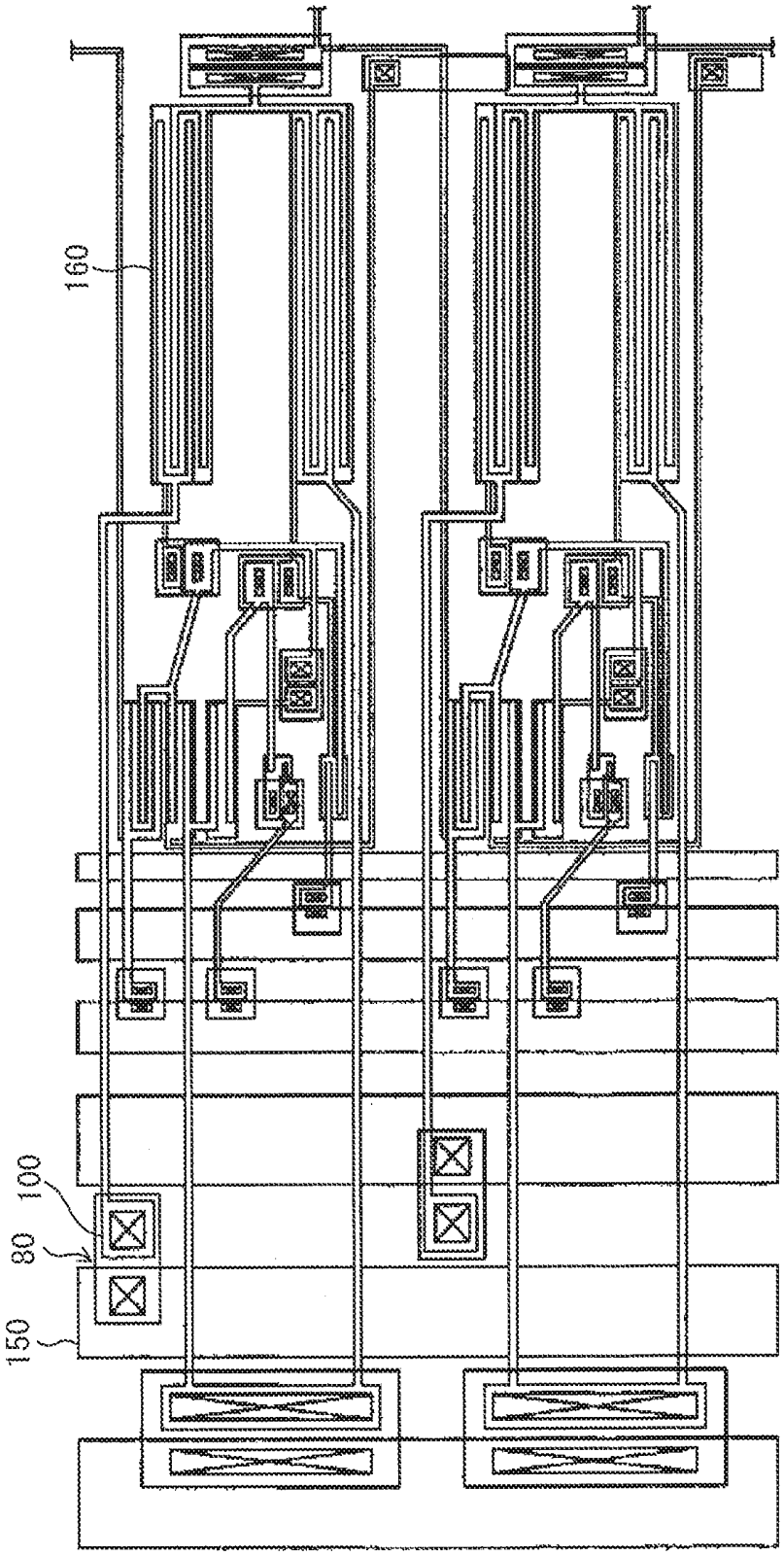


FIG. 15

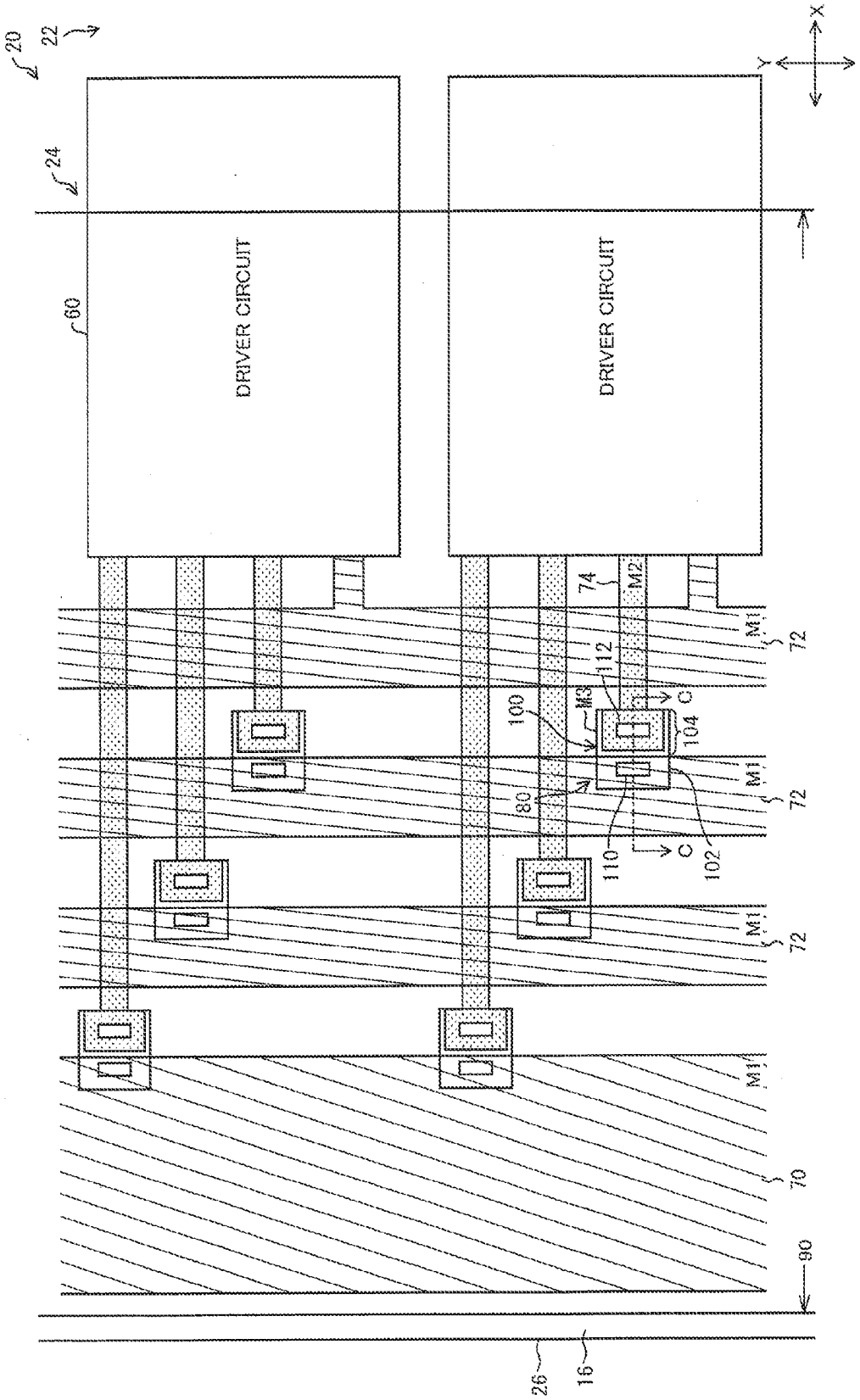

20
22
24
60
DRIVER CIRCUIT
DRIVER CIRCUIT
74
M2
M1
72
112
M3
100
104
C
80
110
102
70
90
26
16
X
Y

FIG. 16

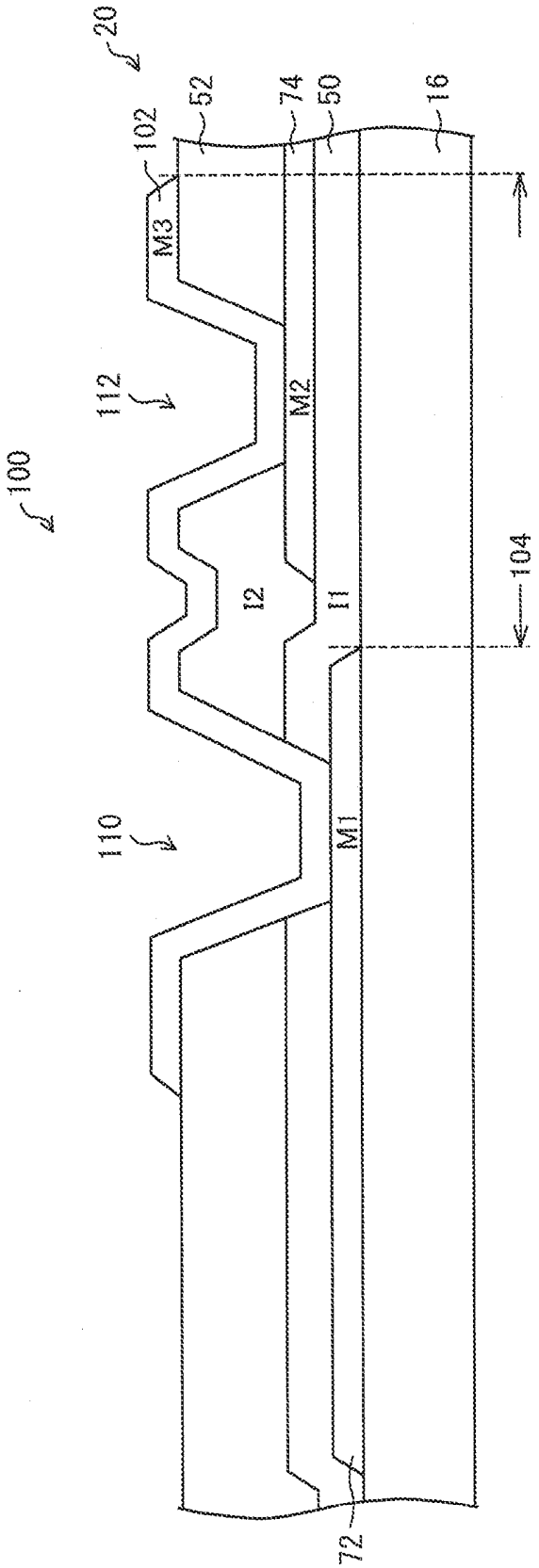


FIG. 17

TFT ARRAY SUBSTRATE, AND LIQUID CRYSTAL DISPLAY PANEL

[0001] This application is a continuation application of and claims priority under 35 U.S.C. §120/121 to U.S. application Ser. No. 14/291,937 filed May 30, 2014, which is a divisional application of and claims priority under 35 U.S.C. §120/121 to U.S. application Ser. No. 13/138,396 filed Aug. 10, 2011, which is a national phase under 35 U.S.C. §371 of PCT International Application No. PCT/JP2009/068905 which has an International filing date of Nov. 5, 2009, which designated the United States of America, and which claims priority to Japanese patent application number JP 2009-033132 filed Feb. 16, 2009, the entire contents of each of which are hereby incorporated herein by reference.

TECHNICAL FIELD

[0002] The present invention relates to a TFT array substrate in which TFT elements are provided on an insulating substrate, and to a liquid crystal display panel using the TFT array substrate.

BACKGROUND ART

[0003] TFT array substrates in which TFT (Thin Film transistor) elements are provided on an insulating substrate have been widely used in display devices (such as liquid crystal panels), and sensor devices. The TFT elements are connected with wirings at their electrodes.

[0004] Specifically, a TFT element is connected with a corresponding gate bus line at its gate electrode, and connected with a corresponding source bus line at its source electrode.

[0005] Moreover, in case where the TFT array substrate is used in a liquid crystal panel, the TFT element is connected with a pixel electrode at its drain electrode.

[0006] In case where the TFT elements are arrayed in matrix, the gate bus lines and the source bus lines are provided perpendicular to each other on the insulating substrate. In this case, the gate bus lines and source bus lines are provided in different layers on the insulating substrate between which an insulating layer is provided, lest the gate bus lines and source bus lines be electrically connected with each other.

[0007] (Schematic Configuration of TFT Array Substrate)

[0008] Next, a configuration of the TFT array substrate is schematically described below.

[0009] FIG. **12** is a plane view schematically illustrating a configuration of a TFT array substrate **20**.

[0010] As illustrated in FIG. **12**, the TFT array substrate **20** has a display area **22** in a central portion thereof in a plane view. In the display area, TFT elements and pixel electrodes correspondingly connected to the TFT elements are arrayed in matrix.

[0011] An area around the display area **22** and in the vicinity of substrate edges **26** of the TFT array substrate **20** is a periphery area **24**. In the periphery area **24**, a driver circuit **60** and the like are provided.

[0012] One specific example of the driver circuit **60** is a gate driver circuit. FIG. **12** illustrates an exemplary configuration in which the driver circuit **60** is provided in the periphery area **24** on either side of the display area **22** in a horizontal direction (the X direction in FIG. **12**).

[0013] In this configuration, the driver **60** is connected with the TFT elements (not illustrated) in the display area **22** via wirings such as the gate bus lines **42**.

[0014] Moreover, the TFT array substrate **20** illustrated in FIG. **12** is provided with a driver **62** in the periphery area **24** on one of both sides of the display area **22** in the vertical direction (the Y direction in FIG. **12**). The driver **62** and the driving circuits **60** are connected via a gate driver circuit signal wiring **46** such as a clock wiring. Moreover, the driver **62** is connected with the TFT element (not illustrated) in the display area **22** via wirings such as the source bus lines **44**.

[0015] Moreover, the TFT array substrate **20** are assembled together with a counter electrode (not illustrated) via a seal **90**, thereby constituting a liquid crystal display panel **10**. The seal **90** is provided in a frame-like shape along and inside the substrate edges **26** of the TFT array substrate **20**.

[0016] (Periphery Area)

[0017] Next, based on FIG. **13**, the periphery area **24** is described in more details.

[0018] FIG. **13** is a plane view schematically illustrating a configuration of the periphery area **24**.

[0019] As illustrated in FIG. **13**, the periphery area **24** is provided with not only the driver circuits **60** but also various wirings connected with the driver **62**. The wirings are provided between the driver circuits **60** and substrate edges **26** of an insulating substrate **16**. FIG. **13** illustrates an example of the TFT array substrate **20** in which a low-potential-side power supply wiring **70**, a clock wiring **72**, and branch wirings **74** are provided as the wirings. Among the wirings, the low-potential-side power supply wiring **70** and the clock wiring **72** are extended in the vertical direction (Y direction) and the branch wirings **74** are extended in the horizontal direction (X direction). Further, the low-potential-side power supply wiring **70** and the clock wiring **72** are electrically connected with the driver circuit **60** via the branch wirings **74**, correspondingly.

[0020] (Metal Materials Etc.)

[0021] Next, metal materials etc. for forming the wirings are explained below.

[0022] The low-potential-side power supply wiring **70** and the clock wiring **72** extended in the Y direction are provided on the insulating substrate in such a manner that the low-potential-side power supply wiring **70** and the clock wiring **72** extended in the Y direction are provided in a layer different from another layer thereon in which the branch wirings **74** extended in the X direction are provided. And, they are formed from different metal materials.

[0023] FIG. **14** is a cross sectional view schematically illustrating a configuration of the TFT array substrate **20**.

[0024] As illustrated in FIG. **14**, it is generally configured such that a first metal material M**1**, a first insulating material I**1**, a second metal material M**2**, a second insulating material **12**, and a third metal material M**3** are laminated in this order on the insulating substrate **16**. The first metal material M**1** is a material from which the gate bus lines **42** are formed. The first insulating material I**1** is a material from which a gate insulating film **50** is formed. The second metal material M**2** is a material from which the source bus lines **44** are formed. The second insulating material **12** is a material from which an interlayer insulating film **52** is formed. And the third metal material M**3** is a material from which pixel electrodes **48** are formed.

[0025] The low-potential-side power supply wiring **70** and the clock wiring **72** are formed from the first metal material M**1**, and the branch wirings **74** are formed from the second metal material M**2**.

[0026] With this configuration, a wiring extended in the X direction can be crossed easily with a wiring extended in the Y direction, without electrically connecting these wirings as illustrated in an intersection part **82** in FIG. **13**.

[0027] On the other hand, it is necessary to provide a contact hole in order to establish electrical connection between a wiring extended in the X direction and a wiring extended in the Y direction, as illustrated at a connection portion **80** in FIG. **13**.

[0028] (Patent Literature 1)

[0029] One conventional configuration of such a contact hole is one as illustrated in Patent Literature 1, for example.

[0030] FIG. **15** is a view illustrating an amorphous silicon thin film transistor liquid crystal display panel as described in Patent Literature 1.

[0031] As illustrated in FIG. **15**, a main wiring **150** and a gate electrode **160** are connected electrically via a contact hole **100** provided in a connection portion **80**.

CITATION LIST

Patent Literatures

[0032] [Patent Literature 1]

[0033] Japanese Translation of PCT Application, Tokuhyo, No. 2005-527856 A (Publication Date: Sep. 15, 2005)

[0034] [Patent Literature 2]

[0035] U.S. Pat. No. 7,379,148 B2, specification (May 27, 2008)

[0036] [Patent Literature 3]

[0037] Japanese Patent Application Publication, Tokukai, No. 2006-259691 (Publication Date: Sep. 28, 2006)

[0038] [Patent Literature 4]

[0039] Japanese Patent Application Publication, Tokukaihei, No. 9-179116 (Publication Date: Jul. 11, 1997)

[0040] [Patent Literature 5]

[0041] Japanese Patent Application Publication, Tokukai, No. 2006-39524 (Publication Date: Feb. 9, 2006)

SUMMARY OF INVENTION

Technical Problem

[0042] However, the conventional configuration of the contact hole **100** has such a problem that it causes deterioration in display quality of the liquid crystal display panel **100**. The following explains the problem.

[0043] FIG. **16** is a view schematically illustrating a configuration of a conventional connection portion **80**. Meanwhile, FIG. **17** is a cross sectional view taken across line C-C of FIG. **16**.

[0044] As illustrated in FIG. **16**, the conventional contact hole **100** is partly on and off the clock wiring **72** when viewed in a plane view. That is, the conventional contact hole **100** has an off-wiring portion **104**.

[0045] As illustrated in FIG. **17**, the contact hole **100** allows the clock wiring **72** to be connected with the branch wiring **74**.

[0046] The clock wiring **72** is formed from the first metal material M1 from which the layer of the gate bus line **42** is formed. Meanwhile, the branch wiring **74** is formed from the second metal material M2 from which the layer of the source bus line **44** is formed. Therefore, the clock wiring **72** and the branch wiring **74** are formed on the different layers on the insulating substrate **16**.

[0047] A connection conductor **102** provided in the contact hole **100** connects the clock wiring **72** with the branch wiring **74**. However, the clock wiring **72** and the branch wiring **74** do not overlap each other in the plane view. Accordingly, the connection conductor **102** is so provided that it can connect the clock wiring **72** with the branch wiring **74** in the plane view.

[0048] (Via Hole)

[0049] More specifically, through a main-wiring via hole **110**, the connection conductor **102** and the clock wiring **72** are connected with each other at a place where the connection conductor **102** and the clock wiring **72** overlap each other in a plane view. Meanwhile, through a branch-wiring via hole **112**, the connection conductor **102** and the branch wiring **74** are connected with each other at a place where the connection conductor **102** and the branch wiring **74** overlap each other in a plane view.

[0050] In other words, the contact hole **100** is so configured that the clock wiring **72** and the branch wiring **74** are connected through the two via holes.

[0051] Here, the connection conductor **102** is formed from the third metal material M3, which is a material from which the pixel electrodes are formed.

[0052] In the vicinity of the main-wiring via hole **110**, the gate insulating film **50** and the interlayer insulating film **52** intervene between the clock wiring **72** and the connection conductor **102**. Accordingly, the main-wiring via hole **110** penetrates the gate insulating film **50** and the interlayer insulating film **52** so as to allow the clock wiring **72** and the connection conductor **102** to be connected with each other.

[0053] Similarly, in the vicinity of the branch-wiring via hole **112**, the interlayer insulating film **52** intervenes between the branch wiring **74** and the connection conductor **102**. Accordingly, the branch-wiring via hole **112** penetrates the interlayer insulating film **52** so as to allow the branch wiring **74** and the connection conductor **102** to be connected with each other.

[0054] (Off-Wiring Portion)

[0055] The main-wiring via hole **110** and the branch-wiring via hole **112** are connected via the connection conductor **102**.

[0056] The conventional TFT array substrate **20** is so configured that the clock wiring **72** and the branch wiring **74** do not overlap each other in a plane view. That is, the branch wiring **74** is extended just short of clock wiring **72**. Accordingly, the connection conductor **102** has an off-wiring portion **104**. The off-wiring portion **104** is that portion of the connection conductor **102** which is off the clock wiring **72** in a plane view.

[0057] The off-wiring portion **104** allows the connection between the main-wiring via hole **110** and the branch-wiring via hole **112**.

[0058] (Seal)

[0059] Next, the seal **90** for bonding the TFT array substrate **20** with the counter substrate.

[0060] The seal **90** is provided in the periphery area **24** of the TFT array substrate **20** so as to be along the substrate edges **26**, as illustrated in FIG. **12**. As illustrated in FIG. **16**, the seal **90** covers the low-potential-side power supply wiring **70**, the clock wiring **72**, and, partly, the driver circuits **60**. That is, in the plane view, the seal **90** overlaps the wiring extended in the X direction, and the wiring extended in the Y direction.

[0061] The seal **90** is so positioned for the sake of sufficiently functioning to bond the TFT array substrate **20** and the counter substrate **18**, and reducing an area of the frame portion.

[0062] Because the seal **90** is so positioned, the contact hole **100** is positioned under the seal **90**.

[0063] (Cell Thickness)

[0064] The conventional liquid crystal display panel **10** likely fails to keep a uniform cell thickness in the vicinity of the seal **90**.

[0065] The failure of keeping uniform cell thickness is due to a level difference caused by the contact hole **100** and to differences in width, density, etc. of the wirings provided under the seal **90**.

[0066] Especially, the conventional liquid crystal display panel **10** in which the connection conductor **102** has the off-wiring portion is apt to have such an uneven cell thickness.

[0067] (Seal Thickness)

[0068] The uneven cell thickness is caused because there are regions with or without the contact hole **100** when viewed along the Y direction. That is, the uneven cell thickness is caused because the seal **90** has an uneven thickness between the two kind regions. In addition to two dent parts due to the main-wiring via hole **110** and the branch-wiring via hole **112**, there is a dent portion formed along the Y direction at or near the contact hole **100**. The dent portion formed along the Y direction at or near the contact hole **100** likely causes the uneven cell thickness.

[0069] As described above, the conventional liquid crystal display panel **10** likely has an uneven cell thickness due to pattern configuration at or near the contact hole **100** or uneven wiring density at or near the contact hole **100**.

[0070] (Display Quality)

[0071] The uneven cell thickness likely deteriorates a display quality.

[0072] Moreover, the conventional liquid crystal display panel **10** with the off-wiring portion has such a problem in that the off-wiring portion makes it difficult to perform uniform light irradiation to a light curing resin or the like in case where the light curing resin or the like is provided at or near the contact hole **100**. This leads to insufficient curing of the light curing resin. In such a case, a material of the sealing **90** would likely seep in a liquid crystal layer, thereby causing poor display quality.

[0073] (Output Characteristics of Driver Circuit)

[0074] Further, in response to recent demands for outer dimensional reduction of display panels, the periphery area **24** of the TFT array substrate **20** may be reduced in area, as a result of which inter-wiring distances between wirings such the low-potential-side power supply wiring **70** and clock wiring **72** should be smaller. In this case, the configuration with the off-wiring portion may be a hindrance to the reduction in the inter-wiring distances. That is, the reduction in the inter-wiring distances cannot be done in such a way that an area in which the off-wiring portion overlaps an adjacent wiring is reduced or a distance from the off-wiring portion to such an adjacent wiring is reduced, because, if the off-wiring portion is so arranged, wiring load will be increased, thereby deteriorating the output characteristics of the driver circuits.

[0075] The present invention was accomplished in order to solve the problems, and an object thereof is to provide a TFT array substrate and a liquid crystal display panel, each of which can avoid display quality deterioration caused by an uneven cell thickness.

Solution to Problem

[0076] In order to attain the object, a TFT array substrate according to the present invention is a TFT array substrate, in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate including: gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material, the pixel electrodes being made from a third metal material, the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area, the periphery area being provided with driver circuits for driving the TFT elements corresponding thereto, the periphery area being provided with (i) branch wirings being correspondingly connected with the driver circuits, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material, the main wiring being formed from the other one of the first metal material and the second metal material, the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings, at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings, the connection conductor being formed from the third metal material, the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings, which is covered with the connection conductor, is exposed, at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0077] Moreover, in order to attain the object, a TFT array substrate according to the present invention is a TFT array substrate in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate including: gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material, the pixel electrodes being made from a third metal material, the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area, the periphery area being provided with periphery TFT elements for driving the TFT elements corresponding thereto, the periphery area being provided with (i) branch wirings being correspondingly connected with the periphery TFT elements, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material, the main wiring being formed from the other one of the first metal material and the second metal material, the periphery area being provided with connection parts, at which the main wiring is connected with the respective

branch wirings, at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings, the connection conductor being formed from the third metal material, the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings is exposed, provided that the connection conductor covers this exposed portion of the corresponding one of the branch wirings, at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0078] In these configurations, in the connection parts, at least part of the branch-wiring via hole overlaps with the main wiring in a plane view. These configurations makes it difficult for the connection conductor to have a off-wiring portion described above, thereby causing the wiring layer to have more uniform thickness in the direction in which the main wirings extend.

[0079] This makes it easy to prevent the uneven cell thickness, for example, in case where the seal is provided in the periphery area. Thus, it becomes easier to prevent display quality deterioration in the TFT array substrate with any of these configurations.

Advantageous Effects of Invention

[0080] As described above, the TFT array substrate according to the present invention is configured to include: gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material, the pixel electrodes being made from a third metal material, the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area, the periphery area being provided with driver circuits or periphery TFT elements for driving the TFT elements corresponding thereto, the periphery area being provided with (i) branch wirings being correspondingly connected with the driver circuits or periphery TFT elements, and (ii) a main wring being connected with the branch wirings, the branch wirings being formed from one of the first metal material and the second metal material, the main wiring being formed from the other one of the first metal material and the second metal material, the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings, at each of the connection parts, a connection conductor connecting the main wiring with corresponding one of the branch wirings, the connection conductor being formed from the third metal material, the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings, which is covered with the connection conductor, is exposed, at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0081] This makes it possible to prevent display quality deterioration caused by uneven cell thickness.

BRIEF DESCRIPTION OF DRAWINGS

[0082] FIG. **1** is a view schematically illustrating a configuration of a TFT array substrate according to one embodiment of the present invention.

[0083] FIG. **2** is a view illustrating a cross section taken along line A-A of FIG. **1**.

[0084] FIG. **3** is a view schematically illustrating a configuration of a TFT array substrate according to another embodiment of the present invention.

[0085] FIG. **4** is a view illustrating a cross section taken along line B-B of FIG. **3**.

[0086] FIG. **5** is a view schematically illustrating a configuration of a TFT array substrate according to still another embodiment of the present invention.

[0087] FIG. **6** is a view schematically illustrating a configuration of a TFT array substrate according to yet another embodiment of the present invention.

[0088] FIG. **7** is a view schematically illustrating a configuration of a TFT array substrate according to yet another embodiment of the present invention.

[0089] FIG. **8** is a view schematically illustrating a configuration of a TFT array substrate according to yet still another embodiment of the present invention.

[0090] FIG. **9** is a view schematically illustrating a configuration of a TFT array substrate according to further another embodiment of the present invention.

[0091] FIG. **10** is a view schematically illustrating a configuration of a TFT array substrate according to further another embodiment of the present invention.

[0092] FIG. **11** is a view schematically illustrating a configuration of a TFT array substrate according to yet further another embodiment of the present invention.

[0093] FIG. **12** is a plane view schematically illustrating a configuration of a TFT array substrate.

[0094] FIG. **13** is a plane view schematically illustrating a configuration of a periphery area of the TFT array substrate.

[0095] FIG. **14** is a cross sectional view schematically illustrating a configuration of the TFT array substrate.

[0096] FIG. **15** is a view illustrating an amorphous silicon thin film transistor liquid crystal display panel as described in Patent Literature 1.

[0097] FIG. **16** is a view illustrating a conventional art and schematically illustrating a configuration of a connection portion.

[0098] FIG. **17** is a cross sectional view taken along line C-C of FIG. **16**.

DESCRIPTION OF EMBODIMENTS

[0099] In the followings, embodiments of the present invention are described in more details.

Embodiment 1

[0100] One embodiment of the present invention is described below referring to FIGS. **1** and **2**.

[0101] FIG. **1** is a view schematically illustrating a configuration of a TFT array substrate **20** of the present embodiment.

[0102] The schematic configuration of the TFT array substrate **20** of the present embodiment is substantially similar to that of the TFT array substrate **20** explained above referring to FIG. **16**.

[0103] That is, various wirings (wiring layer) and driver circuits are provided in a periphery area **24** of the TFT array substrate **20**.

[0104] More specifically, the various wirings encompass a low-potential-side power supply wiring **70** (signal wiring for scanning line driver circuits) and clock wirings **72** (signal wiring for scanning line driver circuits) along the Y direction

of the TFT array substrate **20**. The low-potential-side power supply wiring **70** and clock wirings **72** are each main wirings. More specifically, one low-potential-side power supply wiring **70**, and three clock wirings **72** are aligned in this order in a direction of from one substrate edge **26** to a display area **22**.

[0105] Moreover, driver circuits **60** (such as gate driver circuits) are provided between these wirings and the display area **22**.

[0106] Here, the display area **22** is an area in which TFT elements (not illustrated) and pixel electrodes (not illustrated) connected correspondingly with the TFT elements are arrayed in matrix.

[0107] Further, branch wirings **74** are provided for connecting these wirings correspondingly with the driver circuits **60**. The branch wirings **74** are extended in the X direction.

[0108] A contact hole **100** is provided at each of intersection parts **80** at which the branch wirings **74** are connected with the low-potential-side power supply wiring **70** or any of the clock wirings **72** correspondingly.

[0109] The TFT array substrate **20** according to the present embodiment is so configured that a connection conductor **102** has no off-wiring portion **104** described above. In the following, the configuration of the present embodiment is described referring to a connection portion **80** for connection between a clock wiring **72** and a branch wiring **74**, for example.

[0110] At the connection portion **80**, the clock wiring **72** and the branch wiring **74** are electrically connected with each other through a contact hole **100**.

[0111] Referring to FIG. **2**, this configuration is described in further details. FIG. **2** is a cross sectional view taken along line A-A of FIG. **1**.

[0112] As illustrated in FIG. **2**, the contact hole **100** has two via holes, namely, a main-wiring via hole **110** and a branch-wiring via hole **112**. Through the main-wiring via hole **110**, the connection conductor **102** and the clock wiring **72** are connected with each other. In other words, through the main-wiring via hole **110**, the clock wiring **72** (serving as a main wiring) which is covered with the connection conductor **102**, is exposed.

[0113] Moreover, through the branch-wiring via hole **112**, the connection conductor **102** and the branch wiring **74** are connected with each other. In other words, through the branch-wiring via hole **112**, the branch wiring **74** is exposed, provided that the connection conductor **102** covers this exposed portion of the branch wiring **74**. The clock wiring **72** is formed from a first metal material M1 from which gate bus lines **42** are formed. Meanwhile, the branch wiring **74** is formed from a second metal material M2 from which source bus lines **44** are formed. Moreover, the connection conductor **102** is formed from a third metal material M3 from which the pixel electrodes **48** are formed.

[0114] These metal materials are laminated on an insulting substrate **16** made of glass in an order of the first metal material M1, the second metal material M2, and the third metal material M3. Between the first metal material M1 and the second metal material M2, a gate insulating film **50** is provided. The gate insulating film **50** is formed from a first insulating material I1. Moreover, between the second metal material M2 and the third metal material M3, an interlayer insulating film **52** is provided. The interlayer insulating film **52** is formed from a second insulating material **12**. Moreover, the first metal material M1 and the second metal material M2 may be, but not limited to, aluminum, molybdenum, tantalum, or the like. Moreover, the third metal material M3 may be, for example, ITO (Indium Tin Oxide) or the like.

[0115] With this configuration, at the main-wiring via hole **110**, the connection conductor **102** penetrates the gate insulating film **50** and the interlayer insulating film **52** and is connected with the clock wiring **72**.

[0116] Moreover, at the branch-wiring via hole **112**, the connection conductor **102** penetrates the interlayer insulating film **52** and is connected with the branch wiring **74**.

[0117] Moreover, the TFT array substrate **20** of the present embodiment is so configured that, at the connection portion **80**, the clock wiring **72** and branch wiring **74** overlap each other in a plane view.

[0118] Therefore, the connection conductor **102** has no portion under which neither the clock wiring **72** nor the branch wiring **74** is provided. In other words, either the clock wiring **72** or the branch wiring **74** are provided under the connection conductor **102** with no exception. What is meant by the wording "under" the connection conductor **102** or the portion thereof is under these but above the insulating substrate **16**.

[0119] In the configuration explained above, the connection conductor **102** has no off-wiring portion in which, in a plane view, the connection conductor **102** does not overlap any of the wirings to which the connection conductor **102** is connected. In other words, in the connection portion **80**, the connection conductor **102** is provided only on the wirings to which the connection conductor **102** is connected.

[0120] More specifically, the TFT array substrate **20** exemplified in the present embodiment is so configured that the connection conductor **102** overlaps the clock wiring **72** in a plane view in such a way that both sides of the connection conductor **102** are matched with sides of the clock wiring **72**. Therefore, the connection conductor **102** has no portion that is off the clock wiring **72** in a plane view.

[0121] As described above, the connection conductor **102** of the present embodiment overlaps the clock wiring **72** in a plane view in such a way that both sides of the connection conductor **102** are matched with sides of the clock wiring **72**, wherein the clock wiring is a wiring undermost between two wirings to which the connection conductor **102** is connected, in other words a wiring that is closer to the insulting substrate **16** between the two wirings to which the connection conductor **102** is connected.

[0122] On the other hand, the branch wiring **74** connected with the clock wiring **72** is extended to overlap the clock wiring **72** in a plane view, unlike the conventional TFT array substrate **20** illustrated in FIG. **16**.

[0123] With this configuration, the main-wiring via hole **110** and the branch-wiring via hole **112** can be provided above the clock wiring **72** in a plane view, as illustrated in FIG. **2**. Further, with this configuration, the connection conductor **102** for covering and connecting the main-wiring via hole **110** and the branch-wiring via hole **112** can be provided without being off the clock wiring **72** in a plane view.

[0124] (Display Quality)

[0125] As described above, the connection conductor **102** is provided without being off the clock wiring **72** in a plane view, thereby making it possible to inhibit uneven cell thickness.

[0126] More specifically, the connection conductor **102** can easily attain a stable surface configuration, because the connection conductor **102** is provided over a uniform conductive layer.

[0127] In the present embodiment, the conductive layer under the whole connection conductor **102** is the clock wiring **72** provided on the insulating substrate **16**. Because of this, the connection conductor **102** can easily attain a stable surface configuration.

[0128] Moreover, the connection conductor **102** has no off-wiring portion **104**. Therefore, it becomes easier to have a more uniform wiring density under the seal **90** even if a contact hole is provided on a signal wiring for a scanning line driver circuit.

[0129] As a result, it becomes easy to attain uniform cell thickness in the TFT array substrate **20** of the present embodiment.

[0130] Moreover, because uneven cell thickness is thus inhibited, deterioration in display quality is inhibited in the TFT array substrate **20** of the present embodiment.

[0131] This effect of inhibiting the display quality deterioration caused due to the unevenness in the wirings or the like under the seal **90** is especially effective to a configuration in which the interlayer insulating film **52** is not a flattening film such as an organic film.

[0132] (Seal Curing)

[0133] Moreover, the TFT array substrate **20** according to the present embodiment makes it easier to cure the seal **90** surely.

[0134] As described above referring to FIG. **12** and the like, the seal **90** for bonding the TFT array substrate **20** and the counter substrate (not illustrated) is provided in the periphery area **24** of the TFT array substrate **20**. As a result, the contact holes **100** and their vicinities are covered with the seal **90**.

[0135] In many cases, the seal **90** is UV-light curable. Further, in such a case, the seal **90** is irradiated with UV light from below the insulating substrate **16**. Herein, the wording from below the insulating substrate **16**" means "from that side of the insulating substrate **16** on which the clock wiring **72** is not provided".

[0136] Further, the clock wiring **72**, the branch wiring **74**, etc. are not UV permeable in general, because these wirings, etc. are formed from a conductor(s), that is, metal.

[0137] Therefore, it is preferable that the peripheral area **24** in which the seal **90** is provided does not have too much wirings etc. therein. And if the peripheral area **24** has wirings etc. therein, it is preferable that the wirings has uniform density over the peripheral area **24**.

[0138] In this regard, the TFT array substrate **20** according to the present embodiment is so configured that the connection conductor **102** has no off-wiring portion **104**. More specifically, the connection conductor **102** has no portion that is off the clock wiring **72** in a plane view.

[0139] Consequently, the periphery area **24** has a smaller portion that is provided with the metal.

[0140] Accordingly, it becomes easier to attain more even density in the portion that is provided with the metal. This is attributed to the absence of the off-wiring portion **104** that is a metal protrusion.

[0141] With these reasons, the TFT array substrate **20** according to the present embodiment makes it easy to evenly irradiate light to the seal **90**. As a result, the curing of the seal **90** can be surely performed.

[0142] This ensured effect of the seal **90** is particularly effective in a liquid crystal display panel which is manufactured by One-Drop-Fill method for introducing liquid crystal.

[0143] (Narrower Frame)

[0144] Moreover, with this configuration in which the connect conductor **102** has no off-wiring portion **104**, it is possible to reduce the area occupied by the contact hole **100**. Therefore, a wiring area can be smaller, thereby allowing the frame portion of the liquid crystal display panel to be narrower.

[0145] It should be noted that the present invention is not limited to the wiring width exemplified in FIG. **1** in which the clock wirings **72** are identical in wiring width.

[0146] Moreover, it is preferable that the peripheral area **24** has substantially same wiring density at edges (gate edges) in the X direction in FIG. **1** and at edges (source edges) in the Y direction in FIG. **1**. Here, the wiring density=wiring width/space.

[0147] Moreover, the clock wirings **72** and the low-potential-side power supply wiring **70** (outer wiring) may or may not be formed from an identical metal material. For example, the low-potential-side power supply wiring **70** may be formed from the second metal material. In such a configuration, the low-potential-side power supply wiring **70** and the branch wiring **74** can be electrically connected without using the contact hole **100**.

[0148] Moreover, the present invention is not limited as to how many the low-potential-side power supply wiring **70** is provided, while the present embodiment exemplifies a configuration in which the single low-potential-side power supply wiring **70** is provided. That is, a plurality of low-potential-side power supply wirings **70** may be provided.

Embodiment 2

[0149] Another embodiment of the present embodiment is described below, referring to FIGS. **3** and **4**. FIG. **3** is a view schematically illustrating a configuration of a TFT array substrate **20** according to the present embodiment. Moreover, FIG. **4** is a cross-sectional view taken along line B-B of FIG. **3**.

[0150] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in Embodiment 1, and their explanation is not repeated here.

[0151] The TFT array substrate **20** of the present embodiment is different from the TFT array substrate **20** of Embodiment 1 in terms of the configuration of the contact hole **100**.

[0152] More specifically, the contact hole **100** of the present embodiment is different from that of Embodiment 1 in terms of how many via holes are provided in one contact hole **100**.

[0153] That is, the contact hole **100** of Embodiment 1 has two via holes: the main-wiring via hole **110** and the branch-wiring via hole **112**.

[0154] On the other hand, the contact hole **100** of the present embodiment has only one via hole, namely, a single via hole **114** serving as the branch via hole **112**. In the following, this configuration is described in more details.

[0155] As illustrated in FIG. **4**, the contact hole **100** of the present embodiment is also configured such that a branch wiring **74** overlaps a clock wiring **72** in a plane view. Further, a connection conductor **102** overlaps the clock wiring **72** in a plane view. Moreover, the connection conductor **102** has no off-wiring portion **104** that is off the clock wiring **72**.

[0156] Unlike the contact hole **100** in Embodiment 1, the contact hole **100** of the present embodiment is configured

such that the branch wiring **74** is provided in the vicinity of a via hole through which the connection conductor **102** is connected with the clock wiring **72**.

[0157] Further, the branch wiring **74** is electrically connected with a side wall **116** of the via hole through which the connection conductor **102** and the clock wiring **72** are connected with each other.

[0158] With this configuration, the contact hole **100** of the present embodiment has only one via hole, namely, the single via hole **114**, for the connection between the clock wiring **72** and the branch wiring **74**.

[0159] Moreover, the TFT array substrate **20** of the present embodiment is provided with a semiconductor layer **86**. The semiconductor layer **86** is provided between a gate insulating film **50** and a branch wiring **74**. More specifically, the semiconductor layer **86** includes a lower semiconductor layer **86***a* provided on the gate insulating film **50**, and an upper semiconductor layer **86***b* provided on the lower semiconductor layer **86***a*.

[0160] The lower semiconductor layer **86***a* is a general semiconductor layer. Moreover, the upper semiconductor layer **86***b* is an ohmic contact layer.

[0161] The TFT array substrate **20** of the present embodiment is provided with the semiconductor layer **86**, thereby having a taper portion of the ohmic contact layer. The taper portion of the ohmic contact layer can prevent the connection conductor from being disconnected due to unevenness.

[0162] Moreover, the TFT array substrate **20** of the present embodiment is so configured that the branch wiring **74** includes two metal layers. More specifically, the branch wiring **74** includes a lower branch wiring **74***a* and an upper branch wiring **74***b*, wherein the insulating substrate **16** is closer to the lower branch wiring **74***a* than to the upper branch wiring **74***b*. The lower branch wiring **74***a* is formed from titanium (Ti), which is a metal material M2*a*. Meanwhile, the lower branch wiring **74***b* is formed from aluminum (Al), which is a metal material M2*b*.

[0163] (Modification)

[0164] Referring to FIG. **5**, a modification of the TFT array substrate **20** of the present embodiment is described below. FIG. **5** is a view schematically illustrating a configuration of a TFT array substrate **20** according to the modification of the present embodiment.

[0165] The TFT array substrate **20** of the modification illustrated in FIG. **5** has two contact holes **100** for one connection portion **80**.

[0166] More specifically, the two contact holes **100** along the Y direction in which the clock wiring **72** is extended. A connection conductor **102** in one of the two contact holes **100** is connected with that in the other one of the two contact holes **100**.

[0167] Like the TFT array substrate **20** described above, the connection conductor **102** also overlaps the clock wiring **72** and has no off-wiring portion that is off the clock wiring **72**.

[0168] How many contact holes **100** is provided per one connection portion **80** is not limited to two, and may be three or more.

[0169] In the TFT array substrate **20** according to this modification, a plurality of contact holes **100** is provided per one connection portion **80**. Thereby, it becomes possible to reduce contact resistance.

Embodiment 3

[0170] In the following, yet another embodiment of the present invention is described referring to FIGS. **6** and **7**. FIGS. **6** and **7** are views schematically illustrating a configuration of a TFT array substrate **20** according to the present embodiment.

[0171] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0172] The TFT array substrate **20** of the present embodiment is different from each TFT array substrate **20** of the aforementioned embodiments in terms of a wiring shape. More specifically, a wiring extended in the Y direction has a ladder-like shape.

[0173] In examples respectively illustrated in FIGS. **6** and **7**, a low-potential-side power supply wiring **70**, provided in an outer location toward a substrate edge **26** has a ladder-like shape.

[0174] More specifically, the low-potential-side power supply wiring **70** has rectangular void parts **76**. In the examples illustrated in FIGS. **6** and **7**, the void parts **76** are provided in two rows along the Y directions.

[0175] Each portion between the void parts **76** adjacent in the Y direction is a joint portion **78**. The joint parts **78** correspond to "footsteps" of the ladder.

[0176] The examples illustrated in FIGS. **6** and **7** exemplify configurations in which two ladders are aligned in the X direction. However, the present invention is not limited to the number of "ladders" aligned in the X direction, and the number of ladders aligned in the X direction may be just one or may be three or more.

[0177] As described above, the TFT array substrate **20** of the present embodiment is so configured that a wiring has the void parts **76**.

[0178] UV light passes through the void parts **76**. Consequently, the area permissive to UV light is increased, thereby ensuring the curing of the seal **90** as explained above.

Embodiment 4

[0179] Yet still another embodiment of the present invention is described below, referring to FIG. **8**. FIG. **8** is a view schematically illustrating a TFT array substrate **20** of the present embodiment.

[0180] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0181] The TFT array substrate **20** of the present embodiment is different from each TFT array substrate **20** of the aforementioned embodiments in terms of the configuration of the wirings extended in the Y direction. More specifically, at each intersection portion **82**, a wiring extended in the Y direction has a narrowed portion **84**. The intersection parts **82** are intersections at each of which a wiring extended in the Y direction and a wiring extended in the X direction cross each other without being connected with each other electrically.

[0182] As illustrated in FIG. **8**, the TFT array substrate **20** of the present embodiment is so configured that each clock wiring **72** is narrowed in width at each intersection at which the clock wiring **72** cross a branch wiring **74**. This portion at which the clock wiring **72** (wiring extended in the Y

direction) is narrowed in width is the narrowed portion **84**. In other words, the narrowed portion **84** is a constricted part of the clock wiring **72**.

[0183] In the TFT array substrate **20** of the present embodiment, an area in which the clock wirings **72** and the branch wirings **74** overlap at the intersection parts **82** is reduced by providing the narrowed parts **84** to the clock wirings **72**.

[0184] That is, the wirings extended in the Y directions and the wirings extended in the X directions overlap each other in a smaller area.

[0185] With this configuration, capacitance produced between the wirings extended in the Y directions and the wirings extended in the X directions can be reduced at the intersection parts **82**.

[0186] The reduction in such capacitance may lead to circuit output characteristics improvement such as inhibition of signal delay.

[0187] As to a way of narrowing the wiring width, the present invention is not limited particularly. That is, the wiring may be narrowed from both sides, or may be narrowed from one side. Moreover, the wiring may be substantially narrowed by having a void portion in the vicinity of a middle of its width. In other words, the overlapping area with a wiring extended in the X direction can be reduced by providing a void portion to a wiring overlapping the wiring extended in the X direction.

[0188] (Semiconductor Layer)

[0189] Moreover, a semiconductor layer **86** may be provided, with which the narrowed parts **84** overlap. By providing the semiconductor layer **86**, disconnection with the branch wiring and leakage to signal wiring can be inhibited.

Embodiment 5

[0190] Further another embodiment is described below, referring to FIGS. **9** and **10**. FIGS. **9** and **10** are views schematically illustrating TFT array substrates **20** according to further another embodiment of the present invention.

[0191] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0192] The TFT array substrate **20** according to the present embodiment is different from each TFT array substrate **20** according to the aforementioned embodiment in terms of the configuration of the driver circuit **60** and the configuration of the seal **90**.

[0193] (Driver Circuit)

[0194] Firstly, the driver circuit **60** is described below.

[0195] In each of the aforementioned embodiments, only one row of the driver circuits **60** is provided in the X direction, and there is no driver circuit between the wirings extended in the Y direction in the periphery area **24**. That is, the driver circuit **60** is provided in a border area between the periphery area **24** and the display area **22**.

[0196] On the other hand, the TFT array substrate **20** of the present embodiment is so configured to have two rows of the driver circuits **60** in the X direction. Accordingly, a first row of driver circuits **60***a* and a second row of driver circuits **60***b* are aligned in the X direction. More specifically, the first row of driver circuits **60***a* is provided between a low-potential-side power supply wiring **70** (outer wiring) and a clock wiring **72**. The second row of driver circuits **60***b* is provided in the border area between the display area **22** and the periphery area **24**.

[0197] In other words, a signal wiring for a scanning line driver circuit is provided between the rows of the driver circuits **60** in an area not covered by the seal **90**, that is, between the seal **90** and the display area **22** serving as an active area.

[0198] (Seal)

[0199] Next, the seal **90** is described below.

[0200] In each of the aforementioned embodiments, in the periphery area **24**, the seal **90** covers all the wirings extended in the Y direction. More specifically, the low-potential-side power supply wiring **70** and all the clock wirings **72** are covered with the seal **90**.

[0201] Consequently, the contact holes **100** provided respectively at the connection parts **80** are all covered with the seal **90**.

[0202] On the other hand, the TFT array substrate **20** according to the present embodiment is so configured that the seal **90** covers the low-potential-side power supply wiring **70** and part of the first row of driver circuits **60***a*. The clock wirings **72** and the second row of driver circuit **60***b* are not covered with the seal **90**.

[0203] Consequently, contact holes provided above the clock wirings **72** are not covered with the seal **90**.

[0204] With this configuration, the uneven cell thickness is further inhibited in the TFT array substrate **20** of the present embodiment, because the contact holes **100** covered with the seal **90** can be reduced in number.

[0205] Moreover, with this configuration, the signal wiring for the scanning line driver circuit, which signal wiring provided between the first row of driver circuit **60***a* and the second row of driver circuit **60***b*, can be narrower in wiring width, thereby making it easier to narrow the frame portion of the liquid crystal display panel.

[0206] The effect of the inhibition of uneven cell thickness can be achieved by providing one or more of the wirings extended in the Y direction (for example, the clock wirings **72**) between the first row of driver circuits **60***a* and the second row of driver circuits **60***b* in the X direction.

Embodiment 6

[0207] Yet further another embodiment of the present invention is described below, referring to FIG. **11**. FIG. **11** is a view schematically illustrating configuration of a TFT array substrate **20** according to the present embodiment.

[0208] For the sake of easy explanation, like reference numbers are given to members having the like functions similar to those explained in each of the aforementioned embodiments, and their explanation is not repeated here.

[0209] The TFT array substrate **20** of the present embodiment is different from each TFT array substrate **20** in the aforementioned embodiment in that a low-potential-side power supply wiring **70** is overlapped by some branch wirings **74**. More specifically, the branch wiring **74** extended in the X direction so as to overlap the low-potential-side power supply wiring **70** is further extended in the Y direction above the low-potential-side power supply wiring **70**. That portion of the branch wiring **74** which is extended in the Y direction above the low-potential-side power supply wiring **70** is referred to as a branch wiring extension portion **88**.

[0210] In other words, the TFT array substrate **20** according to the present embodiment is configured such that the

area in which the low-potential-side power supply wiring **70** (outer wiring) is provided includes multi metal wiring layers by laminating the first metal material, the second metal material, and the third metal material therein.

[0211] By providing the branch wiring extension portion **88** as described above, it becomes possible that the number of the contact holes **100** is less than the number of the driver circuits **60**. In other words, the number of the contact holes provided for the low-potential-side power supply wiring **70** (outer wiring) can be less than the number of the wirings (branch wiring such as the branch wirings **74**) branched out of the low-potential-side power supply wiring **70**.

[0212] That is, without the branch wiring extension portion **88**, it is necessary that each driver circuit **60** (such as first-stage driver circuit **601**, second-stage driver circuit **602**, third-stage driver circuit **603**, fourth-stage driver circuit **604**) be provided with a contact hole **100** so as to allow a branch wiring **74** and the low-potential-side power supply wiring **70** to be connected with each other.

[0213] On the other hand, with the branch wiring extension portion **88**, the branch wirings **74** respectively corresponding to the driver circuits **60** are electrically connected with the low-potential-side power supply wiring **70** via the branch wiring extension portion **88** provided on the low-potential-side power supply wiring **70**. With this configuration, by connecting with the low-potential-side power supply wiring **70** one branch wiring **74** corresponding to any one of the driver circuits **60** via the contact hole **100**, the branch wiring(s) **74** corresponding to the other one(s) of the driver circuits **60** is connected with the low-potential-side power supply wiring **70**. By this, the number of the contact holes **100** can be reduced.

[0214] In the example illustrated in FIG. **11**, the branch wiring **74** corresponding to the second-stage driver circuit **602** and the branch wiring **74** corresponding to the fourth-stage driver circuit **604** are electrically connected with the low-potential-side power supply wiring **70** via the contact holes **100**, respectively. Meanwhile, the branch wiring **74** corresponding to the first-stage driver circuit **601** and the branch wiring **74** corresponding to the third-stage driver circuit **603** are connected with the branch wiring extension portion **88**, thereby being connected with the low-potential-side power supply wiring **70** but not being connected therewith directly via the contact holes **100**.

[0215] With this configuration, it is possible to reduce the number of the contact holes provided under the seal **90**. Thereby, it becomes possible to further inhibit the display quality deterioration caused by the uneven cell thickness.

[0216] The TFT array substrate **20** according to the present embodiment may be so configured that the low-potential-side power supply wiring **70**, which is an outer wiring closer to the substrate edge **26**, has a ladder-like shape as illustrated in FIG. **6** or **7**.

[0217] Moreover, in addition to the aforementioned configuration, a connection conductor extension portion of the connection conductor **102** may be provided on and along the low-potential-side power supply wiring **70** (serving as a main wiring), i.e., in an upper layer on the low-potential-side power supply wiring **70**, like the branch wiring extension portion **88**.

[0218] In this configuration, the branch wirings **74** may be formed from a material identical with that of the main wiring such as the low-potential-side power supply wiring **70**, thereby making it possible to electrically connect the branch wirings **74** with the main wiring without the need of the contact holes **100**.

[0219] The invention being thus described, it will be obvious that the same way may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the invention, and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

[0220] A similar configuration may be adopted in a periphery area in which the signal wiring for a signal (source) driver circuit is provided, even though the above explanation discusses an example in which the configuration is applied to the periphery area in which the scanning wiring for a signal (gate) driver circuit is provided.

[0221] Furthermore, the above explanation discusses an exemplary configuration in which the void parts **76** are provided to the low-potential-side power supply wiring **70**. Where to provide the void parts **76** is not limited to the low-potential-side power supply wiring **70**, and the clock wiring **72** may have void parts **76**, for example. Moreover, apart from the wirings extended in the Y direction, a wiring extended in the X direction, such as the branch wiring **74**, may have such void parts **76**.

[0222] While the above explanation discusses an exemplary configuration in which the clock wiring **72** has the narrowed parts **84**. Where to provide the narrowed portion **84** is not limited to the clock wiring **72**. Apart from the wirings extended in the Y direction, a wiring extended in the X direction, such as the branch wiring **74**, may have such narrowed parts **84**.

[0223] Moreover, the above explanation discusses an exemplary configuration in which the main wirings are formed from the first metal material M1 from which the gate bus lines **42** are formed, and the branch wirings are formed from the second metal material M2 from which the source bus lines **44** are formed. The present invention is not limited to this combination of the wirings and the metal materials, and may be such that the first metal material M1 and the second metal material M2 are exchanged to form these wirings, for example.

[0224] Moreover, in the above explanation, the driver circuits are exemplified as the circuits that, in the periphery area of the insulating substrate, are connected with the main wirings via the branch wirings. The present invention is not limited to the driver circuits in terms of the circuits or element to be connected with the main wirings via the branch wirings, and may be so configured, for example, that the circuits or element to be connected with the main wirings via the branch wirings are peripheral TFT elements provided in the periphery area in order to drive the TFT elements provided in the display area.

[0225] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring is formed from the first metal material; the branch wirings is formed from the second metal material; and at least one of the connection parts is such that a whole of the branch-wiring via hole overlaps with the main wiring in a plane view.

[0226] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with a plurality of the main wirings; and the

main wirings except one closest to a substrate edge of the insulating substrate are identical in wiring width.

[0227] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with a plurality of the main wirings; and the plurality of the main wirings are identical in wiring width.

[0228] In there configurations, and the main wirings except one closest to a substrate edge of the insulating substrate or all of the main wirings are identical in wiring width.

[0229] This makes it easier to attain uniform wiring density in the peripheral area. Therefore, it is easier to prevent the uneven cell thickness, for example, in the case where the seal is provided in the periphery area. Therefore, it is easy to prevent the display quality deterioration in the TFT array substrate with any of there configurations.

[0230] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring closest to the substrate edge of the insulating substrate is greater in wiring width than the main wirings except the one closest to the substrate edge of the insulating substrate.

[0231] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring closest to the substrate edge of the insulating substrate is a low-potential-side power supply wiring.

[0232] Moreover, a TFT array substrate according to the present invention may be so configured that the main wiring closest to the substrate edge of the insulating substrate has void parts.

[0233] Moreover, a TFT array substrate according to the present invention may be so configured that at the connection parts in a plane view, the connection conductor is provided on the main wiring or main wirings without being off the main wiring or the main wirings.

[0234] With this configuration, the connection conductor is provided only on the main wiring at the connection part in a plane view. That is, there is the main wiring under the connection conductor.

[0235] Consequently, the TFT array substrate with this configuration is such that a particular metal material layer is present under the whole connection conductor. This makes it possible to prevent the uneven cell thickness more effectively.

[0236] Moreover, a TFT array substrate according to the present invention may be so configured that the connection parts each have a main-wiring via hole through which the main wiring or corresponding one of the main wirings is exposed, which is covered with the connection conductor; the branch-wiring via hole allows the corresponding one of the branch wirings to be electrically connected with the connection conductor; and the main-wiring via hole allows the main wiring or the corresponding one of the main wirings to be electrically connected with the connection conductor.

[0237] In this configuration, the connection part has two via holes thereby allowing the main wiring and the branch wiring to be connected with each other.

[0238] Therefore, it is easy to connect the main wiring with the branch wiring surely.

[0239] Moreover, a TFT array substrate according to the present invention may be so configured that in addition to the corresponding one of the branch wirings, the branch-wiring via hole also exposes the main wiring or corresponding one of the main wirings, which is covered with the connection conductor; and

[0240] at the branch-wiring via hole, the corresponding one of the branch wirings is electrically connected with the main wiring or the corresponding one of the main wirings.

[0241] In this configuration, the connection part has only one via hole. As a result, it is possible to reduce the number of the contact holes provided to the via holes.

[0242] Furthermore, it become easy to prevent the uneven cell thickness at the connection part.

[0243] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least either of the main wiring(s) or the branch wirings has/have void parts in which no metal material is present.

[0244] This configuration changes an effective wiring width, thereby easily providing the wiring with a desired resistance or the like.

[0245] Furthermore, in case where a light-curable resin or the like is provided to the periphery area, this configuration makes it easy to perform uniform irradiation of light to the resin. Accordingly, it becomes easy to cure the resin surely.

[0246] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with intersection parts at which the main wiring(s) respectively crosses the branch wirings without being electrically connected with the branch wirings; and at the intersection parts, at least either of the main wiring(s) or the branch wirings has/have a narrowed part at which a wiring width thereof is narrowed.

[0247] With this configuration, it is possible to reduce an area in which the main wiring and the branch wiring overlap with each other.

[0248] As a result, it becomes possible to reduce capacitance produced between the main wiring and branch wiring. Consequently, it becomes easy to prevent signal delay or the like in the wirings, thereby making it easier to improve circuit output characteristics.

[0249] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with the plural branch wirings; the branch wirings have and are electrically connected with a branch wiring extension part extended on and along the main wiring or corresponding one of the main wirings.

[0250] Moreover, a TFT array substrate according to the present invention may be so configured that the periphery area is provided with the plural branch wirings; the branch wirings have and are electrically connected with a branch wiring extension part extended on and along a first main wiring, the first main wiring being the main wiring or corresponding one of the main wirings, whereby a number of the connection parts provided on the first main wiring is less than a number of the branch wirings.

[0251] Moreover, a TFT array substrate according to the present invention may be so configured that the connection conductor has a connection conductor extension part on and along the first main wiring.

[0252] In these configurations, the main wirings and the plurality of the branch wirings are connected with each other via the branch wiring extension part or the connection conductor extension part, wherein the branch wiring extension part is a portion of the branch wirings which portion is extended along the main wiring, and the connection con-

ductor extension part is a portion of the connection part which portion is extended along the main wiring.

[0253] These configurations make it possible to reduce the number of the connection parts at which the main wiring and the branch wirings are connected with each other correspondingly. Thereby, it becomes easy to prevent the uneven cell thickness in the periphery area.

[0254] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the driver circuits are provided between the connection parts and a substrate edge of the insulating substrate.

[0255] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the periphery TFT elements are provided between the connection parts and a substrate edge of the insulating substrate.

[0256] In these configurations, at least some of the driver circuits or the periphery TFT elements are provided between the connection parts and one substrate edge of the insulating substrate.

[0257] As a result, in case where a resin such as the seal or the like is provided in a region of a certain width from the substrate edge, it becomes easy to reduce the number of the connection parts that are covered by the resin.

[0258] Consequently, it becomes easy to prevent the uneven cell thickness in the periphery area.

[0259] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the driver circuits are provided between the connection parts and a substrate edge of the insulating substrate; and between the at least some of the driver circuits and the rest of the driver circuits, a main wiring is provided and this main wiring is a clock wiring.

[0260] Moreover, a TFT array substrate according to the present invention may be so configured that in the periphery area, at least some of the periphery TFT elements are provided between the connection parts and a substrate edge of the insulating substrate; and between the at least some of the periphery TFT elements and the rest of the periphery TFT elements, a main wiring is provided and this main wiring is a clock wiring.

[0261] Moreover, a liquid crystal display panel according to the present invention is a liquid crystal display panel comprising: a TFT array substrate as mentioned above; and a counter substrate, being assembled with the TFT array substrate by a seal, the seal being provided in the periphery area.

[0262] Moreover, a liquid crystal display panel according to the present invention may be configured such that the connection parts is under the seal.

[0263] With this configuration, it becomes easy to give a uniform thickness to the seal provided in the periphery area.

[0264] This makes it possible to prevent the display quality deterioration caused by the uneven cell thickness.

[0265] Moreover, a liquid crystal display panel according to the present invention may be configured such that the connection parts is under the seal.

INDUSTRIAL APPLICABILITY

[0266] The present invention makes it possible to prevent display quality deterioration, an is suitable applicable to liquid crystal display apparatuses etc., in which high quality display is required.

REFERENCE SIGNS LIST

[0267] **10**: Liquid Crystal Display Panel
[0268] **16**: Insulating Substrate
[0269] **20**: TFT Array Substrate
[0270] **22**: Display Area
[0271] **24**: Periphery Area
[0272] **26**: Substrate Edges
[0273] **42**: Gate Bus Lines
[0274] **44**: Source Bus Lines
[0275] **48**: Pixel Electrodes
[0276] **60**: Driver Circuits
[0277] **70**: Low-Potential-Side Power Supply Wiring (Main Wiring)
[0278] **72**: Clock Wirings (Main Wiring)
[0279] **74**: Branch Wirings (Branch Wiring)
[0280] **76**: Void Parts
[0281] **80**: Connection Parts
[0282] **82**: Intersection Parts
[0283] **84**: Narrowed Parts
[0284] **88**: Branch Wiring Extension Portion
[0285] **90**: Seal
[0286] **102**: Connection Conductor
[0287] **110**: Main-wiring via holes
[0288] **112**: Branch-wiring via holes
[0289] **114**: Single Via Holes

1. A TFT array substrate, in which TFT elements and pixel electrodes being correspondingly connected with the TFT elements are arrayed in matrix on an insulating substrate, the TFT array substrate comprising:

gate bus lines on the insulating substrate, the gate bus lines being correspondingly connected with the TFT elements and being formed from a first metal material; and

source bus lines on the insulating substrate, the source bus lines being correspondingly connected with the TFT elements and being formed from a second metal material,

the pixel electrodes being made from a third metal material,

the insulating substrate having a display area in which the pixel electrodes are arrayed in matrix, and a periphery area around the display area,

the periphery area being provided with driver circuits for driving the TFT elements corresponding thereto,

the periphery area being provided with (i) branch wirings being correspondingly connected with the driver circuits, and (ii) a main wring being connected with the branch wirings,

the branch wirings being formed from one of the first metal material and the second metal material,

the main wiring being formed from the other one of the first metal material and the second metal material,

the periphery area being provided with connection parts, at which the main wiring is connected with the respective branch wirings,

at each of the connection parts, a connection conductor electrically connecting the main wiring with corresponding one of the branch wirings,

the connection conductor being formed from the third metal material,

the connection parts each having a branch-wiring via hole through which the corresponding one of the branch wirings, which is covered with the connection conductor, is exposed,

at least one of the connection parts being such that at least part of the branch-wiring via hole overlaps with the main wiring in a plane view.

* * * * *

专利名称(译)	TFT阵列基板和液晶显示面板		
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摘要(译)

本发明的一个实施例提供了一种TFT阵列基板，其中，TFT元件和像素电极被相应地与TFT元件连接的矩阵排列在绝缘基板上，在TFT阵列基板包括：从第一金属材料制成的栅极总线;由第二金属材料制成源极总线;从第三金属材料制成的像素电极;从第一金属材料制成的时钟布线;从第二金属材料制成的分支布线;并从第三金属材料制成的连接导体，连接在连接部的时钟布线和分支布线中的周边区域中的连接导体，具有通孔的分支布线，它公开其上覆盖的分支布线的连接部与连接导体，和至少部分重叠的时钟布线在平面视图。