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(54) **LIQUID CRYSTAL DISPLAY DEVICE**

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G02F 1/1368 (2006.01)

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(52) **U.S. Cl.**

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(57) **ABSTRACT**

Related U.S. Application Data

(63) Continuation of application No. 13/279,495, filed on Oct. 24, 2011, now Pat. No. 9,268,181.

Foreign Application Priority Data

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Publication Classification

(51) **Int. Cl.**

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G02F 1/1362 (2006.01)

A drain layer lead line connecting an image signal line and a terminal of an IC driver is interrupted in the middle, and the gap is bridged by bridging ITO that is formed at the same time as pixel ITO. Thus, the difference in the length of the lead lines is adjusted such that the length of the bridging ITO in the lead line connected to the terminal in the center of the IC driver is longer than the length of the bridging ITO in the lead line connected to the terminal in the end of the IC driver to reduce the difference in the wiring resistance of the lead lines due to the difference in the length of the lead lines depending on the location.

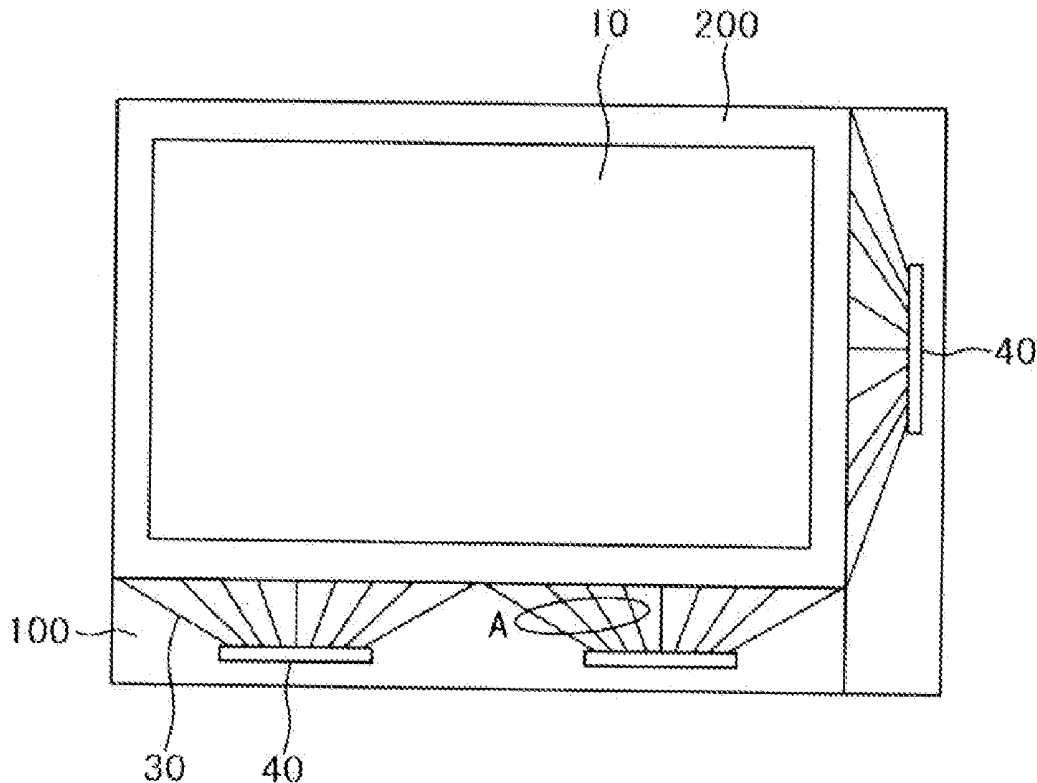


FIG. 1

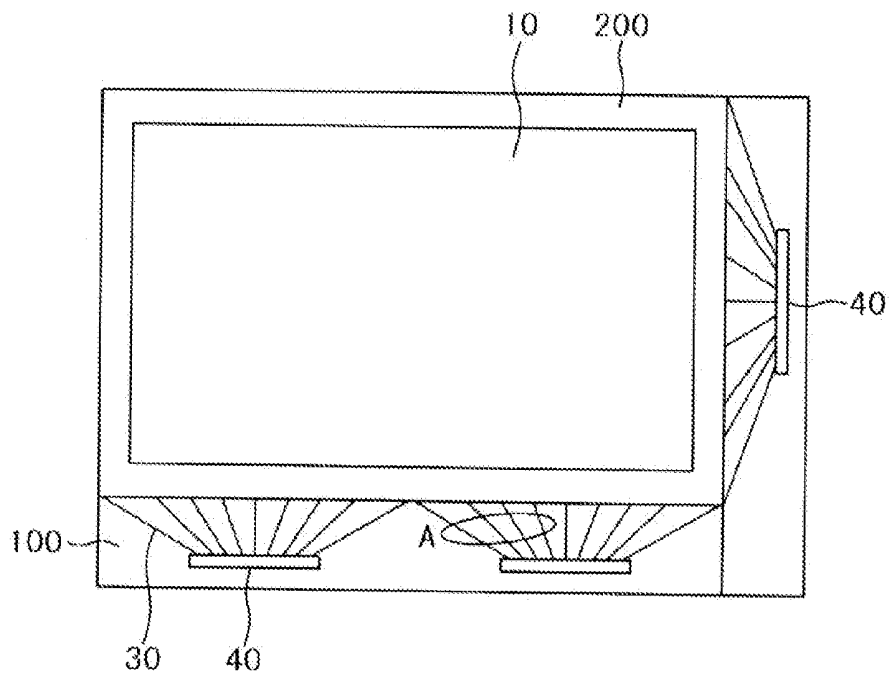


FIG. 2

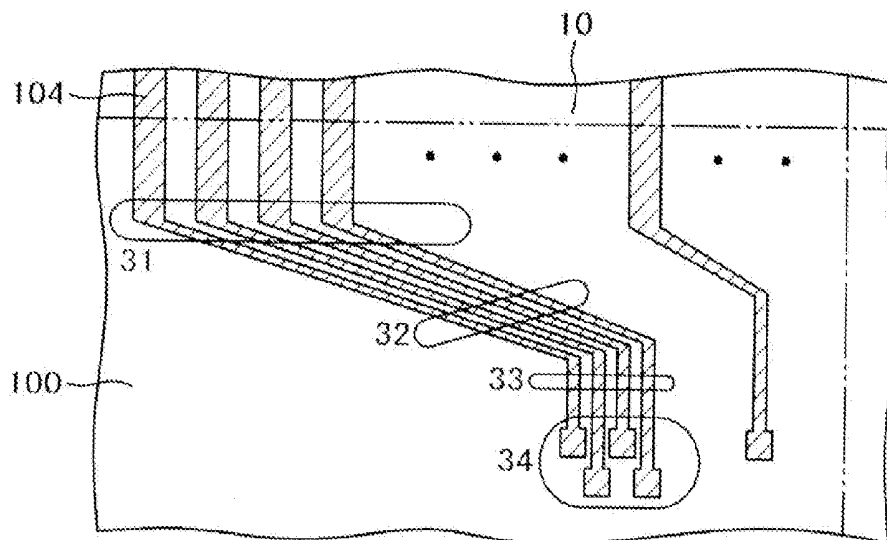


FIG. 3

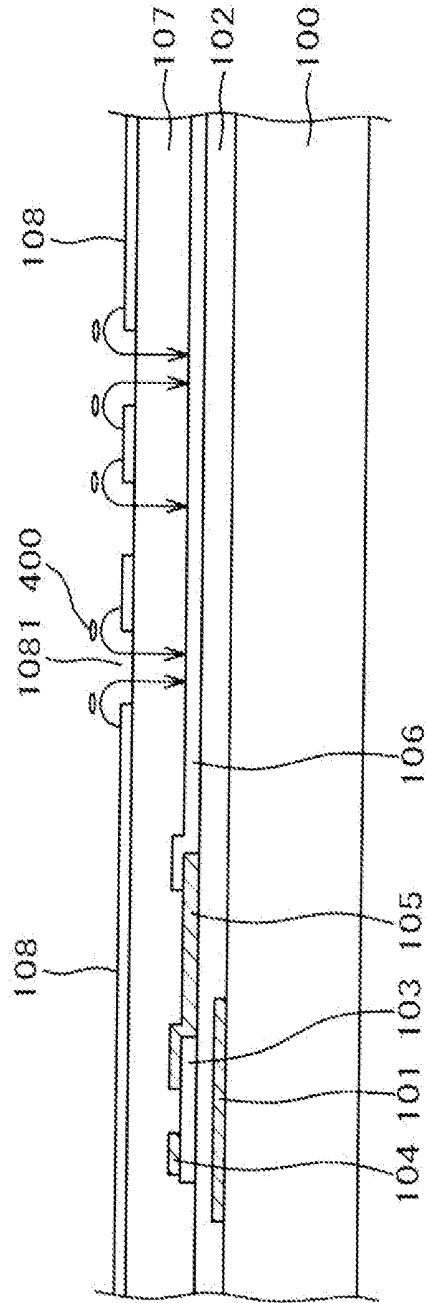


FIG. 4

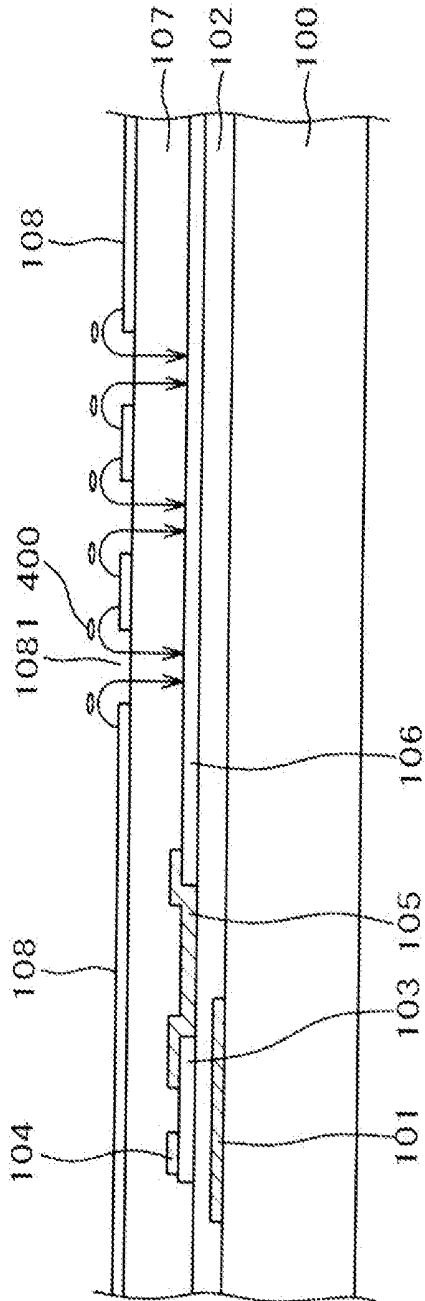


FIG. 5

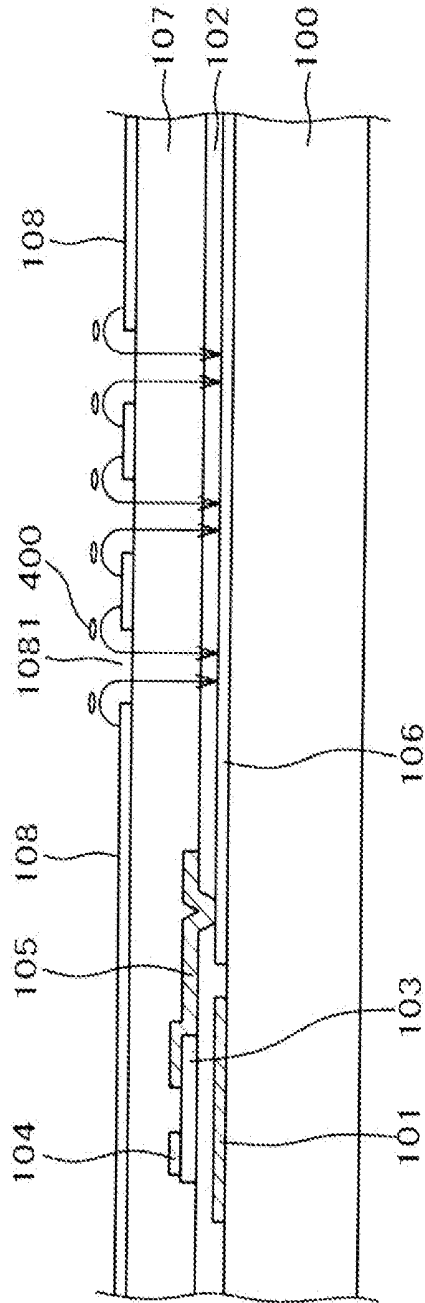


FIG. 6

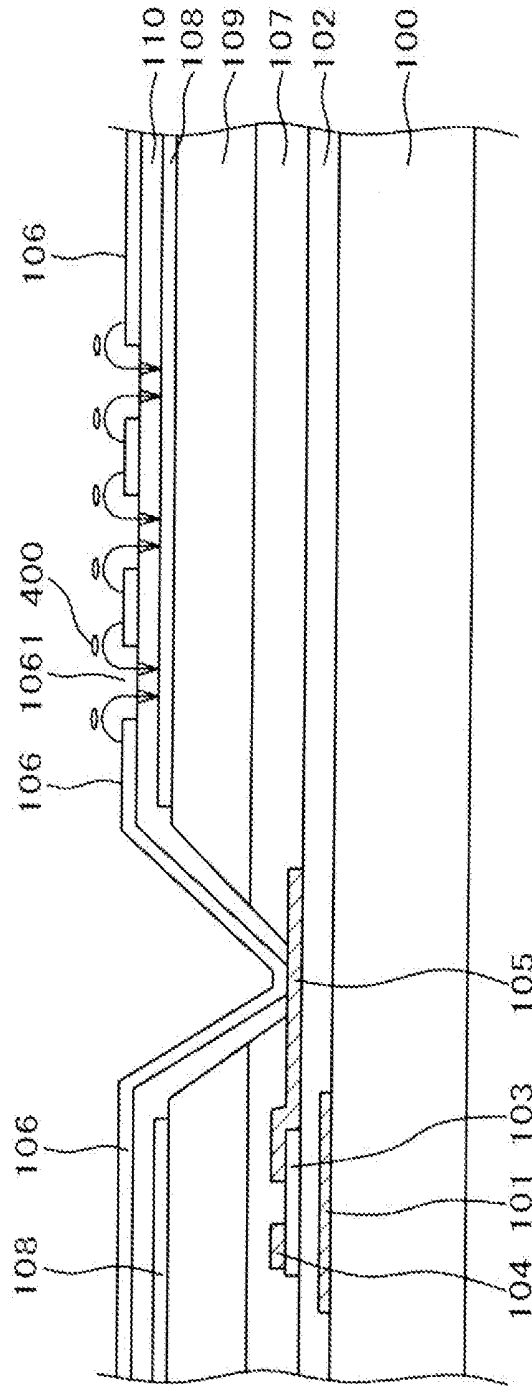


FIG. 7

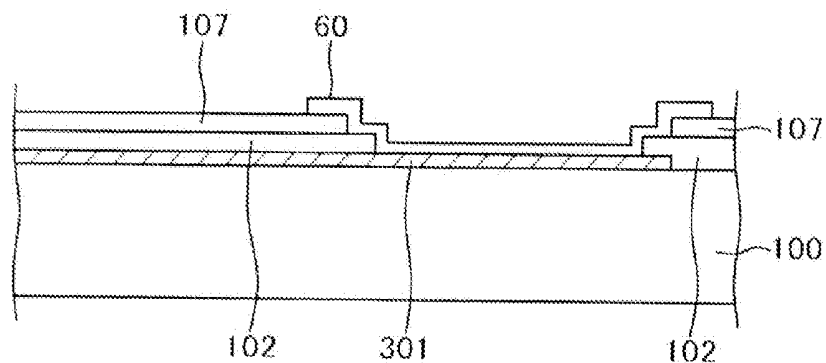


FIG. 8

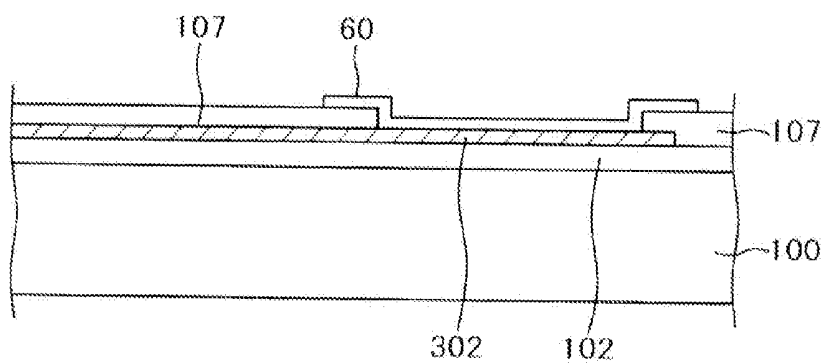


FIG. 9

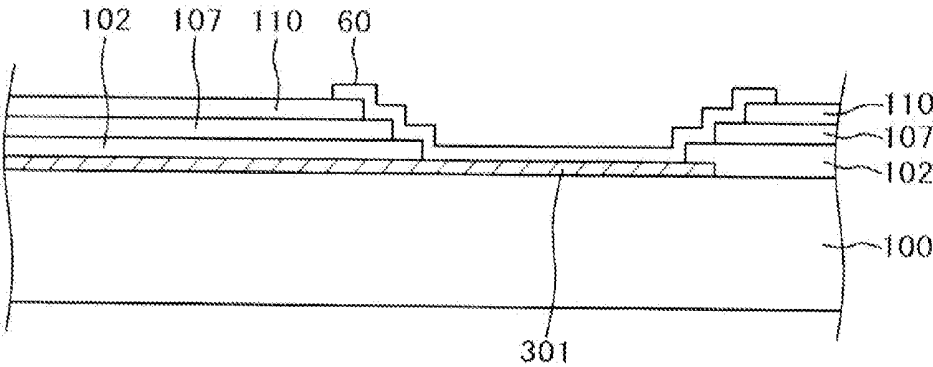


FIG. 10

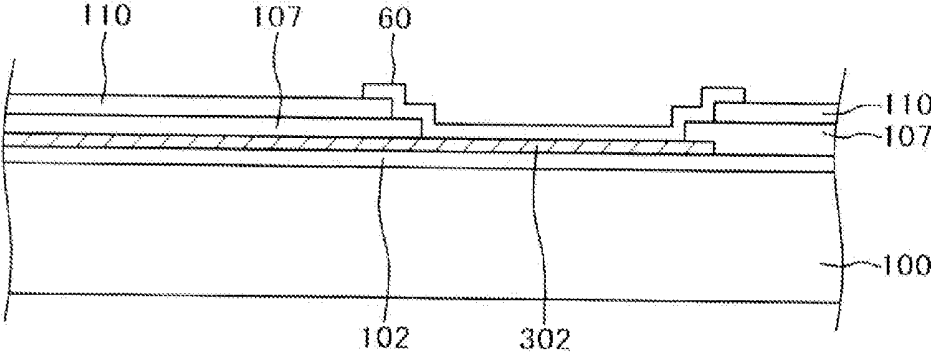


FIG. 11

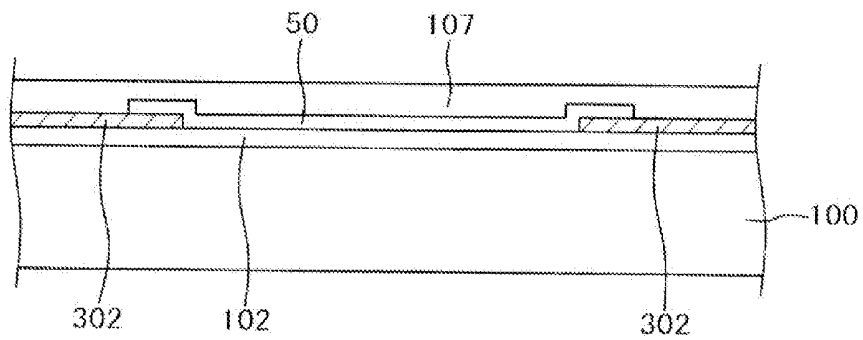


FIG. 12

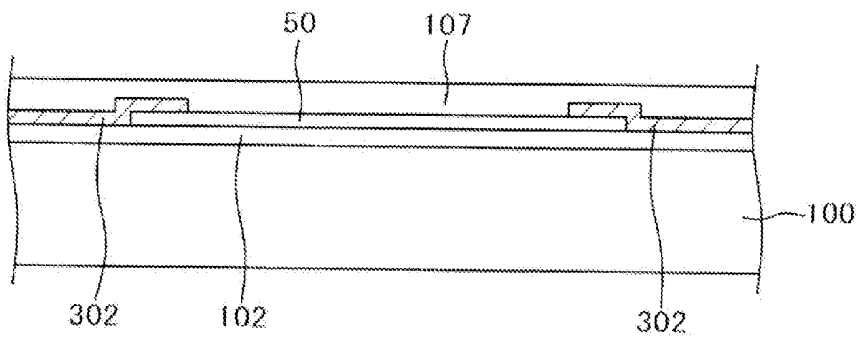


FIG. 13

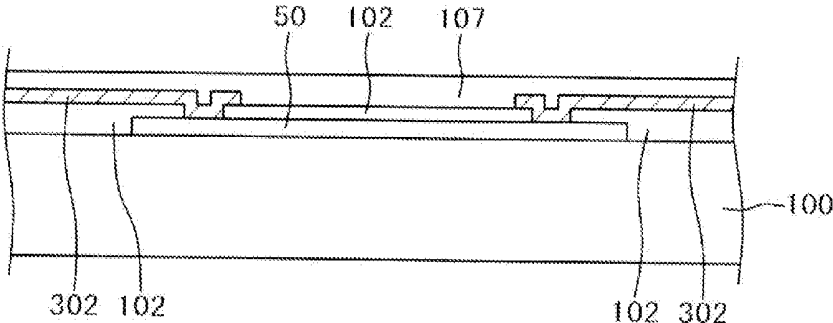


FIG. 14

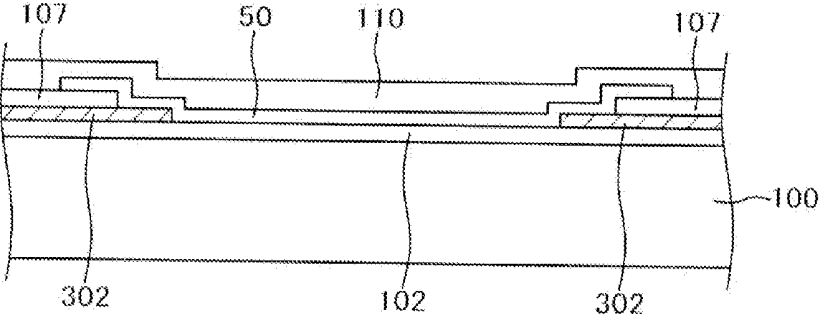


FIG. 15

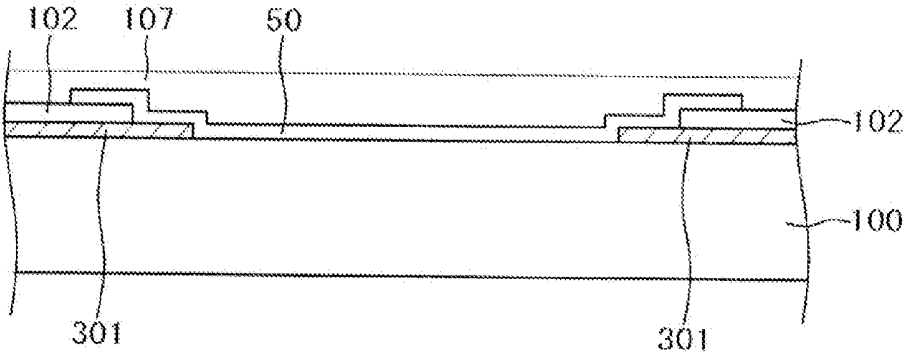


FIG. 16

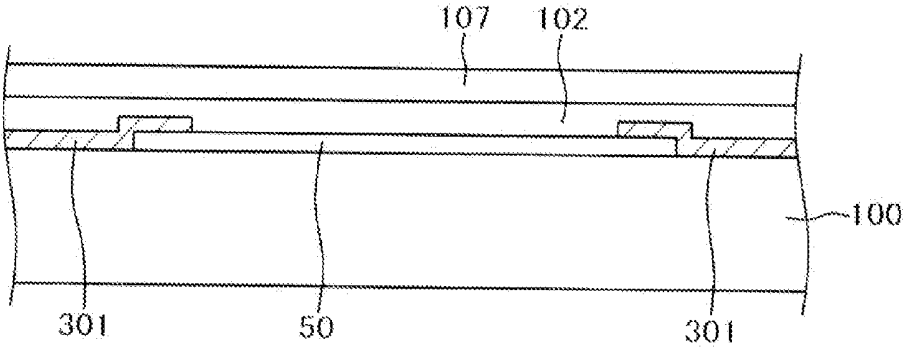


FIG. 17

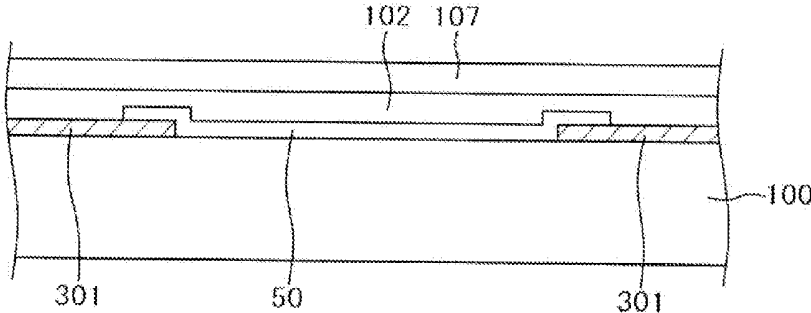


FIG. 18

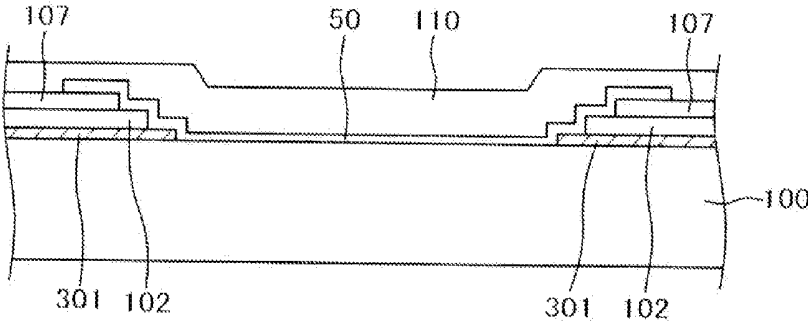


FIG. 19

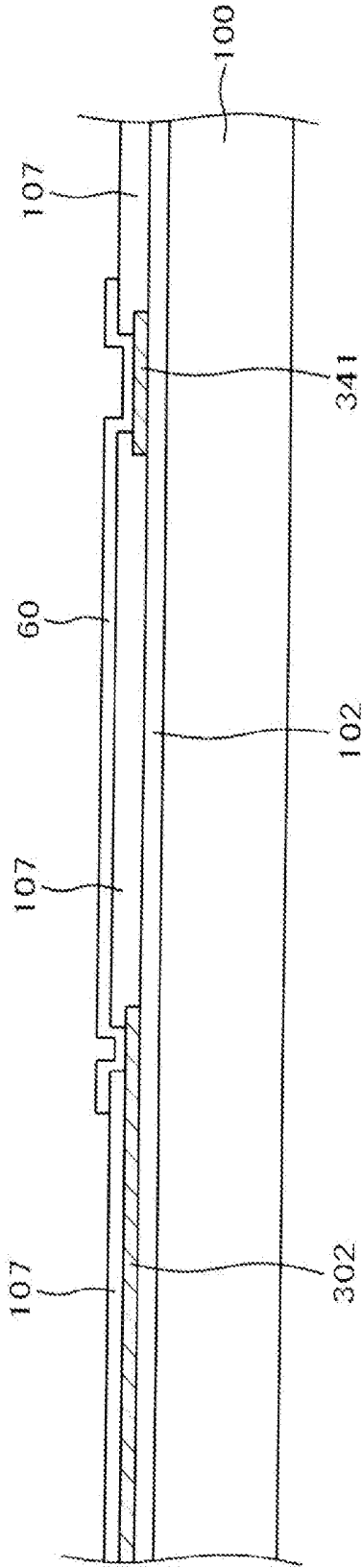


FIG. 20

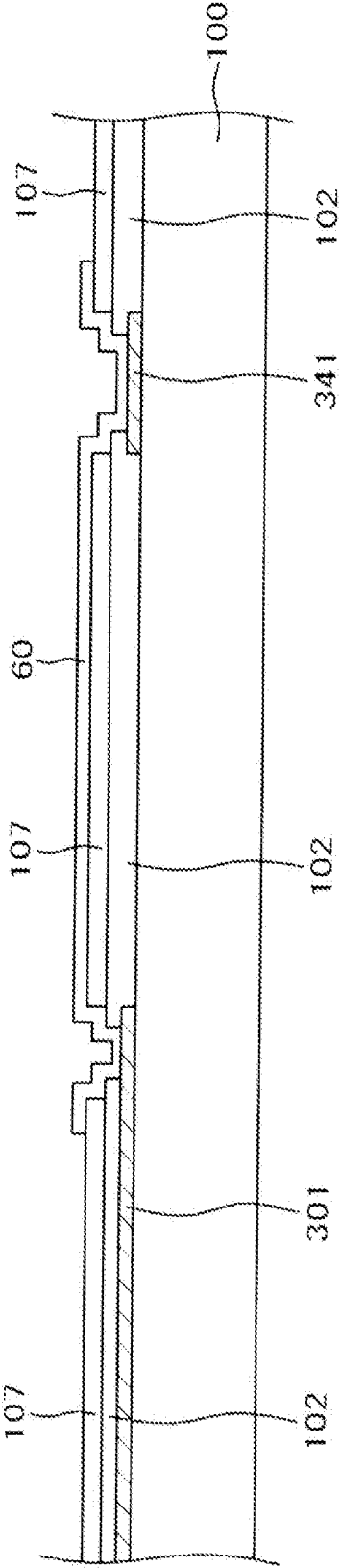


FIG. 21

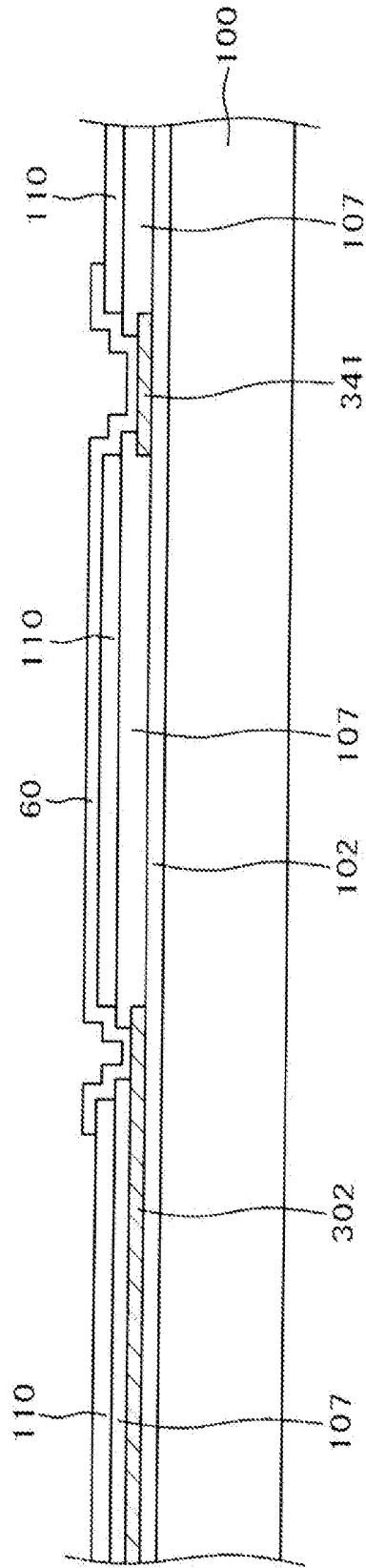


FIG. 22

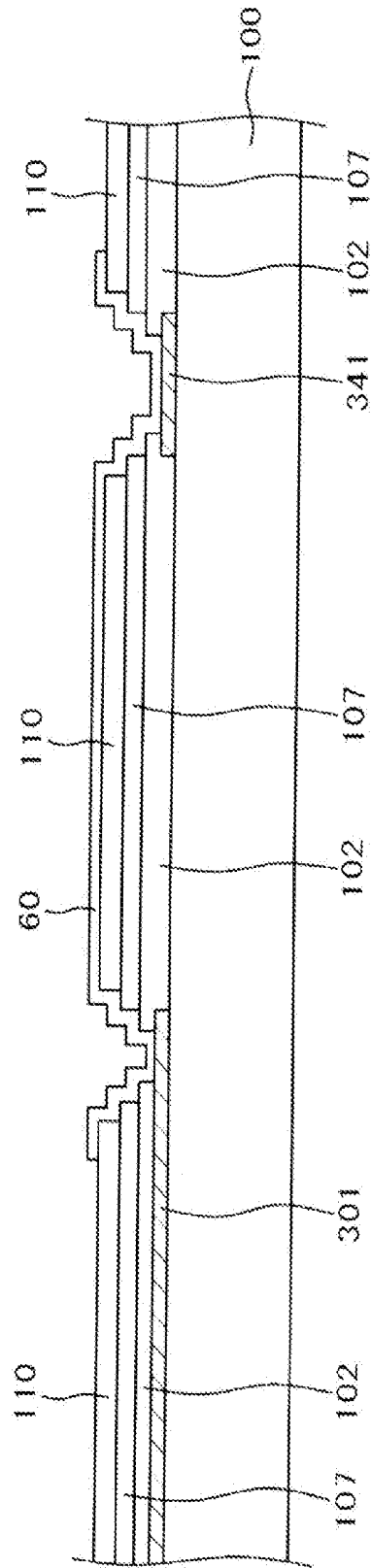


FIG. 23

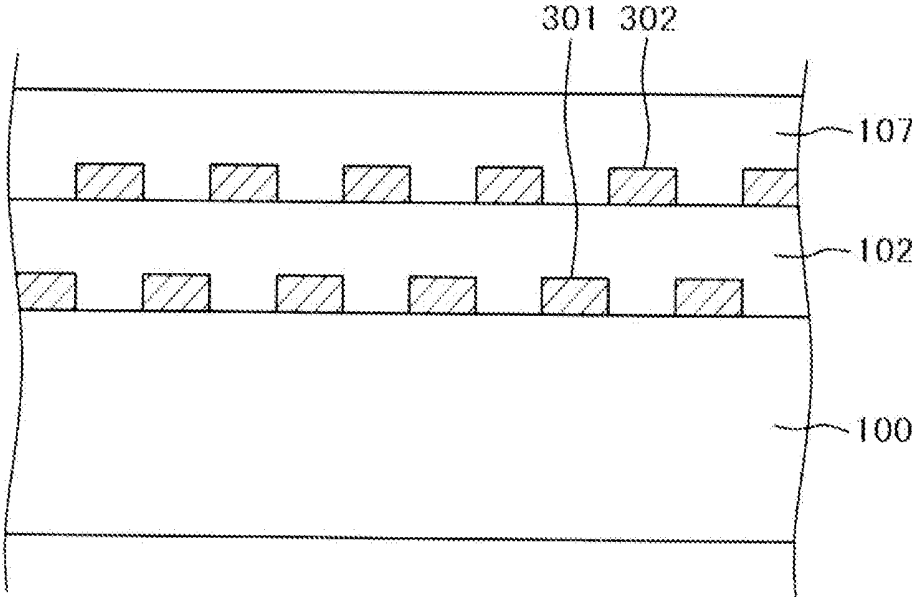


FIG. 24

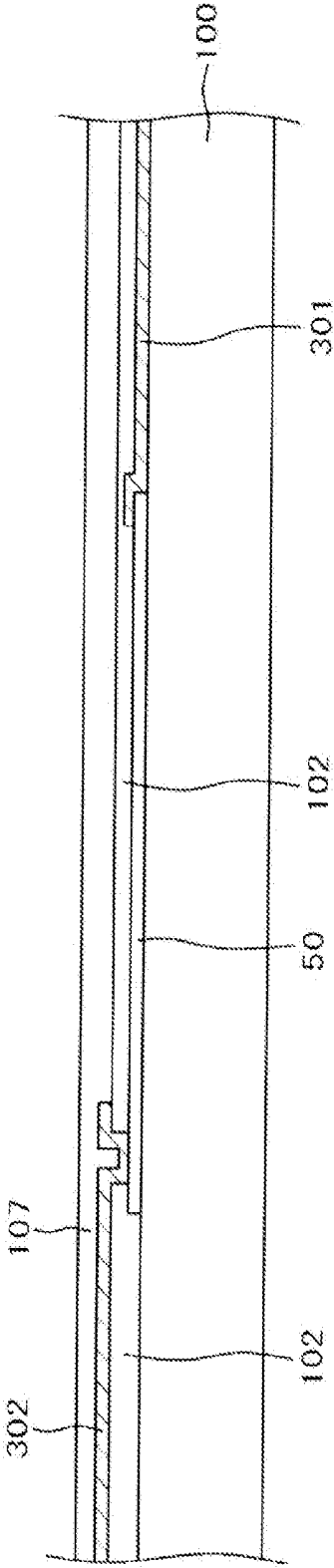


FIG. 25

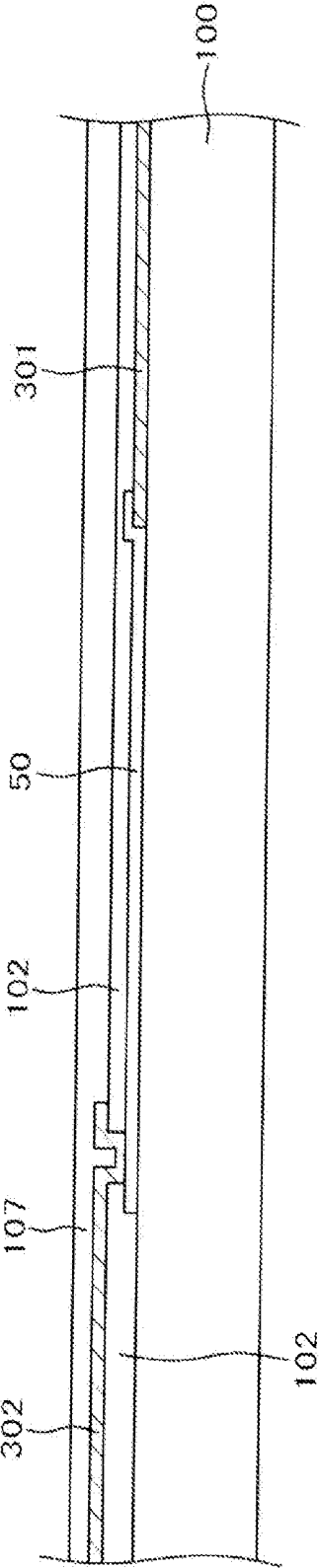


FIG. 26

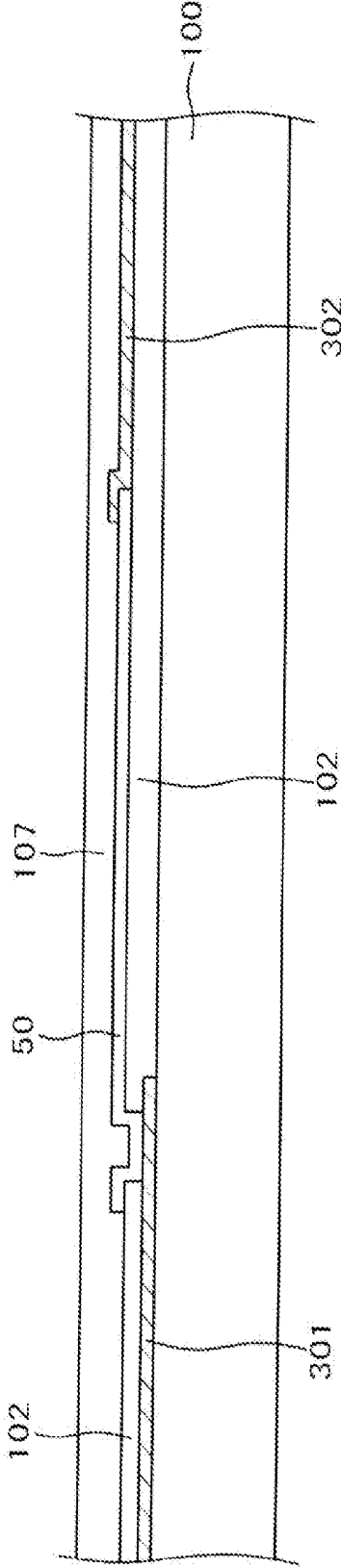


FIG. 27

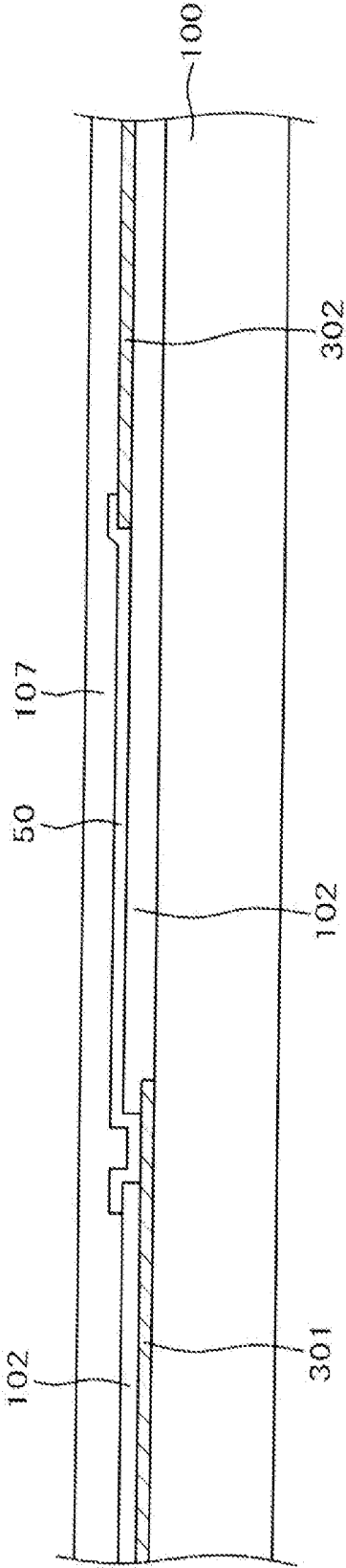
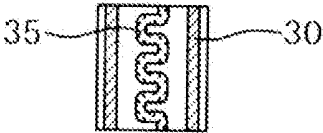


FIG. 28



LIQUID CRYSTAL DISPLAY DEVICE

CLAIM OF PRIORITY

[0001] The present application is a continuation of U.S. patent application Ser. No. 13/279,495, filed on Oct. 24, 2011, which claims priority from Japanese Patent Application JP 2010-245416 filed on Nov. 1, 2010. The entire disclosures of each of these applications are hereby incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates to a display device, and more particularly, to a liquid crystal display device designed to prevent uneven brightness due to wiring resistance.

BACKGROUND OF THE INVENTION

[0003] In a liquid crystal display panel used for a liquid crystal display device, there is provided a TFT substrate in which pixels each having a pixel electrode, a thin film transistor (TFT), and the like are arranged in a matrix form. There is also provided a counter substrate disposed opposite to the TFT substrate, in which color filters and the like are formed at positions corresponding to the pixel electrodes of the TFT substrate. Then, a liquid crystal is interposed between the TFT substrate and the counter substrate. Thus, an image is formed by controlling the transmittance of light from liquid crystal molecules for each pixel.

[0004] In the display area of the liquid crystal display device, for example, scan lines extend in the horizontal direction and are arranged at a predetermined pitch in the vertical direction. Further, image signal lines extend in the vertical direction and are arranged at a predetermined pitch in the horizontal direction. Image signals or scan signals are transmitted to the image signal lines or the scan lines from an IC driver. The terminal pitch of the IC driver is smaller than the pitch of the image signal lines or the pitch of the scan lines. Thus, the length of the lead line between the terminal of the IC driver and the image signal line or scan line is different depending on the location of the liquid crystal display panel.

[0005] Because of the difference in the length of the lead line, the electrical resistance between the terminal of the IC driver, and the image signal line or the scan line differs depending on the location. This results in the difference in the brightness depending on the location. In order to prevent this phenomenon, JP-A No. 67192/1994 describes a configuration in which each lead line has a wider area, in order to equalize the resistance of the lead lines by adjusting the range of the wider area of each lead line.

[0006] JP-A No. 16044/1996 describes a configuration for the case in which a material with a relatively high resistance such as indium tin oxide (ITO) is used for the lead lines. In this case, the influence of the lead line resistance is particularly significant, so that a metal with a relatively low resistance such as Al is used as a laminated material, in addition to the material with relatively high resistance such as ITO.

SUMMARY OF THE INVENTION

[0007] Along with the development of high definition screen in the liquid crystal display device, the terminal pitch of an IC driver becomes smaller to reduce costs of the IC driver. Thus, the pitch of lead lines also becomes smaller. As

a result, it is difficult to have enough room to increase the width of a portion of the lead line as described in JP-A No. 67192/1994.

[0008] Further, in the configuration in which a low-resistance metal is laminated on the lead line as described in JP-A No. 16044/1996, a low-resistance metal is originally used for the lead line. In this case, a further effect of equalizing the resistance of the lead line would not be expected.

[0009] Another method of equalizing the resistance of a lead line **30** is to increase the resistance of a lead line **35** to a desired value. In this case, as shown in FIG. **28**, the length of the lead line **35** is increased by snaking the lead line **35** in order to adjust the resistance. However, also in this method, it is difficult to have enough room to snake the lead line when the pitch of the lead lines becomes small.

[0010] The present invention aims to achieve a configuration in which the resistance value of lead lines can be equalized even if the pitch of the lead lines becomes small without adding additional process steps. Then, it is desirable to achieve a liquid crystal display device having uniform screen brightness.

[0011] The present invention is to solve the above problem, and a key aspect of the present invention is as follows. There is provided a liquid crystal display device including a display area in which scan lines extending in a first direction are arranged at a first pitch in a second direction, image lines extending in the second direction are arranged at a second pitch in the first direction, and pixels are arranged in a matrix form. Further, an IC driver having a rectangular shape is provided on the outside of the display area of the liquid crystal display device. The IC driver has terminals arranged at a third pitch. The third pitch is smaller than the first pitch or the second pitch. The image signal line is connected to the IC driver by a lead line. The lead line has a connecting portion connected to the image signal line, a diagonal wiring portion extending in the diagonal direction with respect to the second direction, and a straight wiring portion extending in the second direction with the third pitch and connected to the IC driver. In the straight wiring portion, the lead line is bridged by bridging ITO. The length of the bridging ITO in the lead line connected to the terminal in the center in a longitudinal direction of the rectangular IC driver is longer than the length of the bridging ITO in the lead line connected to the terminal on the outside in the longitudinal direction of the rectangular IC driver. In this way, the resistance of the lead lines is equalized. The same configuration can be applied to the lead lines connecting the scan lines and the IC driver.

[0012] As another aspect of the present invention, the wiring terminals corresponding to the IC driver are not connected to the lead lines. In this case, each wiring terminal is connected to the end of each lead line by ITO covering both the end of the lead line and the wiring terminal. At this time, the length of the ITO covering the wiring terminal corresponding to the center of the IC driver is longer than the length of the ITO covering the wiring terminal corresponding to the end of the IC driver. Thus, the resistance of the lead lines is equalized.

[0013] Further, when the lead lines have a small pitch and are arranged in a two-layer wiring structure, the layer of the image signal lines is connected to the layer of the scan lines by bridging ITO. At this time, the length of the bridging ITO in the lead line corresponding to the terminal in the center of the IC driver is longer than the length of the bridging ITO in the

lead line corresponding to the terminal in the end of the IC driver. Thus, the resistance of the lead lines is equalized.

[0014] According to the present invention, it is possible to equalize the resistance of the lead lines connecting the display area and the IC driver. This makes it possible to reduce the uneven brightness due to the wiring resistance in the display area. Further, the configuration according to the present invention can be produced in the same process as the existing production process. Thus, the production cost of the liquid crystal display device will not be increased.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a plan view of a liquid crystal display device;

[0016] FIG. 2 is a detailed plan view of a portion of the lead lines in the liquid crystal display device;

[0017] FIG. 3 is a cross-sectional view of a pixel portion in IPSLITE 1;

[0018] FIG. 4 is a cross-sectional view of a pixel portion in IPSLITE 2;

[0019] FIG. 5 is a cross-sectional view of a pixel portion in IPSLITE 3;

[0020] FIG. 6 is a cross-sectional view of a pixel portion in IPSPRO;

[0021] FIG. 7 is a cross-sectional view of a terminal portion when a gate layer lead line is extended to the terminal portion in IPSLITE 1, IPSLITE 2, and IPSLITE 3;

[0022] FIG. 8 is a cross-sectional view of a terminal portion when a drain layer lead line is extended to the terminal portion in IPSLITE 1, IPSLITE 2, and IPSLITE 3;

[0023] FIG. 9 is a cross-sectional view of a terminal portion when the gate layer lead line is extended to the terminal portion in IPSPRO;

[0024] FIG. 10 is a cross-sectional view of a terminal portion when the drain layer lead line is extended to the terminal portion in IPSPRO;

[0025] FIG. 11 is a cross-sectional view of the straight wiring portion of the drain layer lead line, in which the lead line is bridged by bridging ITO in IPSLITE 1;

[0026] FIG. 12 is a cross-sectional view of the straight wiring portion of the drain layer lead line, in which the lead line is bridged by bridging ITO in IPSLITE 2;

[0027] FIG. 13 is a cross-sectional view of the straight wiring portion of the drain layer lead line, in which the lead line is bridged by bridging ITO in IPSLITE 3;

[0028] FIG. 14 is a cross-sectional view of the straight wiring portion of the drain layer lead line, in which the lead line is bridged by bridging ITO in IPSPRO;

[0029] FIG. 15 is a cross-sectional view of the straight wiring portion of the lead line of a scan line, in which the lead line is bridged by bridging ITO in IPSLITE 1;

[0030] FIG. 16 is a cross-sectional view of the straight wiring portion of the lead line of the scan line, in which the lead line is bridged by bridging ITO in IPSLITE 2;

[0031] FIG. 17 is a cross-sectional view of the straight wiring portion of the lead line of the scan line, in which the lead line is bridged by bridging ITO in IPSLITE 3;

[0032] FIG. 18 is a cross-sectional view of the straight wiring portion of the lead line of the scan line, in which the lead line is bridged by bridging ITO in IPSPRO;

[0033] FIG. 19 is a cross-sectional view of an example in which the resistance of the drain layer lead line is adjusted by ITO in the terminal portion in IPSLITE 1, IPSLITE 2, and IPSLITE 3;

[0034] FIG. 20 is a cross-sectional view of an example in which the resistance of the gate layer lead line is adjusted by ITO in the terminal portion in IPSLITE 1, IPSLITE 2, and IPSLITE 3;

[0035] FIG. 21 is a cross-sectional view of an example in which the resistance of the drain layer lead line is adjusted by ITO in the terminal portion in IPSPRO;

[0036] FIG. 22 is a cross-sectional view of an example in which the resistance of the gate layer lead line is adjusted by ITO in the terminal portion in IPSPRO;

[0037] FIG. 23 is a cross-sectional view of an example in which the lead lines are arranged in a multi-layer wiring structure;

[0038] FIG. 24 is a cross-sectional view of an example in which the resistance of the lead line is adjusted by bridging ITO in the connecting portion in IPSLITE 3;

[0039] FIG. 25 is a cross-sectional view of another example in which the resistance of the lead line is adjusted by bridging ITO in the connecting portion in IPSLITE 3;

[0040] FIG. 26 is a cross-sectional view of an example in which the resistance of the lead line is adjusted by bridging ITO in the connecting portion in IPSLITE 2;

[0041] FIG. 27 is a cross-sectional view of an example in which the resistance of the lead line is adjusted by bridging ITO in the connecting portion in IPSLITE 1; and

[0042] FIG. 28 is an example of a method of adjusting the resistance of the lead line in a conventional example.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0043] FIG. 1 is a plan view of a liquid crystal display device to which the present invention is applied. In FIG. 1, a counter substrate 200 is provided on a TFT substrate 100 in which TFTs and pixels are formed. A liquid crystal layer not shown is interposed between the TFT substrate 100 and the counter substrate 200. A display area 10 is present where the TFT substrate 100 and the counter substrate 200 overlap each other. In the display area 10, scan lines not shown extending in the horizontal direction are arranged at a predetermined pitch in the vertical direction. Further, image signal lines not shown extending in the vertical direction are arranged at a predetermined pitch in the horizontal direction. The scan lines or image signal lines are connected to an IC driver 40 by lead lines.

[0044] The pitch of the IC driver 40 is smaller than the pitch of the image signal line or the pitch of the scan line. Thus, the ends of the scan lines or image signal lines are connected to terminals of the IC driver 40 by diagonal lines as shown in FIG. 1. In this case, the lead line connected to the end of the IC driver 40 is the longest. The closer to the center of the IC driver 40 the lead line is, the shorter the length of the lead line. Thus, the resistance from the IC driver 40 varies depending on the location of the scan line or image signal line. This difference results in the difference in the amplitude of the signal, so that the screen brightness is different depending on the location.

[0045] FIG. 2 is a detailed plan view of the shape of the lead lines, for example, which corresponds to A part of FIG. 1. In FIG. 2, the image signal lines extend from the display area 10 and are connected to the lead lines 30 in a connecting portion 31. The lead lines reach the terminal portion 34 through a diagonal wiring portion 32 and a straight wiring portion 33. The width of each wiring terminal should be larger than the width of the lead line 30. Thus, the wiring terminals are

arranged in a staggered fashion. The wiring terminals are connected to the terminals of the IC driver 40.

[0046] As shown in FIG. 2, the closer to the end of the IC driver, the longer the length of the lead line 30. Further, the line width of the diagonal wiring portion 32 is smaller than the line width of the connecting portion 31 or than the straight wiring portion 33. The lead line 30 is formed of the same material as the scan line or the image signal line. For example, the scan line is formed of an AlNb alloy, and the image signal line is formed of MoW. The present invention aims to equalize the resistance of the lead lines. In the present invention, a portion of the lead line 30 is bridged by ITO that is different from the material of the scan line or the material of the image signal line. In this way, the resistance of the lead line 30 is adjusted to make the resistance approximately equal in all the lead lines 30. This ITO will sometimes be referred to as bridging ITO.

[0047] In other words, the resistance of the ITO is 50 to 60 times higher than the resistance of AlNd or MoW, and the like. For this reason, the longer the length of the ITO the higher the resistance of the lead line 30 can be achieved. In other words, the length of the bridging ITO is increased as the lead line 30 approaches the center of the IC driver 40. There is no need to bridge the outermost lead line 30 by ITO.

[0048] Preferably, the bridging by the bridging ITO is performed in the straight wiring portion 33, the terminal portion 34, or the connecting portion 31, because the line width can be relatively large in these portions. As shown in FIG. 2, the wiring width tends to be reduced in the diagonal wiring portion 32. Thus, it is difficult to form the bridging ITO in the diagonal wiring portion 32 in terms of processing accuracy. The following embodiment describes a configuration for adjusting the resistance of the lead line 30 in the straight wiring portion 33, the terminal portion 34, and the connecting portion 31.

[0049] The method of bridging by ITO is affected by the layer structure of the liquid crystal display device. In other words, the terminal portion 34 or the lead line 30 is formed at the same as the display area 10, so that the optimal configuration is different for each structure of the display area 10. This embodiment describes the configuration of the in-plane switching (IPS) liquid crystal display device to which the present invention is applied.

[0050] In the liquid crystal display device, the viewing angle characteristics are a problem. The viewing angle is a phenomenon in which the brightness changes or the color changes between when the screen is viewed from the front, and when the screen is viewed from the diagonal direction. The viewing angle characteristics are excellent in the IPS mode in which liquid crystal molecules are driven by the electric field in the horizontal direction.

[0051] There are many different types of IPS mode. For example, a pixel electrode 106 is formed in a rectangular shape, on which a common electrode 108 having a slit 1081 is disposed with an insulating film interposed therebetween. In this way, the liquid crystal molecules are rotated by the electric field generated between the common electrode 108 and the pixel electrode 106. This method can reduce the number of layers and is becoming a mainstream IPS mode. As described below there are three types of this method, which are called IPSLITE 1, IPSLITE 2, and IPSLITE 3 in this specification. There is another method in which the common electrode 108 is formed in a planar shape, on which the pixel electrode 106 having a slit is disposed with the insulating film

interposed therebetween, so that liquid crystal molecules 400 are rotated by the electric field generated between the pixel electrode 106 and the common electrode 108. This method will be referred to as IPSPRO.

[0052] FIG. 3 is a cross-sectional view of a pixel portion in IPSLITE 1. In FIG. 3, a gate electrode 101 is formed on the TFT substrate 100. Then, a gate insulating film 102 is formed and covers the gate electrode 101. For example, the gate electrode 101 is formed of AlNd, and the gate insulating film 102 is formed of SiN. A semiconductor layer 103 is formed of, for example, a-Si on the gate electrode 101 with the gate insulating film interposed therebetween. A drain electrode 104 and a source electrode 105 are placed opposite to each other on the semiconductor layer 103. The drain electrode 104 is connected to the image signal line. For example, the drain electrode 104 and the source electrode 105 are formed of MoW.

[0053] The pixel electrode 106 connected to the source electrode 105 is formed of ITO on the gate insulating film 102. In the case of IPSLITE 1 shown in FIG. 3, the source electrode 105 is formed prior to the formation of the pixel electrode 106, so that the pixel electrode 106 overlaps a portion of the source electrode 105 to establish connection between the pixel electrode 106 and the source electrode 105. An inorganic passivation film 107 is formed of SiN, covering the TFT and the pixel electrode 106. The common electrode 108 having the slit 1081 is formed in a planar shape on the passivation film 107. When an image signal is applied to the pixel electrode 106, electric field lines are generated between the common electrodes 108 through the slit 1081. The liquid crystal molecules 400 are rotated by the electric field lines to control the transmittance of light from a backlight for each pixel, and thus an image is formed. Note that, as shown in FIG. 3, the pixel includes the TFT, the pixel electrode, and the common electrode, but also the transmission part for controlling the light from the backlight. The configuration is the same as in FIG. 4 (IPSLITE 2), FIG. 5 (IPSLITE 3), and FIG. 6 (IPSPRO), all of which will be described below.

[0054] FIG. 4 is a cross-sectional view of a pixel portion in IPSLITE 2. FIG. 4 is different from FIG. 3 in that the pixel electrode 106 of ITO is formed prior to the formation of the source electrode 105 on the gate insulating film 102. Thus, in FIG. 4, the source electrode 105 overlaps a portion of the pixel electrode 106 to establish connection between the source electrode 105 and the pixel electrode 106. This configuration can solve the problem that when the ITO, which is the pixel electrode 106, is developed by a developer, the image signal line, the drain electrode 104, the source electrode 105, and the like are corroded by the developer. The other configuration is the same as the configuration in FIG. 3 and the description thereof will be omitted.

[0055] FIG. 5 is a cross-sectional view of a pixel portion in IPSLITE 3. In FIG. 5, the gate electrode 101 is formed on the TFT substrate 100. Further, the pixel electrode 106 of ITO is formed separately from the gate electrode 101 on the TFT substrate 100. The gate insulating film 102 is formed and covers both the gate electrode 101 and the pixel electrode 106. The semiconductor layer 103 is formed on the gate electrode 101 through the gate insulating film 102. The drain electrode 104 and the source electrode 105 are formed opposite to each other on the semiconductor layer 103.

[0056] A through hole is formed on the gate insulating film 102 to provide connection between the pixel electrode 106 and the source electrode 105. The inorganic passivation film

107 is formed and covers the TFT. The common electrode **108** having the slit **1081** is formed on the inorganic passivation film **107**. When an image signal is supplied to the pixel electrode **106**, electric field lines are generated through the slit **1081**. The liquid crystal molecules **400** are controlled by the electric field lines. This is the same as in IPSLITE 1 and IPSLITE 2.

[0057] FIG. 6 is a cross-sectional view of a pixel portion in IPSPRO. In IPSPRO, the pixel electrode **106** having the slit **1061** is provided on the top layer. The common electrode **108** formed in a planar shape is provided below the pixel electrode **106** with an inter-layer insulating film **110** interposed therebetween. When electric field lines are generated between the pixel electrode **106** and the common electrode **108**, the liquid crystal molecules **400** are rotated by the electric field lines to control the light transmitted through the liquid crystal layer.

[0058] In FIG. 6, the gate electrode **101** is formed on the TFT substrate **100**. The gate insulating film **102** is formed and covers the gate electrode **101**. The semiconductor layer **103** is formed through the gate insulating film **102** on the gate electrode **101**. Then, the drain electrode **104** and the source electrode **105** are formed on the semiconductor layer **103**. This is the same as in IPSLITE 1 or other modes. The inorganic passivation film **107** is formed and covers the TFT. Then, an organic passivation film **109**, which is also served as a flatterer film, is formed on the inorganic passivation film **107**. The common electrode **108** is formed in a planar shape on the organic passivation film **109**. The inter-layer insulating film **110** is formed and covers the common electrode **108**. Then, the pixel electrode **106** having the slit **1081** is formed on the inter-layer insulating film **110**. A through hole is formed in the organic passivation film **109**, the inorganic passivation film **107**, and the inter-layer insulating film **110**, to ensure electrical continuity between the source electrode **105** of the TFT and the pixel electrode **106**. The configuration of IPSPRO is different from the configuration of IPSLITE 1 or other modes in that the pixel electrode **106** is provided above the common electrode **108**.

[0059] In FIG. 2, the lead lines **30** extend below the terminals in the terminal portion **34**. The lead line **30** extending to the terminal may be formed of the same material as the drain electrode **104**, or may be formed of the same material as the gate electrode **101**. Hereinafter, if the material of the lead line **30** is the same as the drain electrode **104**, it is called a drain layer lead line **302**, and if the material of the lead line **30** is the same as the gate electrode **101**, then it is called a gate layer lead line **301**. The drain electrode **104** and the source electrode **105** or the image signal line are formed of the same material at the same time. Further, the gate electrode **101** and the scan line are formed of the same material at the same time.

[0060] FIG. 7 is an example in which the gate layer lead line **301** extends to the terminal in IPSLITE 1, IPSLITE 2, and IPSLITE 3. The gate layer lead line **301** is formed at the same time as the gate electrode **101**, and the like. Because the AlNd used for the gate layer lead line **301** is corroded by contact with air, the gate layer lead line **301** is covered by the gate insulating film **102** and the inorganic passivation film **107**, except for the portion that is connected to the terminal of the IC driver **40** to form a through hole. In order to prevent the AlNd from being corroded in the through hole, the portion of the through hole is covered by ITO. This ITO is formed at the same time as the common electrode **108** in IPSLITE 1 or other modes. In other words, the ITO is formed at the same time as

the formation of the ITO on the upper side in FIGS. 3, 4, and 5. Hereinafter, the ITO used in the terminal portion **34** is referred to as the upper ITO.

[0061] FIG. 8 is an example in which the drain layer lead line **302** extends to the terminal in IPSLITE 1, IPSLITE 2, and IPSLITE 3. The drain layer lead line **302** on the gate insulating film **102** is formed at the same time as the drain electrode **104** and the like. Because the MoW used for the drain layer lead line **302** is corroded by contact with air, the drain layer lead line **302** is covered by the inorganic passivation film **107**, except for the portion that is connected to the terminal of the IC driver **40** to form a through hole. In order to prevent the MoW from being corroded in the through hole, the portion of the through hole is covered by the upper ITO **60**.

[0062] FIG. 9 is an example in which the gate layer lead line **301** extends to the terminal in IPSPRO. The gate layer lead line **301** is formed at the same time as the gate electrode **101** and the like. FIG. 9 is different from FIG. 7 in that the inter-layer insulating film **110** is formed on the inorganic passivation film **107** and that the through hole of the terminal portion **34** is formed through the inter-layer insulating film **110**, the inorganic passivation film **107**, and the gate insulating film **102**. Also in FIG. 9, the top layer of the terminal portion **34** is covered by the upper ITO **60**. The other configuration is the same as the configuration described with reference to FIG. 7.

[0063] FIG. 10 is an example in which the drain layer lead line **302** extends to the terminal in IPSPRO. The drain layer lead line **302** is formed on the gate insulating film **102** at the same time as the drain electrode **104** and the like. FIG. 10 is different from FIG. 8 in that the inter-layer insulating film **110** is formed on the inorganic passivation film **107** and that the through hole of the terminal portion **34** is formed through the inter-layer insulating film **110**, the inorganic passivation film **107**, and the gate insulating film **102**. Also in FIG. 10, the top layer of the terminal portion **34** is covered by the upper ITO **60**. The other configuration is the same as the configuration described with reference to FIG. 8.

[0064] With respect to the configurations of the pixel portion and the terminal portion **34** in IPSLITE 1, IPSLITE 2, IPSLITE 3, and IPSPRO, the adjustment of the resistance of the lead line **30** according to the present invention will be described with reference to the following examples.

First Example

[0065] FIG. 11 is a cross-sectional view of the configuration for resistance adjustment in the straight wiring portion **33** in IPSLITE 1. In FIG. 11, the drain layer lead line **302** is used for the lead line **30**. In FIG. 11, the drain layer lead line **302** is interrupted in the middle of the straight wiring portion **33**, and the gap is connected with the bridging ITO. The bridging ITO is formed at the same time as the pixel electrode **106**, namely, a lower ITO **50**. In IPSLITE 1, the source electrode **105** is formed prior to the formation of the pixel electrode **106**. Thus, in FIG. 11, the lower ITO **50** overlaps a portion of the drain layer lead line **302** to establish connection between them.

[0066] As described above, in this example, it is possible to adjust the resistance of the lead line **30** by the lower ITO **50**, without using the through hole and the like. The resistance of the lead line **30** can be adjusted by the length of the lower ITO **50**. Here, the number of process steps is not increased compared to the case of not using the resistance adjustment configuration. As described above, according to this example, the

resistance of the lead line 30 can be adjusted without leading to an increase in the process cost or complexity in IPSLITE 1.

Second Example

[0067] FIG. 12 is a cross-sectional view of the configuration for resistance adjustment in the straight wiring portion 33 in IPSLITE 2. In FIG. 12, the drain layer lead line 302 is used for the lead line 30. FIG. 12 is different from FIG. 11 in that the pixel electrode 106, namely, the lower ITO 50 is formed prior to the formation of the source electrode 105 in IPSLITE 2. Thus, the drain layer lead line 302 in FIG. 12 overlaps a portion of the lower ITO 50 to ensure electrical continuity between the two electrodes. The other configuration and effect are the same as those in the first example.

Third Example

[0068] FIG. 13 is a cross-sectional view of the configuration for resistance adjustment in the straight wiring portion 33 in IPSLITE 3. In FIG. 13, the drain layer lead line 302 is used for the lead line 30. In FIG. 13, the pixel electrode 106, namely, the lower ITO 50 is used as the bridging ITO for the resistance adjustment. The resistance of the lead line 30 can be adjusted by the length of the lower ITO 50.

[0069] FIG. 13 is different from FIGS. 11 and 12 in that the lower ITO 50 is directly formed on the TFT substrate 100. Thus, a through hole is formed in the gate insulating film 102 to establish connection between the drain layer lead line 302 and the lower ITO 50 for the resistance adjustment. Of course, the lower ITO 50 below the gate insulating film 102 should be patterned and formed before the gate insulating film 102 is attached thereto. However, the patterning of the lower ITO 50 is performed at the same time as the patterning of the pixel electrode 106, so that the number of process steps is not increased. The configuration and effect are the same as those in the first and second examples.

Fourth Example

[0070] FIG. 14 is a cross-sectional view of the configuration for resistance adjustment in the straight wiring portion 33 in IPSPRO. In FIG. 14, the drain layer lead line 302 is used for the lead line 30. In FIG. 14, the drain layer lead line 302 is interrupted in the middle of the straight wiring portion 33, and the gap is connected with the bridging ITO. FIG. 14 is different from FIGS. 11 to 13 in that the bridging ITO connecting the gap is the common electrode 108 shown in FIG. 6. The bridging ITO is the common electrode 108, but is also referred to as the lower ITO 50 because it is formed on the lower layer.

[0071] FIG. 14 is different from FIGS. 11 to 13 in that the drain layer lead line 302 is covered by the inorganic passivation film 107 and the inter-layer insulating film 110. Further, the common electrode 108 in FIG. 6, namely, the lower ITO 50 in FIG. 14 is formed prior to the formation of the inorganic passivation film 107. Thus, the lower ITO 50 overlaps the end of the inorganic passivation film 107. In FIG. 14, the resistance of the lead line 30 can be adjusted by the length of the lower ITO 50. The effect of FIG. 14 is the same as the effect in the first example or other examples.

Fifth Example

[0072] FIG. 15 is a cross-sectional view of the configuration for resistance adjustment in the straight wiring portion 33 for the case of using the gate layer lead line 301 in IPSLITE

1 or IPSLITE 2. In other words, when the gate layer lead line 301 is used, IPSLITE 1 and IPSLITE 2 have the same configuration. In FIG. 15, the gate layer lead line 301 is interrupted in the middle of the straight wiring portion 33, and the gap is connected with the bridging ITO. The bridging ITO is the lower ITO 50 which is formed at the same time as the pixel electrode 106 in FIG. 3 or FIG. 4. In FIG. 15, the through hole is formed in the gate insulating film 102 to bridge the gate layer lead line 301 by the lower ITO 50. The lower ITO 50 is formed at the same time as the pixel electrode 106. Thus, the lower ITO overlaps a portion of the gate insulating film 102. The lower ITO 50 is covered by the inorganic passivation film 107. Also in this example, the resistance of the lead line 30 can be adjusted by the length of the lower ITO 50.

[0073] In this example, the configuration for resistance adjustment of the lead line 30 can be formed at the same time as the pixel portion or the terminal portion 34 is formed. Thus, the number of process steps is not increased. As a result, according to this example, it is possible to provide the resistance adjustment of the lead line 30 without leading to an increase in the process cost.

Sixth Example

[0074] FIG. 16 is a cross-sectional view of the configuration for resistance adjustment in the straight wiring portion 33 in the case of using the gate layer lead line 301 in IPSLITE 3. In IPSLITE 3, the pixel electrode 106, namely, the lower ITO 50, and the gate electrode 101, namely, the gate layer lead line 301 are formed in the same layer. Thus, the resistance adjustment can be achieved by the bridging ITO without using the through hole. The resistance of the lead line 30 can be adjusted by the length of the lower ITO 50. In FIG. 16, first the lower ITO 50 is formed, and then the gate layer lead line 301 is formed. Thus, the gate layer lead line 301 overlaps a portion of the lower ITO 50 to ensure electrical continuity between the two electrodes.

[0075] In this example, there is no need to form the through hole for the resistance adjustment of the lead line 30. Thus, this example has the advantage that the configuration can be made simpler than the configuration of the fifth example. According to this example, the resistance of the lead line 30 can be adjusted without leading to an increase in process cost.

Seventh Example

[0076] FIG. 17 is a cross-sectional view of another configuration for resistance adjustment in the straight wiring portion 33 for the case of using the gate layer lead line 301 in IPSLITE 3. FIG. 17 is different from FIG. 16 in that the source electrode 105 or the gate layer lead line 301 is formed prior to the formation of the pixel electrode 106 or the lower ITO 50. Thus, the lower ITO 50 overlaps a portion of the gate layer lead line 301 to establish connection between the lower ITO 50 and the gate layer lead line 301. The effect of this example is the same as the effect of the sixth example.

Eighth Example

[0077] FIG. 18 is a cross-sectional view of yet another configuration for resistance adjustment in the straight wiring portion 33 for the case of using the gate layer lead line 301 in IPSPRO. FIG. 18 is different from the fifth example shown in FIG. 15 in that the inorganic passivation film 107 and the inter-layer insulating film 110 are present on the gate insulating film 102. Then, the gate layer lead line 301 is bridged by

the bridging ITO, which is the lower ITO 50 that is formed at the same time as the common electrode 108 in FIG. 6. In FIG. 15 described above, the bridging ITO for the resistance adjustment is formed at the same time as the pixel electrode 106, but is still the lower ITO 50. The resistance of the lead line 30 is adjusted by the length of the lower ITO 50.

[0078] In FIG. 6, the common electrode 108 is formed on the organic passivation film 109. However, the inorganic passivation film 109 is removed from the portion of the lead line 30. Thus, in FIG. 18, the lower ITO 50 is formed on the inorganic passivation film 107 in which the through hole is formed. Also in this example, the configuration for the resistance adjustment can be formed at the same time as the pixel portion or the terminal portion 34. Thus, the resistance adjustment of the lead line 30 can be achieved without an increase in process cost.

Ninth Example

[0079] FIG. 19 is a cross-sectional view of the configuration for adjusting the resistance of the lead line 30 in the terminal portion 34 shown in FIG. 2, with respect to the liquid crystal display device of IPSLITE 1, IPSLITE 2, and IPSLITE 3. FIG. 19 is an example of using the drain layer lead line 302. In FIG. 19, the gate insulating film 102 is formed on the TFT substrate 100, on which the drain layer lead line 302 extends from the display area 10 on the left side. The drain layer lead line 302 does not extend to the terminal and is interrupted in the middle. The gap between the drain layer lead line 302 and the terminal portion 34 is bridged by the upper ITO 60 that is formed at the same time as the common electrode 108.

[0080] In the terminal of FIG. 19, there is a terminal metal 341 formed at the same time as the source electrode 105 or the drain layer lead line 302 on the gate insulating film 102. The upper ITO 60 covers the terminal metal 341 to form the terminal. The resistance of the lead line 30 can be adjusted by the length of the upper ITO 60. Also in the configuration of this example, the resistance adjustment of the lead line 30 can be achieved without an increase in the number of existing process steps.

Tenth Example

[0081] FIG. 20 is a cross-sectional view of the configuration for adjusting the resistance of the lead line 30 in the terminal portion 34 shown in FIG. 2, with respect to the liquid crystal display device of IPSLITE 1, IPSLITE 2, and IPSLITE 3. FIG. 20 is an example in which the gate layer lead line 301 is used for the lead line 30. In FIG. 20, the gate layer lead line 301 and the terminal metal 341 are formed at the same time as the gate electrode 101 on the TFT substrate 100. The gate layer lead line 301 does not extend to the terminal. The gap between the gate layer lead line 301 and the terminal is bridged by the upper ITO 60 that is formed at the same time as the common electrode 108. The resistance of the lead line 30 can be adjusted by the length of the upper ITO 60. Also in this example, the resistance of the lead line 30 can be adjusted in the same process as the existing process.

Eleventh Example

[0082] FIG. 21 is a cross-sectional view of the configuration for adjusting the resistance of the lead line 30 in the terminal portion 34 shown in FIG. 2, with respect to the liquid crystal display device of IPSPRO. FIG. 21 is an example of

using the drain layer lead line 302. FIG. 21 is different from FIG. 19 in that the inter-layer insulating film 110 is present on the inorganic passivation film 107 and that the upper ITO 60, which is formed at the same time as the pixel electrode 106 in FIG. 6, overlaps a portion of the inter-layer insulating film 110. Also in this example, the resistance of the lead line 30 can be adjusted by the length of the upper ITO 60. The other effect is the same as the effect in FIG. 19.

Twelfth Example

[0083] FIG. 22 is a cross-sectional view of the configuration for adjusting the resistance of the lead line 30 in the terminal portion 34 shown in FIG. 2, with respect to the liquid crystal display device of IPSPRO. FIG. 22 is an example in which the gate layer lead line 301 is used for the lead line 30. In FIG. 22, the gate layer lead line 301 and the terminal metal 341 are formed at the same time as the gate electrode 101 on the TFT substrate 100. FIG. 22 is different from FIG. 20 in that the through hole for connecting the gate layer lead line 301 to the terminal is formed with respect to the three layers: the gate insulating film 102, the inorganic passivation film 107, and the inter-layer insulating film 110. Further, the upper ITO 60 for bridging the gap between the gate layer lead line 301 and the terminal is formed at the same time as the pixel electrode 106 shown in FIG. 6. Thus, the upper ITO 60 overlaps a portion of the inter-layer insulating film 110. The resistance of the lead line 30 can be adjusted by the length of the upper ITO 60. The other effect is the same as the effect of the eleventh example.

Thirteenth Example

[0084] When the screen is high definition, the pitch of the image signal lines and the scan lines in the display area 10 is reduced. When the pitch is reduced, it is difficult to have enough space between lines on the side of the lead line 30. In order to solve this problem, the lead lines 30 are arranged in a multi-layer wiring structure as shown in FIG. 23. In other words, for example, in the connecting portion 31 of the image signal lines and the lead lines 30 in FIG. 2, the lead lines 30 are arranged alternately on the layer of the drain layer lead line 302 and on the layer of the gate layer lead line 301. In this way, the lead lines 30 are formed in such a manner that the gate layer lead lines 301 and the drain layer lead lines 302 are arranged alternately.

[0085] FIG. 23 shows the state of the arrangement described above. FIG. 23 is a cross-sectional view in the arrangement direction of the lead lines 30. In FIG. 23, the gate layer lead lines 301 are formed on the TFT substrate 100. On the gate insulating film 102 covering the gate layer lead lines 301, the drain layer lead lines 302 are formed so as to be staggered with respect to the gate layer lead lines 301. Then, the inorganic passivation film 107 is formed and covers the drain layer lead lines 302. In FIG. 23, an image signal is applied to both the gate layer lead lines 301 and the drain layer lead lines 302, both of which are connected to the image signal lines in the connecting portion 31. Note that the basic configuration is the same as the case in which the lead lines 30 are connected to the scan lines in the connecting portion 31.

[0086] The switching from the image signal line to the gate layer lead line 301 or the switching from the scan line to the drain layer lead line 302 is done by the bridging ITO. Thus, it is possible to adjust the resistance of the lead line 30 by adjusting the length of the bridging ITO in the connecting

portion 31. Up to now, the switching from the drain layer lead line 302 to the gate layer lead line 301 or the switching from the gate layer lead line 301 to the drain layer lead line 302 has been done by the upper ITO 60. Even in the case of the switching by the upper ITO 60, it is possible to adjust the resistance of the lead line 30 by adjusting the length of the upper ITO 60.

[0087] On the other hand, in the case of IPSLITE 3, the pixel electrode 106 of ITO, as well as the gate electrode 101 or the lead line of the scan line are formed on the same layer as the gate layer. Thus, there is no need to form a through hole to connect the lower ITO 50, which is formed at the same time as the pixel electrode 106, to the gate layer lead line 301. Because there is no need to form the through hole, the space of the through hole can be saved when viewed from the top. At this point, IPSLITE 3 is advantageous.

[0088] FIG. 24 is an example of adjusting the resistance of the lead line 30 by the lower ITO 50 in the configuration of IPSLITE 3. In this example, the drain layer lead line 302 is switched to the gate layer lead line 301 through the lower ITO 50 that is formed at the same time as the pixel electrode 106. The example of FIG. 24 shows that the pixel electrode 106 is formed prior to the formation of the gate electrode 101. Thus, in FIG. 24, the gate layer lead line 301 overlaps a portion of the lower ITO 50 to establish connection between the gate layer lead line 301 and the lower ITO 50. FIG. 25 is an example in which the gate electrode 101 is formed prior to the formation of the lower ITO 50 in IPSLITE 3. Thus, in FIG. 25, the lower ITO 50 overlaps a portion of the gate layer lead line 301 to establish connection between the lower ITO 50 and the gate layer lead line 301. The other configuration and operation are the same as those in FIG. 24.

[0089] FIG. 26 is an example of adjusting the resistance of the lead line 30 by the lower ITO 50 in IPSLITE 1. In this example, the gate layer lead line 301 is switched to the drain layer lead line 302 through the lower ITO 50. In FIG. 26, the drain layer lead line 302 overlaps a portion of the lower ITO 50 to establish connection between the lower ITO 50 and the drain layer lead line 302, without using the through hole. This is because, in IPSLITE 1, the pixel electrode 106 is formed prior to the formation of the source electrode 106 or the drain layer lead line 302.

[0090] FIG. 27 is an example of adjusting the resistance of the lead line 30 by the lower ITO 50 in IPSLITE 2. In this example, the gate layer lead line 301 is switched to the drain layer lead line 302 through the lower ITO 50. The operation is the same as the operation in FIG. 26. In IPSLITE 2, the source electrode 105 or the drain layer lead line 302 is formed prior to the formation of the pixel electrode 106 or the lower ITO 50. Thus, the lower ITO 50 overlaps a portion of the drain layer lead line 302 to establish connection between the lower ITO 50 and the drain layer lead line 302. In FIGS. 26 and 27, the bridging ITO is connected again to the drain layer lead line 302 without using the through hole. Thus, in this example there is no need to form the through hold, so that the space of the through hole can be saved when viewed from the top.

What is claimed is:

1. A liquid crystal display device comprising:

- a plurality of scan lines and a plurality of image signal lines,
- a display area has a plurality of pixels arranged in a matrix form,

- a plurality of terminals are arranged outside the display area, the terminals are inputted an image signal of the image signal lines,

- a plurality of lead lines made by a metal material, the lead lines are formed between the image signal lines in the display area and the terminals,

- wherein the lead lines have a connecting portion for connecting the image signal lines, the inclined line portion extending inclined to the image signal line, the straight line portion for connecting the terminals,

- a part of the lead lines are formed by a bridging ITO in the straight line portion.

2. The liquid crystal display device according to claim 1, wherein

- a length of the bridging ITO formed in the lead line having the inclined line portion of the large inclination is shorter than the length of the bridging ITO formed in the lead line having the inclined line portion of a small inclination.

3. The liquid crystal display device according to claim 2, wherein the pixel includes a TFT, and a transmission part in which a common electrode having a slit is formed on a pixel electrode through an inter-layer insulating film, a source electrode of the TFT and the image signal line are formed by the same material,

- the source electrode and the pixel electrode are formed on a gate insulating film, and

- the bridging ITO is formed on a same layer as the pixel electrode.

4. The liquid crystal display device according to claim 3, wherein the pixel electrode is formed prior to the source electrode.

5. The liquid crystal display device according to claim 2, wherein the pixel includes a TFT, and a transmission part in which a common electrode having a slit is formed on a pixel electrode through a gate insulating film and an inter-layer insulating film,

- wherein a source electrode of the TFT and the image signal line are formed by the same material,

- wherein the source electrode is formed on the gate insulating film,

- wherein the pixel electrode is formed below the gate insulating film, and

- wherein the bridging ITO is formed on a same layer as the pixel electrode formed by ITO.

6. The liquid crystal display device according to claim 2, wherein the pixel includes a TFT, and a transmission part in which a pixel electrode having a slit is formed on a common electrode through an inter-layer insulating film,

- a source electrode of the TFT and the image signal line are formed by the same material,

- the source electrode is formed on a gate insulating film, and the bridging ITO is formed on a same layer as the common electrode formed by ITO.

7. A liquid crystal display device comprising:

- a plurality of scan lines and a plurality of image signal lines,

- a display area has a plurality of pixels arranged in a matrix form,

- a plurality of terminals are arranged outside the display area, the terminals are inputted a scan signal of the scan signal lines,

- a plurality of lead lines made by a metal material, the lead lines are formed between the scan lines in the display area and the terminals,
wherein the lead lines have a connecting portion for connecting the scan lines, the inclined line portion extending inclined to the scan line, the straight line portion for connecting the terminals,
a part of the lead lines are formed by a bridging ITO in the straight line portion.
- 8.** The liquid crystal display device according to claim **7**, wherein
a length of the bridging ITO formed in the lead line having the inclined line portion of the large inclination is shorter than the length of the bridging ITO formed in the lead line having the inclined line portion of a small inclination.
- 9.** The liquid crystal display device according to claim **8**, wherein the pixel includes a TFT, and a transmission part in which a common electrode having a slit is formed on a pixel electrode through an inter-layer insulating film, a gate electrode of the TFT and the scan line are formed by the same material,
a source electrode of the TFT and the pixel electrode are formed on a gate insulating film, and
the bridging ITO is formed on a same layer as the pixel electrode formed by ITO.
- 10.** The liquid crystal display device according to claim **8**, wherein the pixel includes a TFT, and a transmission part in which a common electrode having a slit is formed on a pixel electrode through a gate insulating film and an inter-layer insulating film,
a gate electrode of the TFT and the scan line are formed by the same material,
a source electrode of the TFT is formed on the gate insulating film,
the pixel electrode is formed below the gate insulating film, and
the bridging ITO is formed on a same layer as the pixel electrode formed by ITO.
- 11.** The liquid crystal display device according to claim **10**, wherein the pixel electrode is formed prior to the source electrode.
- 12.** The liquid crystal display device according to claim **8**, wherein the pixel includes a TFT, and a transmission part in which a pixel electrode having a slit is formed on a common electrode through an inter-layer insulating film, a source electrode of the TFT and the image signal line are formed by the same material,
the source electrode is formed on a gate insulating film, and
the bridging ITO is formed on a same layer as the common electrode formed by ITO.

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摘要(译)

连接图像信号线和IC驱动器的端子的漏极层引线在中间被中断，并且通过桥接与像素ITO同时形成的ITO来桥接间隙。因此，调整引线长度的差异，使得连接到IC驱动器中心的端子的引线中的桥接ITO的长度长于连接的引线中的桥接ITO的长度。在IC驱动器的末端的端子处，由于引线的长度根据位置的不同而减小了引线的布线电阻的差异。

