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(54) **GOA CIRCUIT FOR LIQUID CRYSTAL DISPLAYING AND DISPLAY DEVICE**

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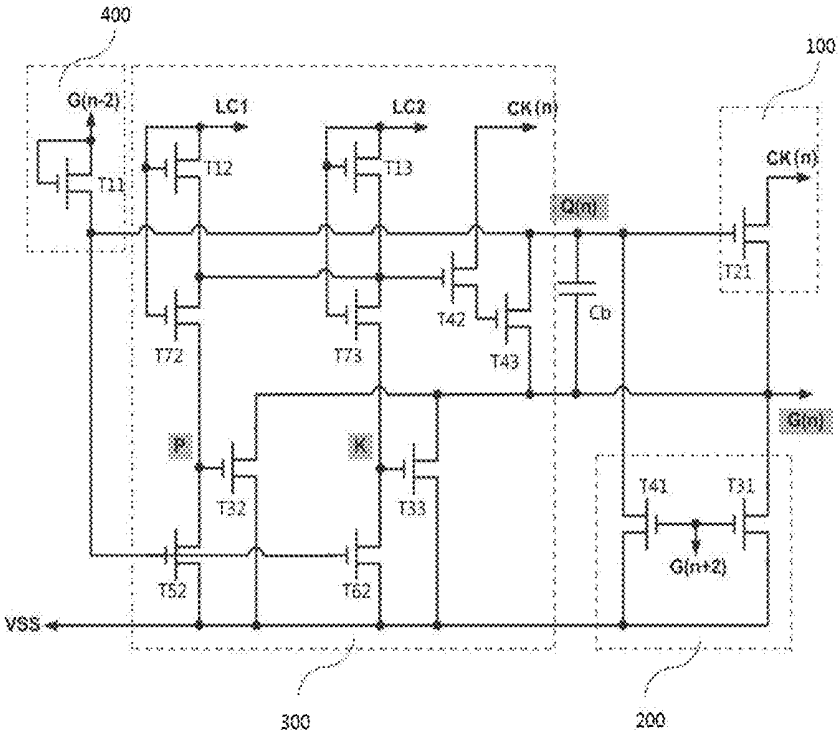
(57) **ABSTRACT**

The present invention relates to a GOA circuit for liquid crystal displaying and a display device. The GOA circuit includes a plurality of cascaded GOA units and the nth-stage GOA unit includes a pull-up part (**100**), a key pull-down part (**200**), a pull-down holding part (**300**), a pull-up control part (**400**), and a boost capacitor (Cb). In operation, a nth-stage clock signal (CK(n)) and first and second clock signals (LC**1** and LC**2**) are inputted. The frequencies of the first clock signal (LC**1**) and the second clock signal (LC**2**) are lower than the nth clock signal (CK(n)). The first clock signal (LC**1**) charging a first circuit point (P) and the second clock signal (LC**2**) charging a second circuit point (K) are alternately carried out. The present invention also provides a corresponding display device. The GOA circuit of the present invention precisely controls the voltage of the gate Q(n) that affects charging of a horizontal scan line by means of the low frequency clock signal and the high frequency clock signal, so as to ensure a stable output of the GOA charging signal.



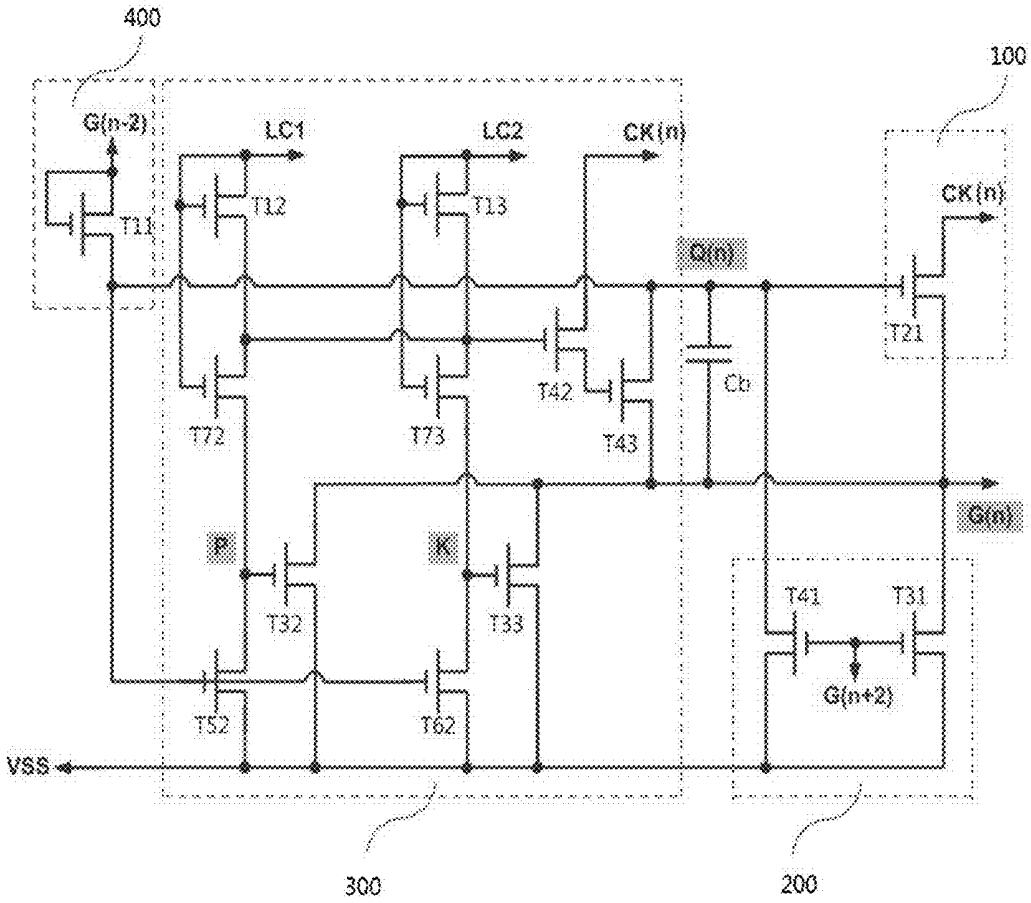

400
100
G(n-2)
LC1
LC2
CK(n)
T11
T12
T13
Q(n)
CK(n)
T21
T42
Cb
T72
T73
T43
Q(n)
P
K
T32
T33
T41
T31
G(n+2)
T52
T62
VSS
300
200

Fig. 1

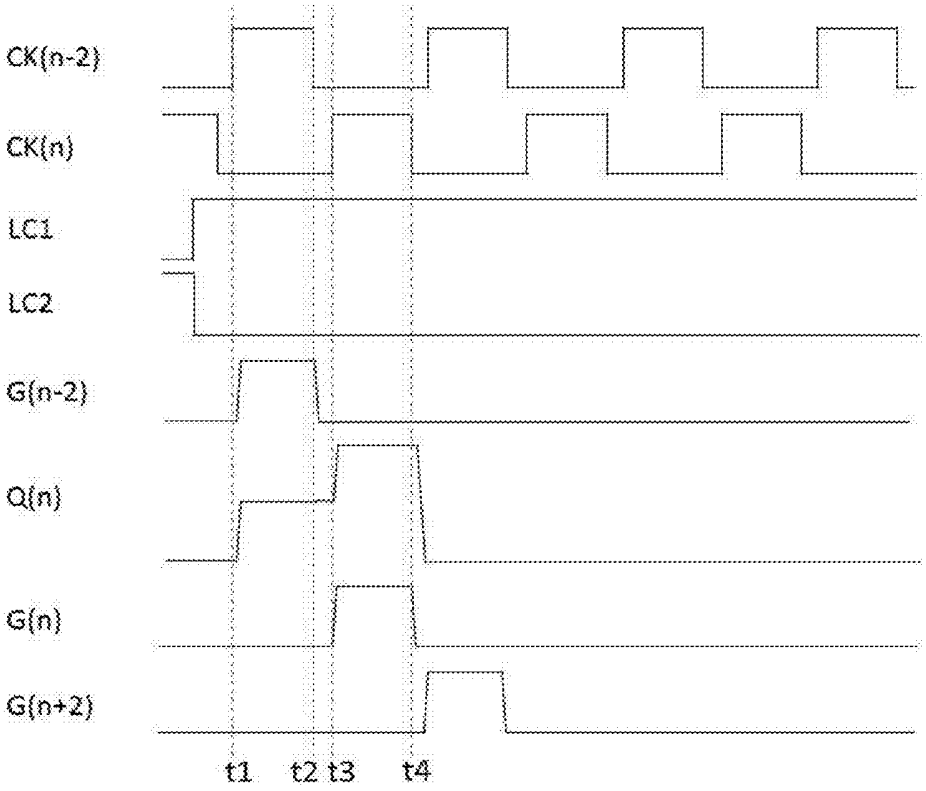


Fig. 2

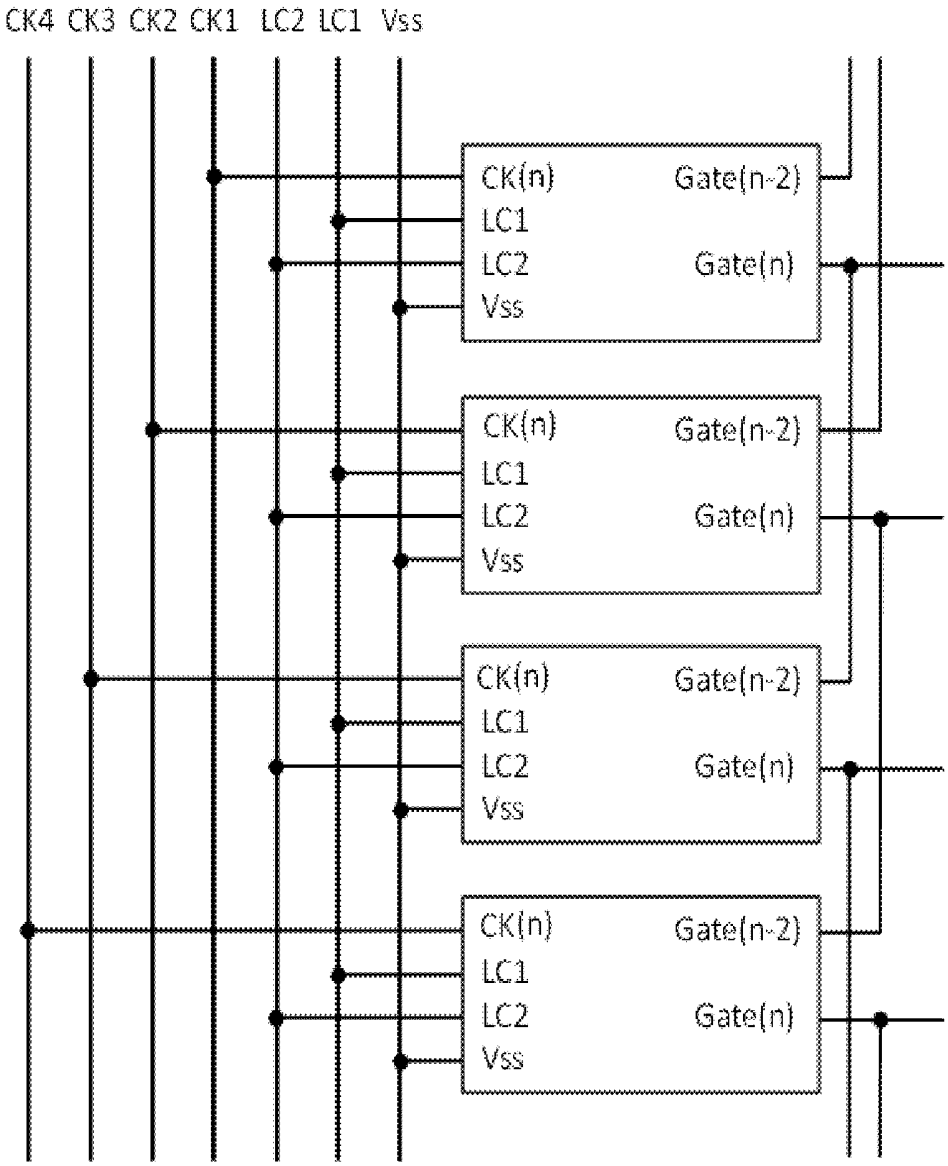

CK4 CK3 CK2 CK1 LC2 LC1 Vss
CK(n)
LC1
LC2
Vss
Gate(n-2)
Gate(n)
CK(n)
LC1
LC2
Vss
Gate(n-2)
Gate(n)
CK(n)
LC1
LC2
Vss
Gate(n-2)
Gate(n)
CK(n)
LC1
LC2
Vss
Gate(n-2)
Gate(n)

Fig. 3

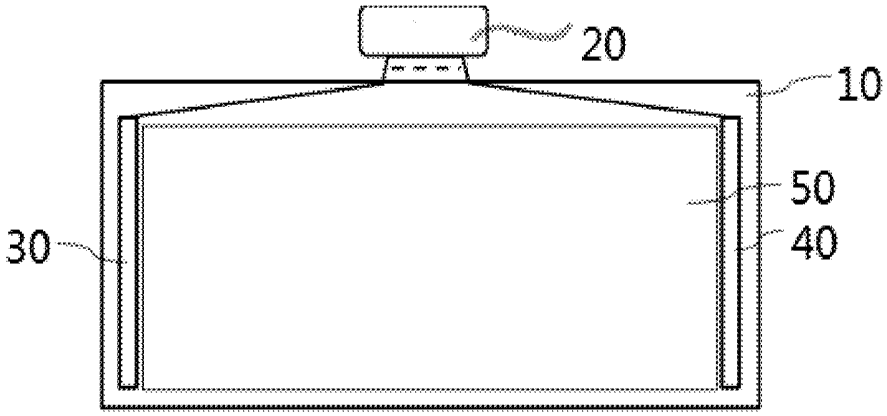


Fig. 4

GOA CIRCUIT FOR LIQUID CRYSTAL DISPLAYING AND DISPLAY DEVICE

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to the field of liquid crystal displaying technology, and in particular to a GOA (Gate Driver on Array) circuit for liquid crystal displaying and a display device.

[0003] 2. the Related Arts

[0004] Liquid crystal displays have many advantages, such as thin device body, power saving, and being free of radiation and are widely used. The existing liquid crystal displays on the market are mostly backlight type liquid crystal displays, which comprise a liquid crystal panel and a backlight module. The operation principle of the liquid crystal panel is to place liquid crystal molecules between two parallel glass substrates and applying a driving voltage to the two glass substrates to control the rotating direction of the liquid crystal molecules, in order to refract the light of the backlight module out to generate an image.

[0005] In an active liquid crystal display, each pixel has a thin film transistor (TFT) having a gate connected with a horizontal scan line, a drain connected with a vertical data line, and a source connected with a pixel electrode. Applying a sufficient voltage on the horizontal scan line can turn on all of the TFTs on this line, and at this time, the pixel electrodes of the horizontal scan line are connected with the vertical data line, thereby writing a display signal of the data line to the pixels to control the transmittance of different liquid crystal thereby achieving an effect of controlling color. The driving of the horizontal scan line of the conventional active liquid crystal display panel is provided by an external IC (Integrated Circuit). The external IC can control charging and discharging of each stage horizontal scan line in stage by stage manner. However, GOA technology, which refers to Gate Driver on Array technology, can utilize an existing manufacturing process of a liquid crystal display panel to form a driving circuit of the horizontal scan line on the substrate surrounding a display region, making it accomplish driving of the horizontal scan line to replace the external IC. The GOA technology can reduce the process of bonding the external IC, making it possible to improve the productivity and reducing the cost, and moreover, it can make the liquid crystal display panel more suitable for display products having a slim bezel or no bezel.

[0006] An existing GOA circuit generally comprises a plurality of cascaded GOA units and each GOA unit corresponds to a horizontal scan line. A general structure of the GOA unit comprises a pull-up part, a pull-up control part, a transfer part, a key pull-down part, a pull-down holding part, and a boost capacitor for boosting voltage. The pull-up part generally supplies an output of a clock signal as a gate signal; the pull-up control part is responsible for controlling the turn-on time of the pull-up part and is generally connected with a transfer signal or a gate signal transmitted from a previous stage GOA circuit; the key pull-down part is responsible for pulling the gate to a low voltage in a first time point, namely shutting off the gate signal; the pull-down holding part is responsible for holding the gate output signal and the gate signal (commonly referred to as a Q point) of the pull-up part in a turn-off status (namely negative voltage), there being generally two pull-down holding modules operating alternately; and the boost capacitor (C) is responsible for boosting Q point for a second time in order to facilitate outputting of G(N) of the pull-up part.

[0007] The purpose of the GOA circuit is to output the scan waveform, which is supplied from an integrated circuit through the circuit operation in order to turn on a pixel switch and thereby supplying a data signal to an ITO (Indium Tin Oxide) electrode. After the data signal has been input, the content of the data signal is held up until a next frame is turned on. During the operation of the circuit, since a scan circuit is set off in the remaining time of a frame after having been turned on, the turn-off (holding) time of the scan circuit is much longer than the scanning time, so that the requirement for the stability of the thin film transistor in the GOA circuit is very high. In order to ensure a stable output of the GOA circuit charging signal, it is extremely desired for a solution that the voltage of the gate Q(n) of the thin film transistor affecting charging of the horizontal scan line in the GOA circuit can be precisely controlled.

SUMMARY OF THE INVENTION

[0008] Therefore, a purpose of the present invention is to provide a GOA (Gate Driver on Array) circuit for liquid crystal displaying, which achieves precise control of the voltage of the gate Q(n) of a thin film transistor that affects charging of a horizontal scan line by means of a low frequency clock signal and a high frequency clock signal so as to ensure a stable output of a GOA charging signal.

[0009] Another purpose of the present invention is to provide a liquid crystal display device that uses the above GOA circuit to achieve precise control of the voltage of the gate Q(n) of a thin film transistor that affects charging of a horizontal scan line by means of a low frequency clock signal and a high frequency clock signal so as to ensure a stable output of a GOA charging signal.

[0010] In order to achieve the above purposes, the present invention provides a GOA circuit for liquid crystal displaying, which comprises a plurality of cascaded GOA units, in which a nth-stage GOA control unit controls charging of a nth-stage horizontal scan line of a display region and the nth-stage GOA unit comprises a pull-up part, a key pull-down part, a pull-down holding part, a pull-up control part, and a boost capacitor, the pull-up part, the key pull-down part, the pull-down holding part, and the boost capacitor being connected with a gate signal point and the nth-stage horizontal scan line, the pull-up control part being connected with the gate signal point;

[0011] wherein the key pull-down part comprises:

[0012] a first thin film transistor, which has a gate connected with a first circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of a direct current low voltage;

[0013] a second thin film transistor, which has a gate connected with a second circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of the direct current low voltage;

[0014] a third thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the first circuit point and receiving an input of the direct current low voltage;

[0015] a fourth thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the second circuit point and receiving an input of the direct current low voltage;

[0016] a fifth thin film transistor, which has a drain and a source respectively connected with the gate signal point and the nth horizontal scan line;

[0017] a sixth thin film transistor, which has a drain and a source respectively receiving an input of a nth-stage clock signal and connected with a gate of the fifth thin film transistor;

[0018] a seventh thin film transistor, which has a gate receiving an input of a first clock signal and a drain and a source respectively connected with a gate of the sixth thin film transistor and the first circuit point;

[0019] an eighth thin film transistor, which has a gate receiving an input of a second clock signal and a drain and a source respectively connected with the gate of the sixth thin film transistor and the second circuit point;

[0020] a ninth thin film transistor, which has a gate receiving an input of the first clock signal and a drain and a source respectively receiving an input of the first clock signal and connected with the gate of the sixth thin film transistor; and

[0021] a tenth thin film transistor, which has a gate receiving an input of the second clock signal and a drain and a source respectively receiving an input of the second clock signal and connected with the gate of the sixth thin film transistor;

[0022] whereby in operation, frequencies of the first clock signal and the second clock signal are set lower than the nth clock signal and the first clock signal charging the first circuit point and the second clock signal charging the second circuit point are alternately carried out.

[0023] The pull-up part comprises: an eleventh thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively receiving an input of the nth-stage clock signal and connected with the nth-stage horizontal scan line.

[0024] The key pull-down part comprises: a twelfth thin film transistor, which has a gate connected with a (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the nth-stage horizontal scan line and receiving an input of the direct current low voltage; and a thirteenth thin film transistor, which has a gate connected with the (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the gate signal point and receiving an input of the direct current low voltage.

[0025] The pull-up control part comprises: a fourteenth thin film transistor, which has a gate connected with a (n−2)th-stage horizontal scan line and a drain and a source respectively connected with the (n−2)th-stage horizontal scan line and the gate signal point.

[0026] The nth-stage clock signal has a duty ratio of 40%.

[0027] The first clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

[0028] The second clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

[0029] The direct current low voltage signal is supplied via a common metal wire to the plurality of cascaded GOA units.

[0030] The present invention also provides a GOA circuit for liquid crystal displaying, which comprises a plurality of cascaded GOA units, in which a nth-stage GOA control unit controls charging of a nth-stage horizontal scan line of a display region and the nth-stage GOA unit comprises a pull-up part, a key pull-down part, a pull-down holding part, a pull-up control part, and a boost capacitor, the pull-up part, the key pull-down part, the pull-down holding part, and the boost capacitor being connected with a gate signal point and the nth-stage horizontal scan line, the pull-up control part being connected with the gate signal point;

[0031] wherein the key pull-down part comprises:

[0032] a first thin film transistor, which has a gate connected with a first circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of a direct current low voltage;

[0033] a second thin film transistor, which has a gate connected with a second circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of the direct current low voltage;

[0034] a third thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the first circuit point and receiving an input of the direct current low voltage;

[0035] a fourth thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the second circuit point and receiving an input of the direct current low voltage;

[0036] a fifth thin film transistor, which has a drain and a source respectively connected with the gate signal point and the nth horizontal scan line;

[0037] a sixth thin film transistor, which has a drain and a source respectively receiving an input of a nth-stage clock signal and connected with a gate of the fifth thin film transistor;

[0038] a seventh thin film transistor, which has a gate receiving an input of a first clock signal and a drain and a source respectively connected with a gate of the sixth thin film transistor and the first circuit point;

[0039] an eighth thin film transistor, which has a gate receiving an input of a second clock signal and a drain and a source respectively connected with the gate of the sixth thin film transistor and the second circuit point;

[0040] a ninth thin film transistor, which has a gate receiving an input of the first clock signal and a drain and a source respectively receiving an input of the first clock signal and connected with the gate of the sixth thin film transistor; and

[0041] a tenth thin film transistor, which has a gate receiving an input of the second clock signal and a drain and a source respectively receiving an input of the second clock signal and connected with the gate of the sixth thin film transistor;

[0042] whereby in operation, frequencies of the first clock signal and the second clock signal are set lower than the nth clock signal and the first clock signal charging the first circuit point and the second clock signal charging the second circuit point are alternately carried out;

[0043] wherein the pull-up part comprises: an eleventh thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively receiving an input of the nth-stage clock signal and connected with the nth-stage horizontal scan line; and

[0044] wherein the key pull-down part comprises: a twelfth thin film transistor, which has a gate connected with a (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the nth-stage horizontal scan line and receiving an input of the direct current low voltage; and a thirteenth thin film transistor, which has a gate connected with the (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the gate signal point and receiving an input of the direct current low voltage.

[0045] The pull-up control part comprises: a fourteenth thin film transistor, which has a gate connected with a (n−2)th-

stage horizontal scan line and a drain and a source respectively connected with the (n−2)th-stage horizontal scan line and the gate signal point.

[0046] The nth-stage clock signal has a duty ratio of 40%.

[0047] The first clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

[0048] The second clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

[0049] The direct current low voltage signal is supplied via a common metal wire to the plurality of cascaded GOA units.

[0050] The present invention further provides a display device, which comprises a GOA circuit for liquid crystal displaying described above.

[0051] The GOA circuit for liquid crystal displaying and the display device according to the present invention can precisely control the voltage of the gate Q(n) of the thin film transistor affecting charging of the horizontal scan line in a charging period and a non-charging period by means of the low frequency clock signal and the high frequency clock signal, thereby ensuring a stable output of the GOA charging signal. Utilizing the GOA circuit of the present invention make it possible to produce a liquid crystal display device having a slim bezel or no bezel with a low cost.

BRIEF DESCRIPTION OF THE DRAWINGS

[0052] The following description combines the drawings, through describing in detail the embodiments in the present invention, making the technical solutions and other beneficial effect in the present invention more obvious.

[0053] In the drawings,

[0054] FIG. **1** is a circuit diagram of an embodiment of a GOA circuit (single stage) for liquid crystal displaying according to the present invention;

[0055] FIG. **2** is a schematic view showing output waveforms of the GOA circuit for liquid crystal displaying according to the present invention at a normal temperature;

[0056] FIG. **3** is a schematic view showing a multi-stage architecture of a GOA circuit for liquid crystal displaying according to the present invention; and

[0057] FIG. **4** is a schematic view showing the structure of a liquid crystal display device to which a GOA circuit for liquid crystal displaying according to the present invention is applied.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0058] Referring to FIG. **1**, which is a circuit diagram of an embodiment of a GOA circuit (single stage) for liquid crystal displaying according to the present invention, the GOA circuit of the present invention comprises a plurality of cascaded GOA units, in which a nth-stage GOA control unit controls charging of a nth-stage horizontal scan line G(n) of a display region and the nth-stage GOA unit comprises a pull-up part **100**, a key pull-down part **200**, a pull-down holding part **300**, a pull-up control part **400**, and a boost capacitor Cb. The pull-up part **100**, the key pull-down part **200**, the pull-down holding part **300**, and the boost capacitor Cb are connected with a gate signal point Q(n) and the nth-stage horizontal scan line G(n). The pull-up control part **400** is connected with the gate signal point Q(n).

[0059] The pull-up part **100** comprises a thin film transistor T**21** that directly controls charging to the nth-stage horizontal scan line G(n) of the display region and has a gate connected with the gate signal point Q(n). A drain and a source of T**21** are respectively connected to a nth-stage high-frequency clock signal CK(n) and the nth-stage horizontal scan line G(n). The voltage of the gate of T**21** directly affects CK(n) charging G(n).

[0060] The key pull-down part **200** comprises a group of thin film transistors for discharging at the time when the charging of G(n) ends and comprises T**31** for discharging G(n) and T**41** for discharging Q(n). The transistor T**31** has a gate connected with a (n+2)th-stage horizontal scan line G(n+2) and a drain and a source respectively connected with the nth-stage horizontal scan line G(n) and receiving an input of a direct current low voltage VSS. The transistor T**41** has a gate connected with the (n+2)th-stage horizontal scan line G(n+2) and a drain and a source respectively connected with the gate signal point Q(n) and receiving an input of the direct current low voltage VSS.

[0061] The pull-up control part **400** comprises a thin film transistor T**11**, which has a gate connected with the (n−2)th-stage horizontal scan line G(n−2) and a drain and a source respectively connected with the (n−2)th-stage horizontal scan line G(n−2) and the gate signal point Q(n). The thin film transistor T**11** controls transfer of a (n−2)th-stage GOA signal to the nth-stage GOA circuit, allowing the GOA circuits to charge and discharge in a stage by stage manner.

[0062] The boost capacitor Cb is connected between Q(n) and G(n), allowing for boosting of the voltage of Q(n) through the coupling effect of Cb when voltage of G(n) is raised, thereby obtaining a higher voltage of Q(n) and a reduced RC delay of the GOA charging signal.

[0063] The pull-down holding part **300** comprises a group of thin-film transistors, which keep the low voltages of G(n) and Q(n) during a non-charge period of the GOA circuit. A thin film transistor T**32** has a gate connected with a first circuit point P and a drain and a source respectively connected with the nth-stage horizontal scan line G(n) and receiving an input of the direct current low voltage VSS. A thin film transistor T**33** has a gate connected with a second circuit point K and a drain and a source respectively connected with the nth horizontal scan line G(n) and receiving an input of the direct current low voltage VSS. A thin film transistor T**52** has a gate connected with the gate signal point Q(n) and a drain and a source respectively connected with the first circuit point P and receiving an input of the direct current low voltage VSS. A thin film transistor **62** has a gate connected with the gate signal point Q(n) and a drain and a source respectively connected with the second circuit point K and receiving an input of the first direct current low voltage VSS. A thin film transistor T**43** has a drain and a source respectively connected with the gate signal point Q(n) and nth-stage horizontal scan line G(n). A thin film transistor T**42** has a drain and a source respectively connected with the nth-stage clock signal CK(n) and a gate of the thin film transistor T**43**. A thin film transistor T**72** has a gate receiving an input of a first clock signal LC**1** and a drain and a source respectively connected with a gate of the thin film transistor T**42** and the first circuit point P. A thin film transistor T**73** has a gate receiving an input of a second clock signal LC**2** and a drain and a source respectively connected with the gate of the thin film transistor T**42** and the second circuit point K. A thin film transistor T**12** has a gate receiving an input of the first clock signal LC**1** and a drain and a source respectively receiving an input of the first clock signal LC**1** and connected with the gate of the thin film transistor T**42**. A thin film transistor T**13** has a gate receiving

an input the second clock signal LC2 and a drain and a source respectively receiving an input of the second clock signal LC2 and connected with the gate of the thin film transistor T42. The direct current low voltage VSS can be connected with a low voltage level or ground. In operation, the nth clock signal CK(n), the first clock signal LC1, and the second clock signal LC2 are input and the frequencies of the first clock signal LC1 and the second clock signal LC2 are lower than that of the nth-stage clock signal CK(n). Moreover, the first clock signal LC1 charging the first circuit point P and the second clock signal LC2 charging the second circuit point K are alternately carried out.

[0064] The circuit points P and K are alternately charged by the low frequency clock signals LC1 and LC2 to be set at high voltages, thereby alternately controlling the thin film transistors T32 and T33 to turn on, in order to keep the low voltage of G(n) at a non-charge period and prevent the thin film transistors T32 or T33 from be long affected by gate voltage stress. The thin film transistor T52 is connected with P and receives an input of the direct current low voltage VSS and the thin film transistor T62 is connected with pint K and receives an input of the direct current low voltage VSS. The transistors T52 and T62 may turn on, when Q(n) is in a high voltage, to pull down the voltages of points P and K in order to turn off T32 and T33, preventing them from affecting charging. During the non-charging period, the thin film transistors T12 and T72 or T13 and T73 are turned on, point P or K is in a high voltage, and therefore, the gate of the thin film transistor T42 is in a high voltage and the high frequency clock signal CK(n) periodically turns on the thin film transistor T43 in order to keep Q(n) in a low voltage. During the charging period, after Q(n) is charged to a high voltage, T52 or T62 is turned on; the gate voltage of T42 is pulled down, making T42 off, T43 being prevented from turning on. Thus, the leakage current of Q(n) flowing through T43 decreases, improving the stability of the voltage of Q(n).

[0065] The GOA circuit of the present invention can precisely control the voltages of the gate Q(n) of the thin film transistor in a charging period and a non-charging period, which affect the charging of the horizontal scan lines through the low frequency clock signal and the high frequency clock signal, so as to ensure a stable output of the GOA charging signal. Specifically, (1) during the non-charging period, the thin film transistor T42 that is connected with the high frequency clock signal CK(n) and the thin film transistor T43 is on so that the high frequency clock signal CK(n) can periodically turn on the thin film transistor T43 in order to keep Q(n) at a low voltage; and (2) during the charging period, after Q(n) is charged to a high voltage, the thin film transistors T42 and T43 are turned off so that the leakage current of Q(n) flowing through T43 can be reduced.

[0066] Referring to FIG. 2, a schematic view is given to show output waveforms of the GOA circuit for liquid crystal displaying according to the present invention at a normal temperature, wherein the duty ratio of the high frequency clock signal is 40%. In FIG. 2, t1-t3 is a preparing period of time before G(n) is charged; t3-t4 is the charging period of G(n); and after t4, G(n) is discharged. The low frequency clock signals LC1 and LC2 can be selected to have the same frequency, but opposite phases. Further understanding of FIG. 2 can be made with reference to FIG. 1, where at t1, the voltage of CK(n−2) begins rising and the voltage of G(n−2) also begins rising; and the thin film transistor T11 is turned on to charge Q(n). After the voltage of Q(n) rises, the thin film transistors T52 and T62 are turned on, thereby shutting off T32, T42, T33, and T43 to prevent them from affecting the charging of Q(n) and G(n) affected. At t2, the voltage of CK(n−2) begins reducing, but the arrangement of connection of the thin film transistor T11 helps avoid the leakage current of Q(n), so that the voltage of Q(n) essentially maintains the same. At t3, the voltage of CK(n) begins rising and the thin film transistor T21 is turned on, so that Q(n) boosts to a higher voltage and controls T21 to charge G(n). At t4, CK(n) begins reducing but the voltage of Q(n) is not pulled down immediately, so that the thin film transistor T21 still maintains on for a short period of time after t4 in order to pull down the voltage of G(n). After that, the voltage of G(n+2) begins rising and the thin film transistors T31 and T41 are turned on so as to ensure the voltages of G(n) and Q(n) are pulled down. T52 and T62 are turned off after the voltage of Q(n) is pulled down. In summary, the present invention can precisely control the voltage of Q(n) through the low frequency clock signal and the high frequency clock signal, ensuring a stable output of the GOA charging signal.

[0067] Referring to FIG. 3, a schematic view is given to show a multi-stage architecture of a GOA circuit for liquid crystal displaying according to the present invention. FIG. 3 provides a multi-stage architecture of a GOA circuit according to the present invention, in which metal wires for transmitting the low frequency clock signals LC1 and LC2, the direct current low voltage VSS, and the four high frequency clock signals CK1-CK4 are placed outside each stage GOA circuit (of which the specific arrangement of connection is shown in FIG. 1). The low frequency clock signal LC1, the low frequency clock signal LC2, and the direct current low voltage VSS are respectively supplied through the common metal wires of their own to the plurality of cascaded GOA units. In the present embodiment, the nth-stage GOA circuit receives LC1, LC2, VSS, one CK signal of CK1-CK4, G(n−2) generated by the (n−2)th-stage GOA circuit, and G(n+2) generated by the (n+2)th-stage GOA circuit and generates G(n) signal. The connection among the stages of GOA circuit shown in FIG. 3 ensures the GOA signal can be transmitted stage by stage, so that the horizontal scan lines of the stages can be charged and discharged in a stage-wise manner. For the GOA units of the first and last stages, an activation signal can be applied to replace the missing input of G(n) signal.

[0068] The GOA circuit according to the present invention can use an existing manufacturing process of a liquid crystal display panel to form a driving circuit of the horizontal scan lines of the panel on a substrate surrounding a display region, making it possible to replace the external IC for driving each stage horizontal scan line of the liquid crystal display panel. The present invention is particularly suitable for producing a liquid crystal display panel having a slim bezel or no bezel.

[0069] Referring to FIG. 4, a schematic view is given to show the structure of a liquid crystal display device to which a GOA circuit for liquid crystal displaying according to the present invention is applied. In FIG. 4, a liquid crystal display device comprises a display substrate 10. A driving control panel 20 is mounted on the top of the display substrate 10 to provide drive and control signals to the display substrate 10. A left region 30 and a right region 40 of the display substrate 10 comprises GOA circuits formed thereon to allow for driving of the horizontal scan lines of the driving display region 50 from the left side and the right side. The GOA circuits receive an input signal from the driving control panel 20 and generates a control signal for the horizontal scan line is a stage

by stage manner so as to control the pixels of the display region **50** to activate line by line.

[0070] In summary, the GOA circuit for liquid crystal displaying and the display device according to the present invention can precisely control the voltage of the gate Q(n) of the thin film transistor affecting charging of the horizontal scan line in a charging period and a non-charging period by means of the low frequency clock signal and the high frequency clock signal, thereby ensuring a stable output of the GOA charging signal. Utilizing the GOA circuit of the present invention make it possible to produce a liquid crystal display device having a slim bezel or no bezel with a low cost.

[0071] The preferred embodiments according to the present invention are mentioned above, which cannot be used to define the scope of the right of the present invention. Those modifications and variations are considered encompassed in the scope of protection defined by the claims of the present invention.

What is claimed is:

1. A GOA (Gate Driver on Array) circuit for liquid crystal displaying, comprising a plurality of cascaded GOA units, in which a nth-stage GOA control unit controls charging of a nth-stage horizontal scan line of a display region and the nth-stage GOA unit comprises a pull-up part, a key pull-down part, a pull-down holding part, a pull-up control part, and a boost capacitor, the pull-up part, the key pull-down part, the pull-down holding part, and the boost capacitor being connected with a gate signal point and the nth-stage horizontal scan line, the pull-up control part being connected with the gate signal point;

wherein the key pull-down part comprises:

a first thin film transistor, which has a gate connected with a first circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of a direct current low voltage;

a second thin film transistor, which has a gate connected with a second circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of the direct current low voltage;

a third thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the first circuit point and receiving an input of the direct current low voltage;

a fourth thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the second circuit point and receiving an input of the direct current low voltage;

a fifth thin film transistor, which has a drain and a source respectively connected with the gate signal point and the nth horizontal scan line;

a sixth thin film transistor, which has a drain and a source respectively receiving an input of a nth-stage clock signal and connected with a gate of the fifth thin film transistor;

a seventh thin film transistor, which has a gate receiving an input of a first clock signal and a drain and a source respectively connected with a gate of the sixth thin film transistor and the first circuit point;

an eighth thin film transistor, which has a gate receiving an input of a second clock signal and a drain and a source respectively connected with the gate of the sixth thin film transistor and the second circuit point;

a ninth thin film transistor, which has a gate receiving an input of the first clock signal and a drain and a source respectively receiving an input of the first clock signal and connected with the gate of the sixth thin film transistor; and

a tenth thin film transistor, which has a gate receiving an input of the second clock signal and a drain and a source respectively receiving an input of the second clock signal and connected with the gate of the sixth thin film transistor;

whereby in operation, frequencies of the first clock signal and the second clock signal are set lower than the nth clock signal and the first clock signal charging the first circuit point and the second clock signal charging the second circuit point are alternately carried out.

2. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the pull-up part comprises: an eleventh thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively receiving an input of the nth-stage clock signal and connected with the nth-stage horizontal scan line.

3. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the key pull-down part comprises: a twelfth thin film transistor, which has a gate connected with a (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the nth-stage horizontal scan line and receiving an input of the direct current low voltage; and a thirteenth thin film transistor, which has a gate connected with the (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the gate signal point and receiving an input of the direct current low voltage.

4. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the pull-up control part comprises: a fourteenth thin film transistor, which has a gate connected with a (n−2)th-stage horizontal scan line and a drain and a source respectively connected with the (n−2)th-stage horizontal scan line and the gate signal point.

5. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the nth-stage clock signal has a duty ratio of 40%.

6. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the first clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

7. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the second clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

8. The GOA circuit for liquid crystal displaying as claimed in claim **1**, wherein the direct current low voltage signal is supplied via a common metal wire to the plurality of cascaded GOA units.

9. A GOA (Gate Driver on Array) circuit for liquid crystal displaying, comprising a plurality of cascaded GOA units, in which a nth-stage GOA control unit controls charging of a nth-stage horizontal scan line of a display region and the nth-stage GOA unit comprises a pull-up part, a key pull-down part, a pull-down holding part, a pull-up control part, and a boost capacitor, the pull-up part, the key pull-down part, the pull-down holding part, and the boost capacitor being connected with a gate signal point and the nth-stage horizontal scan line, the pull-up control part being connected with the gate signal point;

wherein the key pull-down part comprises:

a first thin film transistor, which has a gate connected with a first circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of a direct current low voltage;

a second thin film transistor, which has a gate connected with a second circuit point and a drain and a source respectively connected with the nth horizontal scan line and receiving an input of the direct current low voltage;

a third thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the first circuit point and receiving an input of the direct current low voltage;

a fourth thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively connected with the second circuit point and receiving an input of the direct current low voltage;

a fifth thin film transistor, which has a drain and a source respectively connected with the gate signal point and the nth horizontal scan line;

a sixth thin film transistor, which has a drain and a source respectively receiving an input of a nth-stage clock signal and connected with a gate of the fifth thin film transistor;

a seventh thin film transistor, which has a gate receiving an input of a first clock signal and a drain and a source respectively connected with a gate of the sixth thin film transistor and the first circuit point;

an eighth thin film transistor, which has a gate receiving an input of a second clock signal and a drain and a source respectively connected with the gate of the sixth thin film transistor and the second circuit point;

a ninth thin film transistor, which has a gate receiving an input of the first clock signal and a drain and a source respectively receiving an input of the first clock signal and connected with the gate of the sixth thin film transistor; and

a tenth thin film transistor, which has a gate receiving an input of the second clock signal and a drain and a source respectively receiving an input of the second clock signal and connected with the gate of the sixth thin film transistor;

whereby in operation, frequencies of the first clock signal and the second clock signal are set lower than the nth clock signal and the first clock signal charging the first circuit point and the second clock signal charging the second circuit point are alternately carried out;

wherein the pull-up part comprises: an eleventh thin film transistor, which has a gate connected with the gate signal point and a drain and a source respectively receiving an input of the nth-stage clock signal and connected with the nth-stage horizontal scan line; and

wherein the key pull-down part comprises: a twelfth thin film transistor, which has a gate connected with a (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the nth-stage horizontal scan line and receiving an input of the direct current low voltage; and a thirteenth thin film transistor, which has a gate connected with the (n+2)th-stage horizontal scan line and a drain and a source respectively connected with the gate signal point and receiving an input of the direct current low voltage.

10. The GOA circuit for liquid crystal displaying as claimed in claim **9**, wherein the pull-up control part comprises: a fourteenth thin film transistor, which has a gate connected with a (n−2)th-stage horizontal scan line and a drain and a source respectively connected with the (n−2)th-stage horizontal scan line and the gate signal point.

11. The GOA circuit for liquid crystal displaying as claimed in claim **9**, wherein the nth-stage clock signal has a duty ratio of 40%.

12. The GOA circuit for liquid crystal displaying as claimed in claim **9**, wherein the first clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

13. The GOA circuit for liquid crystal displaying as claimed in claim **9**, wherein the second clock signal is supplied via a common metal wire to the plurality of cascaded GOA units.

14. The GOA circuit for liquid crystal displaying as claimed in claim **9**, wherein the direct current low voltage signal is supplied via a common metal wire to the plurality of cascaded GOA units.

15. A display device, which comprises a GOA circuit for liquid crystal displaying according to claim **1**.

* * * * *

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摘要(译)

本发明涉及一种用于液晶显示的GOA电路和一种显示装置。 GOA电路包括多个级联GOA单元，第n级GOA单元包括上拉部分（ 100 ），键下拉部分（ 200 ）下拉保持部分（ 300 ），上拉控制部分（ 400 ）和升压电容器（Cb）。在操作中，输入第n级时钟信号（CK（n））以及第一和第二时钟信号（LC 1 和LC 2 ）。第一时钟信号（LC 1 ）和第二时钟信号（LC 2 的频率低于第n时钟信号（CK（n））。对第一电路连接点（P）充电的第一时钟信号（LC 1 ）和对第二电路连接点（K）充电的第二时钟信号（LC 2 ）交替进行出。本发明还提供了相应的显示装置。本发明的GOA电路通过低频时钟信号和高频时钟信号精确控制影响水平扫描线充电的栅极Q（n）的电压，以确保稳定输出。 GOA充电信号。