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(19) **United States**(12) **Patent Application Publication**
PARK et al.(10) **Pub. No.: US 2014/0307193 A1**(43) **Pub. Date: Oct. 16, 2014**(54) **LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF****Publication Classification**(51) **Int. Cl.****G02F 1/1362** (2006.01)(52) **U.S. Cl.**CPC **G02F 1/136213** (2013.01)USPC **349/38**(71) Applicant: **Samsung Display Co., Ltd.**,
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Yongin-City (KR)(21) Appl. No.: **14/054,184**(22) Filed: **Oct. 15, 2013****Related U.S. Application Data**

(63) Continuation of application No. 12/985,404, filed on Jan. 6, 2011, now Pat. No. 8,581,816.

(30) **Foreign Application Priority Data**

Sep. 13, 2010 (KR) 10-2010-0089405

(57) **ABSTRACT**

A liquid crystal display, the liquid crystal display comprises a plurality of gate lines which includes a first gate line, a transformation gate line, and a second gate line; a data line; and a pixel, wherein the pixel includes a first liquid crystal capacitor which includes a first sub-pixel electrode and a common electrode and a second liquid crystal capacitor which includes a second sub-pixel electrode and a common electrode; a first switching element connected to the first gate line, the data line, and the first sub-pixel electrode; a second switching element connected to the first gate line, the data line, and the second sub-pixel electrode; a third switching element connected to the transformation gate line and the second switching element; a transformation capacitor which includes a first terminal connected to the second gate line and a second terminal connected to the third switching element; and a first period where a gate-on voltage V_{on} is applied to the first gate line and a second period where the gate-on voltage V_{on} is applied to the transformation gate line do not overlap each other and, a gate-off voltage V_{off} is applied to the second gate line during the second period.

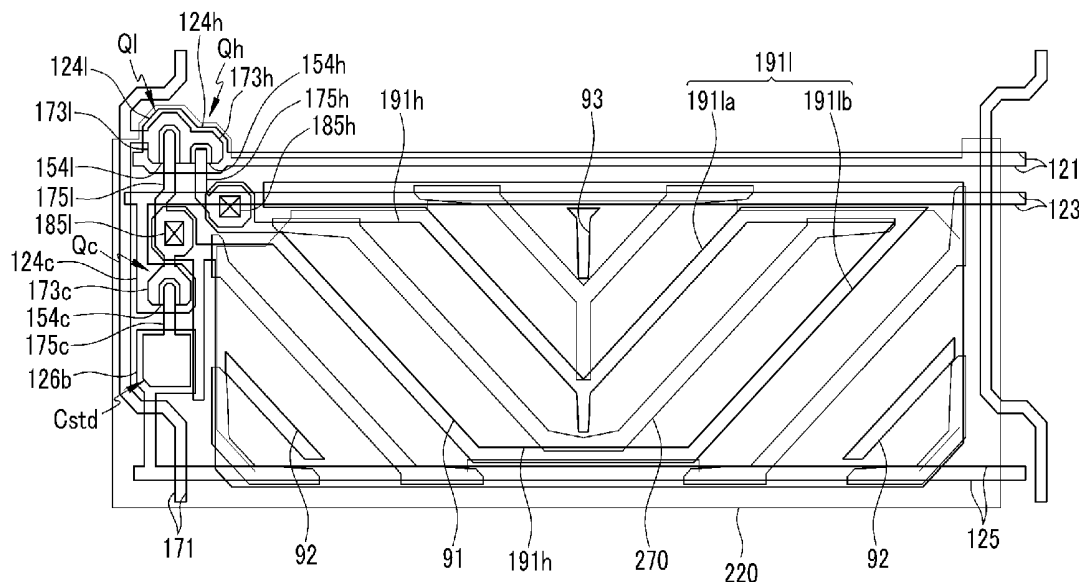


FIG.1

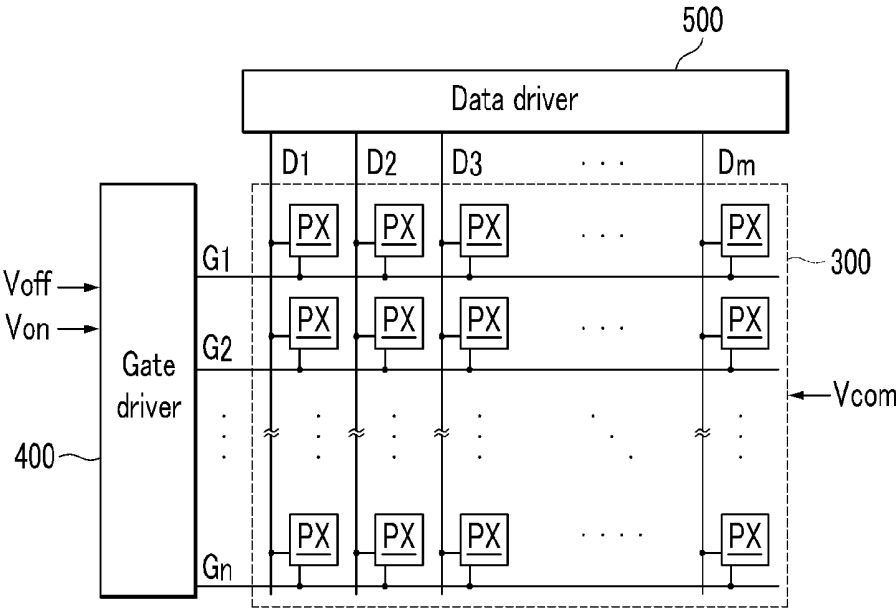


FIG.2

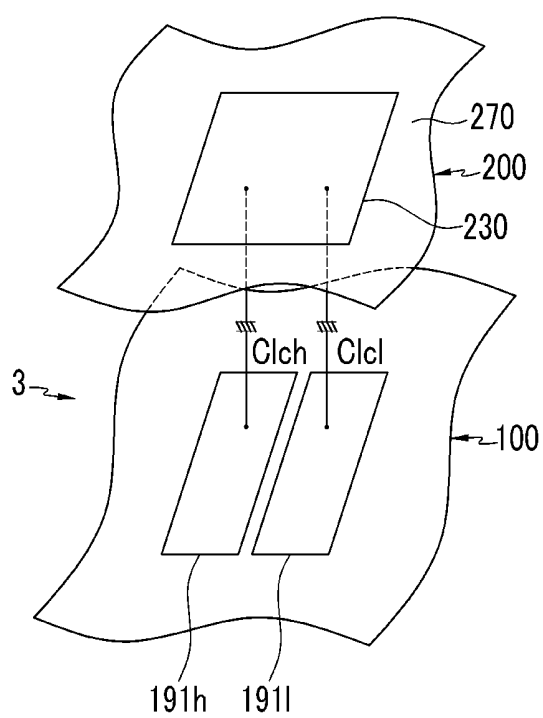


FIG.3

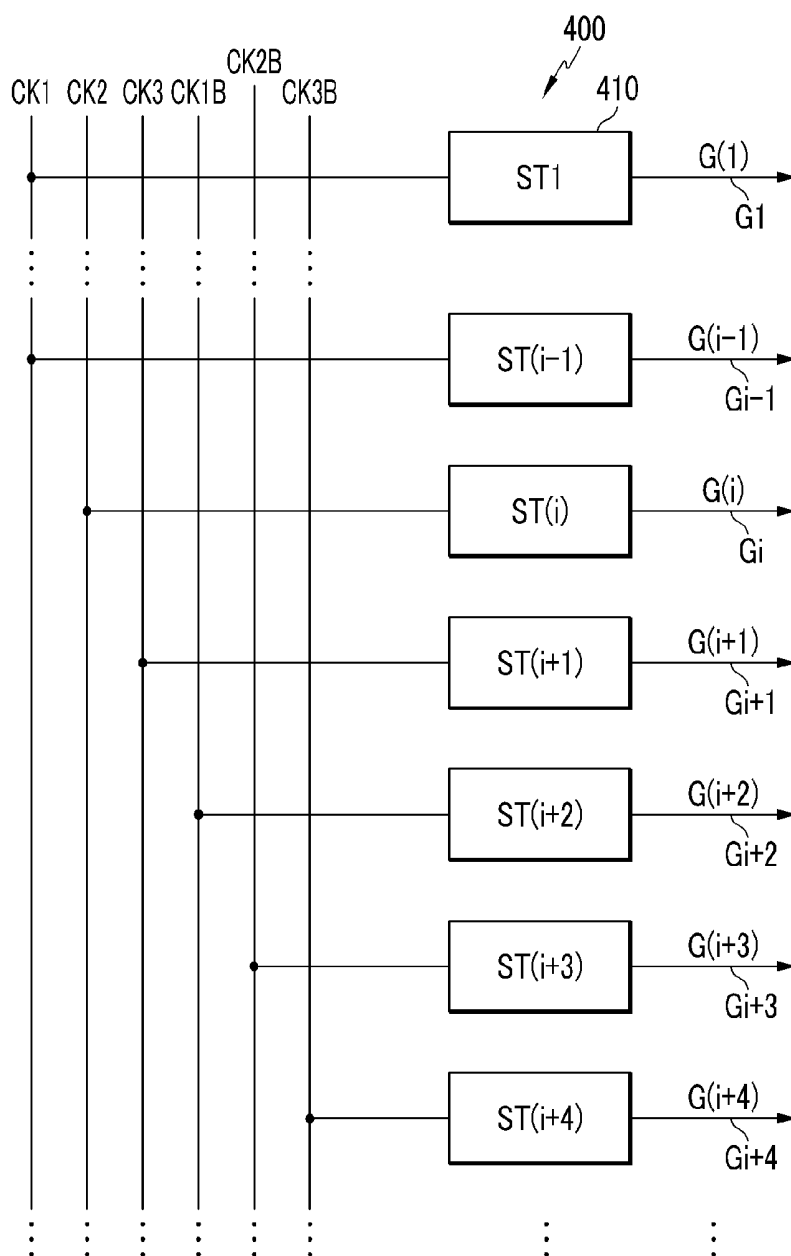


FIG.4

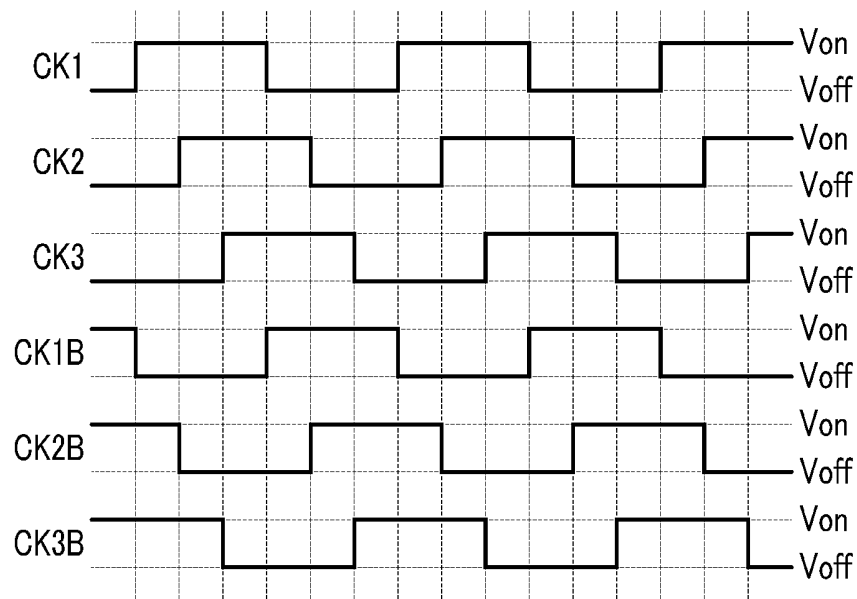


FIG.5

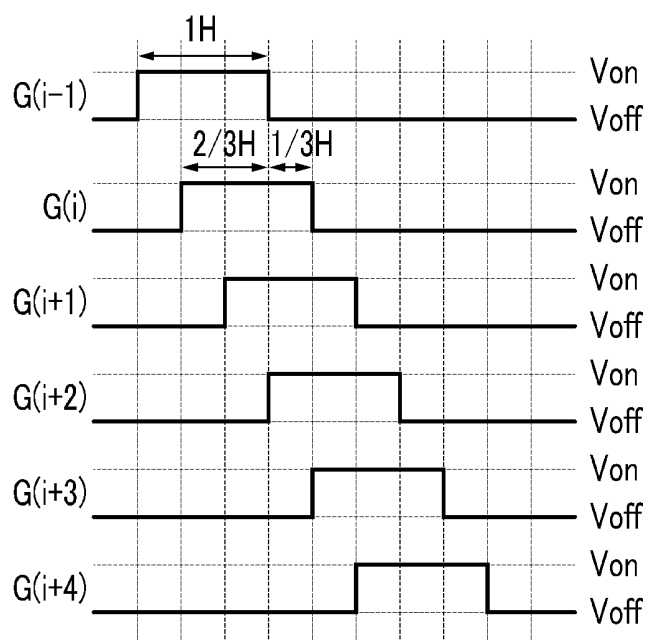


FIG.6

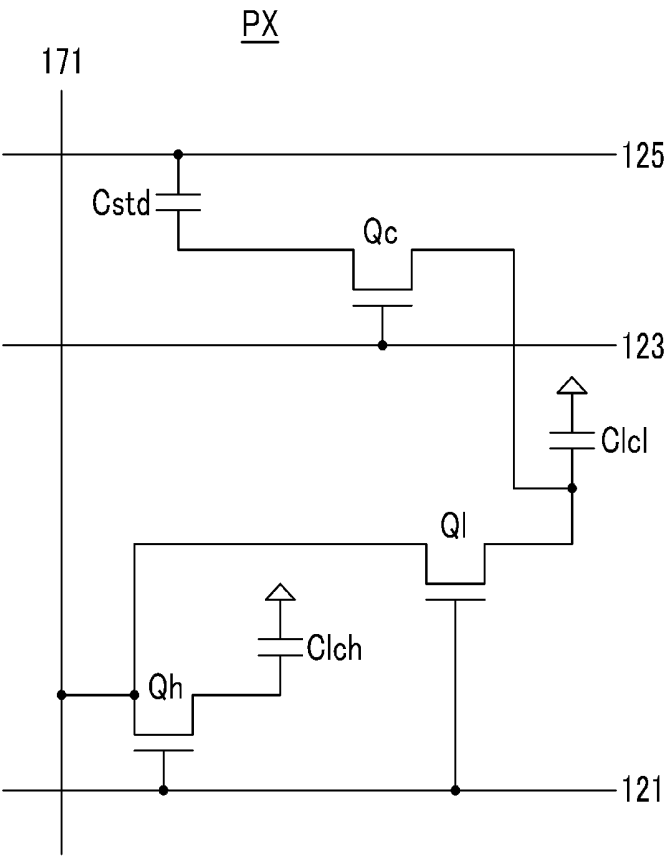


FIG.7

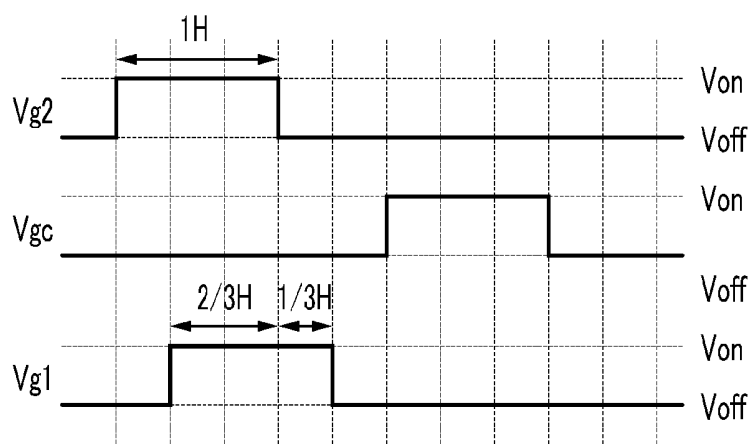


FIG.8

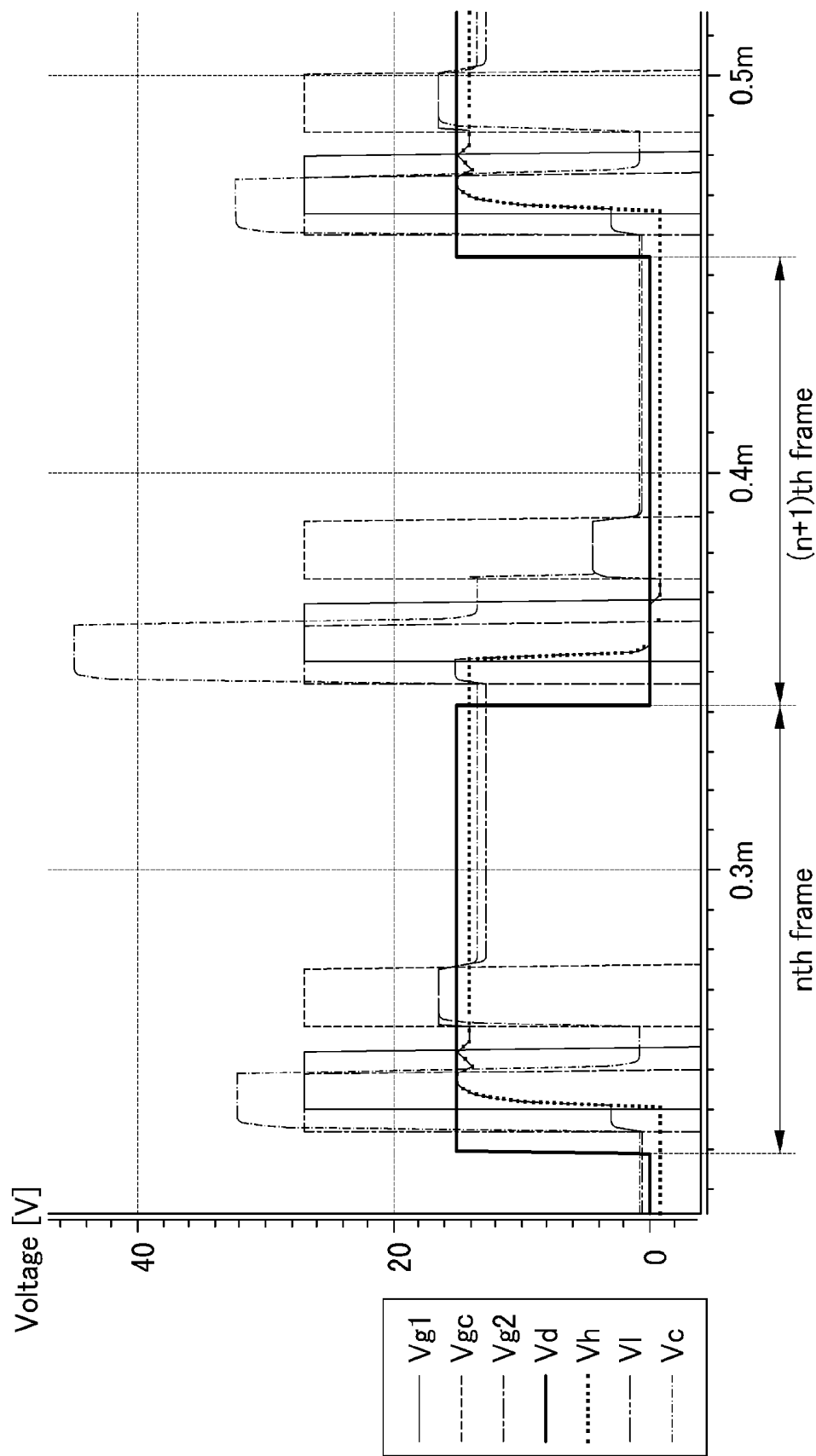


FIG. 9

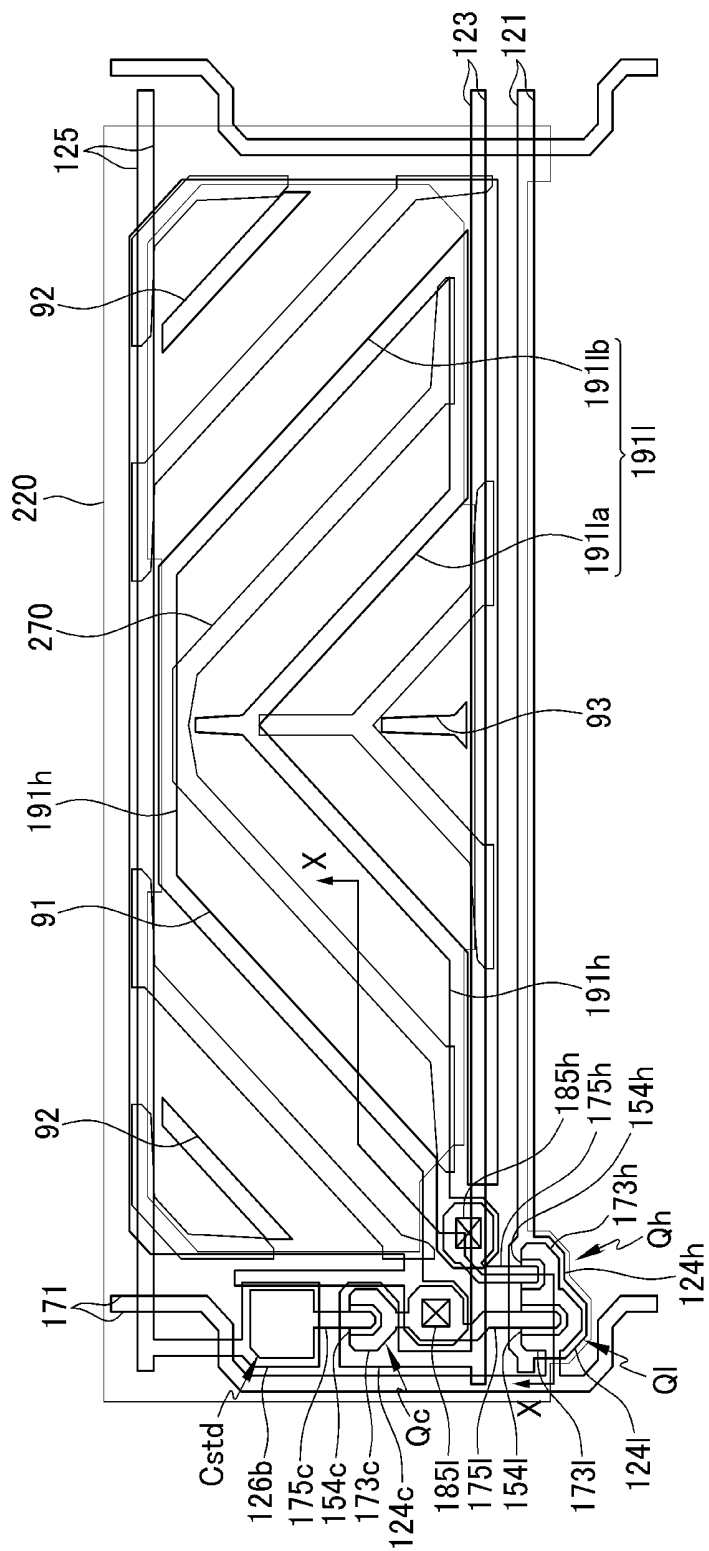


FIG.10

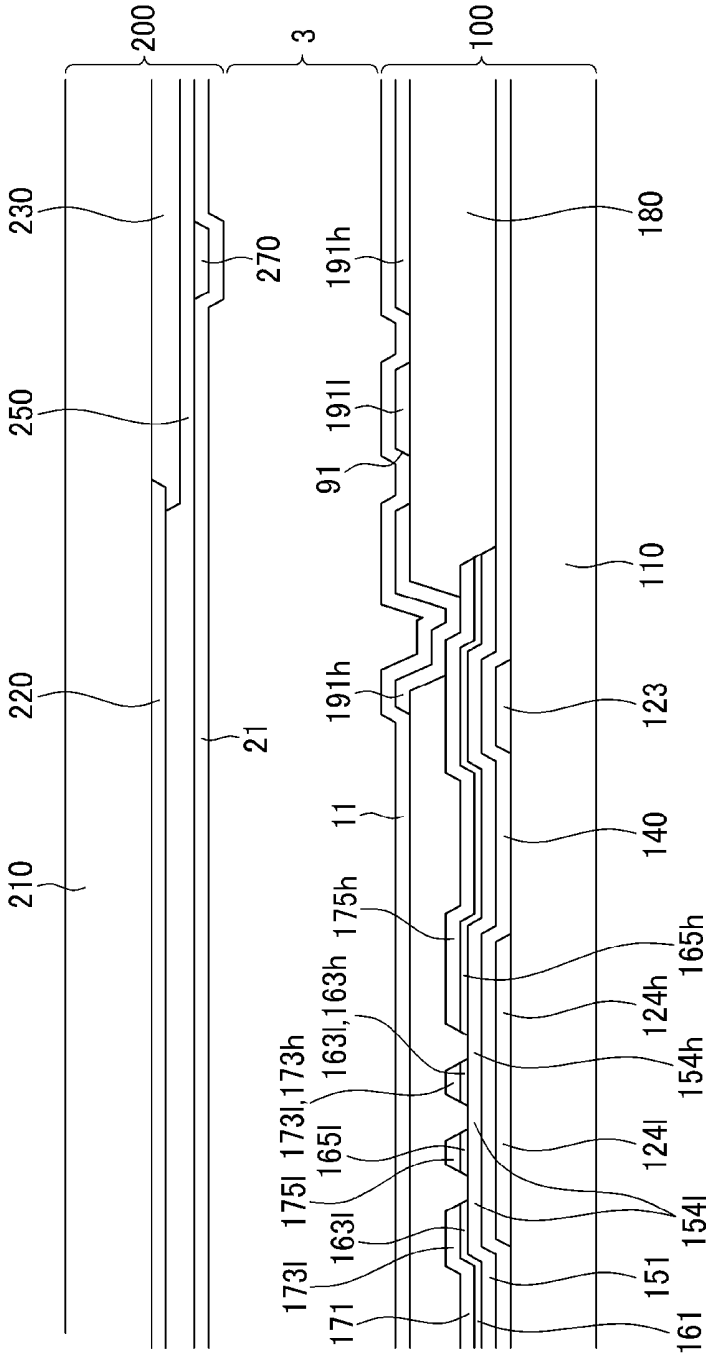


FIG.11

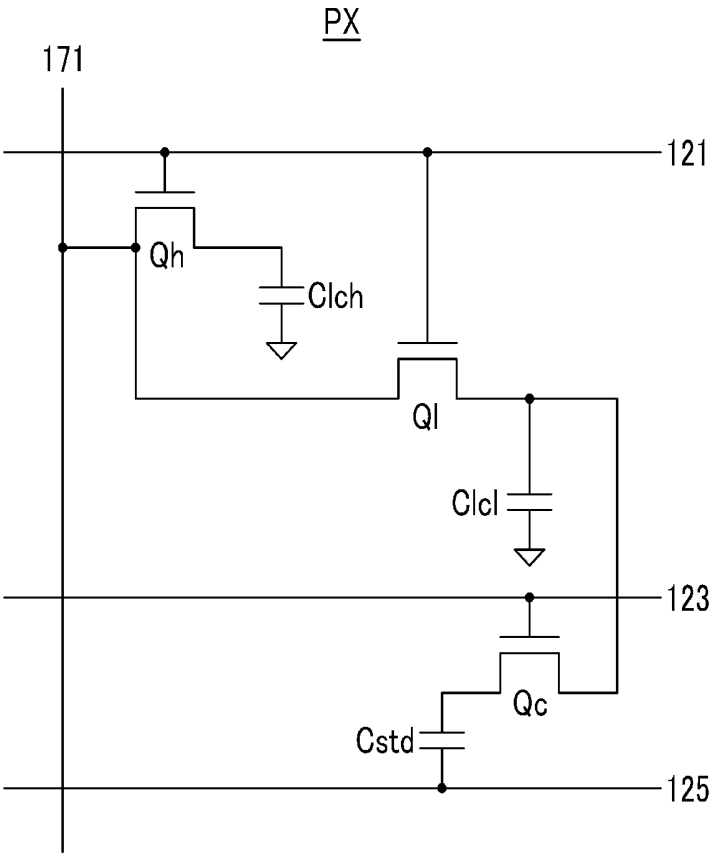
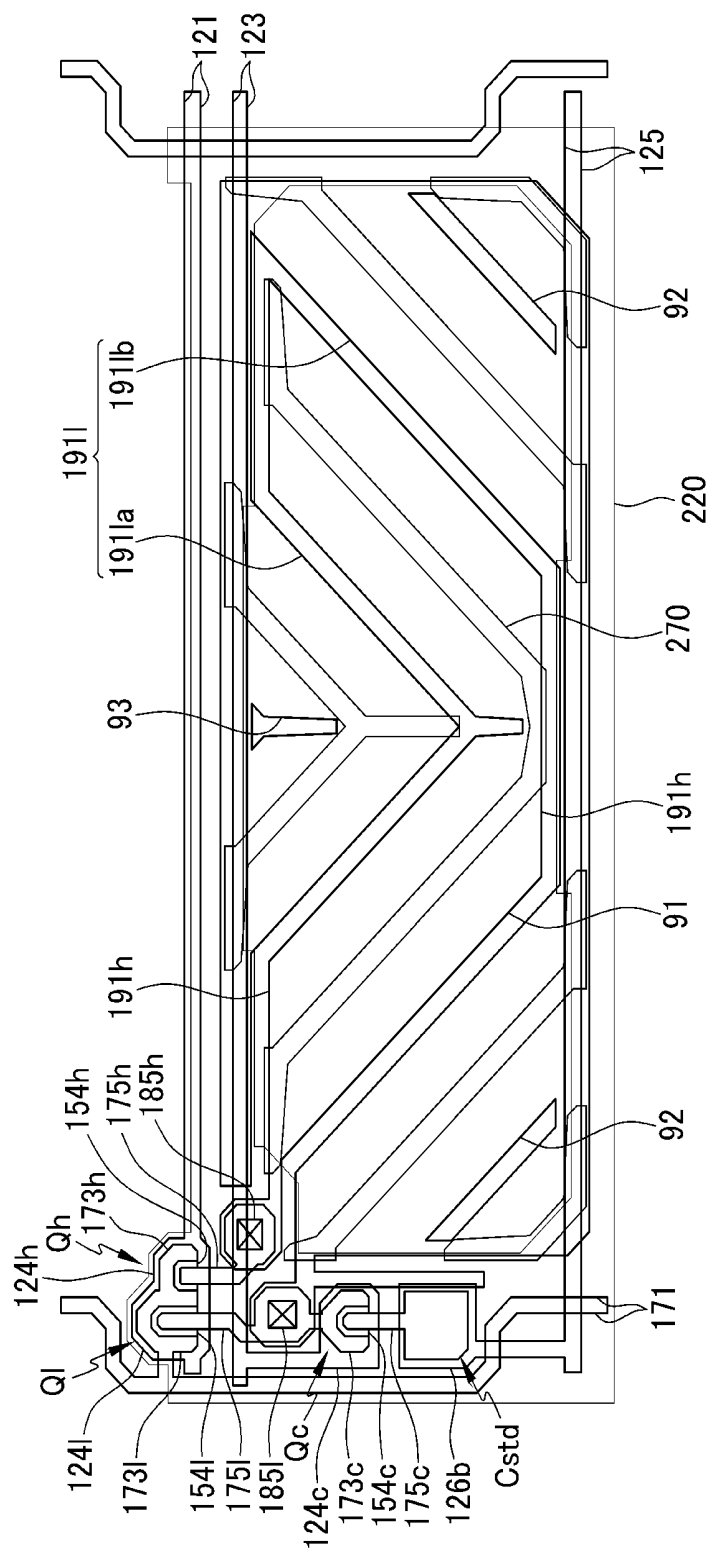


FIG. 12



LIQUID CRYSTAL DISPLAY AND DRIVING METHOD THEREOF

[0001] This application is a continuation of U.S. patent application Ser. No. 12/985,404, filed on Jan. 6, 2011, which claims priority to Korean Patent Application No. 10-2010-0089405, filed on Sep. 13, 2010, and all the benefits accruing therefrom under 35 U.S.C. §119, the content of which in its entirety is herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] (a) Field of the Invention

[0003] The present invention generally relates to a liquid crystal display and a driving method thereof.

[0004] (b) Description of the Related Art

[0005] A liquid crystal display ("LCD") is a widely used type of flat panel displays. The LCD typically includes two sheets of display panels which a field generating electrode, such as a pixel electrode and a common electrode, for example, is formed thereon and a liquid crystal layer is formed therebetween. The LCD generates an electric field in a liquid crystal layer by applying voltage to a field generating electrode, determines a direction of liquid crystal molecules of a liquid crystal layer, and controls polarization of incident light, thereby displaying images.

[0006] An LCD generally includes a pixel including a switching element constituted by a thin film transistor ("TFT") that is a three-terminal element, a display panel including a display signal line such as a gate line and a data line, for example.

[0007] A liquid crystal layer typically includes a liquid crystal material having refractive anisotropy. Due to the refractive anisotropy of the liquid crystal material, a change in color and a change in contrast become substantially large according to a viewing angle. Thus, when a viewing angle is smaller, side visibility may be substantially degraded compared with front visibility. In order to solve the problem, a method of dividing one pixel electrode into two sub-pixel electrodes and applying different voltages to the two sub-pixel electrodes, for example, has been proposed. Each sub-pixel electrode is connected to a first switching element that switches applied voltage.

[0008] In order to apply different voltages to the two sub-pixel electrodes, one of two sub-pixel electrodes is connected to a transformation capacitor through a second switching element that is a three terminal element.

[0009] The first switching element and the second switching element may be controlled using a gate line. However, when a period where the first switching element is turned-on and a period where the second switching element is turned-on overlap with each other, there may be a problem of charging the sub-pixel electrode connected to the second switching element. Further, when signal lines other than gate lines are implemented on a display panel to control the second switching element, transmittance of the display panel is reduced, such that there is a problem of substantially degrading a value of commodities.

BRIEF SUMMARY OF THE INVENTION

[0010] The present invention has been made in an effort to provide a liquid crystal display ("LCD") and a driving method thereof capable of substantially improving visibility while securing transmittance in the LCD wherein one pixel of the LCD includes two sub-pixels.

[0011] An exemplary embodiment of the present invention provides an LCD including a plurality of gate lines including a first gate line, a transformation gate line, and a second gate line; a data line; a pixel wherein the pixel includes a first liquid crystal capacitor including a first sub-pixel electrode and a common electrode and a second liquid crystal capacitor including a second sub-pixel electrode and a common electrode; a first switching element connected to the first gate line, the data line, and the first sub-pixel electrode; a second switching element connected to the first gate line, the data line, and the second sub-pixel electrode; a third switching element connected to the transformation gate line and the second switching element; a transformation capacitor including a first terminal connected to the second gate line and a second terminal connected to the third switching element; and a first period where a gate-on voltage V_{on} is applied to the first gate line and a second period where the gate-on voltage V_{on} is applied to the transformation gate line do not overlap each other, and a gate-off voltage V_{off} is applied to the second gate line during the second period.

[0012] In one exemplary embodiment, the second period may be subsequent to the first period within a frame period.

[0013] In one exemplary embodiment, the first switching element and the second switching element may be turned-on in the first period, such that the first liquid crystal capacitor and the second liquid crystal capacitor are charged to a first voltage.

[0014] In one exemplary embodiment, the third switching element may be turned-on in the second period, such that the second liquid crystal capacitor and the transformation capacitor share charge.

[0015] In one exemplary embodiment, the second liquid crystal capacitor may be charged to the second voltage after the second period.

[0016] In one exemplary embodiment, the second voltage may be substantially lower than the first voltage.

[0017] In one exemplary embodiment, the second gate line and the first gate line are consecutive gate lines.

[0018] In one exemplary embodiment, the second gate line may be a gate line previous to the first gate line.

[0019] In one exemplary embodiment, the second gate line may be a gate line subsequent to the first gate line.

[0020] In one exemplary embodiment, periods of consecutive gate lines of the plurality of gate lines to which the gate-on voltage V_{on} is each applied may overlap each other.

[0021] In one exemplary embodiment, a period where the gate-on voltage is applied to each of the plurality of gate lines may be $1H$ and the periods of the consecutive gate lines to which the gate-on voltage V_{on} is each applied may overlap by $\frac{2}{3}H$.

[0022] In one exemplary embodiment, the first gate line may be an i -th gate line, the second gate line may be an $i-1$ -th gate line, and the transformation gate line may be an $i+4$ -th gate line.

[0023] In one exemplary embodiment, the first gate line may be an i -th gate line, the second gate line may be an $i+1$ -th gate line, the transformation gate line may be an $i+4$ -th gate line.

[0024] In one exemplary embodiment, a gate signal applied to the plurality of gate lines may be generated based on first to sixth clock signals and the first to sixth clock signals may have a $2H$ period and sequentially have a phase difference of about 60° .

[0025] Another exemplary embodiment according to the present invention provides a driving method of an LCD including a plurality of gate lines including a first gate line, a transformation gate line, and a second gate line; a data line, and a pixel, wherein the pixel includes a first liquid crystal capacitor including a first sub-pixel electrode and a common electrode and a second liquid crystal capacitor including a second sub-pixel electrode and a common electrode; a first switching element connected to the first gate line, the data line, and the first sub-pixel electrode; a second switching element connected to the first gate line, the data line, and the second sub-pixel electrode; a third switching element connected to the transformation gate line and the second switching element; a transformation capacitor including a first terminal connected to the second gate line and a second terminal connected to the third switching element, the method including applying gate-on voltage V_{on} to a first gate line to charge the first liquid crystal capacitor and the second liquid crystal capacitor to a first voltage and the second liquid crystal capacitor; applying the gate-on voltage V_{on} to the transformation gate line to allow the second liquid crystal capacitor and the transformation capacitor to share charge; and applying gate-off voltage V_{off} to the transformation gate line to charge the second liquid crystal capacitor to the second voltage, wherein a second period where the gate-on voltage V_{on} is applied to the transformation gate line starts after the first period where the gate-on voltage V_{on} is applied to the first gate line is completed, and the gate-off voltage V_{off} is applied to the second gate line in the second period.

[0026] In one exemplary embodiment, the second voltage may be substantially lower than the first voltage.

[0027] In one exemplary embodiment, the second gate line may be a gate line continued to the first gate line.

[0028] In one exemplary embodiment, periods of consecutive gate lines of the plurality of gate lines to which the gate-on voltage V_{on} is applied may overlap each other.

[0029] The exemplary embodiments according to the present invention provide the LCD capable of securing the transmittance, substantially improving the visibility, and securing a gate driving margin and the driving method thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The above and other aspects, advantages and features of this disclosure will become more apparent by describing in further detail embodiments thereof with reference to the accompanying drawings, in which:

[0031] FIG. 1 is a block diagram of an exemplary embodiment of a liquid crystal display ("LCD") according to the present invention;

[0032] FIG. 2 is an equivalent circuit diagram showing an exemplary embodiment of a structure and two sub-pixels of the LCD according to the present invention;

[0033] FIG. 3 is a block diagram of an exemplary embodiment of a gate driver according to the present invention;

[0034] FIG. 4 is a waveform diagram of a clock signal input to the gate driver;

[0035] FIG. 5 is a waveform diagram of a gate signal output from the gate driver;

[0036] FIG. 6 is an equivalent circuit diagram of an exemplary embodiment of one pixel of the LCD according to the present invention;

[0037] FIG. 7 is a waveform diagram showing an exemplary embodiment of a gate signal V_{g1} of a first signal line

121, a gate signal V_{gc} of a transformation gate line 123, and a gate signal V_{g2} of a second gate line 125 in the LCD shown in FIG. 6;

[0038] FIG. 8 is a waveform diagram showing a data voltage V_d , voltages V_h and V_l of first and second sub-pixel electrodes 191h and 191l, and a first terminal voltage V_c of a transformation capacitor C_{std} when applying the gate signal V_{g1} of the first gate line 121, the gate signal V_{gc} of the transformation gate line 123, and the gate signal V_{g2} of the second gate line 125 as shown in FIG. 7, in the LCD device shown in FIG. 6;

[0039] FIG. 9 is a schematic view showing an exemplary embodiment of a disposition of the LCD shown in FIG. 6;

[0040] FIG. 10 is a cross-sectional view of an LCD taken along line X-X of FIG. 9;

[0041] FIG. 11 is an equivalent circuit diagram of another exemplary embodiment of one pixel of an LCD according to the present invention; and

[0042] FIG. 12 is a schematic view showing an exemplary embodiment of a disposition of the LCD shown in FIG. 11.

DETAILED DESCRIPTION OF THE INVENTION

[0043] The present invention will be described more fully hereinafter with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. As those skilled in the art would realize, the described embodiments may be modified in various different ways, all without departing from the spirit or scope of the present invention.

[0044] In the drawings, the thickness of layers, films, panels, regions, etc., may be exaggerated for clarity. Like reference numerals designate like elements throughout the specification. It will be understood that when an element such as a layer, film, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

[0045] It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0046] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting. As used herein, the singular forms "a," "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0047] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another element as

illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures. For example, if the device in one of the figures is turned over, elements described as being on the “lower” side of other elements would then be oriented on “upper” sides of the other elements. The exemplary term “lower,” can therefore, encompass both an orientation of “lower” and “upper,” depending on the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as “below” or “beneath” other elements would then be oriented “above” the other elements. The exemplary terms “below” or “beneath” can, therefore, encompass both an orientation of above and below.

[0048] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0049] Embodiments are described herein with reference to cross section illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments described herein should not be construed as limited to the particular shapes of regions as illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present claims.

[0050] Hereinafter, an exemplary embodiment of a liquid crystal display (“LCD”) according to the present invention will be described with reference to FIGS. 1 and 2.

[0051] FIG. 1 is a block diagram of an exemplary embodiment of an LCD according to the present invention, and FIG. 2 is an equivalent circuit diagram showing a structure and two sub-pixels of the LCD according to the present invention.

[0052] Referring to FIG. 1, an exemplary embodiment of the LCD according to the present invention includes a liquid crystal panel assembly 300, a gate driver 400, and a data driver 500.

[0053] The liquid crystal panel assembly 300 includes a plurality of signal lines G1-Gn and D1-Dm and a plurality of pixels PX connected thereto and arranged in a substantially matrix form, e.g., arranged in pixel rows and pixel columns.

[0054] As shown in FIG. 2, the liquid crystal panel assembly 300 includes a lower display panel 100 and an upper display panel 200 that face each other and a liquid crystal layer 3 interposed therebetween.

[0055] The plurality of signal lines G1-Gn and D1-Dm is provided in the lower display panel 100 and includes gate lines G1-Gn and data lines D1-Dm transferring data voltage.

[0056] Each of the plurality of pixels pixel PX such as a pixel PX connected to an i-th (where i=1, 2, . . . , n) gate line Gi and a j-th (where j=1, 2, . . . , m) data line Dj, includes first

and second sub-pixels, and the first and second sub-pixels each include first and second liquid crystal capacitors Clch and Clcl. The first and second sub-pixels further include a switching element (not shown) connected to the gate lines G1-Gn and the data lines D1-Dm.

[0057] The first and second liquid crystal capacitors Clch and Clcl use first and second sub-pixel electrodes 191h and 191l of the lower display panel 100 and a common electrode 270 of the upper display panel 200 as two terminals, respectively, and the liquid crystal layer 3 between the first and second sub-pixel electrodes 191h and 191l and the common electrode 270 serves as a dielectric layer. The first and second sub-pixel electrodes 191h and 191l are isolated from each other and form one pixel electrode. The common electrode 270 is disposed on the upper display panel 200 and receives a common voltage Vcom. The liquid crystal layer 3 has negative dielectric anisotropy and liquid crystal molecules of the liquid crystal layer 3 may be aligned so that a major axis thereof is substantially vertical to surfaces of the two display panels 100 and 200, in a state where there is no electric field. In one exemplary embodiment, unlike the exemplary embodiment of FIG. 2, the common electrode 270 may be disposed on the lower display panel 100.

[0058] Meanwhile, in order to implement color display, the pixel PX inherently displays one of primary colors (i.e., spatial division) or each pixel PX alternately displays primary colors over time (i.e., temporal division), such that a desired color is recognized by a spatial and temporal sum of the primary colors. An exemplary embodiment of the primary colors may include three primary colors, such as red, green, and blue, for example. As an exemplary embodiment of the spatial division, FIG. 2 shows the exemplary embodiment where each pixel PX includes a color filter 230 displaying one of the primary colors in a region of the upper display panel 200. In one exemplary embodiment, unlike the exemplary embodiment of FIG. 2, the color filter 230 may be formed on or under the sub-pixel electrode 191h and 191l of the lower display panel 100.

[0059] A pair of polarizers (not shown) may be provided on an outer surface of the display panels 100 and 200, respectively, wherein polarization axes of the polarizers may be orthogonal to each other.

[0060] Referring back to FIG. 1, the data driver 500 is connected to the data lines D1-Dm of the liquid crystal panel assembly 300 and applies data voltage to the data lines D1-Dm.

[0061] The gate driver 400 is connected to the gate lines G1-Gn of the liquid crystal panel assembly 300 and applies a gate signal consisting of a combination of a gate-on voltage Von capable of turning-on a switching element and a gate-off voltage Voff capable of turning-off the switching element to the gate lines G1 to Gn.

[0062] FIG. 3 is a block diagram of an exemplary embodiment of a gate driver 400, and FIG. 4 is a waveform diagram of an exemplary embodiment of a clock signal input to the gate driver 400, and FIG. 5 is a waveform diagram of an exemplary embodiment of a gate signal output from the gate driver according to the present invention.

[0063] Referring to FIG. 3, the gate driver 400 is a shift register including a plurality of stages 410 each connected to gate lines G1, . . . , Gi-1, Gi, . . . , Gi+4, . . . , respectively. The plurality of stages 410 receives clock signals CK1, CK2, CK3, CK1B, CK2B, and CK3B and outputs gate signals [G1, . . . , Gi-1, . . . , Gi+4, . . .].

[0064] For convenience of explanation, FIG. 3 shows only the clock signals as a signal received in the plurality of stages, but the plurality of stages may receive a scanning start signal STV, gate-off voltage Voff, and various other signals, in addition to the clock signals.

[0065] Referring to FIG. 4, a magnitude of voltage corresponding to a high level of the clock signals CK1, CK2, CK3, CK1B, CK2B, and CK3B is the same as the gate-on voltage Von and a magnitude of voltage corresponding to a low level is the same as the gate-off voltage Voff. The clock signals CK1, CK2, CK3, CK1B, CK2B, and CK3B have a duty ratio of about 50 percent (%) and a period of 2H and sequentially have a phase difference of about 60 degrees($^{\circ}$). The clock signals CK1, CK2, and CK3 and the clock signals CK1B, CK2B, and CK3B have a phase difference of about 180 $^{\circ}$.

[0066] Referring back to FIG. 3, the stages [ST(i-1), ST(i), . . . , ST(i+4)] receive the clock signals CK1, CK2, CK3, CK1B, CK2B, and CK3B. In other words, a subsequent stage receives a clock signal delayed by about 60 $^{\circ}$ compared to a clock signal received in a previous stage. The plurality of stages 410 generates the gate signal based on the input clock signal.

[0067] Referring to FIG. 5, the i-1-th stage [ST(i-1)] to i+4-th stage [ST(i+4)] sequentially generate the gate signals [Gi-1, . . . , Gi+4]. The generated gate signals [Gi-1, . . . , Gi+4] each have a width of 1H in a high period where the gate-on voltage Von is applied, and a high period of the subsequent gate signal overlaps by $\frac{1}{3}$ H with a high period of the previous gate signal.

[0068] When the gate-on voltage Von is applied to the i+1-th gate line Gi+1 during a first $\frac{1}{3}$ H part of the 1H period, the gate-on voltage Von is also applied to the i-1-th gate line Gi-1 and i-th gate line Gi. In this case, the data voltage of the pixel connected to the i-1-th gate line Gi-1 is applied to the data line. Therefore, the data voltage of other pixels is previously charged in the pixel connected to the i-th gate line Gi and the pixel connected to the i+1-th gate line Gi+1.

[0069] When the gate-on voltage Von is applied to the i+1-th gate line Gi+1 during a second $\frac{1}{3}$ H part of the 1H period, the gate-on voltage Von is also applied to the i-th gate line Gi and i+2-th gate line Gi+2. In this case, the data voltage of the pixel connected to the i-th gate line Gi is applied to the data line. Therefore, the data voltage of the other pixel is previously charged in the pixel connected to the i+1-th gate line Gi+1 and the pixel connected to the i+2-th gate line Gi+2.

[0070] When the gate-on voltage Von is applied to the i+1-th gate line Gi+1 during a last $\frac{1}{3}$ H part of the 1H period, the gate-on voltage Von is also applied to the i+2-th gate line Gi+2 and the i+3-th gate line Gi+3. In this case, the data voltage of the pixel connected to the i+1-th gate line Gi+1 is applied to the data line. Therefore, the pixel connected to the i+1-th gate line Gi+1 charges its own data voltage.

[0071] In other words, the pixel connected to the i+1-th gate line Gi+1 previously charges the data voltage of the other pixel during a first $\frac{2}{3}$ H part of the 1H period where the gate-on voltage Von is applied to the i+1-th gate line Gi+1, and charges its own data voltage during the last $\frac{1}{3}$ H part of the 1H period.

[0072] As described above, the data voltage of the other pixels may be applied to the pixel as a previous charge voltage during a predetermined time prior to applying the data voltage to the pixel by overlapping a period where the gate-on voltage is applied to the consecutive gate lines. The liquid crystal molecules are already aligned to some degree by previously

charging the liquid crystal capacitor of the pixel. Thereby, the difference between a current voltage and a targeted voltage of the liquid crystal capacitor becomes relatively small, thereby making it possible to reach the targeted voltage within a substantially short time.

[0073] FIGS. 3 to 5 show the exemplary embodiment of an overlapping period of $\frac{2}{3}$ H where the gate-on voltage Von is applied to consecutive gate lines, but the overlapping period is not limited thereto. In one exemplary embodiment, unlike the above mentioned exemplary embodiment, periods of the consecutive gate lines to which the gate-on voltage Von is applied may not overlap with each other.

[0074] The exemplary embodiment of the LCD according to the present invention will be further described with reference to FIG. 6 together with FIGS. 1 and 2 described above.

[0075] FIG. 6 is an equivalent circuit diagram for an exemplary embodiment of one pixel of the LCD according to the present invention.

[0076] Referring to FIG. 6, the exemplary embodiment of the LCD according to the present invention includes a signal line including a first gate line 121, a transformation gate line 123, a second gate line 125, and a data line 171 and the plurality of pixels PX connected thereto.

[0077] The pixel PX includes a first switching element Qh, a second switching element Ql, a third switching element Qc, a first liquid crystal capacitor Clch, a second liquid crystal capacitor Clcl, and a transformation capacitor Cstd.

[0078] The first switching element Qh and the second switching element Ql may be a three terminal element, such as a thin film transistor ("TFT"), for example, included in the lower display panel 100. A control terminal thereof is connected to the first gate line 121, an input terminal is connected to the data line 171, and an output terminal of the first switching element Qh is connected to the first liquid crystal capacitor Clch and an output terminal of the second switching element Ql is connected to the second liquid crystal capacitor Clcl, respectively.

[0079] The third switching element Qc is also a three terminal element such as a TFT, for example, included in the lower display panel 100. A control terminal is connected to the transformation gate line 123, and an input terminal is connected to the output terminal of the second switching element Ql, and an output terminal is connected to the transformation capacitor Cstd.

[0080] The transformation capacitor Cstd is connected to the output terminal of the third switching element Qc and the second gate line 125, and is formed by overlapping the second gate line 125 and the output terminal of the third switching element Qc, having an insulator therebetween.

[0081] The first liquid crystal capacitor Clch and the second liquid crystal capacitor Clcl were already described above and therefore, the detailed description thereof may be omitted.

[0082] The exemplary embodiment of the operation of the LCD according to the present invention will be described with reference to FIG. 7 together with FIGS. 1 to 6 described above.

[0083] FIG. 7 is a waveform diagram showing an exemplary embodiment of a gate signal Vg1 of a first signal line 121, a gate signal Vgc of the transformation gate line 123, and a gate signal Vg2 of a second gate line 125 in the embodiment of the LCD shown in FIG. 6.

[0084] Referring to FIG. 7, a period where the gate signal Vg1 of the first gate line 121 is the gate-on voltage Von and a

period where the gate signal V_{g2} of the second gate line 125 is the gate-on voltage V_{on} overlap each other by $\frac{1}{3}H$. The gate signal V_{g1} applied to the first gate line 121 is converted into the gate-off voltage V_{off} , then after $\frac{1}{3}H$, the gate signal V_{gc} applied to the transformation gate line 123 becomes the gate-on voltage V_{on} . In other words, the period where the gate-on voltage V_{on} is applied to the first gate line 121 and the period where the gate-on voltage V_{on} is applied to the transformation gate line 123 do not overlap each other. The gate-off voltage V_{off} is applied to the second gate line 125 during the period where the gate-on voltage V_{on} is applied to the transformation gate line 123.

[0085] In one exemplary embodiment, the first gate line 121, the second gate line 125, and the transformation gate line 123 may be the i -th gate line G_i , the $i-1$ -th gate line G_{i-1} , the $i+4$ -th gate line G_{i+4} of FIG. 3, respectively. In the above mentioned exemplary embodiment, the gate signals V_{g1} , V_{g2} , and V_{gc} each are the gate signals $[G_i, G_{i-1}, G_{i+4}]$ of FIG. 5, respectively.

[0086] When the gate signal V_{g1} applied to the first gate line 121 becomes the gate-on voltage V_{on} , the first switching element Q_h and the second switching element Q_l connected thereto are turned-on.

[0087] Therefore, the data voltage of the data line 171 is similarly applied to the first and second sub-pixel electrodes 191 h and 191 l through the turned-on first and second switching elements Q_h and Q_l . Since the first and second liquid crystal capacitors Cl_{ch} and Cl_{cl} are charged by the difference between the common voltage V_{com} of the common electrode 270 and a voltage of the first and second sub-pixel electrodes 191 h and 191 l , such that a charging voltage of the first liquid crystal capacitor Cl_{ch} and a charging voltage of the second liquid crystal capacitor Cl_{cl} are also equal to each other. In this case, the gate signal V_{gc} applied to the transformation gate line 123 is the gate-off voltage V_{off} .

[0088] When the gate signal V_{g1} applied to the first gate line 121 becomes the gate-off voltage V_{off} , the first and second switching elements Q_h and Q_l connected to the first gate line 121 turned-off and the first liquid crystal capacitor Cl_{ch} and the second liquid crystal capacitor Cl_{cl} is fully charged with voltage.

[0089] The gate signal V_{g1} applied to the first gate line 121 is converted into the gate-off voltage V_{off} , then after $\frac{1}{3}H$, the gate signal V_{gc} applied to the transformation gate line 123 is the gate-on voltage V_{on} and the third switching element Q_c is turned-on.

[0090] While the gate signal V_{gc} applied to the transformation gate line 123 is the gate-on voltage V_{on} , the second sub-pixel electrode 191 l is connected to the first terminal of the transformation capacitor C_{std} through the turned-on third switching element Q_c . In this case, the gate signal V_{g2} applied to the second gate line 125 becomes the gate-off voltage, such that the second terminal of the transformation capacitor C_{std} maintains the gate-off voltage V_{off} .

[0091] Therefore, the charge of the second sub-pixel electrode 191 l connected to the output terminal of the second switching element Q_l flows into the transformation capacitor C_{std} , such that the voltage of the second liquid crystal capacitor Cl_{cl} falls. As described above, the second liquid crystal capacitor Cl_{cl} and the transformation capacitor C_{std} share charge, such that the voltage of the second liquid crystal capacitor Cl_{cl} falls.

[0092] In particular, when the LCD is driven by a frame inversion, an exemplary embodiment where the data voltage

having the positive (+) polarity with respect to the common voltage V_{com} is applied to the data line 171 in the current frame will be described by way of example. After the previous frame ends, a negative (-) charge is collected in the transformation capacitor C_{std} , such that a positive (+) charge of the second sub-pixel electrode 191 l flows into the transformation capacitor C_{std} through the third switching element Q_c and the negative (-) charge of the transformation capacitor C_{std} flows into the second sub-pixel electrode 191 l when the third switching element Q_c is turned-on in the current frame, thereby reducing a voltage of the second sub-pixel electrode 191 l . When the third switching element Q_c is turned-on in the state where a negative (-) charge is reversely changed in the second sub-pixel electrode 191 l in the subsequent frame, the negative (-) charge of the second sub-pixel electrode 191 l flows into the transformation capacitor C_{std} , such that the negative (-) charge is collected in the transformation capacitor C_{std} and the voltage of the second liquid crystal capacitor Cl_{cl} falls.

[0093] As described above, a side visibility of the LCD can be substantially improved by making the charging voltage of the first and second liquid crystal capacitors Cl_{ch} and Cl_{cl} different.

[0094] FIG. 8 is a waveform diagram showing a data voltage V_d , voltages V_h and V_l of first and second sub-pixel electrodes 191 h and 191 l , and a first terminal voltage V_c of a transformation capacitor C_{std} in the LCD device shown in FIG. 6 when applying the gate signal V_{g1} of the first gate line 121, the gate signal V_{gc} of the transformation gate line 123, and the gate signal V_{g2} of the second gate line 125 as shown in FIG. 7.

[0095] Referring to FIG. 8, the LCD is driven by the frame inversion. The data voltage V_d having a positive polarity with respect to the common voltage V_{com} is applied to the data line 171 based on the common voltage V_{com} in a n -th frame and the data voltage V_d having a negative polarity with respect to the common voltage V_{com} is applied to the data line 171 in a $n+1$ -th frame. In FIG. 8, the data voltage V_d maintains a consistent value during one frame but this is for convenience of explanation.

[0096] First, an operation at the n -th frame will be described.

[0097] Since the second terminal of the transformation capacitor C_{std} is connected to the second gate line 125, when the gate signal V_{g2} of the second gate line 125 is converted from the gate-off voltage V_{off} to the gate-on voltage V_{on} , the voltage V_c of the first terminal of the transformation capacitor C_{std} also rises by an increase in a voltage amplitude of the gate signal V_{g2} . In this case, the voltage V_c of the first terminal of the transformation capacitor C_{std} may be about 32V. When the gate signal V_{g2} is converted from the gate-on voltage V_{on} to the gate-off voltage V_{off} , the voltage V_c of the first terminal of the transformation capacitor C_{std} also falls by a decrease in a voltage amplitude of the gate signal V_{g2} . In this case, the gate-off voltage V_{off} may be between about -7V and about -8V.

[0098] Where the gate signal V_{g1} of the first gate line 121 is the gate-on voltage V_{on} , the voltages V_h and V_l of the first and second sub-pixel electrodes 191 h and 191 l are similarly converted into the data voltage V_d . The first and second liquid crystal capacitors Cl_{ch} and Cl_{cl} are charged by a difference between the common voltage V_{com} of the common electrode 270 and each of the voltages V_h and V_l of the first and second sub-pixel electrodes 191 h and 191 l .

[0099] When the gate signal V_{g1} of the first gate line 121 is converted into the gate-off voltage V_{off} , the voltage V_h of the first sub-pixel electrode 191 h slightly falls and the voltage thereof is then maintained. In this case, the voltage V_h of the first sub-pixel electrode 191 h may be about 14.1V.

[0100] When the gate signal V_{gc} applied to the transformation gate line 123 is converted into the gate-on voltage V_{on} , the second sub-pixel electrode 191 l is connected to the first terminal of the transformation capacitor C_{std} through the turned-on third switching element Q_c . The voltage V_l of the second sub-pixel electrode 191 l and the voltage V_c of the first terminal of the transformation capacitor C_{std} rise to be substantially equal to each other and the second liquid crystal capacitor C_{cl} and the transformation capacitor C_{std} share charge.

[0101] When the gate signal V_{gc} to the transformation gate line 123 is converted into the gate-off voltage V_{off} , the voltage V_l of the second sub-pixel electrode 191 l and the voltage V_c of the first terminal of the transformation capacitor C_{std} slightly fall and the voltage thereof is then maintained. In this case, the voltage V_l of the second sub-pixel electrode 191 l may be about 12.8V and the voltage V_c of the first terminal of the transformation capacitor C_{std} may be about 13.5V.

[0102] After the charge share of the second liquid crystal capacitor C_{cl} and the transformation capacitor C_{std} , the voltage charged in the second liquid crystal capacitor C_{cl} further falls than the voltage charged in the first liquid crystal capacitor C_{clh} .

[0103] Next, the operation at the $n+1$ -th frame will be described.

[0104] When the gate signal V_{g2} of the second gate line 125 is converted from the gate-off voltage V_{off} to the gate-on voltage V_{on} , the voltage V_c of the first terminal of the transformation capacitor C_{std} also rises by an increase in the voltage amplitude of the gate signal V_{g2} . In this case, the voltage V_c of the first terminal of the transformation capacitor C_{std} may be about 45V. When the gate signal V_{g2} is converted from the gate-on voltage V_{on} to the gate-off voltage V_{off} , the voltage V_c of the first terminal of the transformation capacitor C_{std} also falls by a decrease in the voltage amplitude of the gate signal V_{g2} .

[0105] While the gate signal V_{g1} of the first gate line 121 is the gate-on voltage V_{on} , the voltage V_h and V_l of the first and second sub-pixel electrodes 191 h and 191 l are similarly converted into the data voltage V_d .

[0106] When the gate signal V_{g1} of the first gate line 121 is converted into the gate-off voltage V_{off} , the voltage V_h of the first sub-pixel electrode 191 h slightly falls and the voltage thereof is then maintained. In this case, the voltage V_h of the first sub-pixel electrode 191 h may be about -0.86V.

[0107] When the gate signal V_{gc} applied to the transformation gate line 123 is converted into the gate-on voltage V_{on} , the voltage V_l of the second sub-pixel electrode 191 l rises and the voltage V_c of the first terminal of the transformation capacitor C_{std} falls, such that they are equal to each other.

[0108] When the gate signal V_{gc} to the transformation gate line 123 is converted into the gate-off voltage V_{off} , the voltage V_l of the second sub-pixel electrode 191 l and the voltage V_c of the first terminal of the transformation capacitor C_{std} slightly fall and the voltage thereof is then maintained. In this case, the voltage V_l of the second sub-pixel electrode 191 l may be about 0.63V and the voltage V_c of the first terminal of the transformation capacitor C_{std} may be about 0.77V.

[0109] After the charge of the second liquid crystal capacitor C_{cl} and the transformation capacitor C_{std} is shared, the voltage charged in the second liquid crystal capacitor C_{cl} further falls than the voltage charged in the first liquid crystal capacitor C_{clh} .

[0110] Next, the LCD and the manufacturing method thereof according to the exemplary embodiment of the present invention will be described with reference to FIGS. 9 and 10.

[0111] FIG. 9 is a schematic view showing an exemplary embodiment of a disposition of the LCD shown in FIG. 6 and FIG. 10 is a cross-sectional view of the LCD taken along line X-X of FIG. 9.

[0112] The present exemplary embodiment of the LCD according to the present exemplary embodiment includes the lower display panel 100 and the upper display panel 200 that faces each other and the liquid crystal layer 3 inserted between two display panels 100 and 200. The polarizer (not shown) may be provided on the outer surfaces of the display panels 100 and 200.

[0113] First, the lower display panel 100 will be further described.

[0114] A plurality of gate conductors including the plurality of the first gate lines 121, the plurality of transformation gate lines 123, and the second gate lines 125 are formed on the insulating substrate 110.

[0115] The first gate line 121, the second gate line 125, and the transformation gate line 123 mainly extend in a substantially horizontal direction and transfer the gate signals. The first gate line 121 includes a first gate electrode 124 h and a second gate electrode 124 l substantially vertically protruded and the transformation gate line 123 includes a third gate electrode 124 c protruded up. The first gate electrode 124 h and the second gate electrode 124 l are connected to each other, thereby forming one protruding portion.

[0116] The second gate line 125 includes an extending portion 126 b protruded down.

[0117] A gate insulating layer 140 is disposed on the gate conductors 121, 123, and 125.

[0118] A plurality of linear semiconductors 151 including amorphous or crystalline silicon, for example, are formed on the gate insulating layer 140. The linear semiconductor 151 includes first and second semiconductors 154 h and 154 l that mainly extend in a substantially vertical direction, extend toward the first and second gate electrodes 124 h and 124 l , and are connected to each other and a third semiconductor 154 c that is connected to the second semiconductor 154 l .

[0119] A plurality of linear ohmic contacts 161 is disposed on the linear semiconductor 151, a pair of ohmic contacts 163 h and 165 h is formed on the first semiconductor 154 h , and a pair of ohmic contacts 163 l and 165 l is formed on the second semiconductor 154 l . A pair of ohmic contacts (not shown) is also formed on the third semiconductor 154 c . The ohmic contacts 163 l and 163 h are connected to the ohmic contact stripe 161.

[0120] Data conductors including the plurality of data lines 171, a plurality of first drain electrodes 175 h , a plurality of second drain electrode 175 l , a plurality of third source electrodes 173 c , and the plurality of third drain electrodes 175 c are formed on the ohmic contacts 161, 165 h , and 165 l , respectively.

[0121] The data line 171 intersects with the first gate line 121, the second gate line 125, and transformation gate line 123, transfers the data signals and mainly extends in a vertical

direction. Each data line **171** includes a first source electrode **173h** and a second source electrode **173l** extending toward the first gate electrode **124h** and the second gate electrode **124l**. The first source electrode **173h** and the second source electrode **173l** are connected to each other.

[0122] The first drain electrode **175h**, the second drain electrode **175l**, and the third drain electrode **175c** include a wide one end portion and the other end portion that is a substantially bar shape. The bar-shaped end portion of the first drain electrode **175h** and the second drain electrode **175l** are each surrounded partially by the first source electrode **173h** and the second source electrode **173l**, and the third drain electrode **175c** is partially surrounded by the third source electrode **173c**. The wide one end portion of the second drain electrode **175l** is connected to the third source electrode **173c**. The wider end portion of the third drain electrode **175c** overlaps with the extending portion **126b** of the second gate line **125** to form the transformation capacitor Cstd.

[0123] The first/the second/the third gate electrodes **124h/124l/124c**, the first/the second/the third source electrodes **173h/173l/173c**, and the first/the second/the third drain electrodes **175h/175l/175c** forms one switching elements Qh/Ql/Qc that are first/the second/the third TFTs together with the first/the second/the third semiconductors **154h/154l/154c** and a channel of the TFT is formed in each of the semiconductors **154h/154l/154c** between each of the source electrodes **173h/173l/173c** and each of the drain electrodes **175h/175l/175c**.

[0124] The linear semiconductor **151** including the semiconductors **154h**, **154l**, and **154c** has a substantially same plane shape as that of the data conductors **171**, **175h**, **175l**, and **175c** and the ohmic contacts **161**, **165h** and **165l** thereunder, except for a channel region between the source electrodes **173h**, **173l**, and **173c** and the drain electrodes **175h**, **175l**, and **175c**. In other words, an exposed portion while not being covered by the data conductors **171**, **175h**, **175l**, and **175c** is provided between the source electrodes **173h**, **173l**, and **173c** and the drain electrodes **175h**, **175l**, and **175c**, in the linear semiconductor **151** including the semiconductor **154h**, **154l**, and **154c**.

[0125] A passivation layer **180** is disposed on the data conductors **171**, **175h**, **175l**, and **175c** and the exposed semiconductors **154h**, **154l**, and **154c**.

[0126] A plurality of contact holes **185h** and **185l** exposing each of the wide end portion of the first drain electrode **175h** and the wide end portion of the second drain electrode **175l** is formed on the passivation layer **180**.

[0127] A pixel electrode **191** is disposed on the passivation layer **180**.

[0128] Generally, the pixel electrode **191** is an approximately quadrangle shape and includes first and second sub-pixel electrodes **191h** and **191l** connected to each other, having a gap **91** therebetween. The first sub-pixel electrode **191h** is inserted in a substantially center portion of the second sub-pixel electrode **191l** and the gap **91** includes one vertical portion and two pair of oblique line portions positioned up and down based a virtual horizontal central line.

[0129] The second sub-pixel electrode **191l** includes a central electrode **191a** and an upper electrode **191b**. The central electrode **191a** includes a cutout portion **93** formed in a center thereof in an approximate bar-shape and the upper electrode **191b** includes a cutout portion **92**.

[0130] Sides forming an oblique line portion of the gap **91** and a cutout portion **92** may be oblique to the first gate line

121 and the transformation gate lines **123** and the second gate line **125**, that is, form an angle of approximately 45°.

[0131] A number of cutout portions may be changed according to design factors, such as a length ratio of the horizontal side and the vertical side of the pixel electrode **191**, the kind or characteristics of the liquid crystal layer **3**.

[0132] An area of the second sub-pixel electrode **191l** may be approximately 1.0 times or 2.2 times larger than an area of the first sub-pixel electrode **191h**.

[0133] The first sub-pixel electrode **191h** receives the data voltage from the first drain electrode **175h** through the contact hole **185h** and the second sub-pixel electrode **191l** receives the data voltage from the second drain electrode **175l** through the contact hole **185l**.

[0134] An alignment layer **11** is formed on the first and second sub-pixel electrodes **191h** and **191l** and passivation layer **180**. In one exemplary embodiment, the alignment layer **11** may be a vertical alignment layer.

[0135] Next, the upper display panel **200** will be further described.

[0136] A light blocking member **220** and a plurality of color filters **230**, which are called a black matrix, are formed on the insulation substrate **210** and an overcoat **250** is formed on the light blocking member **220** and the color filter **230**.

[0137] The common electrode **270** made of a transparent conductor or a metal such as indium-tin-oxide (ITO) and indium-zinc-oxide (IZO) may be formed on the cover layer **250** and an alignment layer **21** may be formed thereon. In one exemplary embodiment, the alignment layer **21** may be a substantially vertical alignment layer.

[0138] The liquid crystal layer **3** inserted between the lower display panel **100** and the upper display panel **200** includes the liquid crystal molecule including the dielectric anisotropy and the liquid crystal molecules may be aligned so that a major axis of the liquid crystal molecule is substantially vertical to the surfaces of the two display panels **100** and **200** in the state where there is no electric field.

[0139] The first and second sub-pixel electrodes **191h** and **191l** to which the data voltage is applied generate the electric field together with the common electrode **270** of the upper display panel **200**, thereby determining the direction of the liquid crystal molecule of the liquid crystal layer **3** between two electrodes **191** and **270**. A change of a degree of polarization of light incident into the liquid crystal layer **3** is changed according a slope of the liquid crystal molecule. The change in polarization represents a change in transmittance according to the polarizer, such that the LCD displays images.

[0140] The first sub-pixel electrode **191h** and the common electrode **270** form the first liquid crystal capacitor Clch together with the liquid crystal layer **3** therebetween and the second sub-pixel electrode **191l** and the common electrode **270** form the second liquid crystal capacitor Clcl together with the liquid crystal layer **3** therebetween, thereby maintaining the applied voltage even after the first and second switching elements Qh and Ql are turned-off.

[0141] After the first and second switching elements Qh and Ql are turned-off, the third switching element Qc is turned-on such that the second liquid crystal capacitor Clcl is connected to the transformation capacitor Cstd, thereby reducing the voltage of the second liquid crystal capacitor Clcl. When the voltage of the first liquid crystal capacitor Clch and the voltage of the second liquid crystal capacitor Clcl are different from each other, luminance is also different and when the voltage of the first and second liquid crystal

capacitors Clch and Clcl is properly matched, the side visibility can be substantially improved.

[0142] As shown in FIG. 7, the first gate line 121 and the second gate line 125 is the i-th gate line Gi and the i-1-th gate line Gi-1 of FIG. 3 and the transformation gate line 123 may be connected to the i+4-th gate line Gi+4. However, the present exemplary embodiment does not limit the first gate line 121, the second gate line 125, and the transformation gate line 123.

[0143] After the charging is completed in the second liquid crystal capacitor Clcl by the difference between the data voltage and the common voltage Vcom of the pixel PX common voltage, the third switching element Qc should be turned-on. Therefore, the first period where the gate-on voltage Von is applied to the first gate line 121 and the second period where the gate-on voltage Von is applied to the transformation gate line 123 do not overlap each other. In addition, the second period is preceded by the first period within the frame period. In the second period, the second gate line 125 is applied with the gate-off voltage Voff. In one exemplary embodiment, the second gate line 125 may be the gate line continued to the first gate line 121. In other words, the second gate line 125 may be the gate line immediately after the first gate line 121 or the gate immediately before the first gate line 121.

[0144] As shown in FIG. 5, when the periods where the gate-on voltage Von is applied to the consecutive gate lines overlap by $\frac{2}{3}H$, if the first gate line 121 is the i-th gate line Gi, the transformation gate line 123 may be one of the i+3-th gate line Gi+3 and the gate line subsequent to the i+3-th gate line Gi+3. If the periods where the gate-on voltage Von is applied to the consecutive gate lines do not overlap, the transformation gate line 123 may be the gate line just subsequent to the first gate line 121. As described above, a gate line that does not overlap with the first gate line 121 while being subsequent to the first gate line 121 may be used as the transformation gate line 123. The gate line to which the gate-off voltage Voff is applied may be the second gate line 125 during the second period where the gate-on voltage Von is applied to the transformation gate line 123. As shown in FIG. 5, when the periods where the gate-on voltage Von is applied to the consecutive gate lines overlap by $\frac{2}{3}H$, the first gate line 121 is the i-th gate line Gi and the transformation gate line 123 is the i+4-th gate line Gi+4, the second gate line 125 may be the i-1-th gate line Gi-1 or the i+1-th gate line Gi+1.

[0145] FIG. 11 is an equivalent circuit diagram of another exemplary embodiment of one pixel of an LCD according to the present invention.

[0146] FIG. 6 shows the exemplary embodiment where the gate line prior to the first gate line 121 is used as the second gate line 125 and FIG. 11 shows an exemplary embodiment where the gate line subsequent to the first gate line is used as the second gate line 125. Except for this, the exemplary embodiment shown in FIG. 11 is substantially same as the exemplary embodiment shown in FIG. 6 and the detailed description thereof will be omitted.

[0147] When the first gate line 121 is the i-th gate line Gi, for example, the second gate line 125 may be the i+1-th gate line Gi+1. As shown in FIG. 5, when the periods where the gate-on voltage Von is applied to the consecutive gate lines overlap by $\frac{2}{3}H$, the transformation gate line 123 may be the i+4-th gate line Gi+4.

[0148] FIG. 12 is a schematic view showing an exemplary embodiment of a disposition of the LCD shown in FIG. 11.

[0149] The exemplary embodiment of FIG. 12 is substantially same as the exemplary embodiment of FIG. 9 except that the disposition diagram of FIG. 9 is inverted up and down and therefore, the detailed description thereof will be omitted.

[0150] As described above, according to the exemplary embodiments of the present invention, the LCD and the driving method thereof can substantially improve the visibility and secure a gate driving margin while securing the transmittance.

[0151] The first period where the gate-on voltage Von is applied to the first gate line 121 and the second period where the gate-on voltage Von is applied to the transformation gate line 123 do not overlap each other, such that the second liquid crystal capacitor Clcl and the transformation capacitor Cstd can share charge and the voltages of the first and second liquid crystal capacitors Clch and Clcl, respectively, are different from each other, such that the visibility can be substantially improved.

[0152] In one exemplary embodiment, the transmittance can be secured without adding a signal line using a gate line consecutive to the first gate line 121 as the second gate line 125.

[0153] The second gate line 125 is connected to the second terminal of the transformation capacitor Cstd, such that the second terminal of the transformation capacitor Cstd maintains the gate-off voltage Voff that is a negative voltage. This is advantageous in applying an active capacitor.

[0154] In addition, the second liquid crystal capacitor Clcl and the transformation capacitor Cstd can share charge even where the pixel is previously charged, by overlapping a period where the gate-on voltage Von is applied to the consecutive gate lines. Therefore, the gate driving margin can be secured.

[0155] While this invention has been described in connection with what is presently considered to be practical exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

What is claimed is:

1. A liquid crystal display, the liquid crystal display comprising:

a plurality of gate lines which includes a first gate line, a transformation gate line, and a second gate line;

a data line; and

a pixel, wherein the pixel includes:

a first liquid crystal capacitor which includes a first sub-pixel electrode and a common electrode, and a second liquid crystal capacitor which includes a second sub-pixel electrode and a common electrode;

a first switching element connected to the first gate line, the data line, and the first sub-pixel electrode;

a second switching element connected to the first gate line, the data line, and the second sub-pixel electrode;

a third switching element connected to the transformation gate line and the second switching element;

a transformation capacitor which includes a first terminal directly connected to the second gate line and a second terminal connected to the third switching element.

2. The liquid crystal display of claim 1, wherein the second gate line and the first gate line are consecutive gate lines.

3. The liquid crystal display of claim 2, wherein the second gate line is a gate line previous to the first gate line.
4. The liquid crystal display of claim 2, wherein the second gate line is a gate line subsequent to the first gate line.
5. The liquid crystal display of claim 1, wherein the first gate line is an i -th gate line (where $i=2, 3, \dots, n$), the second gate line is an $i-1$ -th gate line, and the transformation gate line is an $i+4$ -th gate line.
6. The liquid crystal display of claim 1, wherein the first gate line is an i -th gate line (where $i=2, 3, \dots, n$), the second gate line is an $i+1$ -th gate line, the transformation gate line is an $i+4$ -th gate line.

* * * * *

专利名称(译)	液晶显示器及其驱动方法		
公开(公告)号	US20140307193A1	公开(公告)日	2014-10-16
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[标]申请(专利权)人(译)	三星显示有限公司		
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摘要(译)

一种液晶显示器，液晶显示器包括多条栅极线，包括第一栅极线，变换栅极线 and 第二栅极线；数据线；像素包括：第一液晶电容器，包括第一子像素电极和公共电极；以及第二液晶电容器，包括第二子像素电极和公共电极；第一开关元件，连接第一栅极线，数据线和第一子像素电极；第二开关元件，连接第一栅极线，数据线和第二子像素电极；第三开关元件，连接到变换栅极线 and 第二开关元件；变换电容器，包括连接到第二栅极线的第一端子和连接到第三开关元件的第二端子；栅极导通电压 V_{on} 施加到第一栅极线的第一周期和栅极导通电压 V_{on} 施加到变换栅极线的第二周期彼此不重叠，栅极截止电压 V_{off} 是在第二期间应用于第二栅极线。

