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(54) **GATE DRIVER AND LIQUID CRYSTAL DISPLAY INCLUDING SAME**

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(57) **ABSTRACT**

Provided are a gate-lines driver circuit and a liquid crystal display (LCD) device including the same. The gate-lines driver may be in danger of being subjected to static electricity and it includes: a wiring unit which receives signals from an external source and a circuit unit which outputs driving signals in response to a plurality of control signals received from the wiring unit. The circuit unit includes a plurality of shift registers, each having shift register wirings, wherein the wiring unit includes first through n-th vertical signal lines arranged sequentially in order of distance from the shift registers, with the first vertical signal line being located farthest from the shift registers. The first vertical signal line is connected to each of the shift registers by a first horizontal connection line, and the first horizontal connection line includes a first contact portion which is formed over and contacting with the first signal line and a second contact portion which is located between the n-th vertical signal line and a boundary of the shift registers and is connected to each of the shift registers by a shift register wiring. The first horizontal connection line is structured to reduce a danger that the shift registers will be burned out by a surge of static electricity current received through the wiring unit.

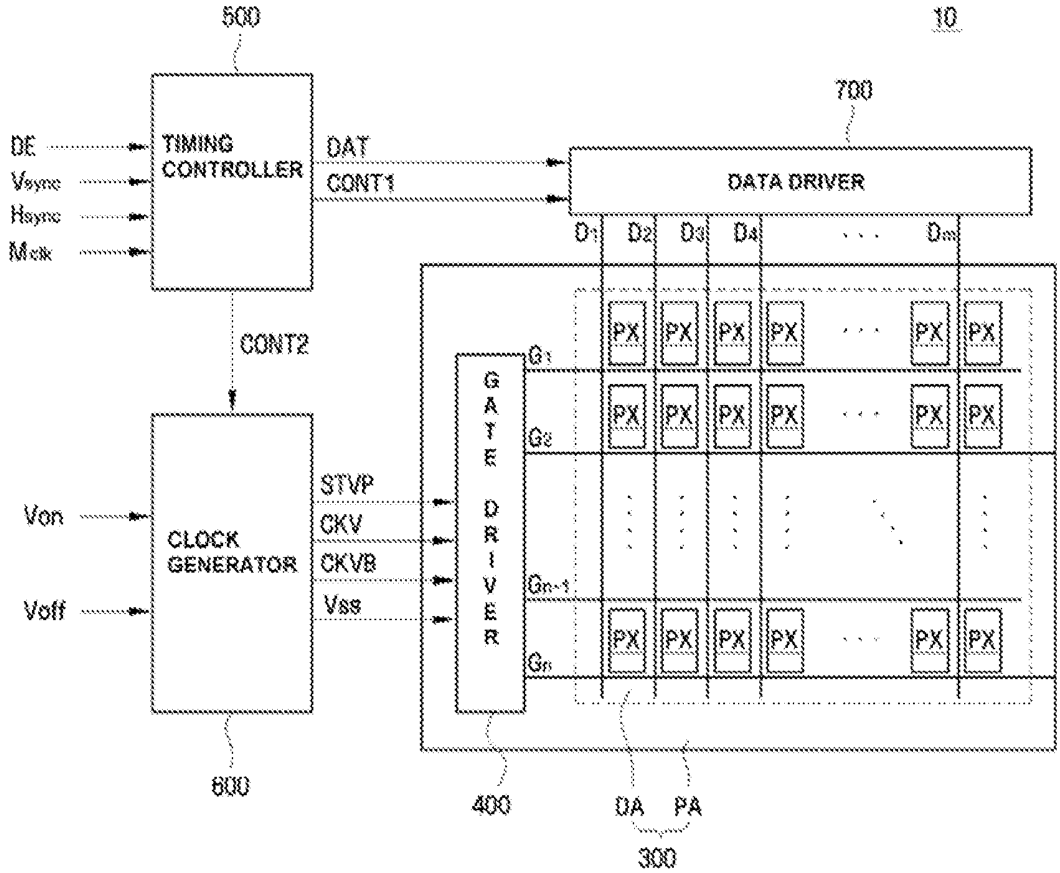
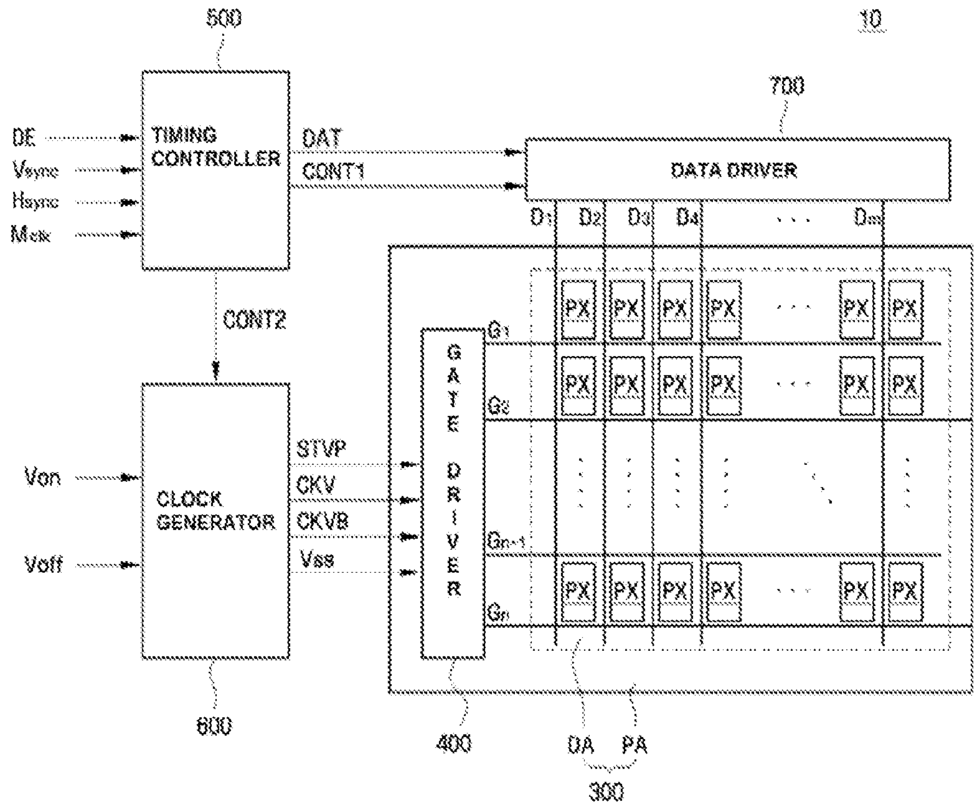


FIG. 1



500
10
700
DE
Vsync
Hsync
Mclk
TIMING CONTROLLER
DAT
CONT1
DATA DRIVER
D1
D2
D3
D4
Dm
CONT2
PX
G1
G2
Gn-1
Gn
GATE DRIVER
Von
Voff
CLOCK GENERATOR
STVP
CKV
CKVB
Vss
600
400
DA
PA
300

FIG. 2

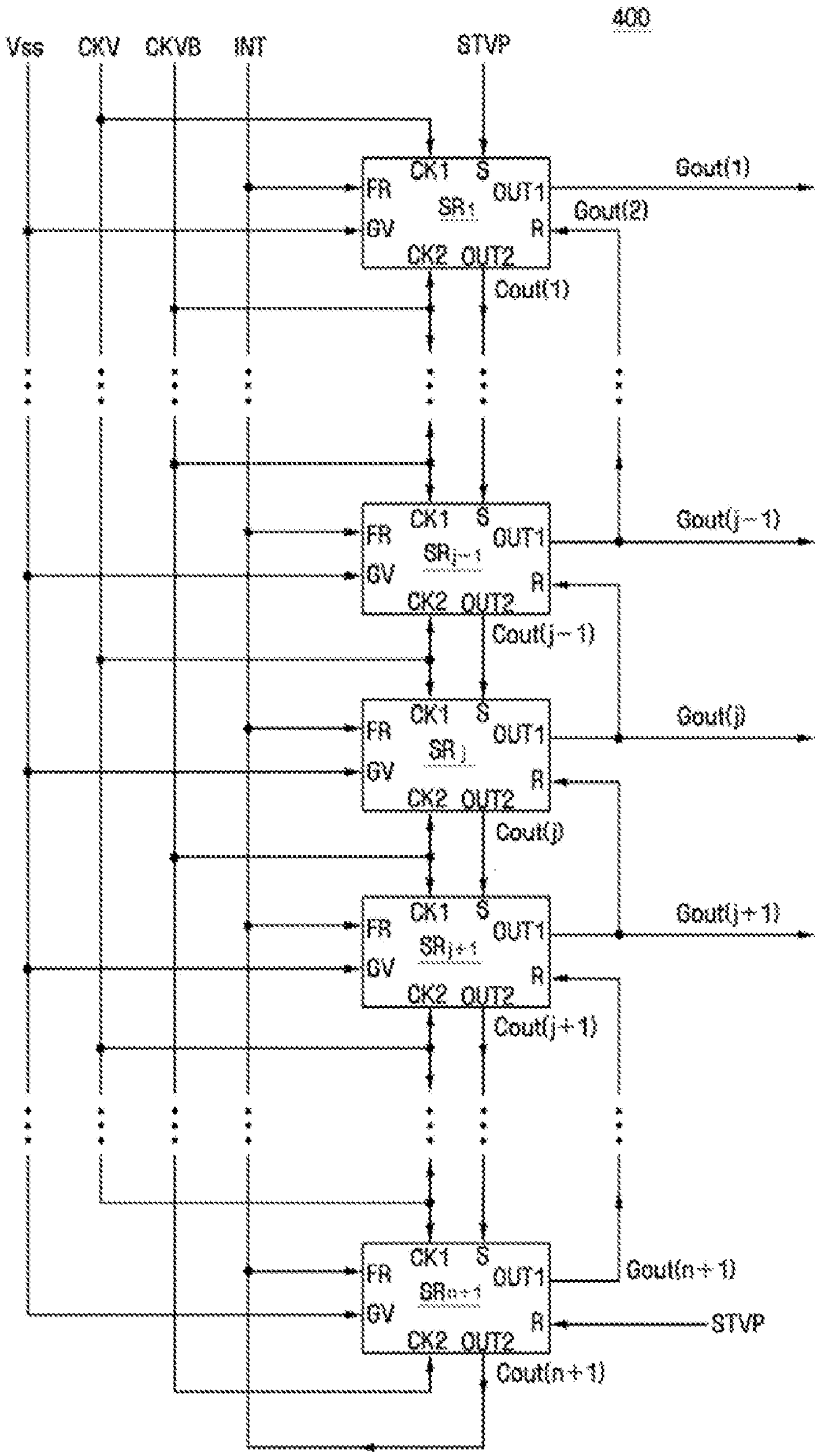
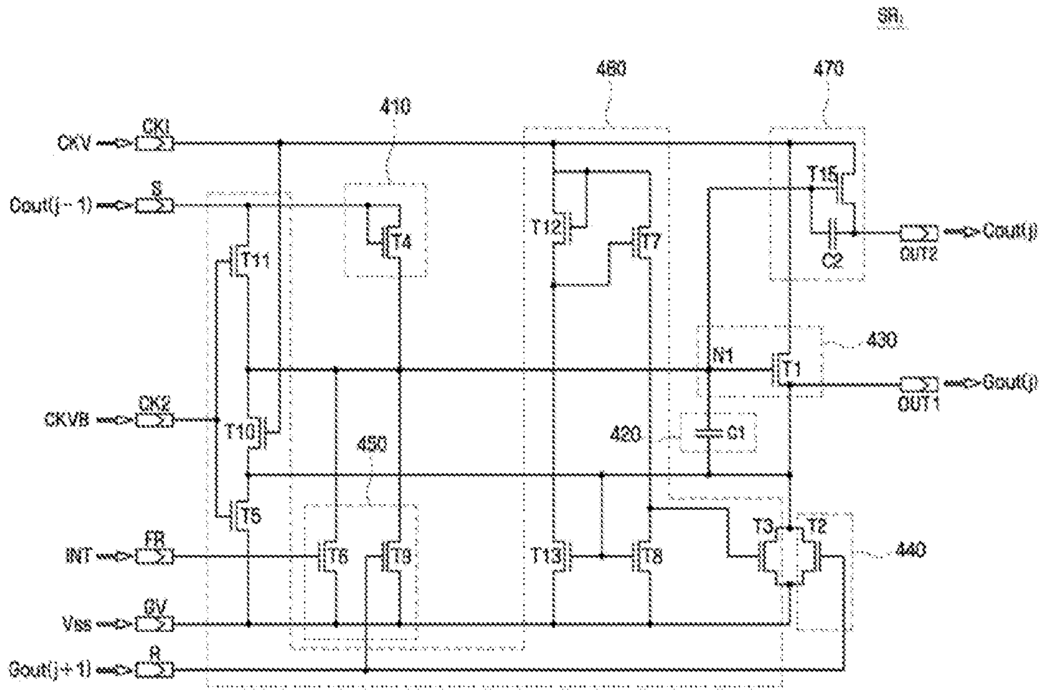

400
Vss
CKV
CKVB
INT
STVP
CK1
S
FR
OUT1
SR1
GV
R
CK2
OUT2
Gout(1)
Gout(2)
Cout(1)
SRj-1
Gout(j-1)
Cout(j-1)
SRj
Gout(j)
Cout(j)
SRj+1
Gout(j+1)
Cout(j+1)
SRn+1
Gout(n+1)
Cout(n+1)

FIG. 3



SRj
480
470
410
CKV
CK1
Cout(j-1)
S
T15
T12
T7
T4
C2
OUT2
Cout(j)
T11
430
N1
T1
Gout(j)
OUT1
CKVB
CK2
T10
420
C1
450
T5
T3
T2
440
INT
FR
T6
T9
T13
T8
Vss
GV
Gout(j+1)
R

FIG. 4

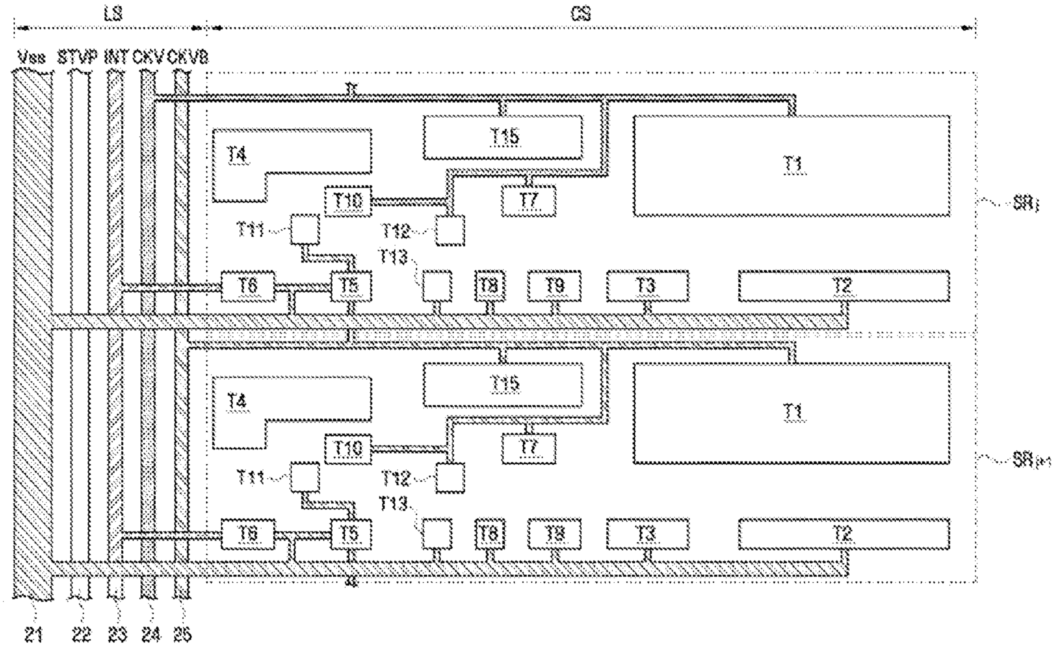

LS
CS
Vss
STVP
INT
CKV
CKVB
T4
T15
T1
T10
T7
T11
T12
T13
T6
T5
T8
T9
T3
T2
SRj
SRj+1
21
22
23
24
25

FIG. 5

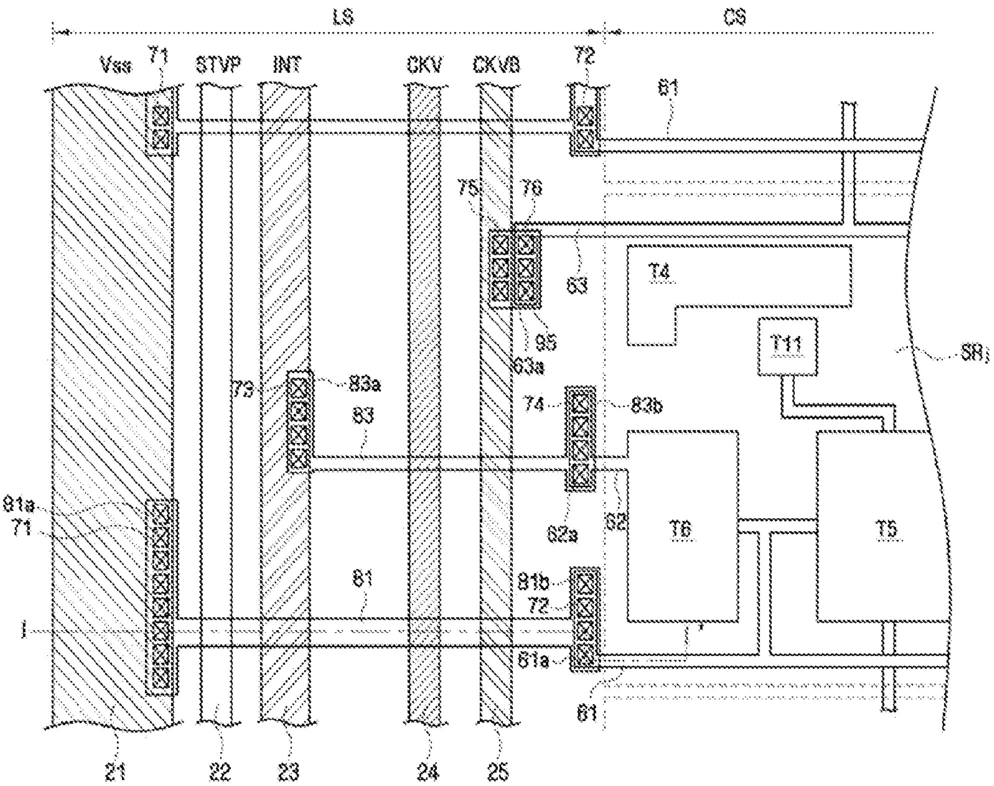
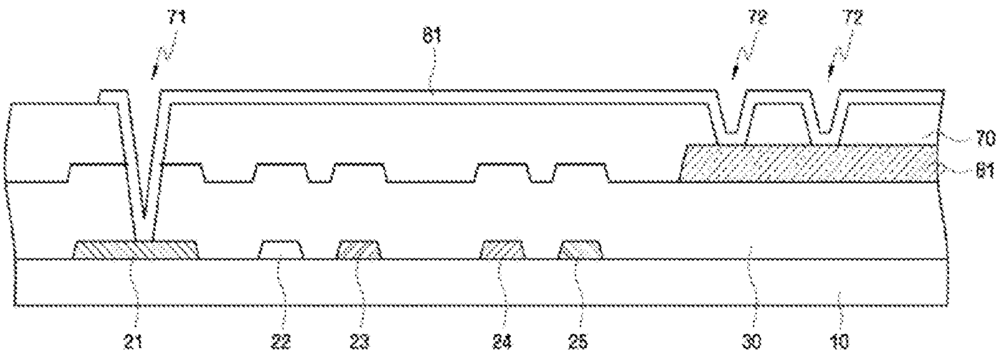

LS
CS
Vss
71
STVP
INT
CKV
CKVB
72
61
75
76
63
T4
95
63a
T11
SRj
73
83a
83
74
83b
81a
71
62a
62
T6
T5
81
81b
72
81a
I
61
21
22
23
24
25

FIG. 6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10

FIG. 7

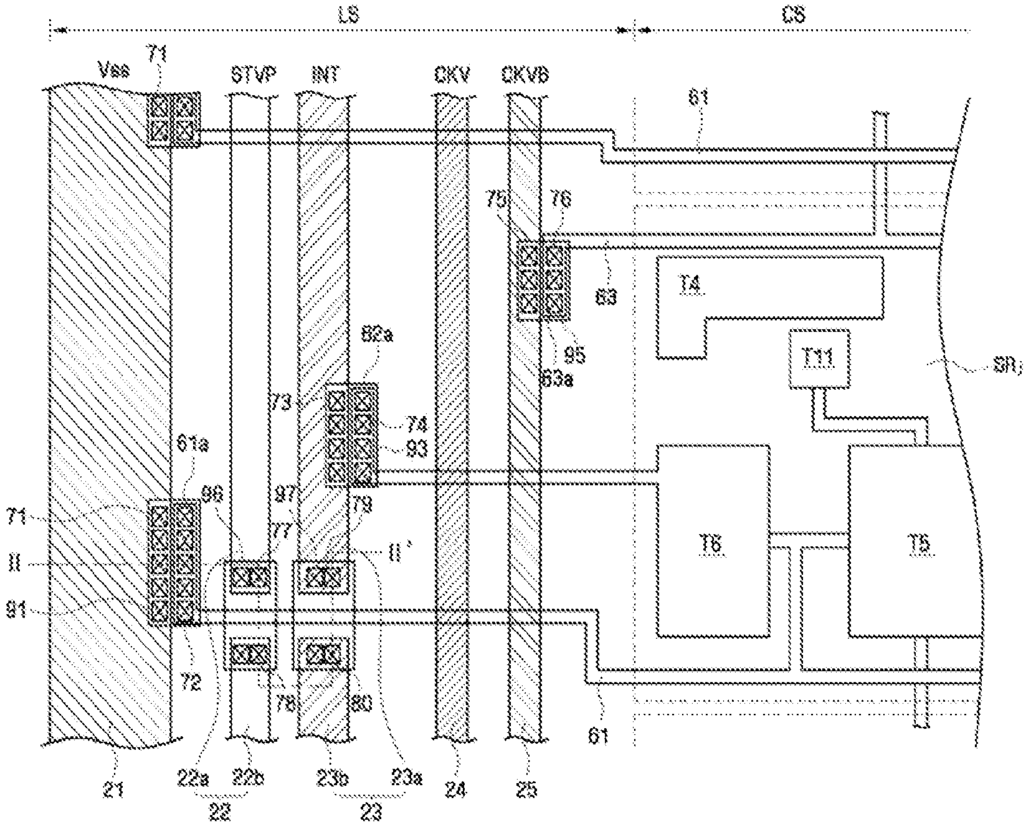
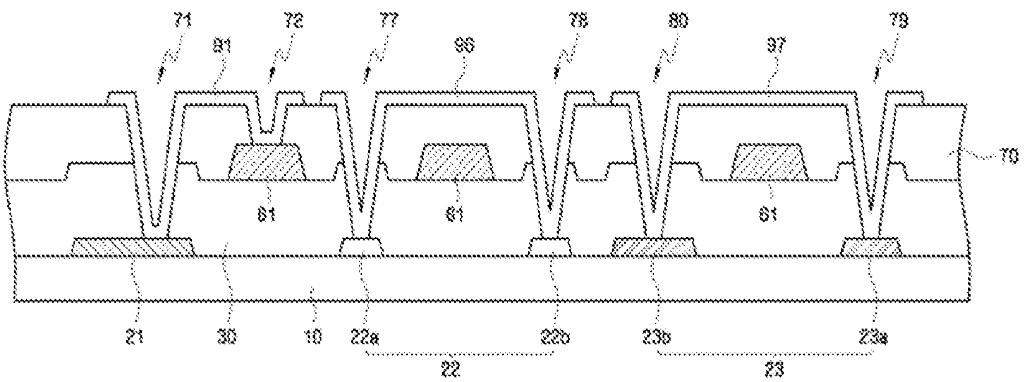

LS
CS
Vss
71
STVP
INT
CKV
CKVB
61
75
76
63
T4
95
63a
T11
SRj
62a
73
74
93
61a
96
97
79
71
77
II
II'
T6
T5
91
72
78
80
61
21
22a
22b
23b
23a
24
25
22
23

FIG. 8


71
91
72
77
96
78
80
97
79
70
61
61
61
21
30
10
22a
22b
23b
23a
22
23

GATE DRIVER AND LIQUID CRYSTAL DISPLAY INCLUDING SAME

[0001] This application claims priority from Korean Patent Application No. 10-2010-0102434 filed on Oct. 20, 2010 in the Korean Intellectual Property Office, the disclosure of which application is incorporated herein by reference in its entirety.

BACKGROUND

[0002] 1. Field of Disclosure

[0003] The present disclosure of invention relates to a gate driver structured such that its elements are better protected against being burned by static electricity and a liquid crystal display (LCD) including the gate driver.

[0004] 2. Description of Related Technology

[0005] Generally, a liquid crystal display (LCD) includes a display panel having a plurality of gate lines and a plurality of data lines, a gate driver transmitting a plurality of gate signals to the gate lines, and a data driver transmitting a plurality of data signals to the data lines.

[0006] In a conventional LCD, each of the gate driver and data driver is mounted on a display panel in the form of one or more respective IC chips. However, attempts are being made to monolithically integrate at least one of the gate driver and the data driver on a same substrate having the thin-film transistors (TFTs) of the LCD in order to reduce the total size of the display device and to improve productivity and reliability. That is, a gate driver circuit which generates the gate signals of a TFTs-containing substrate is integrally formed on that substrate using an amorphous silicon TFT technology that directly mounts the gate driver circuit on the same glass substrate where the pixels and their respective TFT switching transistors are formed.

[0007] However, when a plurality of amorphous silicon TFTs are disposed on a glass or alike substrate to thus integrally form such a gate driver, static electricity generated in manufacturing facilities may flow to a gate driving circuit through an edge of the substrate and undesirably burn out elements of the gate driving circuit. Since the generation of static electricity in the manufacturing facilities cannot be prevented completely, it is desirable to develop a gate driver structured such that its elements are protected against being burned out by static electricity flowing thereto.

[0008] It is to be understood that this background of the technology section is intended to provide useful background for understanding the here disclosed technology and as such, the technology background section may include ideas, concepts or recognitions that were not part of what was known or appreciated by those skilled in the pertinent art prior to corresponding invention dates of subject matter disclosed herein.

SUMMARY

[0009] Aspects of the present disclosure provide a gate-lines driver circuit structured such that the danger of its elements being burned out by static electricity is reduced.

[0010] Aspects of the present disclosure also provide a liquid crystal display (LCD) including the static electricity tolerant gate-lines driver circuit.

[0011] According to a more detailed aspect of the present teachings, there is provided a gate-lines driver circuit including: a wiring unit which receives signals from an external source ( ); and a circuit unit which outputs gate lines driving signals in response to a plurality of control signals received from the wiring unit, where the circuit unit includes a plurality of shift registers, each having internal shift register wirings, and wherein the wiring unit includes first through n-th vertical signal lines that are spaced apart and arranged sequentially to thus define an ordering of respective distance from the shift registers, with the first vertical signal line being located farthest away from the shift registers, where n is a natural number, wherein the first signal line is connected to each of the shift registers by a first horizontal connection line, and the first horizontal connection line includes a first contact portion which is formed on the first signal line and a second contact portion which is located between the n-th signal line and the shift registers and is connected to each of the shift registers by a shift register wiring.

[0012] According to another aspect of the present disclosure, there is provided a gate driver including: a wiring unit which receives signals from an external source; and a circuit unit which outputs driving signals in response to a plurality of control signals received from the wiring unit and includes a plurality of shift registers, each having shift register wirings, wherein the wiring unit includes first through n-th signal lines arranged sequentially in order of distance from the shift registers, with the first signal line being located farthest from the shift registers, where n is a natural number, wherein the first signal line is connected to each of the shift registers by a shift register wiring extending to the first signal line, at least one of the second through n-th signal lines is divided into two spaced apart sections that have centered between them a line of the shift register wiring, and the two spaced apart sections are electrically connected (bridged) together by a connection line extending insulatively over the line of the shift register and having plural contact portions.

[0013] According to another aspect of the present disclosure, there is provided an LCD including a gate driver formed on a substrate, wherein the gate driver includes: a wiring unit which receives signals from an external source; and a circuit unit which outputs driving signals in response to a plurality of control signals received from the wiring unit and includes a plurality of shift registers, each having shift register wirings, wherein the wiring unit includes first through n-th signal lines arranged sequentially in order of distance from the shift registers, with the first signal line being located farthest from the shift registers, where n is a natural number, wherein the first signal line is connected to each of the shift registers by a first connection line, and the first connection line includes a first contact portion which is formed over and contacts the first signal line and a second contact portion which is located between the n-th signal line and the shift registers and is connected thereat to each of the shift registers by a shift register wiring.

[0014] According to another aspect of the present disclosure, there is provided an LCD including a gate driver formed on a substrate, wherein the gate driver includes: a wiring unit which receives signals from an external source; and a circuit unit which outputs driving signals in response to a plurality of control signals received from the wiring unit and includes a plurality of shift registers, each having shift register wirings, wherein the wiring unit includes first through n-th signal lines arranged sequentially in order of distance from the shift registers, with the first signal line being located farthest from the shift registers, where n is a natural number, wherein the first signal line is connected to each of the shift registers by a shift register wiring extending to but not directly connecting to the first signal line, at least one of the second through n-th signal lines is divided into two spaced apart sections between which is disposed a line of the shift register wiring, and the two sections are electrically connected together by a connection line extending insulatively over the line of the shift register wiring and having contact portions.

[0015] Other aspects of the present teachings will become apparent from the below detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] The above and other aspects and features of the present disclosure of invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings, in which:

[0017] FIG. **1** is a plan view of a gate driver and a liquid crystal display (LCD) including the same according to an exemplary embodiment of the present disclosure;

[0018] FIG. **2** is an exemplary block diagram illustrating shift registers that constitute the gate driver shown in FIG. **1**;

[0019] FIG. **3** is an exemplary circuit diagram of a j^{th} shift register shown in FIG. **2**;

[0020] FIG. **4** is a schematic layout diagram of the gate driver shown in FIG. **1**;

[0021] FIG. **5** is an exemplary schematic layout diagram of a wiring unit of the gate driver shown in FIG. **1**;

[0022] FIG. **6** is a cross-sectional view of the wiring unit taken along the line I-I' of FIG. **5**;

[0023] FIG. **7** is a layout diagram of a wiring unit of a gate driver according to another exemplary embodiment of the present disclosure; and

[0024] FIG. **8** is a cross-sectional view of the wiring unit taken along the line II-II' of FIG. **7**.

DETAILED DESCRIPTION

[0025] Advantages and features of the present teachings may be understood more readily by reference to the following detailed description of exemplary embodiments and the accompanying drawings. The present teachings may, however, be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete and will fully convey the concepts of the present teachings to those skilled in the corresponding art. In the drawings, sizes and relative sizes of layers and regions may be exaggerated for clarity.

[0026] It will be understood that when an element or layer is referred to as being "on" another element or layer, the element or layer can be directly on another element or layer or intervening elements or layers may also be present. In contrast, when an element is referred to as being "directly on" another element or layer, there are no intervening elements or layers present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0027] Spatially relative terms, such as "below", "beneath", "lower", "above", "upper", and the like, may be used herein for ease of description to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation, in addition to the orientation depicted in the figures. Like reference numerals refer to like elements throughout the specification.

[0028] Embodiments in accordance with the disclosure are described herein with reference to plan and cross-section illustrations that are schematic illustrations of idealized embodiments. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the actual shape of a region of a device and are not intended to limit the scope of the present disclosure.

[0029] Also, since a drain (or drain electrode) and a source (or source electrode) may be named differently according to the direction of current, an element called a drain or drain electrode hereinafter may operate as a source or source electrode, and an element called a source or source electrode may operate as a drain or drain electrode. Accordingly, an element called a drain or drain electrode is not limited to the drain or drain electrode. Also, the element called the source or source electrode is not limited to the source or source electrode.

[0030] Hereinafter, exemplary embodiments of a gate-lines driver circuit and a liquid crystal display (LCD) including the same will be described in detail with reference to the accompanying drawings.

[0031] A gate-lines driver and an LCD that integrally incorporates the same according to a first exemplary embodiment of the present disclosure will now be described with reference to FIGS. **1** through **6**. FIG. **1** is a schematic of a gate driver **400** and an LCD **10** including the same according to the first exemplary embodiment. FIG. **2** is an exemplary block diagram illustrating shift registers SR_1 through SR_{n+1} that constitute the gate driver **400** shown in FIG. **1**. FIG. **3** is an exemplary circuit diagram of a j^{th} shift register SR_j shown in FIG. **2**. FIG. **4** is a schematic layout diagram of the gate driver **400** shown in FIG. **1**. FIG. **5** is an exemplary schematic layout diagram of a wiring unit LS of the gate driver **400** shown in FIG. **1**. FIG. **6** is a cross-sectional view of the wiring unit LS taken along the line I-I' of FIG. **5**.

[0032] Referring first to FIG. **1**, the display device **10** according to the current exemplary embodiment includes a liquid crystal panel **300**, a gate driver **400** integrally incorporated in the panel **300**, a timing controller **500**, a clock generator **600**, and a data driver **700**.

[0033] The liquid crystal display **300** is divided into a display area DA in which an image is displayed and a non-display or peripheral area PA in which the image is not displayed.

[0034] To display the image, the display area DA includes a first substrate (not explicitly shown) on which there are formed a plurality of gate lines G**1** through Gn, a plurality of data lines D**1** through Dm, a plurality of pixel switching devices (not explicitly shown) and a plurality of pixel electrodes (not explicitly shown) are disposed. Moreover, a second substrate (not shown) is further provided and spaced apart from the first substrate where the second substrate has a plurality of color filters (not shown) and a common electrode (not shown). A liquid crystal layer (not shown) is interposed between the first and second substrates and orientations of its liquid crystal molecules are controlled by electric fields formed between the pixel-electrodes and corresponding portions of the common electrode.

[0035] The gate lines G**1** through Gn and the data lines D**1** through Dm respectively extend on their supporting first substrate in the display area DA thereof and in respective a row and column directions. In addition, switching devices and a plurality of pixels PX connected to the gate lines G**1** through Gn and the data lines D**1** through Dm are formed in pixel regions PX defined by intersections of the gate lines G**1** through Gn and the data lines D**1** through Dm.

[0036] The non-display area PA is a region in which no image is displayed. One reason why no image is displayed there in the PA area of a given embodiment can be because the first substrate of that embodiment is wider than the second substrate.

[0037] The timing controller **500** receives input control signals, such as a horizontal synchronization signal Hsync, a main clock signal Mclk and a data enable signal DE, and outputs an image signal DAT and a first control signal CONT**1**. The first control signal CONT**1** controls the operations of the data driver **700**. Examples of the first control signal CONT**1** include a horizontal start signal for starting the data driver **700** and a load signal for instructing the output of corresponding analog data voltages. The timing controller **500** sends a vertical synchronization start signal to the clock generator **600** by being synchronized with a vertical synchronization signal Vsync and provides a second control signal CONT**2** to the clock generator **600**.

[0038] The clock generator **600** receives the second control signal CONT**2** from timing controller **500** and outputs a clock signal CKV and a clock bar signal CKVB. That is, in response to the second control signal CONT**2**, the clock generator **600** outputs the clock signal CKV and the clock bar signal CKVB using a gate-on voltage level, Von and a gate-off voltage level Voff. Examples of the second control signal CONT**2** include an output enable signal OE and a gate clock signal CPV. The clock signal CKV and the clock bar signal CKVB are pulse signals that swing between the gate-on voltage level Von and the gate-off voltage level Voff. The clock signal CKV may be a reverse phase signal of the clock bar signal CKVB.

[0039] The data driver **700** receives the image signal DAT and the first control signal CONT**1** from the timing controller **500** and provides corresponding image data voltages to the data lines D**1** through Dm, respectively. The data driver **700** may be disposed as monolithically integrated circuits (ICs) whose terminals are connected to the liquid crystal panel **300** in the form of a tape carrier package (TCP). However, the present disclosure of invention is not limited to such discrete coupling of the data driver **700**. The data driver **700** may alternatively be disposed in the non-display area PA of the first substrate.

[0040] The gate driver **400** may be disposed in the non-display area PA of the first substrate. Although only a one-side version is shown in the drawings, a plurality of the gate drivers **400** may be respectively disposed on two opposed sides of the non-display region PA of the first substrate with the display area DA between them. In the latter case, a gate driver **400***a* (not shown) disposed on a first side of the non-display area PA of the first substrate may drive, e.g., even gate lines of the gate lines, while a different gate driver **400***b* (not shown) disposed on the opposite second side of the non-display area PA may drive, e.g., odd gate lines of the gate lines. Alternatively, the gate drivers **400** formed on both sides of the non-display region PA may each drive all of the gate lines G**1** through Gn, respectively.

[0041] When enabled by a scan start signal STVP, the gate driver **400** generates a plurality of gate signals using the clock signal CKV, the clock bar signal CKVB and a direct current (DC) voltage signal Vss. The gate driver **400** sequentially transmits Von pulses of the gate signals to corresponding ones the gate lines G**1** through Gn, one after the next.

[0042] Referring to FIG. **2**, the gate driver **400** includes a plurality of shift registers SR_1 through SR_{n+1}, where n is a natural number greater than one. The shift registers SR_1 through SR_{n+1} receive the clock signal CKV, the clock bar signal CKVB and the DC voltage signal Vss and sequentially provide a plurality of gate signals to the gate lines G**1** through Gn. The gate lines G**1** through Gn are connected to output terminals of the shift registers SR_1 through SR_{n+1}, respectively. The shift registers SR_1 through SR_{n+1} are connected to each other in a cascade manner. The shift registers SR_1 through SR_n, (this excluding the last shift register SR_{n+1}), are connected to the gate lines G**1** through Gn, respectively, and output their corresponding gate signals $Gout_{(1)}$ through $Gout_{(n)}$ to the gate lines G**1** through Gn, respectively. That is, the shift registers SR_1 through SR_n receive the DC voltage signal Vss, the clock signal CKV and the clock bar signal CKVB and a direct or relayed version of the scan start signal STVP and they responsively and sequentially output their respective gate signals $Gout_{(1)}$ through $Gout_{(n)}$, each having a predetermined turn-on level of voltage (Von) for a predetermined period of time, to the gate lines G**1** through Gn.

[0043] Each of the shift registers SR_1 through SR_{n+1} includes a first clock terminal CK**1**, a second clock terminal CK**2**, a set terminal S, a reset terminal R, a source voltage terminal GV (ground voltage), a frame reset terminal FR, a gate signal output terminal OUT**1** and a carry output terminal OUT**2**.

[0044] For purposes of explanation, the j^{th} shift register SR_j, for example, connected to a j^{th} gate line (where $j \neq 1$ and is a natural number ranging from 2 through n−1) will now be described in further detail still with reference to FIG. **2**. A carry signal $Cout_{(j-1)}$ of a previous shift register, e.g., the $(j-1)^{th}$ shift register SR_{j-1}, is input to the set terminal S of the j^{th} shift register SR_j, the gate signal $Gout_{(j-1)}$ of a subsequent shift register, e.g., the $(j+1)^{th}$ shift register SR_{j+1}, is input to the reset terminal R of the j^{th} shift register SR_j, and the clock signal CKV and the clock bar signal CKVB are input to the first clock terminal CK**1** and the second clock terminal CK**2**, respectively, of the j^{th} shift register SR_j. (However, in the next shift register SR_{j+1}, the respectiveness between CKV and CK1 versus CKVB and CK2 is reversed. CK1 gets the CKVB signal and CK2 gets the CKV signal.)

[0045] In addition, the DC voltage signal Vss is input to the source voltage terminal GV of the j^{th} shift register SR_j, and an initialization signal INT or, alternatively, a carry signal $Cout_{(n+1)}$ of a last shift register, e.g., the $(n+1)^{th}$ shift register SR_{n+1}, is input to the frame reset terminal FR of the j^{th} shift register SR_1. The gate output terminal OUT**1** outputs the gate signal $Gout_{(j)}$, and the carry output terminal OUT**2** outputs a carry signal $Cout_j$) for application to the S input of the next stage.

[0046] In the case of the first shift register SR_1 of the chain however, the scan start signal STVP, instead of a carry signal of a previous shift register of the first shift register SR_1, is input to the first shift register SR_1. In addition, the scan start signal STVP, instead of a gate signal of a next shift register of the last shift register SR_{n+1}, is input to the last shift register SR_{n+1}. The scan start signal STVP input to the first shift register SR_1 is substantially the same as the scan start signal STVP input to the last shift register SR_{n+1}.

[0047] The internal circuitry of the j^{th} shift register SR_j shown in FIG. **2** will now be described in further detail with reference to FIG. **3**. Referring to FIG. **3**, The j^{th} shift register SR_j includes a buffer unit **410**, a charging unit **420**, a pull-up unit **430**, a carry signal generation unit **470**, a pull-down unit **440**, a discharging unit **450**, and a holding unit **460**. Each of the charging unit **420**, discharging unit **450**, and buffer unit **410** is connected to a so-called node N1 line within the j^{th} shift register SR_j. The carry signal $Cout_{(j-1)}$ of the previous shift register SR_{j-1}, the clock signal CKV, and the clock bar signal CKVB are provided to the j^{th} shift register SR_j.

[0048] The buffer unit **410** includes a transistor T**4**. A gate electrode and a drain electrode of the transistor T**4** are shorted together and connected to the set terminal S of the j^{th} shift register SR_j. Since the gate and drain electrode of the transistor T**4** are connected to each other, transistor T**4** operates substantially like a diode. The buffer unit **410** provides to the N1 node, the high level if present of the carry signal $Cout_{(j-1)}$ of the previous shift register SR_{j-1}, which is received through the set terminal S. In other words, if **N1** is low, the buffer unit **410** provides a recharging voltage to the charging unit **420**, as well as to the gate of the carry signal generation unit **470**, and to the gate of the pull-up unit **430**.

[0049] The charging unit **420** includes a capacitor C**1** including a first terminal, which first terminal is connected to a source electrode of the transistor T**4** , to the gate of the pull-up unit **430** and to the drain of the discharging unit **450**. The capacitor C**1** further includes a second terminal which is connected to the first output terminal OUT**1**.

[0050] The pull-up unit **430** includes a gate-line driving transistor (TFT) T**1** including a drain electrode connected to the first clock terminal CK**1**, a gate electrode connected to the charging unit **420**, and a source electrode connected to the gate-line driving first output terminal, OUT**1**.

[0051] The carry signal generation unit **470** includes a transistor T**15** and a second capacitor C**2**. The transistor T**15** includes a drain electrode connected to the first clock terminal CK**1**, a source electrode connected to the carry signal outputting terminal OUT**2**, and a gate electrode connected to the buffer unit **410**. In addition, the capacitor C**2** is connected between the gate electrode and source electrode of the transistor T**15**.

[0052] The pull-down unit **440** includes a transistor T**2** including a drain electrode connected to the source electrode of the transistor T**1** and the second terminal of the capacitor C**1**, a source electrode connected to the voltage source terminal GV, and a gate electrode connected to the reset terminal R. Here, the gate electrode controls the transistor T**2** by receiving the gate signal $Gout_{(j+1)}$ of the next shift register SR_{j+1}. Accordingly, if the $Gout_{(j+1)}$ signal of the next shift register SR_{j+1} is high (logic high ("1") as well as voltage high), the pull-down unit **440** will be activated to pull the gate-line driving first output terminal, OUT**1** low.

[0053] The discharging unit **450** includes transistors T**6** and T**9**. The transistor T**9** includes a gate electrode connected to the reset terminal R, a drain electrode connected to the first terminal of the capacitor C**1**, and a source electrode connected to the voltage source terminal GV. The transistor T**9** discharges the charging unit **420** in response to the gate signal $Gout_{(j+1)}$ of the next shift register $SR_{(j+1)}$. In other words, if the $Gout_{(j+1)}$ signal of the next shift register SR_{j+1} is high, the discharging unit **450** will be activated to pull the **N1** node low. The transistor T**6** includes a gate electrode connected to the frame reset terminal FR, a drain electrode connected to the first terminal of the capacitor C**1**, and a source electrode connected to the voltage source terminal GV. The transistor T**6** discharges the charging unit **420** in response to the initialization signal INT. In other words, if the INT signal is high, the discharging unit **450** will be activated to pull the **N1** node low.

[0054] The holding unit **460** includes a large plurality of transistors, namely, T3, T**5**, T**7**, T**8**, T**10**, T**11**, T**12** and T**13**. When the gate-line driving signal $Gout_{(j)}$ shifts from a low level to a high level, the holding unit **460** switches to state in which it urges the gate signal $Gout_{(j)}$ to remain at the high level. Likewise, when the gate-line signal $Gout_{(j)}$ shifts from a high level to a low level, the holding unit **460** switches to state in which it urges the gate signal $Gout_{(j)}$ to remain at the low level during a frame, where the held level is without regard to switching voltage levels of other signals such as those of the clock signal CKV or the clock bar signal CKVB. (It is understood that the driven gate line connected to the OUT1 terminal has inherent capacitance and this works to keep the gate-line signal $Gout_{(j)}$ steady.)

[0055] Hereinafter, a layout of the drive signals wiring of the gate-line driver circuit **400** shown in FIG. **1** will be described in detail with reference to FIGS. **4** through **6**.

[0056] Referring to FIGS. **4** and **5**, the layout of the gate driver **400** includes circuit unit (CS). This circuit unit(CS) includes the plurality of shift registers SR_1 through SR_{n+1}. The layout of the gate driver **400** further includes a wiring unit (LS). This wiring unit (LS) contains vertically elongated conductors and horizontally elongated conductors which deliver various external signals (Vss, STVP, INT, CKV, CKVB, etc.) to the shift registers SR_1 through SR_{n+1}.

[0057] In more detail, the circuit unit CS includes the shift registers SR_1 through SR_{n+1}, each including its respective plurality of TFTs T1 through T13 and T**15**. Referring to the arrangement of the transistors T1 through T13 and T**15** in, for example, the j^{th} shift register SR_j shown in the upper portion of FIG. **4**, the transistor T**4** to which the carry signal $Cout_{(j-1)}$ of the previous shift register SR_{j-1} is input is disposed in an upper part of the j^{th} shifter register SR_j which is close to the lower boundary of previous shift register SR_{j-1} (not shown). The transistors T**15** and T1 of SR_j which receive the CK1 clock signal from the CKV transmission line extend horizontally adjacent to the upper boundary of the j^{th} shifter register SR_j, and the transistors T**7**, T**10** and T**12** which also receive the CK1 clock signal from the CKV transmission line are also disposed adjacent to the upper boundary of the j^{th} shifter register SR_j, but vertically under the transistor T**15**. In addition, the transistors T**11** and T5 of SR_j which receive the CK2 clock bar signal from the CKVB transmission line arriving from thereunder are disposed in a lower left boundary part of the j^{th} shifter register SR_j. The transistor T6 which receives the initialization signal INT arriving from the left of SR_j is disposed in a leftmost part of the j^{th} shifter register SR_j. Also, the transistors T**2**, T**3**, T**8**, T**9**, T**13**, T**5**, T**6** which receive the DC voltage signal of terminal GV from the Vss transmission line extend horizontally in a lower boundary part of the j^{th} shifter register SR_j.

[0058] The wiring unit LS includes first through n^{th} vertically elongated signal lines, where n is a natural number. The first through n^{th} vertical signal lines (e.g., the ones denoted as

21-25 in FIG. 5) extend parallel to each other in a substantially vertical direction. The first through n^{th} vertical signal lines are arranged sequentially in order of their distance from the left side boundaries of adjacent shift registers SR_1 through SR_{n+1}, with the first such vertical signal line (e.g., Vss **21**) being farthest away from the corresponding adjacent edge boundaries of the adjacent layouts of shift registers SR_1 through SR_{n+1}. In FIGS. **4** through **6**, first through fifth signal lines **21** through **25**, for example, are arranged sequentially in order of their distance from the shift registers SR_1 through SR_{n+1}, with the first signal line **21** (Vss) being farthest from the shift registers SR_1 through SR_{n+1}.

[0059] More specifically, the wiring unit LS includes as its first vertical signal line **21**, the DC voltage signal line which delivers the DC voltage signal Vss. Moreover, the wiring unit LS includes as its second vertical signal line **22**, the scan start signal line which delivers the scan start signal STVP, as its third vertical signal line **23**, the initialization signal line which delivers the initialization signal INT, as its fourth vertical signal line **24**, the clock signal line which delivers the clock signal CKV, and as its fifth vertical signal line **25**, the clock bar signal line which delivers the clock bar signal CKVB. The number of differently phased ones of such vertical clock signal lines (e.g., **24**, **25**) may vary and when more than two such vertical clock signal lines (e.g., **24**, **25**) are provided, the connections to the CK**1** and CK**2** terminals of each register stage may vary depending on design specifics. In FIGS. **4** and **5**, the DC voltage signal line (e.g., the first vertical signal line **21**), the scan start signal line (e.g., the second vertical signal line **22**), the initialization signal line (e.g., the third vertical signal line **23**), the clock signal line (e.g., the fourth vertical signal line **24**) and the clock bar signal line (e.g., the fifth vertical signal line **25**) are arranged sequentially from left to right adjacent to the left edge boundaries of the corresponding shift registers, with the clock bar vertical signal line **25** being located closest to such adjacent to the left edge boundaries of the shift registers SR_1 through SR_{n+1} and the DC voltage vertical signal line **25** being located farthest away from the left edge boundaries.

[0060] The first through n^{th} vertical signal lines are connected to the shift registers SR_1 through SR_{n+1}. The DC voltage signal line (e.g., the first signal line **21**) and the initialization signal line (e.g., the third signal line **23**) are connected to each of the shift registers SR_1 through SR_{n+1}. On the other hand, the scan start signal line (e.g., the second signal line **22**) is connected only to the first and to the last shift registers SR_1 and SR_{n+1}. Accordingly, in FIGS. **4** and **5**, the scan start signal line (e.g., the second signal line **22**) is not shown as being connected to the j^{th} shift register SR_j. In FIGS. **4** and **5**, the clock signal line (e.g., the fourth signal line **24**) and the clock bar signal line (e.g., the fifth signal line **25**) are located near the upper and lower boundaries of the shift registers SR_1 and SR_{n+1} and are alternately connected to respective ones of the Ck**1** and CK**2** terminals of each of the shift registers SR_1 and SR_{n+1}. Since substantially all current is sunk through it, the DC voltage vertical signal line carries more current. Therefore, the DC voltage vertical signal line **21** should have a smaller resistivity per unit length than the other vertical signal lines. In one embodiment, the DC voltage vertical signal line is formed with a greater width (as seen from a top plan view) than the other vertical signal lines.

[0061] Referring to FIG. **5** and in terms of more specifics, the first vertical signal line **21** is connected into the interiors of each of the shift registers SR_1 through SR_{n+1} by way of a corresponding set of first horizontal connection lines **81**. Each first horizontal connection line **81** includes a first cross-layer contact portion **81***a* and a second cross-layer contact portion **81***b*.

[0062] The first cross-layer contact portion **81***a* is a region which is formed by contiguously extending an end of the first horizontal connection line **81** through corresponding openings in one or more insulation (dielectric) layers so as to directly contact the first vertical signal line **21**. In one embodiment, the first contact portion **81***a* is formed through a plurality of contact holes **71** that expose an upper surface of the first vertical signal line **21**. The first connection line **81** is thus directly connected to the first signal line **21** by way of the contact holes **71**.

[0063] The second cross-layer contact portion **81***b* is a region which is formed by extending the other end of the first connection line **81** contiguously through one or more openings of a one or more insulation (dielectric) layers so as to directly contact a shift register wiring **61** provided in the corresponding one of shift registers SR_1 through SR_{n+1}. In one embodiment, the second contact portion **81***b* overlaps a bent extension portion **61***a* of the shift register wiring **61**, and a plurality of contact holes **72** are provided along that bent extension portion **61***a* for exposing the underlying shift register wiring **61** whereby any one or more of the plural contact holes **72** can provide a good contact between the second contact portion **81***b* and its overlapped area along the extension portion **61***a* of the shift register wiring **61**.

[0064] Referring to the example embodiment of FIG. **6**, a first insulating film **30** is formed over the base substrate **10** after the first through fifth vertical signal lines **21** through **25** are formed on the base substrate **10**. The shift register wiring **61** is thereafter formed on the first insulating film **30**. A second insulating film **70** is then formed over the shift register wiring **61** and the first insulating film **30**. Respective contact holes **71** and **72** are formed and then the first horizontal connection line **81** is formed on the second insulating film **70**.

[0065] The first through fifth vertical signal lines **21** through **25** and the shift register wiring **61** may each be made for example of an aluminum (Al)-based metal such as Al and/or an Al alloy, a silver (Ag)-based metal such as Ag and/or an Ag alloy, a copper (Cu)-based metal such as Cu and/or a Cu alloy, a molybdenum (Mo)-based metal such as Mo and/or a Mo alloy, chrome (Cr), titanium (Ti), or tantalum (Ta) or appropriate multi-layer combinations of two or more of these.

[0066] The first insulating film **30** may be formed of an inorganic material such as a silicon nitride or a silicon oxide, or a low-k insulating material formed by plasma enhanced chemical vapor deposition (PECVD), such as a-Si:C:O or a-Si:O:F. The first insulating film **30** may be formed to a thickness of 3,000 to 5,000 Å.

[0067] The shift register wiring **61** extends on the first insulating film **30**. However, the shift register wiring **61** does not extend onto the first through n^{th} vertical signal lines **21** through **25**. Also, as shown in FIG. **6**, the shift register wiring **61** is spaced apart from the second through n^{th} vertical signal lines **21**-**25** by the combined thickness of dielectric layers **70** and **30**. Thus, even when static electricity flows into one or more of the second through n^{th} vertical signal lines **21**-**25** of the gate-line driver **400**, it is unlikely to rapidly breakdown and through the double layer of dielectric layers **70** and **30** and thus it is unlikely to produce a surge current that can cause one or more of the shift register wiring **61** and the second through n^{th} vertical signal lines **21-25** to be burned out.

[0068] The second insulating film **70** is formed on the first insulating film **30** as mentioned. The second insulating film **70** may be formed of an inorganic material such as a silicon nitride or a silicon oxide, an organic material having photosensitivity and superior planarization characteristics, or a low-k insulating material formed by PECVD, such as a-Si:C:O or a-Si:O:F. The second insulating film **70** may be formed to a thickness of 1,500 through 3,000 Å. The second insulating film **70** includes the contact holes **71** exposing the first signal line **21** and the contact holes **72** exposing the shift register wiring **61**.

[0069] As mentioned, the first horizontal connection line **81** is formed on the second insulating film **70**. The first contact portion **80***a* and the second contact portion **80***b* are connected to form the first connection line **81**. The first connection line **81** may be made of indium tin oxide (ITO) or indium zinc oxide (IZO) and it may be formed to a width of 5 to 50 μm.

[0070] As described above, the first contact portion **81***a* is formed on or close to the first vertical signal line **21** in order to be in contact with the first signal line **21**. However, the second contact portion **81***b* is located between the bulk of circuitry of each of the shift registers SR_1 through SR_{n+1} and the fifth vertical signal line **25** most adjacent to the left boundary of that bulk of circuitry. Accordingly, the shift register wiring **61** formed on the first insulating film **30** terminates before crossing above the fifth signal line **25** as opposed to extending above any of the first through n^{th} signal lines **21-25**. That is, the shift register wiring **61** is not formed in close overlapping proximity with one or more of the second through fifth signal lines **22** through **25** such that that static current can easily surge from one of those lines **22** through **25** up through the dielectric and into the shift register wiring **61**.

[0071] In addition, since the first horizontal connection line **81** including the first and second contact portions **81***a* and **81***b* is formed on the second insulating film **70**, a double dielectric layer comprised of the first and second insulating films **30** and **70** is interposed between the second through fifth vertical signal lines **22** through **25** and the first connection line **81**. That is, a thicker insulating film is formed between the second through fifth signal lines **22** through **25** and the first connection line **81** and this helps to reduce the danger that they will by burned out by a surge of static electricity current flowing into the gate-line driver **400** by way of any one or more of lines **22-25**.

[0072] Additionally, the first vertical signal line **21** is located farthest from the bulk circuitry of the shift registers SR_1 through SR_{n+1}. To connect the first vertical signal line **21** to each of the shift registers SR_1 through SR_{n+1}, the shift register wiring **61** may be formed on the first insulating film **30** to overlap the second through n^{th} signal lines. In this case, however, only the first insulating film **30** exists as separation for example between the second through n^{th} vertical signal line Thus, the relative distance between the second vertical through n^{th} signal lines and the shift register wiring **61**. is reduced, thus putting the shift registers at risk of being burned out by static electricity. For this reason, the first signal line **21** is connected to each of the shift registers SR_1 through SR_{n+1} only by way of the first connection line **81** which line is also spaced apart by double films **30** and **70** from the other vertical lines **21-25**.

[0073] As shown in FIGS. **4** through **6**, the first vertical signal line **21** may be the DC voltage signal line. The DC voltage signal line may be formed wider than the other vertical signal lines in order to reduce its resistivity. Also it may be placed first and thus closest to an edge of the substrate so as to protectively ring around the substrate and first absorb and redistribute any static shock that comes in from the edge of the substrate.

[0074] The shift register wiring **61** includes a gate line and a source or drain line formed in each of the shift registers SR_1 through SR_{n+1}. The shifter register wiring **61** includes the extension portion **61***a* formed by extending an end thereof The extension portion **61***a* is overlapped by the second contact portion **81***b*, and the contact holes **72** expose the shift register wiring **61** multiple times. In addition, the first through n^{th} signal lines formed in the wiring unit LS are connected to deliver respective external signals to the bulk circuitry of each of the shift registers SR_1 through SR_{n+1}. When the first signal line **21** is the DC voltage signal line, it may be connected to serve as a static electricity absorbing and redistributing conductor for each of the shift registers SR_1 through SR_{n+1}.

[0075] Here, at least one of the second through n^{th} vertical signal lines **22-25** may be connected to each of the shift registers SR_1 through SR_{n+1} by at least one of second through n^{th} horizontal connection lines of similar structure to the detailed structure of the first horizontal connection line **81**. In FIG. **5** for example, the third vertical signal line **23** INT) is shown connected to SR_j by a third horizontal connection line **83**.

[0076] The third horizontal connection line **83** includes its own corresponding first contact portion **83***a* and a second contact portion **83***b*. The first contact portion **83***a* extends through plural dielectric layers (e.g., **30** and **70**) to contact the third vertical signal line **23** at multiple locations there-along. The second contact portion **83***b* is located between the n^{th} vertical signal line (**25**) and the left boundary each of the shift registers SR_1 through SR_{n+1} and is connected multiple times to each of the shift registers SR_1 through SR_{n+1} as is indicated in FIG. **5**.

[0077] In other words, the first contact portion **83***a* extends through plural ones of spaced apart contact holes **73** which expose the third signal line **23** in multiple places so as to thereby more assuredly connect its end of the third horizontal connection line **83** to the third vertical signal line **23**. The second contact portion **83***b* similarly overlaps an extension portion **62***a* formed by extending an end of a shift register wiring **62** and includes multiple spaced apart contact holes **74** exposing the shift register wiring **62** in different places so as to thereby more assuredly connect its end of the third horizontal connection line **83** to the corresponding extension portion **62***a* of the shift register wiring.

[0078] Although not shown in the drawings, the corresponding shift register wiring **62** is formed on the first insulating film **30** but does not extend directly over the third through n^{th} signal lines. In addition, the third horizontal connection line **83** is formed on the second insulating film **70** which is disposed above the first insulating film **30**. Since the first and second insulating films **30** and **70** are interposed between the third through n^{th} signal lines and the third connection line **83**, the third through n^{th} signal lines are located relatively far apart from the third connection line **83**. Accordingly, the third through n^{th} signal lines and the third connection line **83** can be prevented from being burned by static electricity flowing into the gate driver **400**.

[0079] The third vertical signal line **23** may be any type of signal line, such as the scan start signal line (STVP), the initialization signal line (INT), a first clock signal line (e.g., CKV), or a clock bar signal line (e.g., CKVB). In the embodiment of FIG. **5**, the third vertical connection line **23** is shown to be the initialization signal line. When the third signal line **23** is the initialization signal line, the shift register wiring **62** may be a gate line of transistor T**6**. This is because the initialization signal line is connected to the gate line of the T**6** transistor of each of the shift registers SR_1 through SR_{n+1}.

[0080] The n^{th} vertical signal line (e.g., the fifth signal line **25**) which is the last signal line and thus closest to the shift registers SR_1 through SR_{n+1} is connected to each of the shift registers SR_1 through SR_{n+1} by a shift register clock wiring **63** extending to the n^{th} signal line.

[0081] Specifically, as shown in FIG. **5**, the shift register wiring **63** is extended to the fifth signal line **25**, and the extended shift register wiring **63** and the fifth signal line **25** are connected to each other by a fifth and relatively short, horizontal connection line **95**. Here, an extension portion **63***a* is formed at an end of the extended shift register wiring **63**.

[0082] The fifth connection line **95** overlaps the fifth signal line **25** and overlaps the extension portion **63***a* of the shift register wiring **63**, and uses contact holes **75** and **76** to make contact with the underlying conductors. More specifically, the fifth signal line **25** and the shift register wiring **63** are connected by the contact holes **75** and **76**.

[0083] Although the shift register wiring **63** is extended to the n^{th} signal line (e.g., the fifth signal line **25**) which is the last signal line and closest to the shift registers SR_1 through SR_{n+1}, it is not formed directly above the first through n^{th} signal lines. Therefore, the shift register wiring **63** and the first through n^{th} signal lines are prevented from being burned by static electricity flowing into the gate driver **400**.

[0084] Hereinafter, another gate-line driver circuit and an LCD including the same according to another exemplary embodiment will be described with reference to FIGS. **7** and **8**. FIG. **7** is a layout diagram of a wiring unit LS of the second gate-line driver **400'** according to the second exemplary embodiment. FIG. **8** is a cross-sectional view of the wiring unit LS taken along the line II-II' of FIG. **7**. For simplicity, elements having the same functions as those of the previous exemplary embodiment of FIGS. **1** through **6** are indicated by like reference numerals, and thus their description will be omitted. The gate-line driver **400'** and the LCD according to the current exemplary embodiment have substantially the same structures as the gate driver **400** and the LCD **10** according to the previous exemplary embodiment, except for the connection structure between the wiring unit LS of the gate driver **400** and shift registers SR_1 through SR_{n+1}. Thus, the following description will focus on this difference.

[0085] The gate driver **400'** includes a circuit unit CS which includes a plurality of shift registers SR_1 through SR_{n+1} and the wiring unit LS which delivers various signals (Vss, STVP, INT, CKV, CKVB, etc.) to the shift registers SR_1 through SR_{n+1}.

[0086] The wiring unit LS includes first through n^{th} vertical signal lines, where n is a natural number. The first through n^{th} vertical signal lines extend parallel to each other in a substantially vertical direction. The first through n^{th} vertical signal lines are arranged sequentially in order of their distance from the shift registers SR_1 through SR_{n+1}, with the first vertical signal line being farthest from the shift registers SR_1 through SR_{n+1}.

[0087] A first vertical signal line **21** is connected to each of the shift registers SR_1 through SR_{n+1} by a relatively short sixth horizontal connection line **91**. Here, a shift register wiring **61** extends to the first signal line **21** and is connected to the relatively short sixth connection line **91**.

[0088] The Vss conveying shift register wiring **61** includes a vertically elongated extension portion **61***a* formed by extending an end thereof. The sixth connection line **91** overlaps the extension portion **61***a* and makes contact to it at plural points (**72**). The sixth connection line **91** also overlaps the first signal line **21** and makes contact to it at plural points (**71**). As seen, plural contact holes **71** and **72** are formed in regions in which the sixth connection line **91** overlaps the first signal line **21** and the extension portion **61***a*, respectively. The first signal line **21** (Vss) and the shift register wiring **61** are thus connected plural times to each other by means of the corresponding portions of the sixth connection line **91** where the latter extends in and out through the contact holes **71** and **72**.

[0089] Since the shift register wiring **61** extends to and contacts the first signal line **21**, as shown in FIG. **8**, the shift register wiring **61** extends closely under (bit not connected to) electrostatic bridge conductors **96** and **97** which are provided to overlap the shift register wiring **61** at predetermined regions of one or more of the second through n^{th} signal lines **22-25**. More specifically, in FIG. **8**, at least two of the second through n^{th} vertical signal lines (**22**, **23**) are forked and the space between the fork tongs is partially overlapped with the shift register wiring **61** while the forks are connected to one another by electrostatic bridge conductors **96** and **97** (also referred to herein as horizontal connection lines).

[0090] Thus in FIGS. **7** and **8**, each of a second vertical signal line **22** and a third vertical signal line **23** is divided into two sections (fork tongs) **22***a* and **22***b* of second vertical signal line **22**, or **23***a* and **23***b* of third vertical signal line **23** and the space between the two sections (fork tongs) is insulatively overlapped by the Vss-carrying shift register wiring **61**. Here, the second signal line **22** may be a scan start signal line, and the third signal line **23** may be an initialization signal line.

[0091] The two sections **22***a* and **22***b* of the second signal line **22** are connected by a **(7-1)**th horizontal connection line **96** (also called an electrostatic bridge conductor here), and the two sections **23***a* and **23***b* of the third signal line **23** are connected by a **(8-1)**th horizontal connection line **97** (also referenced to as a second electrostatic bridge conductor here). The **(7-1)**th connection line **96** extends into contact holes **77** and **78** formed to expose respective ends of the two sections **22***a* and **22***b* of the second signal line **22**, and the **(8-1)**th connection line **97** extends into contact holes **79** and **80** formed to expose respective ends of the two sections **23***a* and **23***b* of the third signal line **23**. The two sections **22***a* and **22***b* of the second signal line **22** are thus electrically connected or bridged to each other by the bridge **96** made between contact holes **77** and **78**, and the two sections **23***a* and **23***b* of the third signal line **23** are electrically connected or bridged to each other by the bridge **97** made between contact holes **79** and **80**.

[0092] Referring to the details of FIG. **8**, a first insulating film **30** is formed on the first through fifth vertical signal lines **21** through **25**, and the shift register wiring **61** extends on the first insulating film **30**. Here, the second vertical signal line **22** and the third vertical signal line **23** are not formed under regions of the shift register wiring **61** so that the second signal line **22** and the third signal line **23** are not directly overlapped with the shift register wiring **61** A second insulating film **70** is formed on the first insulating film **30** and on the shift register wiring **61**. The sixth connection line **91**, the **(7-1)**th connection line **96** and the **(8-1)**th connection line **97** are formed on the second insulating film **70**. The first insulating film **30** and the second insulating film **70** include contact holes **71**, **72**, **77**, **78**, **79** and **80** exposing the first through third signal lines **21** through **23** and the shift register wiring **61**. The respective two sections **22***a* and **22***b* of the second signal line **22** and the respective two sections **23***a* and **23***b* of the third signal line **23** are connected (bridged to each other) by the **(7-1)**th connection line **96** and the **(8-1)**th connection line **97**, respectively. The **(7-1)**th connection line **96** and the **(8-1)**th connection line **97** may be made of ITO or IZO As described above, in the current exemplary embodiment, the shift register wiring **61** is extended to and connected to the first signal line **21**. In addition, a signal line located under the extended shift register wiring **61** is divided into two spaced apart sections (fork tongs) where the spacing is overlapped by the shift register wiring **61**, and the two sections are connected to each other (bridged) by a connection line formed on the shift register wiring **61**.

[0093] Here, since the non-grounded vertical signal line (e.g., **22** or **23**) is not formed directly under the shift register wiring **61**, static electricity that may flow into the gate-line driver circuit **400** by way of one of the non-grounded vertical signal lines (e.g., **22** or **23**) does not dissipate its energy by burning out the signal line or the shift register wiring **61** but instead does so more preferentially by burning out the sacrificial fuse provided by one of the electrostatic bridge conductors or by dissipated itself into the wide conductive region provided by the outermost and first vertical signal line **21**. In other words, due to the process of forming the sacrificial connection lines (e.g., **96**, **97**) on the second insulating film **70**, the shift register wiring **61** and the main vertical connection lines (e.g., **22**, **23**) are prevented from being burned by the static electricity.

[0094] A gate driver circuit according to an exemplary embodiment of the present disclosure is thus structured such that its elements are prevented from being burned by static electricity which might flow into the gate driver circuit in the process of forming (e.g., assembling) the Liquid Crystal Display (LCD) device.

[0095] Thus an LCD device according to an exemplary embodiment of the present disclosure includes a gate driver circuit formed on a substrate and structured to prevent its active elements and/or the vertical signal lines (e.g., **22-25**) that connect to the gate driver circuit from being burned by static electricity that may flow into the LCD device from activities occurring in the manufacturing facilities or elsewhere. Accordingly, productivity can be improved, and costs are reduced.

[0096] While the present disclosure of invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood in light of the foregoing by those of ordinary skill in the art that various changes in form and detail may be made without departing from the spirit and scope of the present teachings. The exemplary embodiments should be considered in a descriptive sense only and not for purposes of limitation.

What is claimed is:

1. A gate-lines driver circuit comprising:

a wiring unit which is structured and laid out on a substrate to receive signals from one or more external sources; and

a circuit unit which is laid out on the substrate adjacent to the wiring unit and which is structured to output driving signals to corresponding gate lines of the display device in response to control signals received from the one or more external sources and by way of the wiring unit, where the circuit unit comprises a plurality of shift registers each having respective shift register wirings,

wherein the wiring unit comprises first through n-th signal lines spaced apart from one another and arranged sequentially to thus define an ordering of distance from the shift registers of the adjacent circuit unit, with the first vertical signal line being located farthest from the shift registers and the nth being closest, where n is a natural number greater than two, wherein the first signal line is connected to each of the shift registers by a first connection line, where the first connection line includes a first contact portion which is formed above and connecting to on the first signal line and where the first **1** connection line includes a second contact portion which is located between the n-th signal line and the shift registers and which connects thereat to respective shift register wirings of one or more of the shift registers of the adjacent circuit unit.

2. The gate-lines driver circuit of claim **1** and further comprising:

a first insulating film formed on the first through n-th signal lines, where the shift register wiring is formed on the first insulating film; and

a second insulating film disposed on the first insulating film, where the first connection line is formed on the second insulating film.

3. The gate-lines driver circuit of claim **1**, wherein the first connection line is made of indium tin oxide (ITO) or indium zinc oxide (IZO).

4. The gate-lines driver circuit of claim **1**, wherein the first signal line is a direct current (DC) voltage conveying signal line which is connected to receive a DC reference voltage signal from an external source.

5. The gate-lines driver circuit of claim **1**, wherein the shift register wiring to which the first connection line connects is a contiguous extension of a transistor gate line or a transistor source or drain line of at least one of the shift registers of the adjacent circuit unit.

6. The gate-lines driver circuit of claim **1**, wherein at least one of the second through n-th signal lines is connected to a corresponding one or more of the shift registers by a respective at least one of second through n-th **1** connection lines, where the at least one non-first horizontal connection line has a respective first contact portion which contacts the corresponding non-first signal line and a second contact portion which is located between the n-th signal line and the corresponding one or more shift registers and which connects thereat to corresponding shift register wiring of the corresponding one or more shift registers.

7. The gate-lines driver circuit of claim **1**, wherein the first through n-th vertical signal lines comprise a DC voltage signal line which receives a DC voltage from an external source, a scan start signal line which receives a start signal for starting an operation of the circuit unit, a clock signal line which receives a clock signal, a clock bar signal which receives a clock bar signal, and an initialization signal line which receives an initialization signal.

8. A driver circuit comprising:

a wiring unit which is structured to receive and convey signals provided from an external source; and

a circuit unit which is structured to output a sequence of driving signals in response to plural control signals received from and conveyed to the circuit unit by the wiring unit, where the circuit unit is disposed on a substrate adjacent to the wiring unit and the circuit unit comprises a plurality of shift registers, each having respective shift register wirings,

wherein the wiring unit comprises first through n-th signal lines spaced apart from one another and arranged sequentially to thereby define an ordering of distance from the shift registers of the adjacent circuit unit, with the first signal line being located farthest from the shift registers, where n is a natural number,

wherein the first signal line is connected to each of the shift registers by a shift register wiring extending to the first signal line,

wherein at least one of the second through n-th signal lines is divided into two spaced apart sections between which part of the shift register wiring is insulatively disposed, and the two sections which are separated from each other are electrically connected by a bridging connection line having contact portions and extending insulatively over the shift register wiring.

9. The driver circuit of claim **8** and further comprising:

a first insulating film is formed on the second through n-th signal lines, where the shift register wiring is formed on the first insulating film; and

a second insulating film disposed on the first insulating film, where the connection line is formed on the second insulating film.

10. The driver circuit of claim **8**, wherein the contact portions are respectively formed on respective ends of the two sections which are close to the shift register wiring.

11. The driver circuit of claim **8**, wherein the connection line is made of ITO or IZO.

12. The driver circuit of claim **8**, wherein the shift register wiring is an extension of a transistor gate line or of a transistor source or drain line provided in at least one of each of the shift registers.

13. The driver circuit of claim **8**, wherein the first signal line is a DC voltage signal line which receives a DC voltage signal from an external source.

14. The driver circuit of claim **8**, wherein each of the second signal line and the third signal line is divided into two sections which are separated from each other and extend in directions so as to have centered there between the shift register wiring wherein the second signal line is a scan start signal line which receives a start signal for starting an operation of the circuit unit, and the third signal line is an initialization signal line which receives an initialization signal.

15. The driver circuit of claim **8**, wherein the first through n-th signal lines comprise a DC voltage signal line which receives a DC voltage from an external source, a scan start signal line which receives a start signal for starting the operation of the circuit unit, a clock signal line which receives a clock signal, a clock bar signal which receives a clock bar signal, and an initialization signal line which receives an initialization signal.

16. A liquid crystal display (LCD) device comprising a gate-lines driver circuit formed on a substrate, wherein the gate-lines driver circuit comprises:

a wiring unit which is disposed on the substrate and is structured to receive signals from an external source; and

a circuit unit which is disposed on the substrate, adjacent to the wiring unit and is structured to output driving signals in response to a plurality of control signals received from the wiring unit and where the circuit unit comprises a plurality of shift registers, each having shift register wirings,

wherein the wiring unit comprises first through n-th signal lines arranged sequentially in an order of distance from the shift registers, with the first signal line being located farthest from the shift registers, where n is a natural number, wherein the first signal line is connected to each of the shift registers by a first connection line, and the first connection line comprises a first contact portion which is formed to contact the first signal line and a second contact portion which is located between the n-th signal line and each of the shift registers and is connected to each of the shift registers by a shift register wiring.

17. The LCD device of claim **16**, wherein the substrate is divided into a display region in which an image is displayed and a non-display region in which the image is not displayed, wherein the gate driver is formed in the non-display region.

18. The LCD device of claim **16** and further comprising:

a first insulating film is formed on the first through n-th signal lines, where the shift register wiring is formed on the first insulating film, and

a second insulating film which disposed on the first insulating film, where the first connection line is formed on the second insulating film.

19. The LCD device of claim **16**, wherein the shift register wiring is formed of an extension of at least one a transistor gate line or a transistor source or drain line of one of the shift registers.

20. An LCD device comprising a gate-lines driver circuit formed on a substrate, wherein the gate-lines driver circuit comprises:

a wiring unit which is structured to receive signals from an external source; and

a circuit unit which is structured to output driving signals in response to a plurality of control signals received from the wiring unit and comprises a plurality of shift registers, each having shift register wirings,

wherein the wiring unit comprises first through n-th signal lines arranged sequentially in order of distance from the shift registers, with the first signal line being located farthest from the shift registers, where n is a natural number, wherein the first signal line is connected to each of the shift registers by a shift register wiring extending to the first signal line, at least one of the second through n-th signal lines is divided into two spaced apart sections having centered there between the shift register wiring, and the two spaced apart sections which are electrically connected by a bridging connection line having contact portions.

* * * * *

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专利名称(译)	栅极驱动器和包括其的液晶显示器		
公开(公告)号	[US20120098800A1]()	公开(公告)日	2012-04-26
申请号	US13/070394	申请日	2011-03-23
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优先权	1020100102434 2010-10-20 KR		
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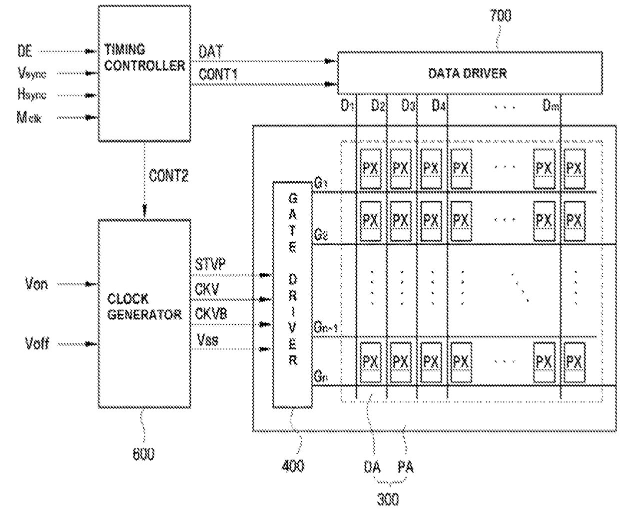
摘要(译)

提供一种栅极线驱动电路和包括该栅极线驱动电路的液晶显示（LCD）装置。栅极线驱动器可能存在受到静电的危险，并且它包括：接收来自外部源的信号的布线单元和响应于从布线单元接收的多个控制信号输出驱动信号的电路单元。 。电路单元包括多个移位寄存器，每个移位寄存器具有移位寄存器布线，其中布线单元包括按照与移位寄存器的距离的顺序依次排列的第一至第n垂直信号线，第一垂直信号线位于距离移位寄存器最远的位置。移位寄存器。第一垂直信号线通过第一水平连接线连接到每个移位寄存器，第一水平连接线包括形成在第一信号线上并与第一信号线接触的第一接触部分和位于第二接触部分的第二接触部分在第n垂直信号线和移位寄存器的边界之间，通过移位寄存器布线连接到每个移位寄存器。第一水平连接线被构造成降低由通过布线单元接收的静电电流的浪涌烧掉的移位寄存器的危险。



TIMING CONTROLLER
DE
Vsync
Hsync
Mclk
DAT
CONT1
700
DATA DRIVER
D1
D2
D3
D4
Dm
CONT2
CLOCK GENERATOR
Von
Voff
STVP
CKV
CKVB
Vss
GATE DRIVER
G1
G2
Gn-1
Gn
PX
600
400
DA
PA
300