



US 20170357134A1

(19) **United States**(12) **Patent Application Publication**
WANG et al.(10) **Pub. No.: US 2017/0357134 A1**(43) **Pub. Date: Dec. 14, 2017**(54) **ARRAY SUBSTRATE AND LIQUID CRYSTAL
DISPLAY DEVICE COMPRISING THE SAME**(71) Applicants: **Shenzhen China Star Optoelectronics
Technology Co., Ltd.**, Shenzhen (CN);
**Wuhan China Star Optoelectronics
Technology Co., Ltd.**, Wuhan (CN)(72) Inventors: **Cong WANG**, Shenzhen (CN); **Peng
DU**, Shenzhen (CN)(73) Assignees: **Shenzhen China Star Optoelectronics
Technology Co., Ltd.**, Shenzhen (CN);
**Wuhan China Star Optoelectronics
Technology Co., Ltd.**, Wuhan (CN)(21) Appl. No.: **14/907,915**(22) PCT Filed: **Dec. 8, 2015**(86) PCT No.: **PCT/CN2015/096676**

§ 371 (c)(1),

(2) Date: **Aug. 29, 2017**(30) **Foreign Application Priority Data**

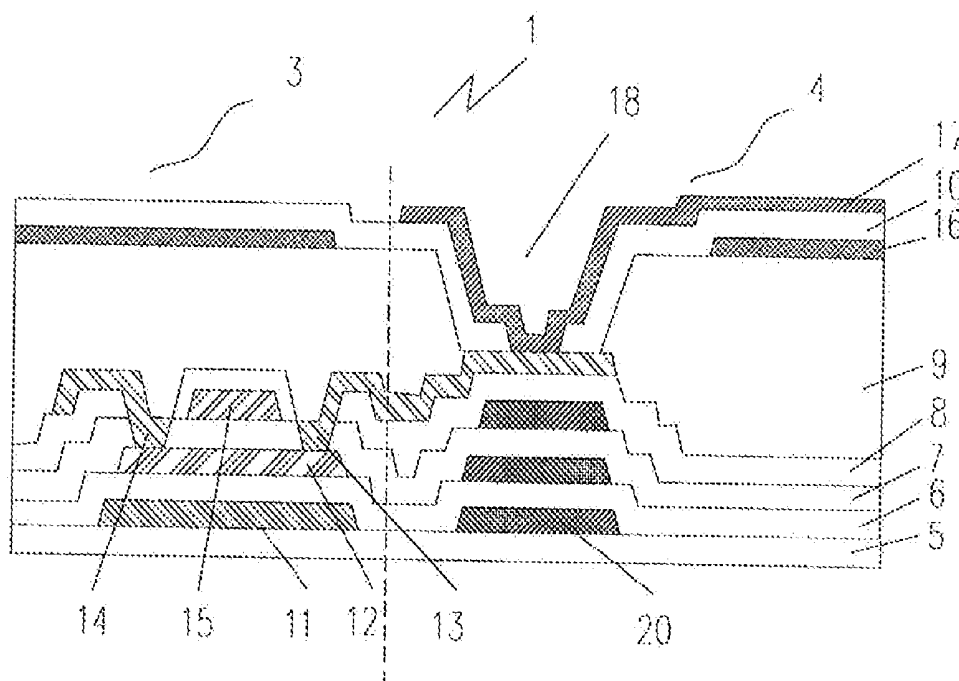
Oct. 10, 2015 (CN) 201510652234.9

Publication Classification(51) **Int. Cl.****G02F 1/1362** (2006.01)**G02F 1/1368** (2006.01)**G02F 1/1343** (2006.01)**H01L 27/12** (2006.01)(52) **U.S. Cl.**CPC .. **G02F 1/136227** (2013.01); **G02F 1/134309**
(2013.01); **G02F 1/1368** (2013.01); **G02F**
1/136209 (2013.01); **G02F 2202/104**
(2013.01); **G02F 2201/121** (2013.01); **G02F**
2001/13685 (2013.01); **H01L 27/1248**
(2013.01); **G02F 2201/123** (2013.01); **H01L**
27/124 (2013.01)

(57)

ABSTRACT

An array substrate and a liquid crystal display device comprising the array substrate are disclosed. The array substrate comprises a pixel unit having a thin film transistor region and a through-hole region. The pixel unit comprises a glass substrate, a first insulation layer, a second insulation layer, a third insulation layer, a fourth insulation layer, and a fifth insulation layer stacked from bottom up in sequence. In the thin film transistor region, the glass substrate is provided with a light-shading metal member that is covered by the first insulation layer, the first insulation layer is provided with an active layer that is covered by the second insulation layer, two ends of the active layer are respectively connected with a source and a drain formed between the third insulation layer and the fourth insulation layer, the second insulation layer is provided with a gate that is covered by the third insulation layer, and the fourth insulation layer is provided with a common electrode that is covered by the fifth insulation layer. In the through-hole region, a pixel electrode is arranged on the fifth insulation layer and a through hole is configured in the fourth insulation layer, so that the pixel electrode is connected with the source or the drain after passing through the fifth insulation layer. A cushion layer is arranged under the through hole in an insulated manner.



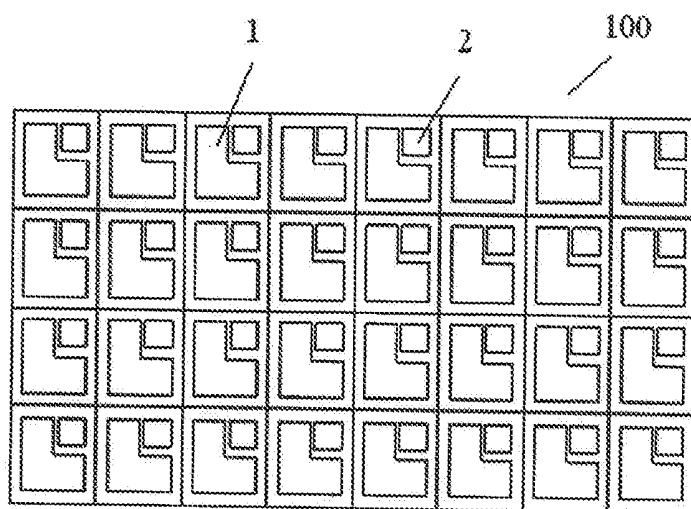


Fig. 1

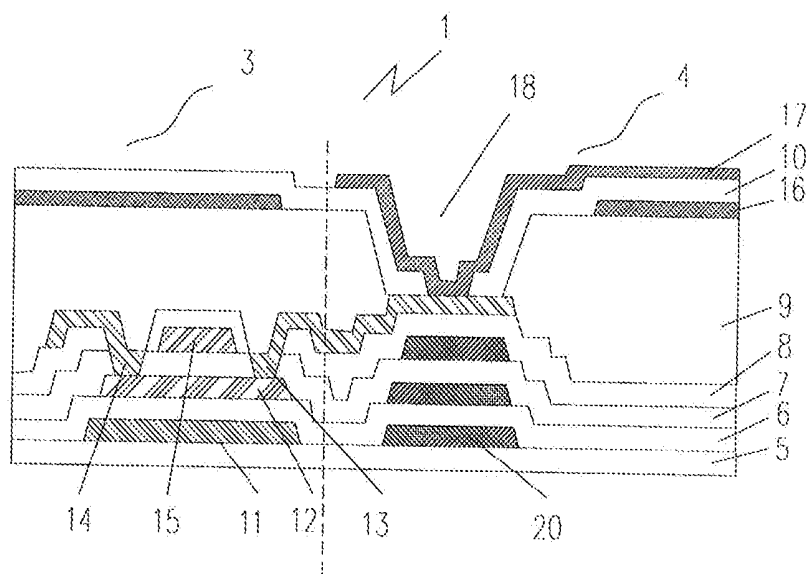


Fig. 2

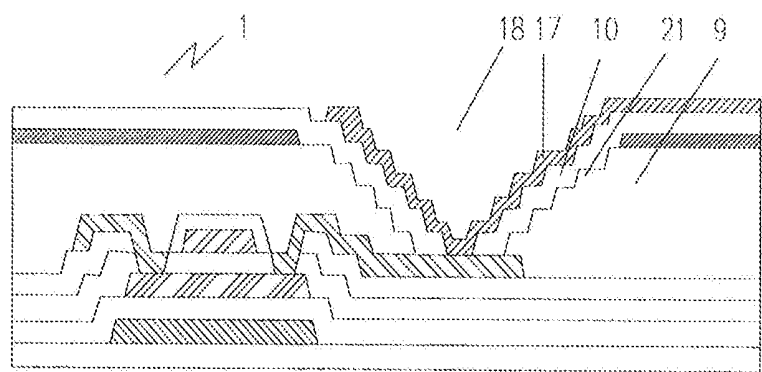


Fig. 3

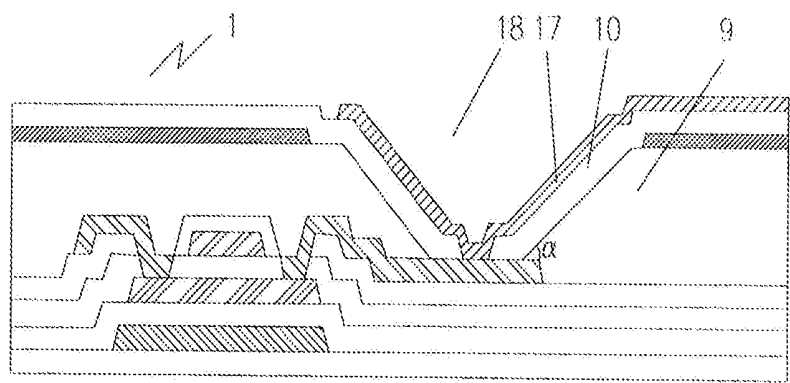


Fig. 4

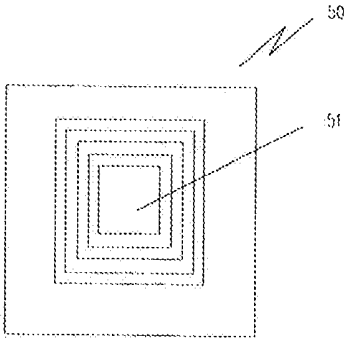


Fig. 5

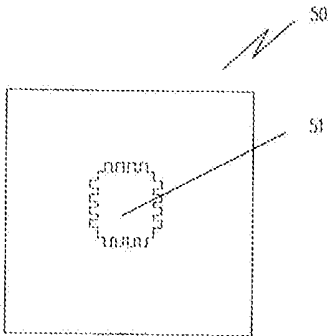


Fig. 6

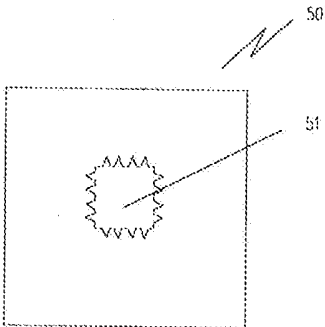


Fig. 7

ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE COMPRISING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims the priority of Chinese patent application CN201510652234.9, entitled “array substrate and liquid crystal display device comprising the same” and filed on Oct. 10, 2015, the entirety of which is incorporated herein by reference.

TECHNICAL FIELD

[0002] The present disclosure relates to the technical field of display, in particular to an array substrate and a liquid crystal display device comprising the array substrate.

TECHNICAL BACKGROUND

[0003] During designing and manufacturing procedure of a low temperature poly-silicon panel, if a film surface on a side of an array substrate is irregular, poor alignment of liquid crystal of a liquid crystal display device would occur.

[0004] In the prior art, a thickness of an insulation layer between a common electrode and a source/drain is usually increased so as to flatten the film surface and improve the alignment performance of liquid crystal. However, since the insulation layer has a relative larger thickness compared with other film layers, it is necessary to arrange a via hole in the insulation layer when the source/drain of a thin film transistor breakerover needs to be connected with a pixel electrode. Because the insulation layer is made from high molecular material and comprises relatively deep via holes, in the preparation procedure, it will be easy for the insulation layer to be separated from a film layer which is originally in contact with the insulation layer. As a result, the pixel electrode and the source or the drain would have a poor contact or even be disconnected from each other, thereby affecting normal display of the liquid crystal display device. In this case, the thickness of the insulation layer should be reduced so as to lower the risk of poor contact. However, if the thickness of the insulation layer is reduced, a flatness of the insulation layer would be affected, which would causes poor alignment of the liquid crystal.

[0005] In this case, a new array substrate that can improve the contact between the pixel electrode and the source/drain without affecting the flatness of the insulation layer is needed.

SUMMARY OF THE INVENTION

[0006] Directed at the technical problems in the prior art, the present disclosure provides an array substrate and a liquid crystal display device comprising the array substrate. The array substrate according to the present disclosure can not only guarantee a flatness of an insulation layer, so as to satisfy requirements for an alignment of liquid crystal, but also improve contact between a pixel electrode and a source/drain, thereby improving a display performance of the liquid crystal display device.

[0007] According to one aspect of the present disclosure, an array substrate is provided. The array substrate comprises a pixel unit having a thin film transistor region and a through-hole region. The pixel unit comprises a glass substrate, a first insulation layer, a second insulation layer, a third insulation layer, a fourth insulation layer, and a fifth

insulation layer stacked from bottom up in sequence. In the thin film transistor region, the glass substrate is provided with a light-shading metal member that is covered by the first insulation layer, the first insulation layer is provided with an active layer that is covered by the second insulation layer, two ends of the active layer are respectively connected with a source and a drain formed between the third insulation layer and the fourth insulation layer, the second insulation layer is provided with a gate that is covered by the third insulation layer, and the fourth insulation layer is provided with a common electrode that is covered by the fifth insulation layer. In the through-hole region, a pixel electrode is arranged on the fifth insulation layer and a through hole is configured in the fourth insulation layer, so that the pixel electrode is connected with the source or the drain after passing through the fifth insulation layer. A cushion layer is arranged under the through hole in an insulated manner.

[0008] In an embodiment, the cushion layer is a metal layer, and at least one metal layer that corresponds to the light-shading metal member, the active layer or the gate is arranged under the through hole.

[0009] In an embodiment, three metal layers that respectively correspond to the light-shading metal member, the active layer and the gate are arranged under the through hole.

[0010] In an embodiment, the metal layers are formed by a same procedure as the corresponding light-shading metal member, the active layer or the gate.

[0011] In an embodiment, an inner wall of the through hole is structured as stepladder, and the fifth insulation layer and the pixel electrode are both structured to match the stepladder through hole.

[0012] In an embodiment, teeth of the stepladder through hole are distributed in a uniform manner.

[0013] In an embodiment, the through hole is formed by an exposure process and a light transmittance of a photomask for forming the through hole gradually decreases from a central part to a peripheral part thereof.

[0014] In an embodiment, a taper angle of the through hole is structured in a range from 45° to 50°.

[0015] In an embodiment, the through hole is formed by an exposure process, and a photomask for forming the through hole comprises a cut-out with a wall thereof being structured as a tooth.

[0016] According to the other aspect of the present disclosure, a liquid crystal display device comprising said array substrate is provided.

[0017] Compared with the prior art, the present disclosure has the following advantages. Through arranging a cushion layer under the through hole, a thickness under the through hole can be increased, thereby reducing a depth of the through hole without changing the fourth insulation layer. Therefore, poor contact or even disconnection between the pixel electrode and the source or the drain can be effectively alleviated, and a qualified rate of the liquid crystal display device can be improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] A brief introduction will be provided below to the accompanying drawings involved in the embodiments. In the drawings:

[0019] FIG. 1 shows an array substrate according to an embodiment of the present disclosure;

[0020] FIG. 2 shows a pixel unit according to a first embodiment of the present disclosure;

[0021] FIG. 3 shows a pixel unit according to a second embodiment of the present disclosure;

[0022] FIG. 4 shows a pixel unit according to a third embodiment of the present disclosure;

[0023] FIG. 5 shows a photomask according to the first embodiment of the present disclosure;

[0024] FIG. 6 shows a photomask according to the second embodiment of the present disclosure; and

[0025] FIG. 7 shows a photomask according to the third embodiment of the present disclosure.

[0026] In the drawings, the same components are indicated with the same reference sign. The drawings are not drawn to actual scale.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0027] The present disclosure will be further described in view of the accompanying drawings.

[0028] FIG. 1 shows an array substrate 100 according to the present disclosure. The array substrate 100 comprises a plurality of pixel units 1 (i.e., sub pixel units) distributed as an array. Each pixel unit 1 is comprised of a thin film transistor 2, a pixel electrode 17 (as shown in FIG. 2), a common electrode 16 (as shown in FIG. 2) and a storage capacitor (not shown herein). The thin film transistor 2 is a low temperature poly-silicon (hereinafter referred to as LTPS) thin film transistor, which has a higher carrier mobility ratio compared with traditional amorphous silicon (a-Si) thin film transistor, and thus higher resolution and lower power consumption, as well as a higher integration level of members on the array substrate can be realized.

[0029] As shown in FIG. 2, the pixel unit 1 comprises a glass substrate 5, a first insulation layer 6, a second insulation layer 7, a third insulation layer 8, a fourth insulation layer 9, and a fifth insulation layer 10 stacked from bottom up in sequence. In a thin film transistor region 3, the glass substrate 5 is provided with a light-shading metal member 11, and the light-shading metal member 11 can be covered by the first insulation layer 6. The first insulation layer 6 is provided with an active layer 12, and the active layer 12 can be covered by the second insulation layer 7. A source 13 and a drain 14 are formed between the third insulation layer 8 and the fourth insulation layer 9, and the source 13 and the drain 14 are respectively arranged at two ends of the active layer 12. The second insulation layer 7 is provided with a gate 15 that can be covered by the third insulation layer 8. The fourth insulation layer 9 is provided with the common electrode 16 that can be covered by the fifth insulation layer 10. In the through-hole region 4, the pixel electrode 17 is arranged on the fifth insulation layer 10. A through hole 18 is configured in the fourth insulation layer 9, so that the pixel electrode 17 is connected with the source 13 or the drain 14 after passing through the fifth insulation layer 10. A cushion layer for reducing a depth of the through hole 18 is arranged under the through hole 18 in an insulated manner. In this case, disconnection between the pixel electrode 17 and the source 13 or the drain 14 can be alleviated or even avoided, thereby guaranteeing a firm contact between the pixel electrode 17 and the source 13 or the drain 14. Therefore, a qualified rate of the array substrate 100 can be guaranteed.

[0030] According to an embodiment of the present disclosure, the cushion layer is configured as a metal layer 20

arranged under the through hole 18. The metal layer 20 is insulated from outside environment. That is, no signal is provided to the metal layer 20, which only acts as a member to increase a thickness of a layer under the through hole 18, so that a depth of the through hole 18 decreases without changing the fourth insulation layer 9. If the through hole 18 is too deep, the fourth insulation layer 9 and the fifth insulation layer 10 are easily separated from each other, which would cause disconnection or poor contact between the pixel electrode 17 and the source 13 or the drain 14. With the abovementioned arrangement, the depth of the through hole 18 can be effectively reduced, and thus the disconnection or poor contact risk can be effectively reduced or even avoided. Therefore, with the arrangement of the metal layer 20, a safety of connection between the pixel electrode 17 and the source 13 or the drain 14 can be improved. In addition, such arrangement has a simple structure and can be realized easily.

[0031] Preferably, at least one metal layer 20 corresponding to the light-shading metal member 11, the active layer 12 or the gate 15 is arranged under the through hole 18. For example, one metal layer 20 can be arranged under the through hole 18, and the metal layer 20 corresponds to one of the light-shading metal member 11, the active layer 12 and the gate 15. Alternatively, two metal layers 20 can be arranged under the through hole 18, and the metal layers 20 respectively correspond to two of the light-shading metal member 11, the active layer 12 and the gate 15. Of course, three metal layers 20 can be arranged under the through hole 18, the metal layers 20 respectively correspond to the light-shading metal member 11, the active layer 12 and the gate 15, and are respectively arranged between adjacent first insulation layer 6, second insulation layer 7 and third insulation layer 8.

[0032] Further preferably, the metal layer 20 is formed by a same procedure as the corresponding light-shading metal member 11, the active layer 12 or the gate 15. In this manner, the metal layer 20 can be formed simultaneously with the light-shading metal member 11, the active layer 12 or the gate 15 through a photoetching technology. In this case, the metal layer 20 can be manufactured through the existing production technology and procedure, whereby not only the goal of preventing disconnection according to the present disclosure can be reached, but also a production efficiency can be improved and a production cost can be reduced.

[0033] As shown in FIG. 3, an inner wall of the through hole 18 is structured as stepladder. That is, the inner wall of the through hole 18 is structured as a stepladder with teeth 21. Correspondingly, the fifth insulation layer 10 and the pixel electrode 17 are both structured to match the stepladder through hole 18. Through such arrangement, a contact area between the fifth insulation layer 10 and the fourth insulation layer 9 and a contact area between the fifth insulation layer 10 and the pixel electrode 17 can both be increased. Under the condition that the depth of the through hole 18 does not change, the larger the contact area between the fifth insulation layer 10 and the fourth insulation layer 9 and the contact area between the fifth insulation layer 10 and the pixel electrode 17, the smaller a deformation of the fifth insulation layer 10 and the pixel electrode 17, and the more difficult for the fifth insulation layer 10 and the fourth insulation layer 9 to be separated from the pixel electrode 17. Therefore, the risk of disconnection between the pixel electrode 17 and the source 13 or the drain 14 can be

effectively reduced or prevented. In order to facilitate manufacturing and reduce production cost, the teeth 21 of the stepladder through hole 18 are distributed in a uniform manner, thereby reducing production difficulty.

[0034] For example, the through hole 18 with teeth 21 can be formed by an exposure procedure. In a production procedure, a photomask 50 can be used to form the through hole 18 as shown in FIG. 3. The photomask 50 has a cut-out 51 therein. A size of the cut-out 51 matches a shape of an opening on a lower end of the through hole 18 and a light transmittance of the photomask 50 gradually decreases from the cut-out 51 to a peripheral part thereof (the frames in FIG. 5 schematically show the difference of light transmittance from a central part of the mask 50 to a peripheral part thereof). In this manner, a through hole 18 as shown in FIG. 3 can be formed after etching procedure.

[0035] It should be noted that, since the metal layer 20 is arranged under the through hole 18 and the through hole 18 is configured as a stepladder, the risk of disconnection between the pixel electrode 17 and the source 13 or the drain 14 can be further reduced or prevented. That is, a firmness and security of the connection between the pixel electrode 17 and the source 13 or the drain 14 can be improved. Of course, if the array substrate 100 comprises only the stepladder through hole 18 or only the metal layer 20, the effect of improving security of connection between the pixel electrode 17 and the source 13 or the drain 14 can also be achieved.

[0036] As shown in FIG. 4, a taper angle α of the through hole 18 is structured in a range from 45° to 50° . In the prior art, the taper angle α is about 56° . When the depth of the through hole 18 does not change, the larger the taper angle α , the smaller the contact area between the fourth insulation layer 9 and the fifth insulation layer 10, and the easier for the fifth insulation layer 10 to be separated from the fourth insulation layer 9 and the pixel electrode 17. In this case, by reducing the taper angle α to a range from 45° to 50° , the contact area between fourth insulation layer 9 and the fifth insulation layer 10 can be increased, and a climbing angle of the fifth insulation layer 10 relative to the fourth insulation layer 9 can be reduced and increasing the contact area therebetween. As a result, the risk of disconnection between the pixel electrode 17 and the source 13 or the drain 14 can be reduced or prevented.

[0037] For example, the through hole 18 can be formed by an exposure procedure. The photomask 50 used for forming the through hole 18 has a cut-out 51 and a wall of the cut-out 51 is structured as teeth, as shown in FIGS. 6 and 7. In a production procedure, since the wall of the cut-out 51 is structured as teeth, under light irradiation, teeth-like slits around the cut-out 51 of the photomask 50 would form slit diffraction, such that the periphery of the through hole 18 allows slight transmittance of light. After etching procedure, the taper angle α would become smaller.

[0038] It should be noted that, since the metal layer 20 is arranged under the through hole 18, and the taper angle α is configured in a range from 45° to 50° , the risk of disconnection between the pixel electrode 17 and the source 13 or the drain 14 can be further reduced or prevented. That is, a firmness and security of connection between the pixel electrode 17 and the source 13 or the drain 14 can be improved. Of course, as shown in FIG. 4, in the array substrate 100, the risk of disconnection can also be reduced by only configuring the taper angle α in a range from 45° to 50° . In a word,

in order to reach the goal of ensuring solid connection between the pixel electrode 17 and the source 13 or the drain 14, the three techniques, i.e., arranging the cushion layer, configuring the inner wall of the through hole 18 as a stepladder, and arranging a taper angle, can be selected separated or simultaneously according to actual needs.

[0039] The present disclosure further comprises a liquid crystal display device (not shown in the drawings). The liquid crystal display device comprises said array substrate 100. Of course, the liquid crystal display device further comprises some other members and structures, which are well known to the person skilled in the art, and thus will not be described in detail.

[0040] Although the present disclosure has been described in view of preferred embodiments, the scope of the present disclosure is not limited hereto. Various modifications and variants to the present disclosure may be made by anyone skilled in the art, without departing from the scope and spirit of the present disclosure. Therefore, the scope of the present disclosure is subject to the scope of the claims.

1. An array substrate, comprising a pixel unit having a thin film transistor region and a through-hole region,

wherein the pixel unit comprises a glass substrate, a first insulation layer, a second insulation layer, a third insulation layer, a fourth insulation layer, and a fifth insulation layer stacked from bottom up in sequence;

wherein in the thin film transistor region, the glass substrate is provided with a light-shading metal member that is covered by the first insulation layer, the first insulation layer is provided with an active layer that is covered by the second insulation layer, two ends of the active layer are respectively connected with a source and a drain formed between the third insulation layer and the fourth insulation layer, the second insulation layer is provided with a gate that is covered by the third insulation layer, and the fourth insulation layer is provided with a common electrode that is covered by the fifth insulation layer;

wherein in the through-hole region, a pixel electrode is arranged on the fifth insulation layer and a through hole is configured in the fourth insulation layer, so that the pixel electrode is connected with the source or the drain after passing through the fifth insulation layer; and

wherein a cushion layer is arranged under the through hole in an insulated manner.

2. The array substrate according to claim 1, wherein the cushion layer is a metal layer, and at least one metal layer that corresponds to the light-shading metal member, the active layer or the gate is arranged under the through hole.

3. The array substrate according to claim 2, wherein three metal layers that respectively correspond to the light-shading metal member, the active layer and the gate are arranged under the through hole.

4. The array substrate according to claim 3, wherein the metal layers are formed by a same procedure as the corresponding light-shading metal member, the active layer or the gate.

5. The array substrate according to claim 1, wherein an inner wall of the through hole is structured as stepladder, and the fifth insulation layer and the pixel electrode are both structured to match the stepladder through hole.

6. The array substrate according to claim 2, wherein an inner wall of the through hole is structured as stepladder, and

the fifth insulation layer and the pixel electrode are both structured to match the stepladder through hole.

7. The array substrate according to claim 3, wherein an inner wall of the through hole is structured as stepladder, and the fifth insulation layer and the pixel electrode are both structured to match the stepladder through hole.

8. The array substrate according to claim 4, wherein an inner wall of the through hole is structured as stepladder, and the fifth insulation layer and the pixel electrode are both structured to match the stepladder through hole.

9. The array substrate according to claim 5, wherein teeth of the stepladder through hole are distributed in a uniform manner.

10. The array substrate according to claim 6, wherein teeth of the stepladder through hole are distributed in a uniform manner.

11. The array substrate according to claim 7, wherein teeth of the stepladder through hole are distributed in a uniform manner.

12. The array substrate according to claim 8, wherein teeth of the stepladder through hole are distributed in a uniform manner.

13. The array substrate according to claim 9, wherein the through hole is formed by an exposure process and a light transmittance of a photomask for forming the through hole gradually decreases from a central part to a peripheral part thereof.

14. The array substrate according to claim 1, wherein a taper angle of the through hole is structured in a range from 45° to 50°.

15. The array substrate according to claim 2, wherein a taper angle of the through hole is structured in a range from 45° to 50°.

16. The array substrate according to claim 3, wherein a taper angle of the through hole is structured in a range from 45° to 50°.

17. The array substrate according to claim 4, wherein a taper angle of the through hole is structured in a range from 45° to 50°.

18. The array substrate according to claim 14, wherein the through hole is formed by an exposure procedure, and a photomask for forming the through hole comprises a cut-out with a wall thereof being structured as a tooth.

19. The array substrate according to claim 15, wherein the through hole is formed by an exposure procedure, and a photomask for forming the through hole comprises a cut-out with a wall thereof being structured as a tooth.

20. A liquid crystal display device, comprising an array substrate, which comprises a pixel unit having a thin film transistor region and a through-hole region,

wherein the pixel unit comprises a glass substrate, a first insulation layer, a second insulation layer, a third insulation layer, a fourth insulation layer, and a fifth insulation layer stacked from bottom up in sequence; wherein in the thin film transistor region, the glass substrate is provided with a light-shading metal member that is covered by the first insulation layer, the first insulation layer is provided with an active layer that is covered by the second insulation layer, two ends of the active layer are respectively connected with a source and a drain formed between the third insulation layer and the fourth insulation layer, the second insulation layer is provided with a gate that is covered by the third insulation layer, and the fourth insulation layer is provided with a common electrode that is covered by the fifth insulation layer;

wherein in the through-hole region, a pixel electrode is arranged on the fifth insulation layer and a through hole is configured in the fourth insulation layer, so that the pixel electrode is connected with the source or the drain after passing through the fifth insulation layer; and wherein a cushion layer is arranged under the through hole in an insulated manner.

* * * * *

专利名称(译)	阵列基板和包括其的液晶显示装置		
公开(公告)号	US20170357134A1	公开(公告)日	2017-12-14
申请号	US14/907915	申请日	2015-12-08
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司 武汉华星光电技术有限公司		
申请(专利权)人(译)	深圳市中国星光电科技有限公司. 中国武汉恒星光电科技有限公司.		
当前申请(专利权)人(译)	深圳市中国星光电科技有限公司. 中国武汉恒星光电科技有限公司.		
[标]发明人	WANG CONG DU PENG		
发明人	WANG, CONG DU, PENG		
IPC分类号	G02F1/1362 G02F1/1368 G02F1/1343 H01L27/12		
CPC分类号	G02F1/136227 G02F1/136209 G02F1/1368 G02F1/134309 G02F2201/123 H01L27/1248 G02F2202/104 G02F2001/13685 G02F2201/121 H01L27/124 G02F1/133345 H01L29/78633		
优先权	201510652234.9 2015-10-10 CN		
其他公开文献	US10162236		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种阵列基板和包括该阵列基板的液晶显示装置。阵列基板包括具有薄膜晶体管区域和通孔区域的像素单元。像素单元包括玻璃基板，第一绝缘层，第二绝缘层，第三绝缘层，第四绝缘层和从下向上依次堆叠的第五绝缘层。在薄膜晶体管区域中，玻璃基板设置有遮光金属构件，该遮光金属构件被第一绝缘层覆盖，第一绝缘层设置有被第二绝缘层覆盖的有源层，两端为有源层分别与形成于第三绝缘层与第四绝缘层之间的源极和漏极连接，第二绝缘层设置有被第三绝缘层覆盖的栅极，第四绝缘层设置有由第五绝缘层覆盖的公共电极。在通孔区域中，像素电极设置在第五绝缘层上，并且通孔配置在第四绝缘层中，使得像素电极在穿过第五绝缘层之后与源极或漏极连接。衬垫层以绝缘方式设置在通孔下方。

