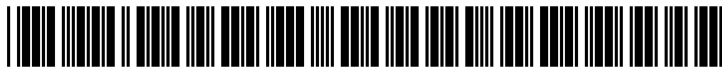

US 20130295701A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2013/0295701 A1**

(43) **Pub. Date: Nov. 7, 2013**

AHN et al.

(54) **LIQUID CRYSTAL DISPLAY OF HORIZONTAL ELECTRONIC FIELD APPLYING TYPE AND FABRICATING METHOD THEREOF**

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(21) Appl. No.: **13/933,837**

(22) Filed: **Jul. 2, 2013**

Related U.S. Application Data

(62) Division of application No. 10/962,461, filed on Oct. 13, 2004, now Pat. No. 8,502,944.

(30) **Foreign Application Priority Data**

Nov. 4, 2003 (KR) 10-2003-77658

Publication Classification

(51) **Int. Cl.**
G02F 1/1333 (2006.01)

(52) **U.S. Cl.**
CPC *G02F 1/1333* (2013.01)
USPC **438/30**

(57) **ABSTRACT**

A liquid crystal display (LCD) device of a horizontal electric field type is disclosed. The LCD device is fabricated by a three-mask process, and has gate pad, common pad and data pad electrodes, each including a upper electrode formed of a transparent conductive material. With a lift-off process, these upper electrodes are formed within contact holes.

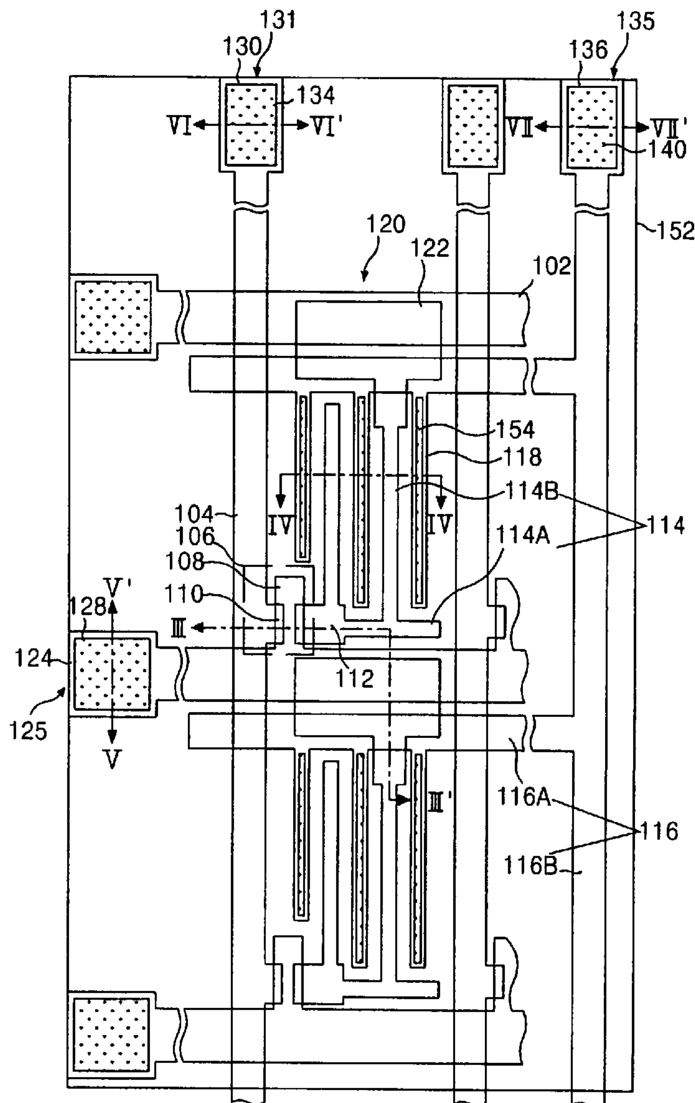
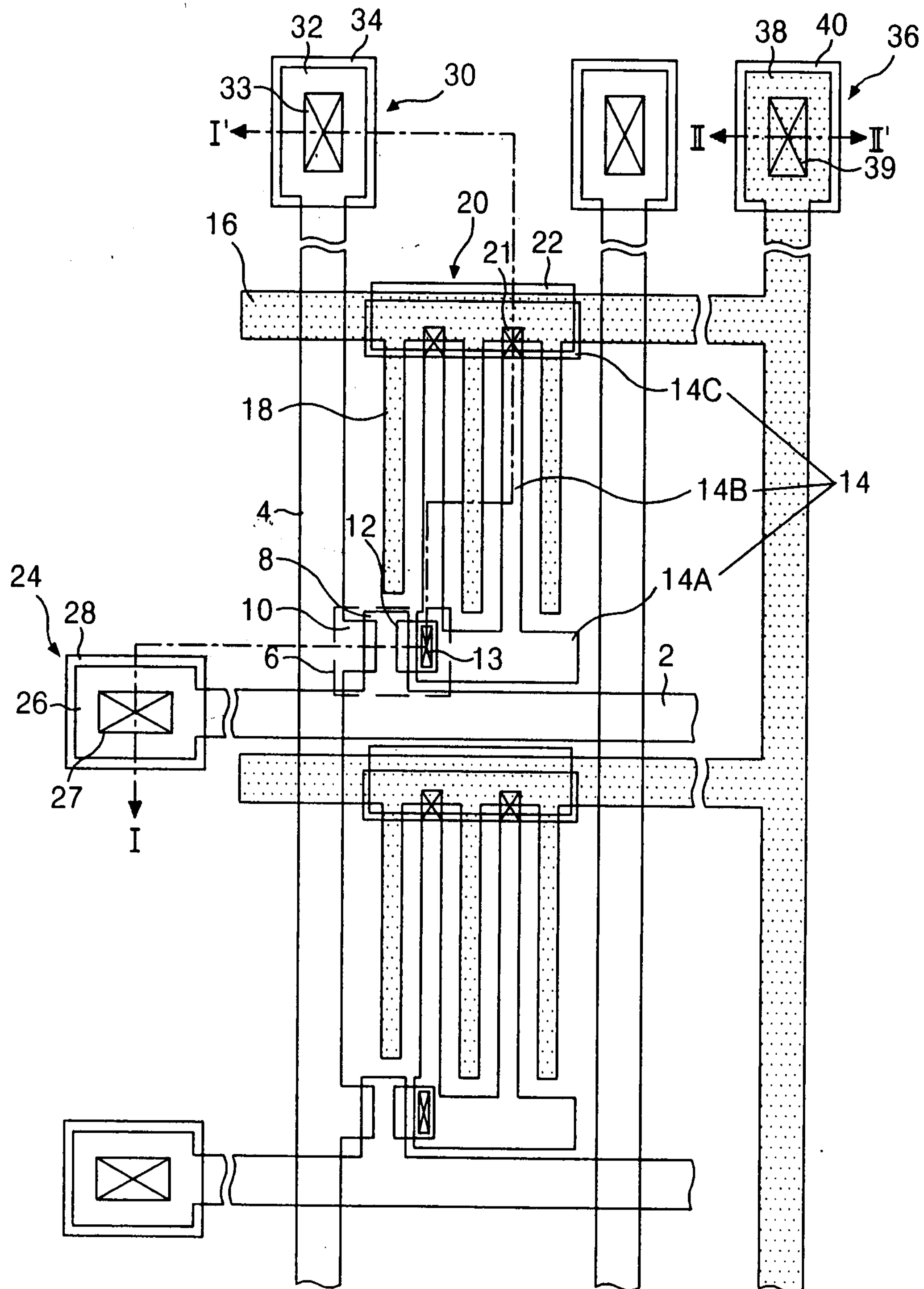


FIG.1
RELATED ART



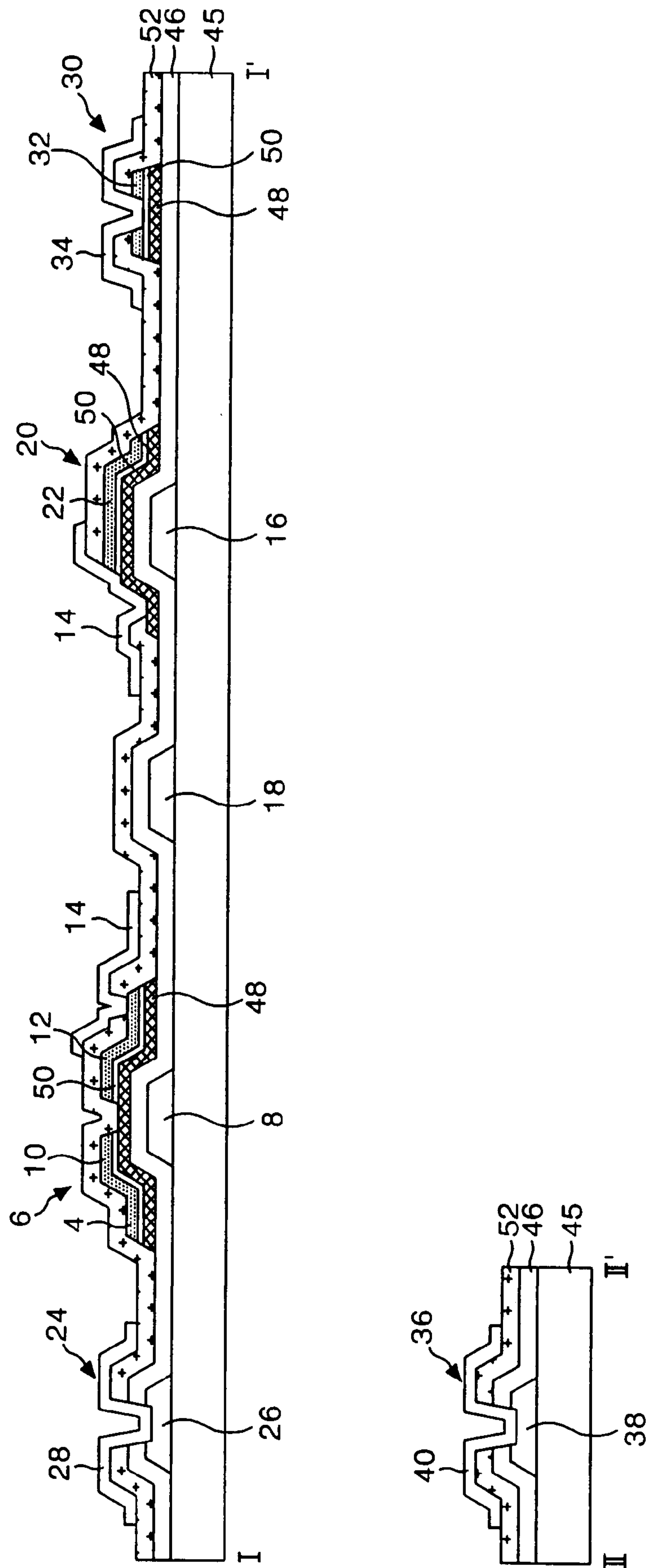


FIG. 2
RELATED ART

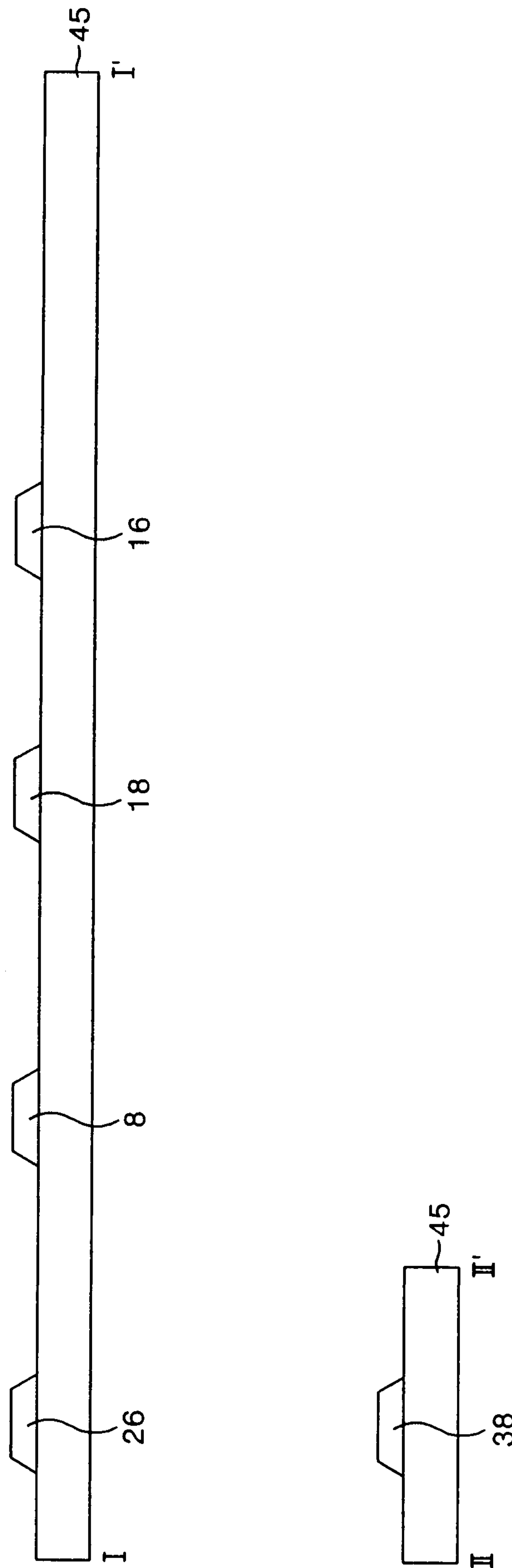


FIG.3A
RELATED ART

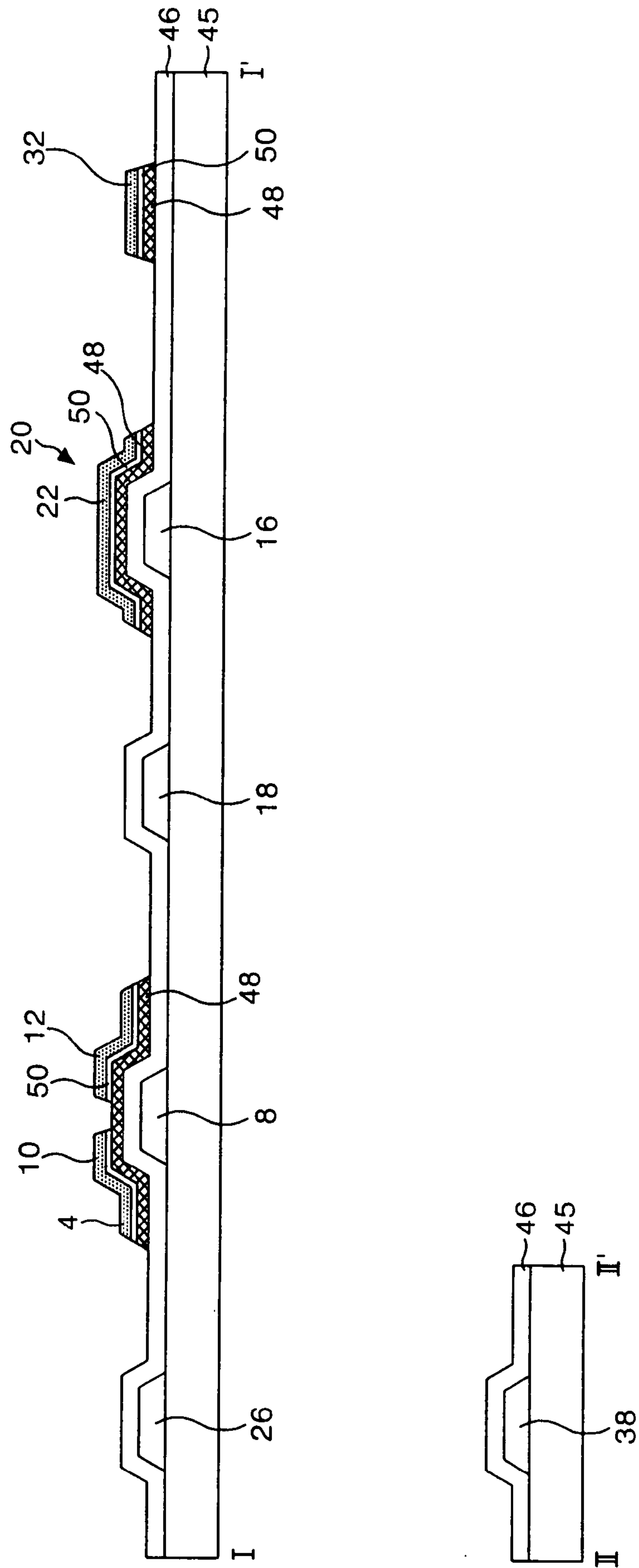


FIG.3B
RELATED ART
46
45
I'
32
50
48
20
50
48
22
16
18
12
50
48
10
8
4
26
I
46
45
II'
38
II

FIG.3C
RELATED ART

I 27 26 4 10 50 12 13 48 8 18 21 22 20 50 48 16 33 32 48 50 52 46 45 I'

II 39 38 52 46 45 II'

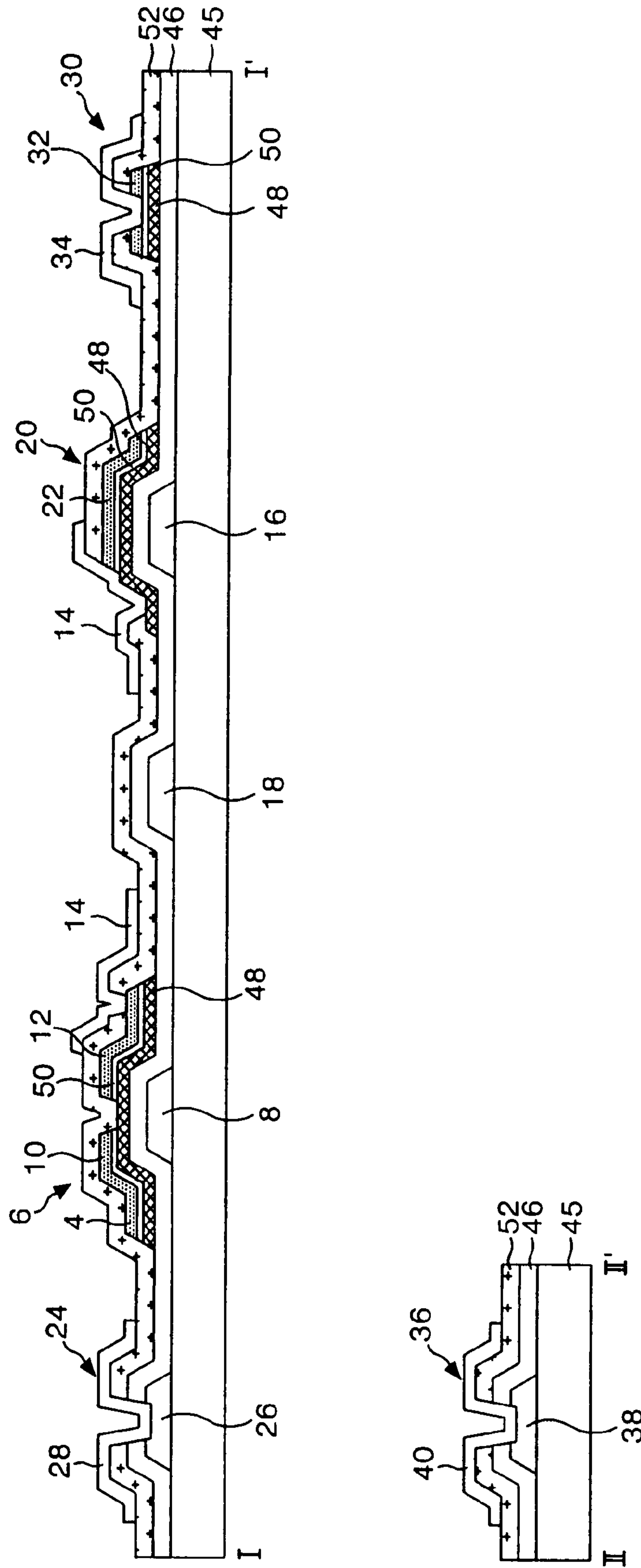


FIG.3D
RELATED ART

FIG. 4

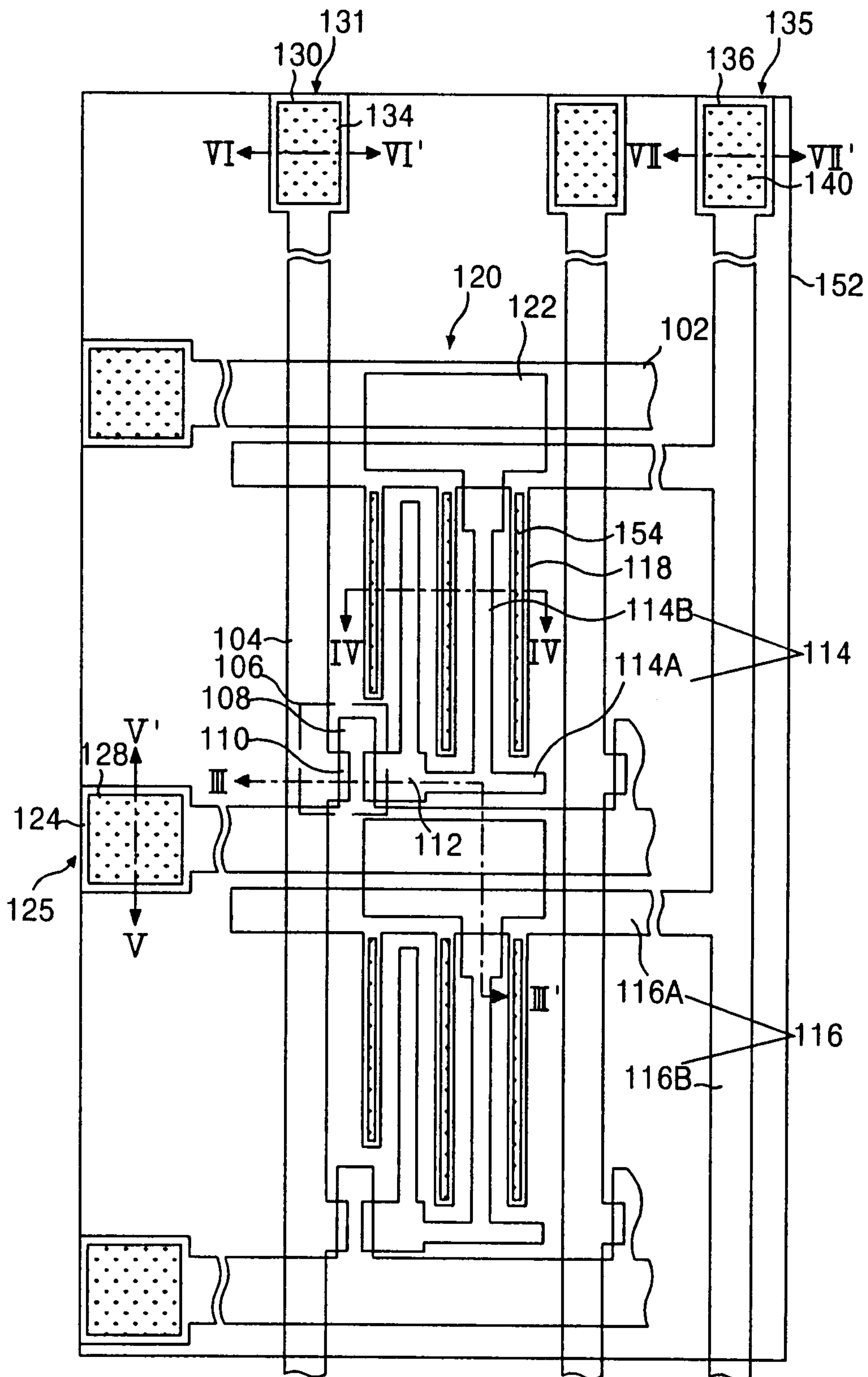


FIG.5

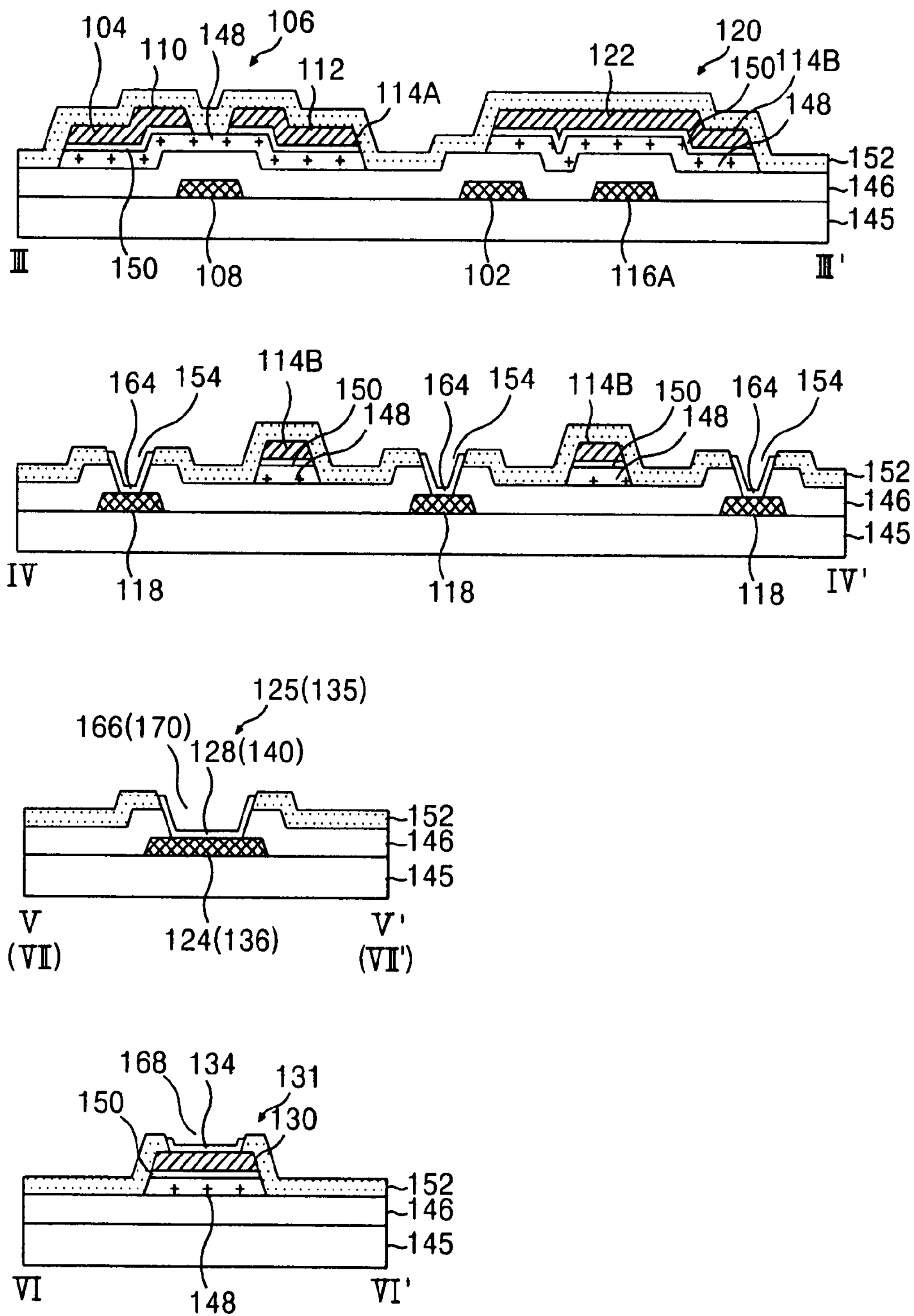


FIG. 6A

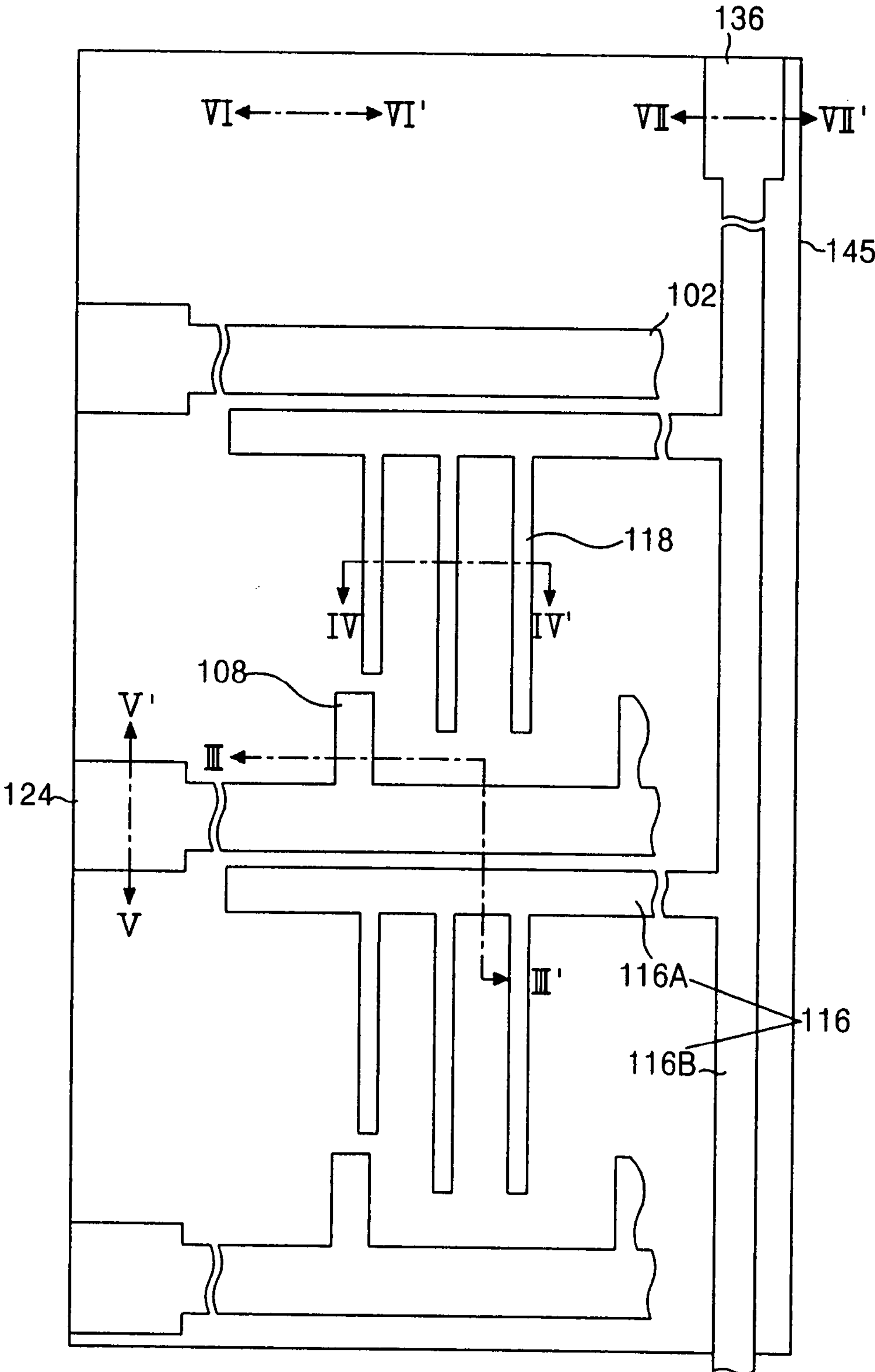
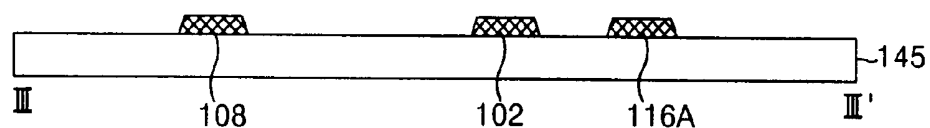
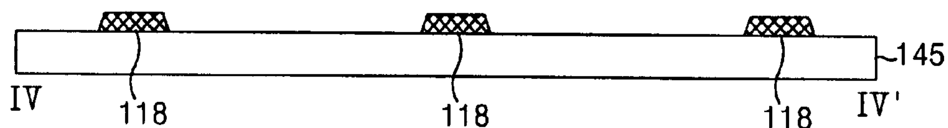
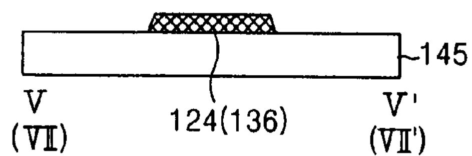


FIG.6B







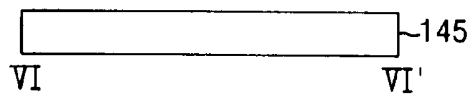


FIG.7A

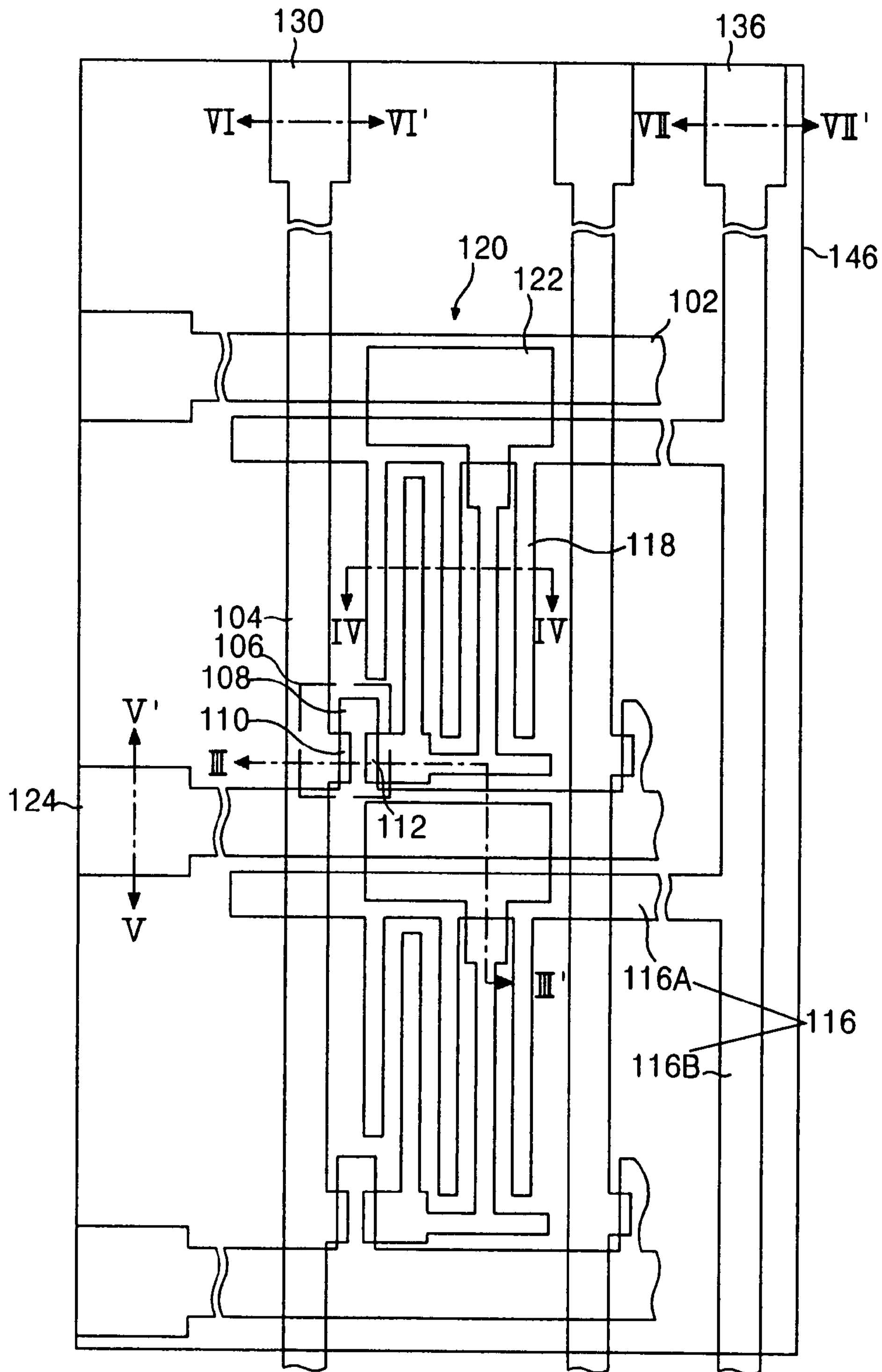


FIG.7B

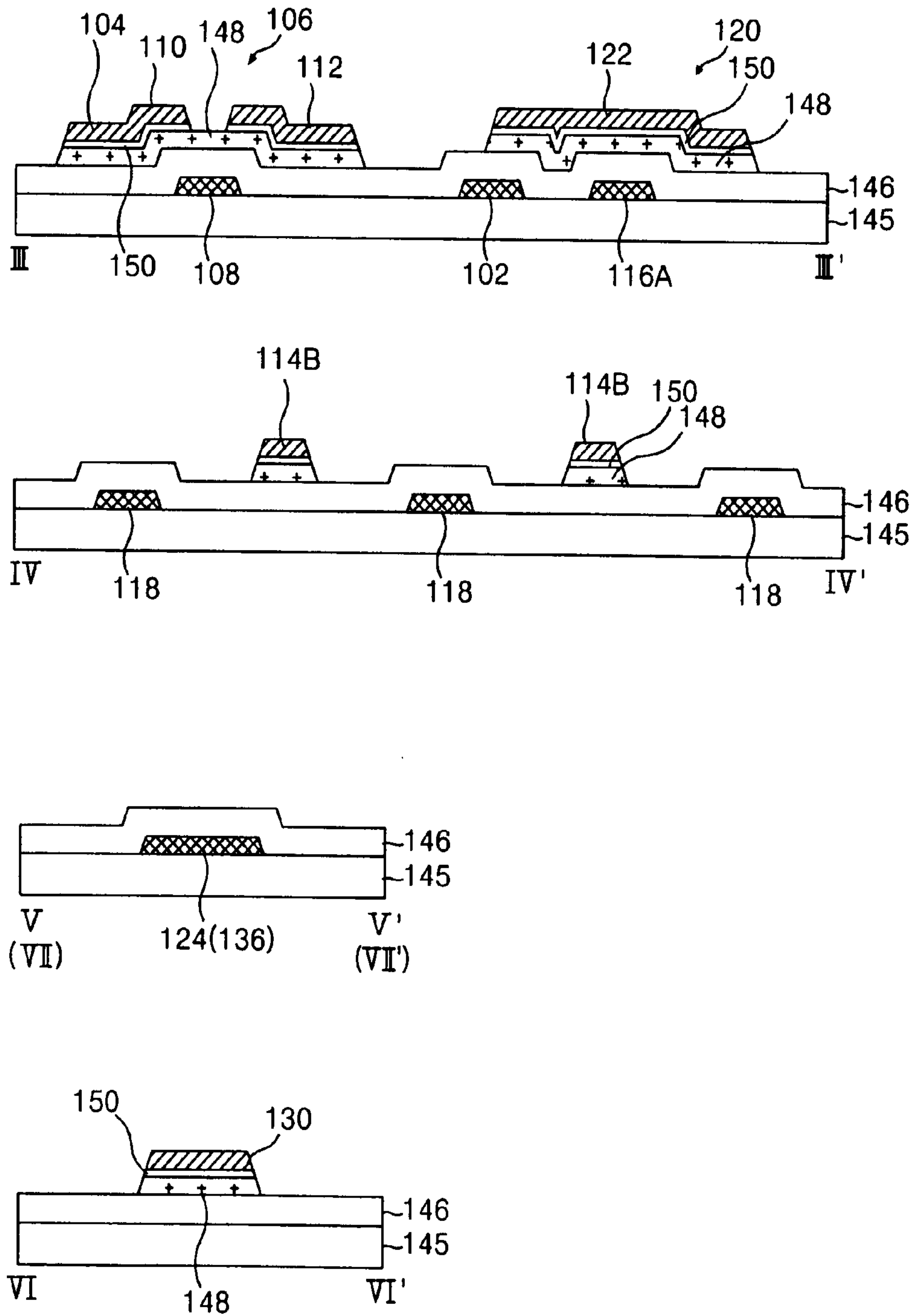
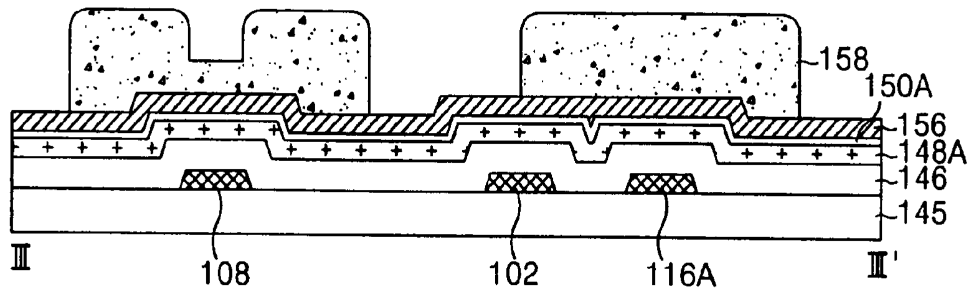
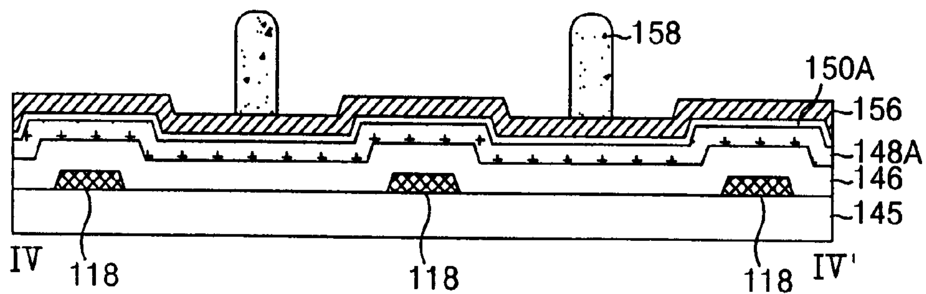
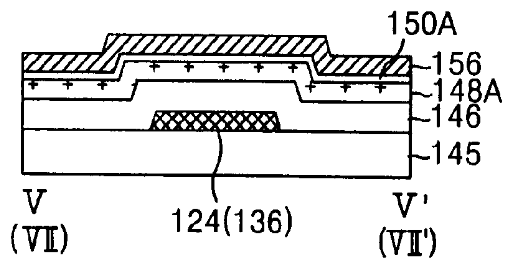


FIG.8A







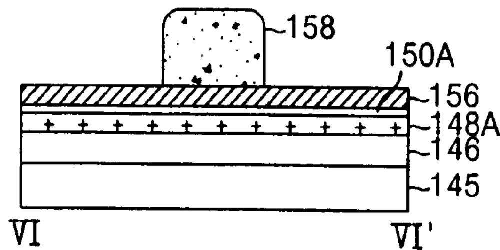
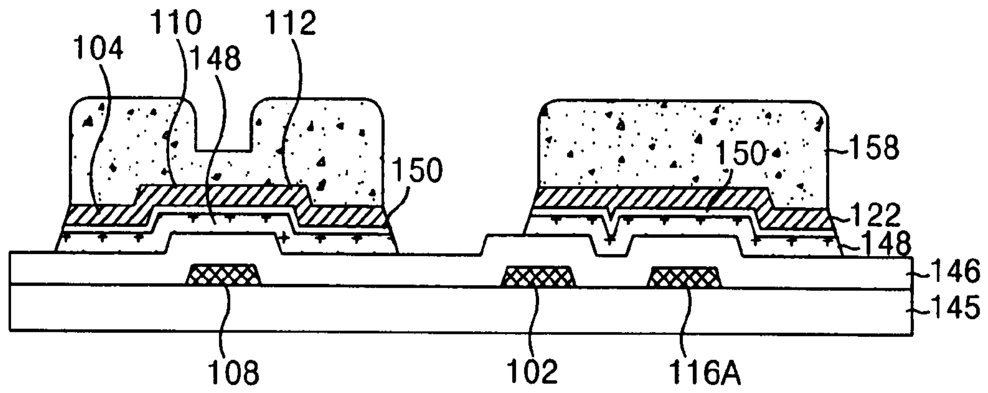
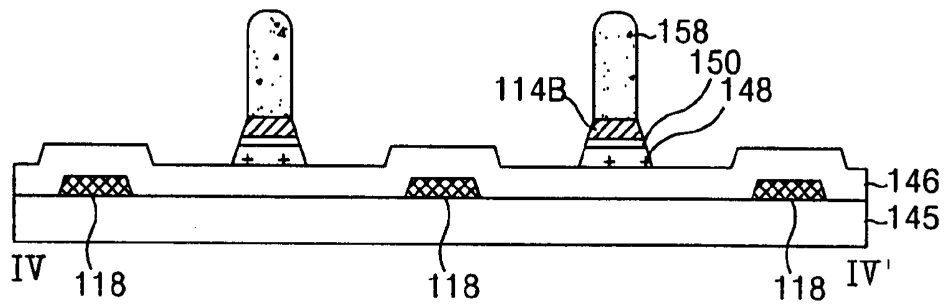
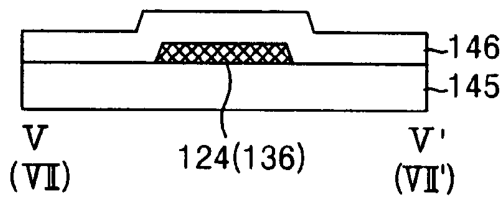


FIG.8B







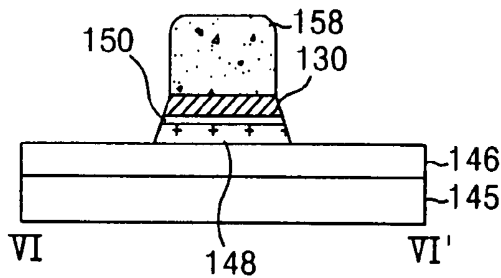
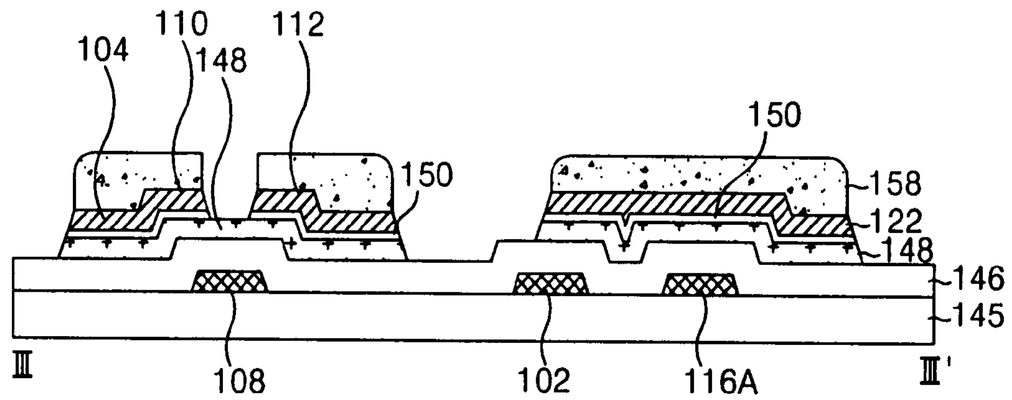
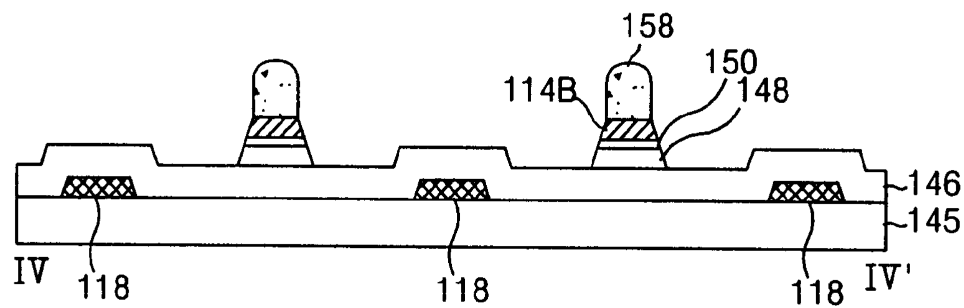
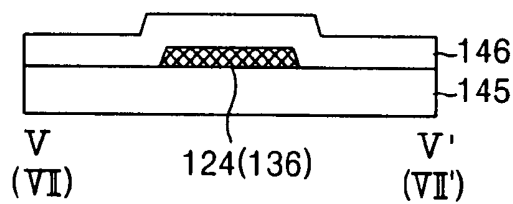


FIG.8C







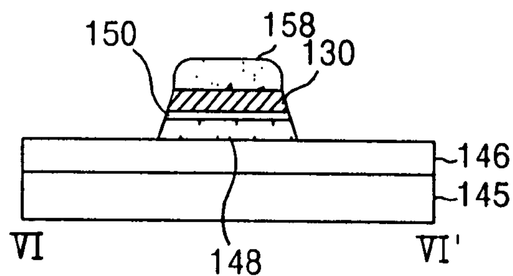


FIG.8D

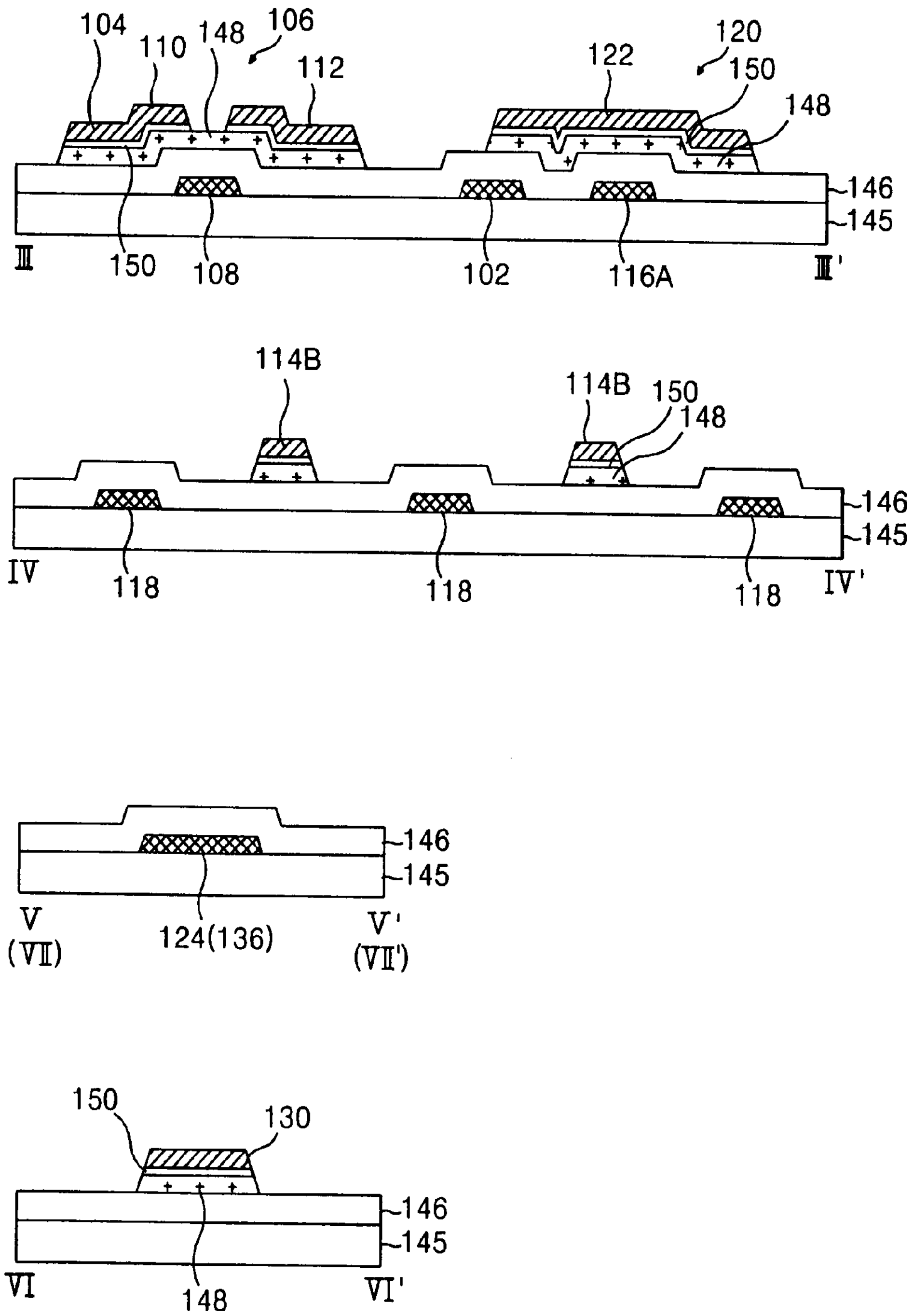


FIG.9A

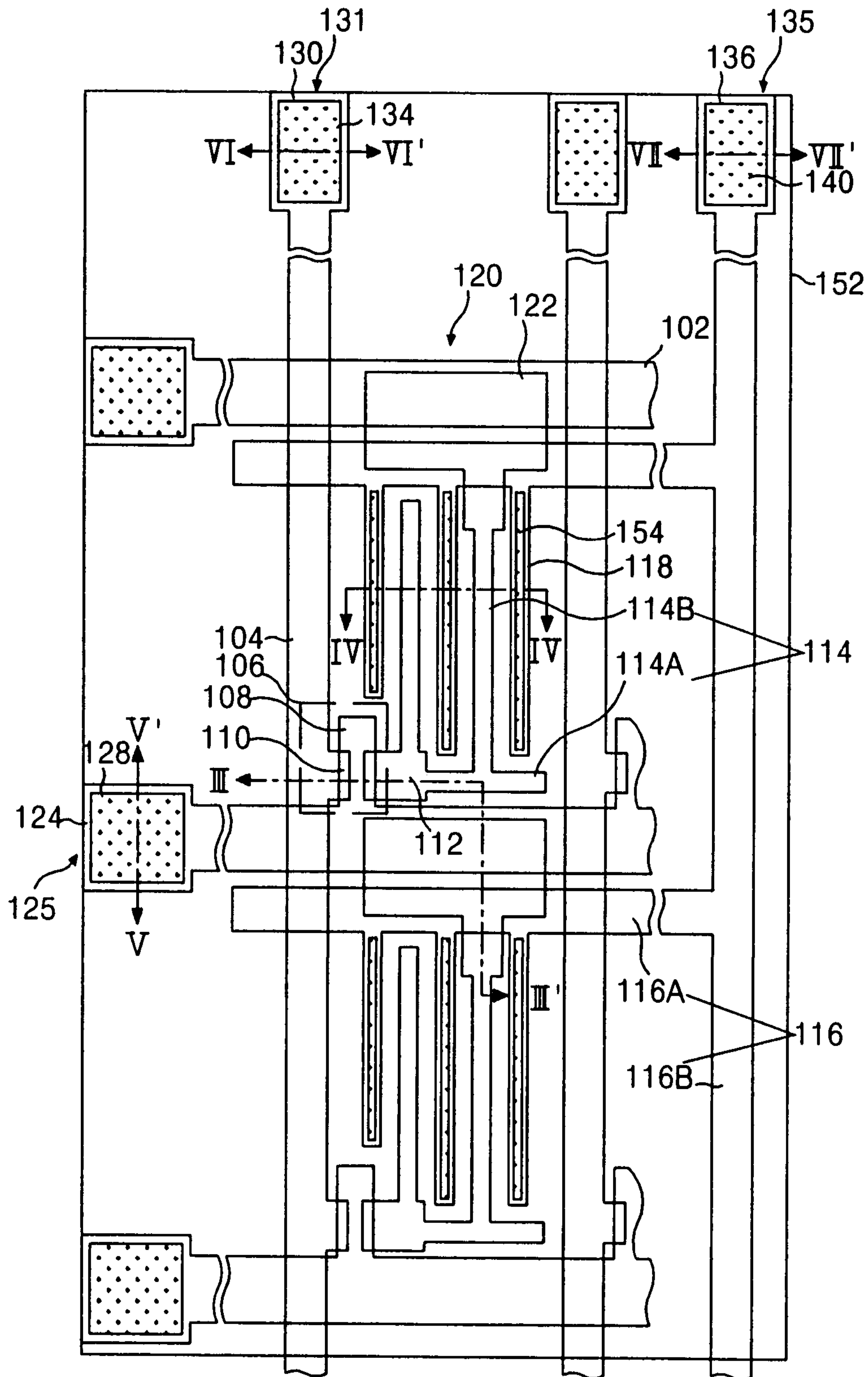
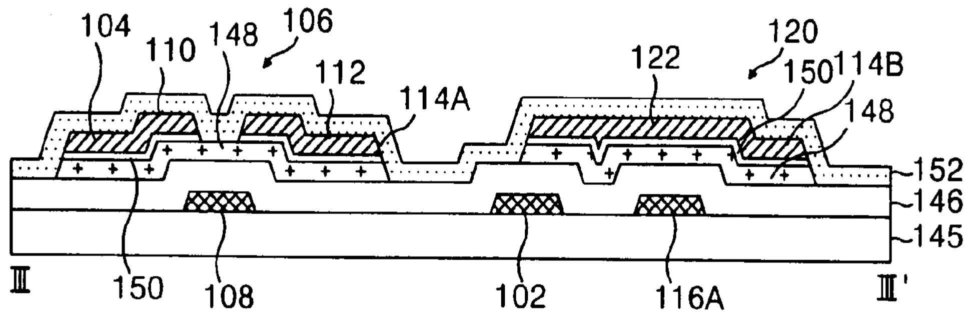
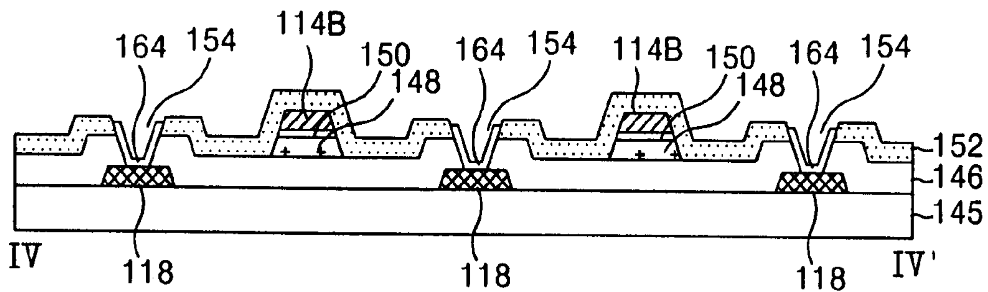
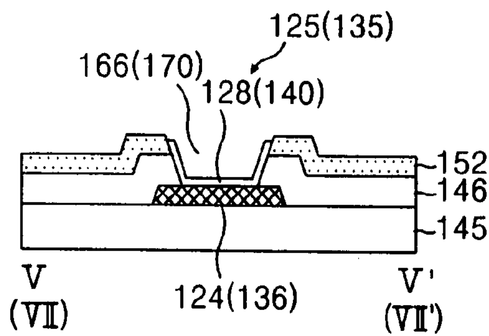


FIG.9B







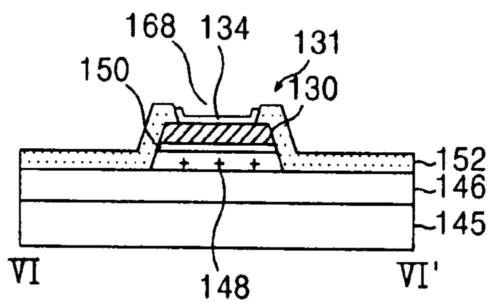
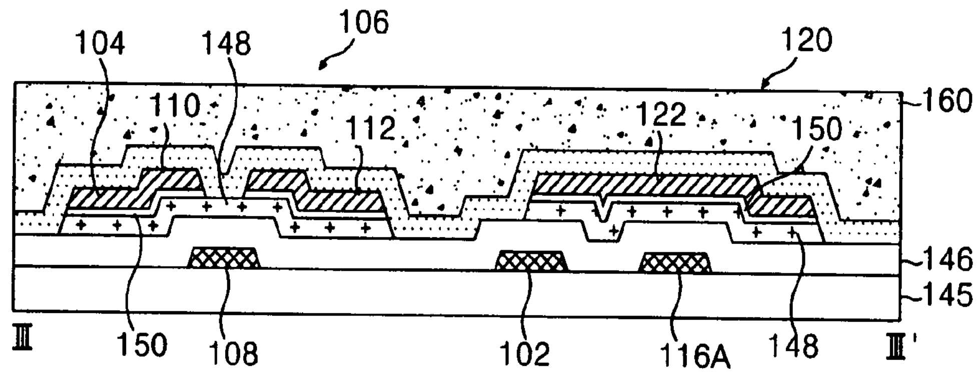
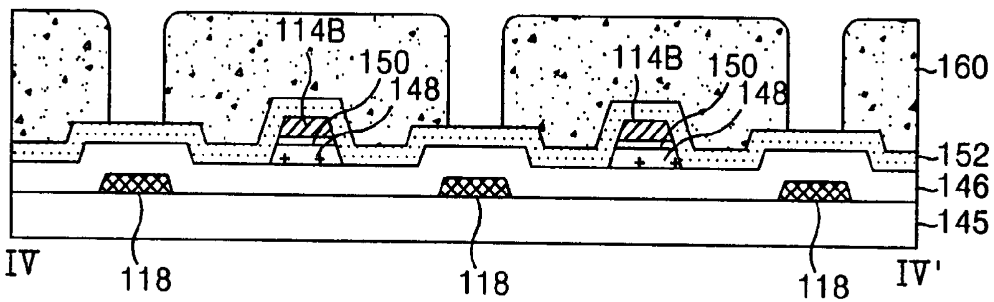
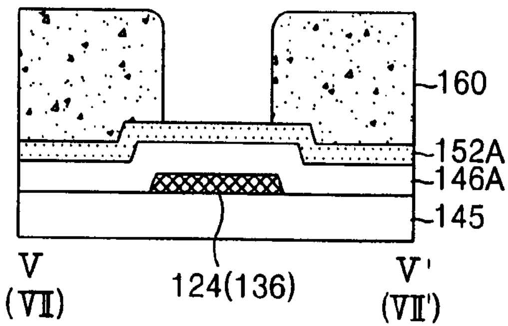
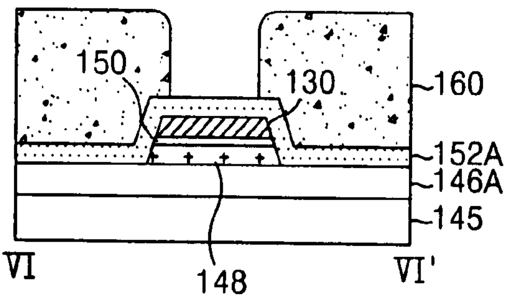


FIG.10A









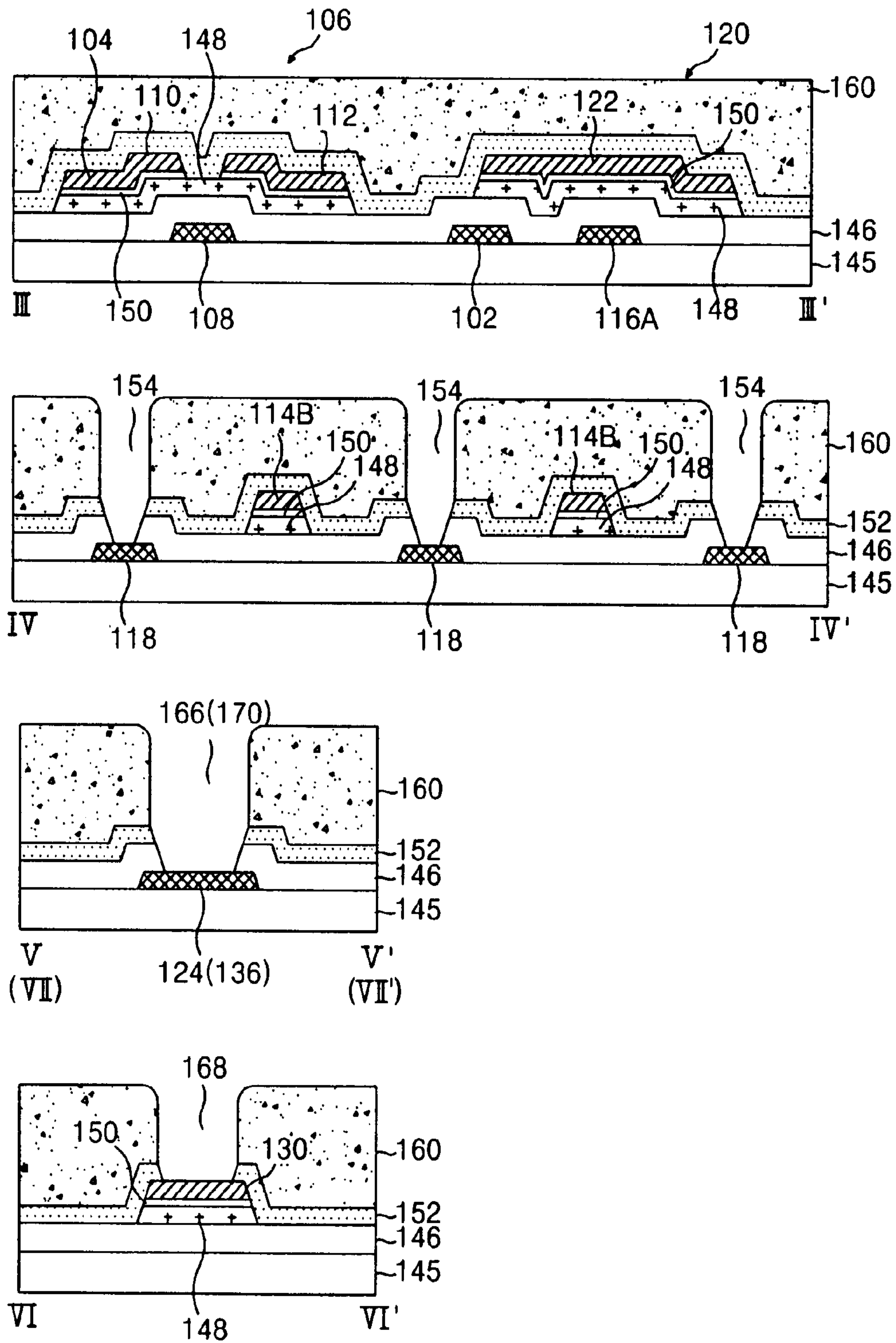


FIG.10B
106
120
104
148
110
112
122
150
160
146
145
Ⅲ
150
108
102
116A
148
Ⅲ'
154
114B
150
148
152
Ⅳ
118
Ⅳ'
166(170)
Ⅴ
(Ⅶ)
124(136)
Ⅴ'
(Ⅶ')
168
130
Ⅵ
Ⅵ'

FIG.10C

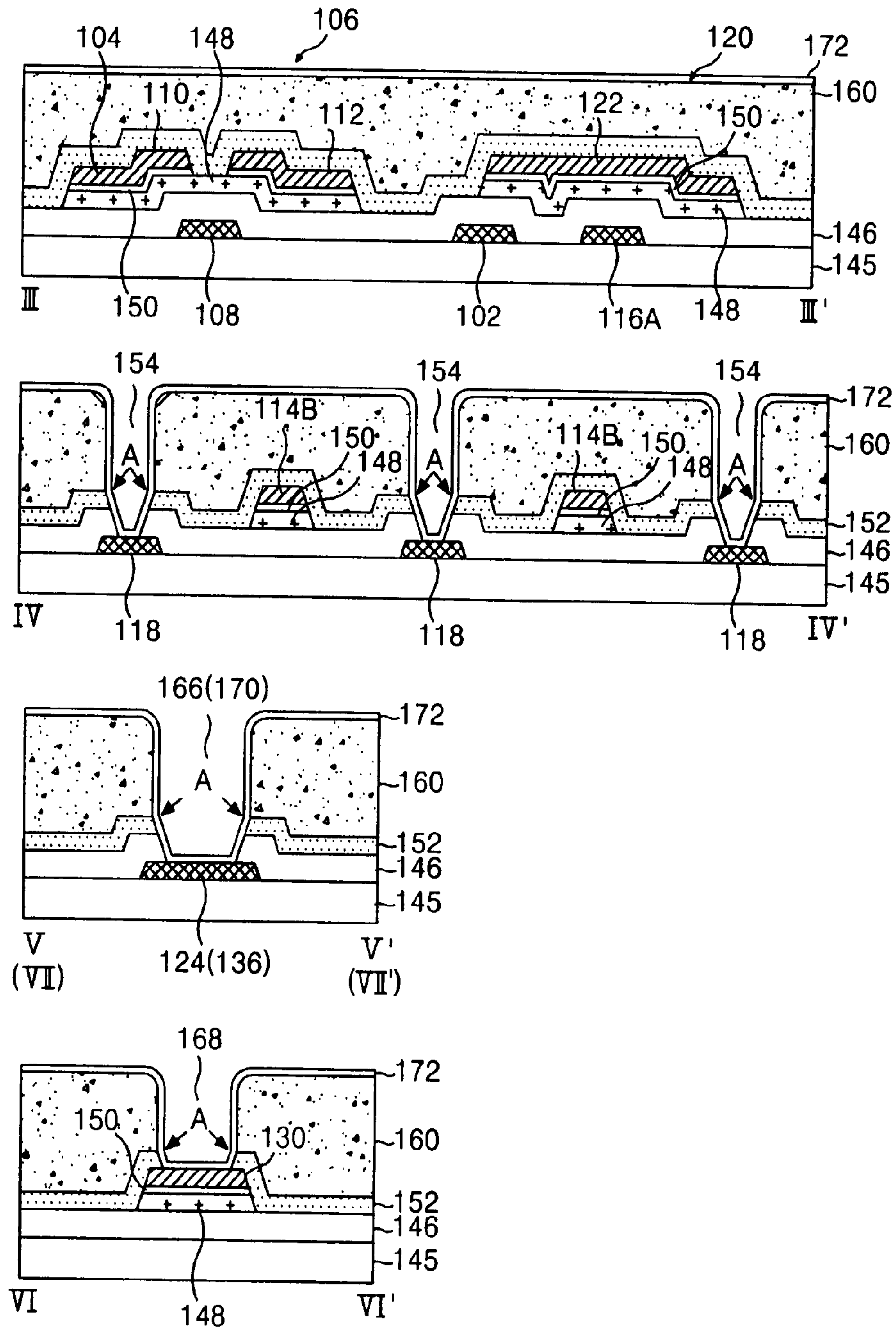


FIG.10D

104 110 148 106 112 114A 122 120 150 114B 148 152 146 145
Ⅲ 150 108 102 116A Ⅲ'

164 154 114B 150 148 164 154 114B 150 148 164 154 152 146 145
IV 118 118 118 IV'

125(135) 166(170) 128(140) 152 146 145
V (Ⅶ) 124(136) V' (Ⅶ')

168 134 131 150 130 152 146 145
VI 148 VI'

FIG.11A

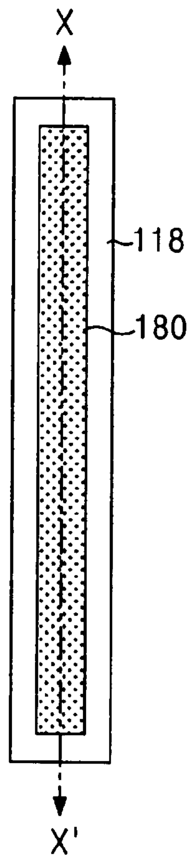


FIG.11B

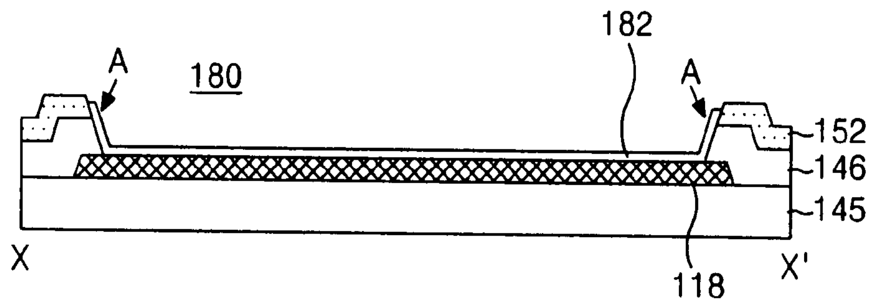


FIG.12A

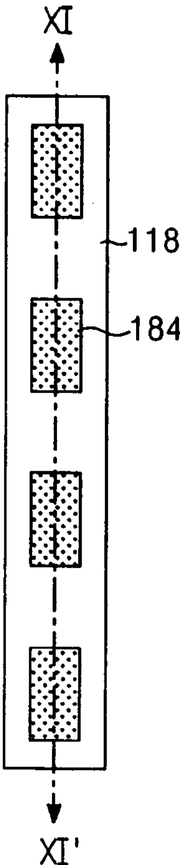
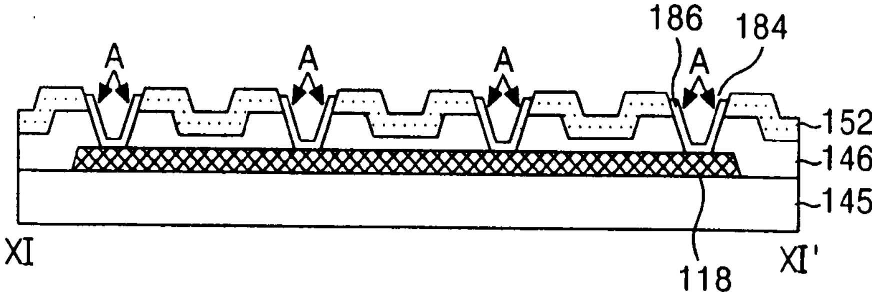


FIG.12B



LIQUID CRYSTAL DISPLAY OF HORIZONTAL ELECTRONIC FIELD APPLYING TYPE AND FABRICATING METHOD THEREOF

[0001] This application claims the benefit of the Korea Patent Application No. 2003-77658 filed on Nov. 4, 2003, which is hereby incorporated by reference for all purposes as if fully set forth herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display, and more particularly to a thin film transistor substrate of a horizontal electric field type and a fabricating method thereof that can reduce the number of mask processes.

[0004] 2. Discussion of the Related Art

[0005] Generally, liquid crystal displays (LCDs) control the light transmittance of liquid crystal using an electric field to display pictures. LCDs are largely classified into a vertical electric field type and a horizontal electric field type, depending upon the direction of the electric field driving the liquid crystal.

[0006] An LCD of the vertical electric field type drives a liquid crystal in a twisted nematic (TN) mode with a vertical electric field formed between a pixel electrode on a lower substrate and a common electrode on a upper substrate, with the pixel and common electrodes facing each other. Such an LCD of the vertical electric field type has an advantage of a high aperture ratio, while having a drawback of a narrow viewing angle of about 90°. An LCD of the horizontal electric field type drives a liquid crystal in an in plane switch (IPS) mode with a horizontal electric field between a pixel electrode and a common electrode on a lower substrate, which are arranged in parallel to each other. Such an LCD of the horizontal electric field type has an advantage of a wide viewing angle of about 160°.

[0007] Hereinafter, an LCD of the horizontal electric field type will be described in detail. An LCD of a horizontal electric field type includes a thin film transistor substrate (i.e., a lower substrate) and a color filter substrate (i.e., an upper substrate) attached to and facing each other. The LCD further includes a spacer for uniformly maintaining a cell gap between the two substrates and a liquid crystal filled into the cell gap. The thin film transistor substrate includes a plurality of signal wirings for forming a horizontal electric field for each pixel, a plurality of thin film transistors, and an alignment film coated thereon to align the liquid crystal. The color filter substrate includes a color filter for implementing a color, a black matrix for preventing a light leakage and an alignment film coated thereon to align the liquid crystal.

[0008] In such a liquid crystal display, completing the thin film transistor substrate requires a complicated fabrication process with several mask processes, leading to an increased manufacturing cost. In order to solve this problem, active researches are in progress to reduce the number of the mask processes in completing the thin film transistor substrate. This is because one mask process includes many sub-processes such as thin film deposition, cleaning, photolithography, etching, photo-resist stripping and inspection processes, etc. Recently, a four-mask process has been developed. This four-mask process reduces one mask process from the existent five-mask process that was a standard mask process in manufacturing the thin film transistor substrate.

[0009] FIG. **1** is a plan view illustrating a structure of a thin film transistor substrate of a horizontal electric type fabricated by a four-mask process according to a related art, and FIG. **2** is sectional views of the thin film transistor substrate taken along the lines I-I' and II-II' in FIG. **1**.

[0010] Referring to FIG. **1** and FIG. **2**, the thin film transistor substrate includes a gate line **2** and a data line **4** provided on a lower substrate **45** in such a manner to cross each other with a gate insulating film **46** therebetween, a thin film transistor **6** provided near each crossing, a pixel electrode **14** and a common electrode **18** provided at a pixel area defined by the gate line **2** and the data line **4** for forming a horizontal electric field, and a common line **16** connected to the common electrode **18**. Further, the thin film transistor substrate includes a storage capacitor **20** provided at an overlapping portion between the pixel electrode **14** and the common line **16**, a gate pad **24** connected to the gate line **2**, and a data pad **30** connected to the data line **4** and a common pad **36** connected to the common line **16**. The gate line **2** supplied with a gate signal and the data line **4** supplied with a data signal define the pixel area, with the gate insulating film therebetween **46**. The common line **16** supplied with a reference voltage for driving the liquid crystal is provided in parallel to the gate line **2** within the pixel area.

[0011] The thin film transistor **6** charges the data signal of the data line **4** to the pixel electrode **14** in response to the gate signal of the gate line **2**. To this end, the thin film transistor **6** includes a gate electrode **8** connected to the gate line **2**, a source electrode **10** connected to the data line **4**, and a drain electrode **12** connected to the pixel electrode **14**. The thin film transistor **6** further includes an active layer **48** overlapping the gate electrode **8** with a gate insulating film **46** therebetween to define a channel between the source electrode **10** and the drain electrode **12**. The active layer **48** also overlaps the data line **4**, a lower data pad electrode **32** and an upper storage electrode **22**. On the active layer **48** is an ohmic contact layer **50** to form an ohmic contact with the data line **4**, the source electrode **10**, the drain electrode **12**, and the lower data pad electrode **32**.

[0012] The pixel electrode **14** is connected to the drain electrode **12** of the thin film transistor **6** via a first contact hole **13** passing through a protective film **52**, and is provided at the pixel area. More specifically, the pixel electrode **14** includes a first horizontal part **14**A connected to the drain electrode **12** and provided in parallel with adjacent gate lines **2**, a second horizontal part **14**B overlapping the common line **16**, and a finger part **14**C provided in parallel between the first and second horizontal parts **14**A and **14**B. The common electrode **18** is connected to the common line **16** and is provided at the pixel area. More specially, the common electrode **18** is provided in parallel with the finger part **14**C of the pixel electrode **14** at the pixel area.

[0013] Accordingly, a horizontal electric field is formed between the pixel electrode **14** to which a data signal is applied via the thin film transistor **6** and the common electrode **18** to which a reference voltage is applied via the common line **16**. More specifically, a horizontal electric field is formed between the finger part **14**C of the pixel electrode **14** and the common electrode **18**. Liquid crystal molecules arranged in a horizontal direction between the thin film transistor substrate and the color filter substrate rotate by such a horizontal electric field due to a dielectric anisotropy of the liquid crystal molecules. Transmittance of the pixel area is

differentiated depending upon an extent of the rotation of the liquid crystal molecules, thereby implementing gray scale levels.

[0014] The storage capacitor **20** is constructed with the common line **16**, an upper storage electrode **22** overlapping the common line **16**, the gate insulating film **46**, the active layer **48** and the ohmic contact layer **50**, as shown in FIG. **2**. The gate insulating film **46**, the active layer **48** and the ohmic contact layer **50** are sandwiched between the common line **16** and the upper storage electrode **22**. In the storage capacitor **20**, the pixel electrode **14** is connected to the upper storage electrode **22** via a second contact hole **21** passing through the protective film **52**. The storage capacitor **20** maintains a data signal charged in the pixel electrode **14** until the next data signal is charged.

[0015] The gate line **2** is connected to a gate driver (not shown) via the gate pad **24**. The gate pad **24** is constructed with a lower gate pad electrode **26** extended from the gate line **2**, and an upper gate pad electrode **28** connected to the lower gate pad electrode **26** via a third contact hole **27** passing through the gate insulating film **46** and the protective film **52**. The data line **4** is connected to the data driver (not shown) via the data pad **30**. The data pad **30** is constructed with a lower data pad electrode **32** extended from the data line **4**, and an upper data pad electrode **34** connected to the lower data pad electrode **32** via a fourth contact hole **33** passing through the protective film **52**. The common line **16** receives a reference voltage from an external reference voltage source (not shown) through the common pad **36**. The common pad **36** is constructed with a lower common pad electrode **38** extended from the common line **16**, and an upper common pad electrode **40** connected to the lower common pad electrode **38** via a fifth contact hole **39** passing through the gate insulating film **46** and the protective film **52**.

[0016] A method of fabricating the thin film transistor substrate having the above-mentioned structure by a four-mask process will be described in detail with reference to FIGS. **3**A to **3**D.

[0017] Referring to FIG. **3**A, a gate metal pattern group (or a first conductive pattern group) including the gate line **2**, the gate electrode **8** and the lower gate pad electrode **26**, the common line **16**, the common electrode **18** and the lower common pad electrode **38** is provided on the lower substrate **45** by a first mask process. More specifically, a gate metal layer (or a first conductive layer) is formed on the lower substrate **45** by a deposition technique such as sputtering. Then, the gate metal layer is patterned by photolithography and etching processes using a first mask to thereby form the gate metal pattern group including the gate line **2**, the gate electrode **8**, the lower gate pad electrode **26**, the common line **16**, common electrode **18** and the lower common pad electrode **38**. Herein, the gate metal layer is formed of metal such as aluminum-group metal, chrome (Cr) or molybdenum (Mo).

[0018] Referring to FIG. **3**B, the gate insulating film **46** is deposited onto the lower substrate **45** provided with the gate metal pattern group. Further, a semiconductor pattern including the active layer **48** and the ohmic contact layer **50** and a source/drain metal pattern group (or a second conductive pattern group) including the data line **4**, the source electrode **10**, the drain electrode **12**, the lower data pad electrode **32** and the upper storage electrode **22** are formed on the gate insulating film **46** by a second mask process. More specifically, the gate insulating film **46**, an amorphous silicon layer, an n^+ amorphous silicon layer and a source/drain metal layer (or a second conductive layer) are sequentially deposited on the lower substrate **45** provided with the gate metal pattern group by such deposition techniques as plasma enhanced chemical vapor deposition (PECVD) and sputtering, etc. Herein, the gate insulating film **46** is formed of an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x). The source/drain metal layer is formed of molybdenum (Mo), titanium (Ti), tantalum (Ta) or molybdenum alloy, etc.

[0019] Then, a photo-resist pattern is formed on the source/drain metal layer by a photolithography process using a second mask. In this case, a diffractive exposure mask having a diffractive exposing part at a channel portion of the thin film transistor is used as a second mask, thereby allowing the photo-resist pattern at the channel portion to have a lower height than other source/drain pattern portions. Subsequently, the source/drain metal layer is patterned by a wet-etching process using the photo-resist pattern to thereby form the source/drain metal pattern group including the data line **4**, the source electrode **10**, the drain electrode **12** which is integral to the source electrode **10** and the upper storage electrode **22**.

[0020] Next, the n^+ amorphous silicon layer and the amorphous silicon layer are patterned at the same time by a dry-etching process using the same photo-resist pattern to thereby form the ohmic contact layer **50** and the active layer **48**. The photo-resist pattern having a relatively low height at the channel portion is removed by an ashing process, and thereafter the source/drain metal pattern and the ohmic contact layer **50** at the channel portion are etched by a dry-etching process. Thus, the active layer **48** of the channel portion is exposed to disconnect the source electrode **10** from the drain electrode **12**. Then, the photo-resist pattern left on the source/drain metal pattern group is removed by a stripping process.

[0021] Referring to FIG. **3**C, the protective film **52** including the first to fifth contact holes **13**, **21**, **27**, **33** and **39** are formed on the gate insulating film **46** provided with the source/drain metal pattern group by a third mask process. More specifically, the protective film **52** is entirely deposited on the gate insulating film **46** provided with the source/drain metal pattern group by a deposition technique such as plasma enhanced chemical vapor deposition (PECVD). The protective film **52** is patterned by photolithography and etching processes using a third mask to thereby define the first to fifth contact holes **13**, **21**, **27**, **33** and **39**. The first contact hole **13** passes through the protective film **52** to expose the drain electrode **12**, whereas the second contact hole **21** passes through the protective film **52** to expose the upper storage electrode **22**. The third contact hole **27** passes through the protective film **52** and the gate insulating film **46** to expose the lower gate pad electrode **26**. The fourth contact hole **32** passes through the protective film **52** to expose the lower data pad electrode **32**. The fifth contact hole **30** passes through the protective film **52** and the gate insulating film **48** to expose the lower common pad electrode **38**. Herein, when the source/drain metal layer is formed of a metal material having a large dry-etching ratio such as molybdenum (Mo), then each of the first, second and fourth contact holes **13**, **21** and **33** passes through the drain electrode **12**, the upper storage electrode **22** and the lower data pad electrode **32** to thereby expose the side surfaces thereof. The protective film **50** is formed of an inorganic material identical to the gate insulating film **46**, or an organic material having a small dielectric constant such as an acrylic organic compound, BCB (benzocyclobutene) or PFCB (perfluorocyclobutane), etc.

[0022] Referring to FIG. 3D, a transparent conductive film pattern group (or a third conductive pattern group) including the pixel electrode **14**, the upper gate pad electrode **28**, the upper data pad electrode **34** and the upper common pad electrode **40** are formed on the protective film **52** by a fourth mask process. More specifically, a transparent conductive film (or a third conductive layer) is deposited onto the protective film **52** by a deposition technique such as sputtering, etc. Then, the transparent conductive film is patterned by photolithography and etching processes using a fourth mask to thereby provide the transparent conductive pattern group including the pixel electrode **14**, the upper gate pad electrode **28**, the upper data pad electrode **34** and the upper common pad electrode **40**. The pixel electrode **14** is electrically connected to the drain electrode **12** via the first contact hole **13**, and is also electrically connected to the upper storage electrode **22** via the second contact hole **21**. The upper gate pad electrode **28** is electrically connected to the lower gate pad electrode **26** via the third contact hole **37**. The upper data pad electrode **34** is electrically connected to the lower data pad electrode **32** via the fourth contact hole **33**. The upper common pad electrode **40** is electrically connected to the lower common pad electrode **38** via the fifth contact hole **39**. Herein, the transparent conductive film is formed of indium-tin-oxide (ITO), tin-oxide (TO) or indium-zinc-oxide (IZO), or the like.

[0023] The thin film transistor substrate of a horizontal electric field type and the fabricating method thereof as described above employs a four-mask process, thereby reducing the number of fabricating processes and reducing the manufacturing cost in comparison with such thin film transistor substrates fabricated by a five-mask process. However, because such a four-mask process still requires a complicate fabricating process and has a limit in cost reduction, a more simplified fabricating process would be beneficial to reduce the manufacturing cost.

SUMMARY OF THE INVENTION

[0024] Accordingly, the present invention is directed to an LCD and fabricating method thereof that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

[0025] Accordingly, it is an advantage of the present invention to provide a thin film transistor substrate of horizontal electric field type and a fabricating method thereof that can reduce the number of mask processes.

[0026] Another advantage of the present invention is to provide a thin film transistor substrate of horizontal electric field type and a fabricating method thereof that have a stripper penetration path on a signal line to facilitate a lift-off process

[0027] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0028] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, an liquid crystal display (LCD) of a horizontal electric field type having a liquid crystal between upper and lower substrates includes a gate line and a common line formed from a first conductive layer on the lower substrate; a data line crossing the gate line with a gate insulating film therebetween formed from a second conductive layer, the gate and data lines defining a pixel area; a thin film transistor connected to the gate and data lines; a common electrode extended from the common line into the pixel area and formed from the first conductive layer; a pixel electrode electrically connected to a drain electrode of the thin film transistor and formed from the second conductive layer in the pixel area, the pixel electrode and the common electrode in the pixel area forming a horizontal electric field during an operation of the LCD; a protective film for covering at least the thin film transistor; a gate pad having a lower gate pad electrode extended from the gate line, a upper gate pad electrode formed from a third conductive layer and a first contact hole, the upper gate pad electrode electrically connected to the lower gate pad electrode via the first contact hole; a common pad having a lower common pad electrode connected to the common line, a upper common pad electrode formed from the third conductive layer and a second contact hole, the upper common pad electrode electrically connected to the lower common pad electrode via the second contact hole; and a data pad having a lower data pad electrode connected to the data line, a upper data pad electrode formed from the third conductive layer and a third contact hole, the upper data pad electrode electrically connected to the lower data pad electrode through the third contact hole, wherein the upper gate pad, upper common pad and upper data pad electrodes are formed within the first to third contact holes, respectively.

[0029] A stripper penetration path is formed on at least one of the gate line, the data line, the common line, the pixel electrode and the common electrode in the pixel area.

[0030] The stripper penetration path is formed either in the protective film or in the protective film and the gate insulating film to easily remove a photo-resist pattern used for the patterning of the protective film during a lift-off process.

[0031] The stripper penetration path is formed to have a shape of a slit or a plurality of holes.

[0032] The stripper penetration path is formed at the same time as the first to third contact holes.

[0033] A dummy pattern formed from said third conductive layer is left within the stripper penetration path.

[0034] The LCD further includes a storage capacitor having first and second lower storage electrodes formed from the first conductive layer; and a upper storage electrode formed from the second conductive layer, the upper storage capacitor electrode electrically connected to the pixel electrode.

[0035] Herein, the upper storage electrode is integral to any one of fingers of the pixel electrode.

[0036] In another aspect of the present invention, a method of fabricating an LCD of a horizontal electric field type having a liquid crystal between lower and upper substrates includes forming a first conductive pattern group including a gate line, a gate electrode connected to the gate line, a lower gate pad electrode, a common line, a common electrode extended from the common line, a lower common pad electrode connected to the common line on the lower substrate by patterning a first conductive layer; forming a gate insulating film on the first conductive pattern group; forming a semiconductor pattern on the gate insulating film; forming a second conductive pattern group including a data line crossing the gate line to define a pixel area, a source electrode and a lower data pad electrode connected to the data line, a drain electrode opposed to the source electrode and a pixel electrode connected to the drain electrode on the semiconductor pattern by pattering a second conductive layer, the common electrode and the pixel electrode forming a horizontal electric field in

the pixel area during an operation of the LCD; forming a protective film on the second conductive pattern group; forming first to third contact holes for the lower gate pad electrode, the lower common pad electrode and the lower data pad electrode by patterning at least one of the protective film and the gate insulating film using a photo-resist pattern; and forming a third conductive pattern group including an upper gate pad electrode, an upper common pad electrode and an upper data pad electrode by depositing a third conductive layer on the photo-resist pattern and then by lifting-off the photo-resist pattern, the upper gate pad electrode, the upper common pad electrode and the upper data pad electrode connected to the lower gate pad electrode, the lower common pad electrode and the lower data pad electrode, respectively, via the first to third contact holes.

[0037] In the method, a stripper penetration path hole is further formed on at least one of the gate line, the data line, the common line, the pixel electrode and the common electrode in the pixel area, and at the same time

[0038] In the method, the stripper penetration path hole facilitates the lifting off process of the photo-resist pattern.

[0039] The photo-resist pattern has protrusions in an interface with the protective film.

[0040] The stripper penetration path hole is formed to have a shape of a slit or a plurality of holes.

[0041] The method further includes forming an upper storage electrode overlapping a portion of the gate line and a portion of the common line adjacent to the gate line with the gate insulating film and the semiconductor pattern therebetween and electrically connected to the pixel electrode.

[0042] In another aspect of the present invention, a method of fabricating a thin film transistor substrate of horizontal electric field applying type includes a first mask process of forming a gate line, a gate electrode and a lower gate pad electrode connected to the gate line, a common line parallel to the gate line, a lower common pad electrode connected to the common line and a common electrode extended from the common line into a pixel area on a substrate from a first conductive layer; a second mask process of entirely coating a gate insulating film, and forming a semiconductor pattern at a desired area of the gate insulating film and forming a data line crossing the gate line and the common line, a source electrode and a lower data pad electrode connected to the data line, a drain electrode opposed to the source electrode and a pixel electrode connected to the drain electrode to form a horizontal electric field along with the common electrode on said semiconductor pattern from a second conductive layer; and a third mask process of entirely coating the protective film, patterning the protective film along with the gate insulating film to define first to fourth contact holes for exposing the lower gate pad electrode, the lower common pad electrode and a lower data pad electrode, and forming an upper gate pad electrode, an upper common pad electrode and an upper data pad electrode from a third conductive layer within the first to fourth contact holes.

[0043] In the method, said third mask process includes entirely coating the protective film; forming a photo-resist pattern on the protective film using a mask; patterning the protective film and the gate insulating film by the photo-resist pattern; entirely coating a transparent conductive film onto the photo-resist pattern; and removing the photo-resist pattern covered with the transparent conductive film to pattern the transparent conductive film.

[0044] Said third mask process further includes providing a penetration path of a stripper going through a protective film on any at least one of a plurality of signal lines and electrodes formed from said first and second conductive layers in order to remove said photo-resist pattern.

[0045] The stripper penetration path is formed in such a manner to go through until the gate insulating film under the protective film.

[0046] The stripper penetration path includes any at least one of a slit and a plurality of holes provided along any at least one of said plurality of signal lines and electrodes.

[0047] The stripper penetration path is provided on any at least one of a common electrode and a pixel electrode.

[0048] Herein, said third conductive layer making an interface with the patterned protective film is left within the stripper penetration path.

[0049] Herein, the first to third contact holes are used as the stripper penetration path.

[0050] Said second mask process further includes forming an upper storage electrode overlapping with a portion of the gate line and a portion of the common line adjacent to the gate line with having the gate insulating film and the semiconductor pattern therebetween and connected to the pixel electrode from said second conductive layer.

[0051] Said third conductive layer contains any one of a transparent conductive layer, titanium and tungsten.

[0052] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0053] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

[0054] In the drawings:

[0055] FIG. **1** is a plan view illustrating a structure of a thin film transistor substrate of a horizontal electric type fabricated by a four-mask process according to a related art;

[0056] FIG. **2** is sectional views of the thin film transistor substrate taken along the lines I-I' and II-II' in FIG. **1**;

[0057] FIGS. **3**A to **3**D are sectional views illustrating a method of fabricating the thin film transistor substrate shown in FIG. **2**;

[0058] FIG. **4** is a plan view illustrating a structure of a thin film transistor substrate of a horizontal electric field type according to an embodiment of the present invention;

[0059] FIG. **5** is a sectional view of the thin film transistor substrate taken along the lines III-III', IV-IV', V-V, VI-VI and VII-VII in FIG. **4**;

[0060] FIG. **6**A and FIG. **6**B are a plan view and a sectional view, respectively, for explaining a first mask process in a fabricating method of the thin film transistor substrate according to the embodiment of the present invention;

[0061] FIG. **7**A and FIG. **7**B are a plan view and a sectional view, respectively, for explaining a second mask process in a fabricating method of the thin film transistor substrate according to the embodiment of the present invention;

[0062] FIG. **8**A to FIG. **8**D are sectional views for explaining the second mask process in more detail;

[0063] FIG. **9**A and FIG. **9**B are a plan view and a section view, respectively, for explaining a third mask process in a

fabricating method of the thin film transistor substrate according to the embodiment of the present invention;

[0064] FIG. **10**A to FIG. **10**D are section views for explaining the third mask process in more detail;

[0065] FIG. **11**A and FIG. **11**B are a plan view and a section view, respectively, illustrating an example of a stripper penetration path according to the embodiment of the present invention; and

[0066] FIG. **12**A and FIG. **12**B are a plan view and a section view, respectively, illustrating another example of a stripper penetration path according to the embodiment of the present invention.

DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

[0067] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0068] FIG. **4** is a plan view illustrating a structure of a thin film transistor substrate of a horizontal electric field type according to an embodiment of the present invention, and FIG. **5** is a sectional view of the thin film transistor substrate taken along the lines III-III', IV-IV', V-V, VI-VI and VII-VII in FIG. **4**.

[0069] Referring to FIG. **4** and FIG. **5**, the thin film transistor substrate includes a gate line **102** and a data line **104** provided on a lower substrate **145** in such a manner to cross each other with a gate insulating film **146** therebetween, a thin film transistor **106** provided near each crossing, a pixel electrode **114** and a common electrode **118** provided at a pixel area defined by the gate line **102** and the data line **104** for forming a horizontal field, and a common line **116** connected to the common electrode **118**. The thin film transistor substrate further includes a storage capacitor **120** provided at an overlapping portion among a pre-stage gate line **102**, the common line **116** and an upper storage electrode **122**, a gate pad **125** connected to the gate line **102**, a data pad **131** connected to the data line **104**, and a common pad **135** connected to the common line **116**. The gate line **102** supplied with a gate signal and the data line **104** supplied with a data signal define the pixel area, with the gate insulating film **146** therebetween. Herein, the gate line **102** is formed from a first conductive layer (i.e., a gate metal layer), while the data line **104** is formed from a second conductive layer (i.e., a source/drain metal layer).

[0070] The common line **116** and the common electrode **118** supply a reference voltage for driving the liquid crystal. The common line **116** further includes an internal common line **116**A provided in parallel to the gate line **102** at a display area, and an external common line **116**B commonly connected to the internal common line **116**A at a non-display area. The common electrode **118** has a finger shape and is extended from the internal common line **116**A into the pixel area. The common line **116** and the common electrode **118** are formed from the first conductive layer, along with the gate line **102**.

[0071] The thin film transistor **106** charges the data signal of the data line **104** to the pixel electrode **114** in response to the gate signal of the gate line **102**. To this end, the thin film transistor **106** includes a gate electrode **108** connected to the gate line **102**, a source electrode **110** connected to the data line **104**, and a drain electrode **112** opposed to the source electrode **110**. The thin film transistor **106** further includes an active layer **148** overlapping the gate electrode **108** with a gate insulating film **146** therebetween to define a channel between the source electrode **110** and the drain electrode **112**. On the active layer **148** excluding the channel region is an ohmic contact layer **150** to form an ohmic contact with the source electrode **110** and the drain electrode **112**. Further, the active layer **148** and the ohmic contact layer **150** overlaps the data line **104**, a lower data pad electrode **130** and an upper storage electrode **122**, which are formed from the second conductive layer, along with the source electrode **110** and the drain electrode **112**.

[0072] The pixel electrode **114** forms a horizontal electric field at the pixel area, along with the common electrode **118**, and is connected to the drain electrode **112** of the thin film transistor **106**. The pixel electrode **114** is formed from the second conductive layer along with the drain electrode **112** and is integral thereto. More specifically, the pixel electrode **114** includes a horizontal part **114**A provided in parallel to the gate line **102** and integral to the drain electrode **112**, and a finger part **114**B extended from the horizontal part **114**A into the pixel area to be in parallel to the common electrode **118**.

[0073] Thus, a horizontal electric field is formed between the pixel electrode **114** to which a data signal is applied via the thin film transistor **106** and the common electrode **118** to which a reference voltage is applied via the common line **116**. More specifically, a horizontal electric field is formed between the finger part **114**B of the pixel electrode **114** and the common electrode **118**. Liquid crystal molecules arranged in a horizontal direction between the thin film transistor substrate and the color filter substrate rotate by such a horizontal electric field due to a dielectric anisotropy of the liquid crystal molecules. Transmittance of the pixel area is differentiated depending upon an extent of the rotation of the liquid crystal molecules, thereby implementing gray scale levels.

[0074] The storage capacitor **120** is constructed with a portion of the pre-stage gate line **102** as a first lower storage electrode, a portion of an internal common line **116**A as a second lower storage electrode, an upper storage electrode **122** overlapping the gate line **102** and the internal common line **116**A, the gate insulating film **146**, the active layer **148** and the ohmic contact layer **150**, as shown in FIG. **5**. The gate insulating film **146**, the active layer **148** and the ohmic contact layer **150** are sandwiched between the first and second lower storage electrodes **102** and **116** A and the upper storage electrode **122**. Herein, the upper storage electrode **122** is formed from the second conductive layer along with the pixel electrode **114** and is integral thereto. The storage capacitor **120** maintains a data signal charged in the pixel electrode **114** until the next data signal is charged.

[0075] The gate line **102** is connected to a gate driver (not shown) via the gate pad **125**. The gate pad **125** is constructed with a lower gate pad electrode **124** extended from the gate line **102**, and an upper gate pad electrode **128** connected to the lower gate pad electrode **124** via a first contact hole **166** passing through the gate insulating film **146** and the protective film **152**.

[0076] The common line **116** receives a reference voltage from an external reference voltage source (not shown) through the common pad **135**. The common pad **135** includes a lower common pad electrode **136** extended from the common line **116**, and an upper common pad electrode **140** connected to the lower common pad electrode **136** via a second contact hole **170** passing through the gate insulating film **146** and the protective film **152**.

[0077] The data line **104** is connected to the data driver (not shown) via the data pad **131**. The data pad **131** includes a lower data pad electrode **130** extended from the data line **104**, and an upper data pad electrode **134** connected to the lower data pad electrode **130** via a third contact hole **168** passing through the protective film **152**.

[0078] In such a thin film transistor substrate, the upper gate pad electrode **128**, the upper data pad electrode **134** and the upper common pad electrode **140** are formed from a third conductive layer. The third conductive layer is patterned by a lift-off process when removing a photo-resist pattern used for patterning the protective film **152** and the gate insulating film **146**. Thus, the patterned third conductive layer makes an interface with the protective film **152**. A method of fabricating the thin film transistor substrate according to the embodiment of the present invention can reduce one mask process by patterning the third conductive layer using such a lift-off process.

[0079] In order to facilitate such a lift-off process, a stripper penetration path **154** passing through the gate insulating film **146** and the protective film **152** or passing through the protective film **152** are further provided on the above-mentioned signal lines and electrodes. For instance, the stripper penetration path **154** is provided on the common electrode **118** or the pixel electrode **114**, and the third conductive pattern makes an interface with the protective film **152** within the stripper penetration path **154**. Such a stripper penetration path **154** provided at portions having no photo-resist pattern allows a stripper to easily infiltrate into the interface between the photo-resist pattern and the protective film **152**, along with the first to third contact holes **166**, **170** and **168**.

[0080] A method of fabricating the thin film transistor substrate according to the embodiment of the present invention will be described in detail.

[0081] FIG. **6**A and FIG. **6**B are a plan view and a sectional view, respectively, for explaining a first mask process in a fabricating method of the thin film transistor substrate of a horizontal electric field type according to the embodiment of the present invention.

[0082] As shown in FIG. **6**A and FIG. **6**B, a first conductive pattern group including the gate line **102**, the gate electrode **108** and the lower gate pad electrode **124**, the common line **116**, the common electrode **118** and the lower common pad electrode **136** is provided on the lower substrate **145** by a first mask process. More specifically, a first conductive layer is formed on the upper substrate **145** by a deposition technique such as sputtering. Then, the first conductive layer is patterned by photolithography and etching processes using a first mask to thereby form the first conductive pattern group including the gate line **102**, the gate electrode **108**, the lower gate pad electrode **124**, the common line **116**, common electrode **118** and the lower common pad electrode **136**. Herein, the first conductive layer is formed of Cr, MoW, Cr/Al, Cu, Al(Nd), Mo/Al, Mo/Al(Nd) or Cr/Al(Nd), etc.

[0083] FIG. **7**A and FIG. **7**B are a plan view and a sectional view, respectively, for explaining a second mask process in a fabricating method of the thin film transistor substrate of a horizontal electric field type according to the embodiment of the present invention, and FIG. **8**A to FIG. **8**E are sectional views for explaining the second mask process in more detail.

[0084] The gate insulating film **146** is formed on the lower substrate **145** provided with the first conductive pattern by such deposition techniques as plasma enhanced chemical vapor deposition (PECVD), sputtering and the like. Herein, the gate insulating film **146** is formed of an inorganic insulating material such as silicon nitride (SiN_x) or silicon oxide (SiO_x).

[0085] As shown in FIG. **7**A and FIG. **7**B, a semiconductor pattern including the active layer **148** and the ohmic contact layer **150** disposed on the gate insulating film **146** and a second conductive pattern group including the data line **104**, the source electrode **110**, the drain electrode **112**, the lower data pad electrode **130**, the pixel electrode **114** and the upper storage electrode **122** are formed by a second mask process. More specifically, as shown in FIG. **8**A, an amorphous silicon layer **148**A, an n^+ amorphous silicon layer **150**A and a second conductive layer **156** are sequentially formed on the gate insulating film **146** by such deposition techniques as plasma enhanced chemical vapor deposition (PECVD) and sputtering, etc. Herein, the second conductive layer **156** is formed of Cr, MoW, Cr/Al, Cu, Al(Nd), Mo/Al, Mo/Al(Nd) or Cr/Al (Nd), etc.

[0086] Next, a photo-resist film is entirely coated onto the second conductive layer **156** and then a photo-resist pattern **158** having a step coverage shown in FIG. **8**A is formed thereon by a photolithography process using a second mask that is a partial-exposure mask. In this case, a partial-exposure mask having a diffractive exposing part (or a semi-transmitting or transflective part) at a portion where a channel of the thin film transistor is to be formed is used as the second mask. Thus, the photo-resist pattern **158** corresponding to the diffractive exposing part (or the semi-transmitting part) of the second mask has a lower height than the photo-resist pattern **158** corresponding to a transmitting part (or a shielding part) of the second mask. In other words, the photo-resist pattern **158** at the channel portion has a lower height than the photo-resist pattern **158** at other source/drain metal pattern portions.

[0087] Subsequently, the second conductive layer **156** is patterned by a wet-etching process using the photo-resist pattern **158** to thereby form the second conductive metal pattern group including the data line **104**, the source electrode **110** of the thin film transistor portion, the drain electrode **112** being integral to the source electrode **110**, the pixel electrode **114**, the lower data pad electrode **130** and the upper storage electrode **122**, as shown in FIG. **8**B. Herein, the upper storage electrode **122** overlaps a portion of the gate line **102** and the internal common line **116**A, while the pixel electrode **114** is integral to the drain electrode **112** and the upper storage electrode **122**. Further, the n^+ amorphous silicon layer **150**A and the amorphous silicon layer **148**A are patterned at the same time by a dry-etching process using the same photo-resist pattern **158** to thereby provide a structure in which the ohmic contact layer **150** and the active layer **148** are formed with the second conductive pattern group as, shown in FIG. **8**B.

[0088] Then, as shown in FIG. **8**C, the photo-resist pattern **158** at the channel portion having a relatively low height is removed by an ashing process using an oxygen (O_2) plasma, while the photo-resist pattern **158** at other second conductive pattern group portions becomes to have a lower height than the height before the ashing process. The second conductive layer and the ohmic contact layer **150** at a portion in which the channel is formed are etched by a dry-etching process using the photo-resist pattern **158** left in this manner, thereby disconnecting the source electrode **110** from the drain electrode **112** and exposing the active layer **148**, as shown in FIG. **8**C. Thus, a channel made from the active layer **148** is formed between the source electrode **110** and the drain electrode **112**.

Then, the photo-resist pattern **158** left on the second conductive pattern group portion is entirely removed by a stripping process, as shown in FIG. **8**D.

[0089] FIG. **9**A and FIG. **9**B are a plan view and a sectional view, respectively, for explaining a third mask process in a fabricating method of the thin film transistor substrate of a horizontal electric field type according to the embodiment of the present invention, and FIG. **10**A to FIG. **10**D are sectional views for explaining the third mask process in more detail.

[0090] As shown in FIG. **9**A and FIG. **9**B, the protective film **152** and the gate insulating film **146** are patterned by a third mask process, and the third conductive pattern group including the upper gate pad electrode **128**, the upper data pad electrode **134** and the upper common pad electrode **140** is formed. The third conductive pattern group makes an interface with the patterned protective film **152** without any overlapping portions. More specifically, the protective film **152** is entirely formed on the gate insulating film **146** provided with the second conductive pattern group, as shown in FIG. **10**A. Herein, the protective film **152** is formed of an inorganic insulating material similar to the gate insulating film **146** or an organic insulating material. Further, a photo-resist pattern **160** is formed on the protective film **152** by a photolithography process using a third mask, as shown in FIG. **10**A. The protective film **152** and the gate insulating film **146** are patterned by a dry-etching process using the photo-resist pattern **160** to thereby form the first to third contact holes **166**, **170** and **168** passing through the protective film **152** or the protective film **152** and the gate insulating film **146** and the stripper penetration path **154**, as shown in FIG. **10**B. Herein, the first contact hole **166** exposes the lower gate pad electrode **124**, the second contact hole **170** exposes the lower common pad electrode **136**, and the third contact hole **168** exposes the lower data pad electrode **130**. Further, the stripper penetration path **154** exposes the common electrode **118** or the pixel electrode **114**.

[0091] Subsequently, as shown in FIG. **10**C, a third conductive layer **172** is entirely formed on the thin film transistor substrate, on which the photo-resist pattern **160** remains, by a deposition technique such as sputtering or the like. The third conductive layer **172** is formed of a transparent conductive layer including indium-tin-oxide (ITO), tin-oxide (TO), indium-zinc-oxide (IZO) or SnO_2, etc. Alternatively, the third conductive film **172** is formed of a metal material having a high corrosion-resistance and a high strength property, such as titanium (Ti) or tungsten (W), etc.

[0092] Then, the photo-resist pattern **160** is removed by a lift-off process, along with the third conductive layer **172** thereon, to thereby form the upper gate pad electrode **128**, the upper common pad electrode **140**, the upper data pad electrode **134** and the dummy transparent conductive pattern **164** in each of the first to third contact holes **166**, **170** and **168** and the stripper penetration path **154**, as shown in FIG. **10**D.

[0093] In this case, the first to third contact holes **162**, **166** and **170** and the stripper penetration path **154** are formed at a portion in which the photo-resist pattern **160** does not exist such that a greater amount of a stripper, for example, stripper A, can be infiltrated into the interface between the photo-resist pattern **160** and the protective film **152**. As a result, the photo-resist pattern **160** covered with the third conductive layer **172** can be easily separated from the protective film **152** by the stripper A. This is because the edge of the photo-resist pattern **160** has more protrusions (not shown) than the edge of the protective film **152** at portions where the stripper penetration path **154** and the first to third contact holes **162**, **166** and **170** are provided in the protective film **152** due to an over-etching of the protective film **152**. Further, this is because the third conductive layer **172** deposited in a direction perpendicular to the substrate **145** between the edge of the photo-resist pattern **160** and the edge of the protective film **152** has openings, or is relatively thinly deposited due to the protruded edge of the photo-resist pattern **160**, thereby allowing the stripper A to easily infiltrate the photo-resist pattern **160**.

[0094] As described above, an unnecessary portion of the third conductive layer **172** and the photo-resist pattern **160** are removed by the lift-off process, so that the third conductive pattern group can make an interface with the protective film **152**. More specifically, the upper gate pad electrode **128**, the upper common pad electrode **140** and the upper data pad electrode **134** are provided within the corresponding contact holes **166**, **170** and **168** to be connected to the lower gate pad electrode **124**, the lower common pad electrode **136** and the lower data pad electrode **130**, respectively. Further, the third dummy conductive pattern **164** left in the stripper penetration path **154** also makes an interface with the protective film **152** within the stripper penetration path **154**.

[0095] Examples of a shape of the stripper penetration path **154** passing through the gate insulating film **146** and/or the protective film **152** on the common electrode **118** and/or the pixel electrode **114** will be described.

[0096] Referring to FIG. **11**A and FIG. **11**B, the stripper penetration path **154** is formed to have a shape of a slit **180** passing through the gate insulating film **146** and the protective film **152** on the common electrode **118**. Further, the third dummy conductive pattern **182** remains in the slit **180**. Such a slit **180** may be provided on any one of the signal lines including the gate line, the common line and the data line and the pixel electrode.

[0097] Referring to FIG. **12**A and FIG. **12**B, the stripper penetration path **154** is formed to have a plurality of holes **184** passing through the gate insulating film **146** and the protective film **152** on the common electrode **118**. The third dummy conductive pattern **186** separated from each other remains within the plurality of holes **184**. The plurality of holes **184** may be provided on any one of the signal lines including the gate line, the common line and the data line and the pixel electrode.

[0098] As described above, according to the present invention, a lift-off process is employed to eliminate the mask process of the third conductive layer. Accordingly, the thin film transistor substrate is fabricated by a three-mask process, so that the simplified fabrication process reduces the manufacturing cost and improves the production yield. Furthermore, according to the present invention, the stripper penetration path is provided on the signal lines in the protective film, so that the lift-off process for removing the photo-resist pattern covered with the third conductive layer can be effectively facilitated.

[0099] It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

1-8. (canceled)

9. A method of fabricating an LCD of a horizontal electric field type having a liquid crystal between lower and upper substrates, comprising:

forming a first conductive pattern group including a gate line, a gate electrode connected to the gate line, a lower gate pad electrode, a common line, a common electrode extended from the common line, a lower common pad electrode connected to the common line on the lower substrate by patterning a first conductive layer;

forming a gate insulating film on the first conductive pattern group;

forming a semiconductor pattern on the gate insulating film;

forming a second conductive pattern group including a data line crossing the gate line to define a pixel area, a source electrode and a lower data pad electrode connected to the data line, a drain electrode opposed to the source electrode and a pixel electrode connected to the drain electrode on the semiconductor pattern by pattering a second conductive layer, the common electrode and the pixel electrode forming a horizontal electric field in the pixel area during an operation of the LCD;

forming a protective film on the second conductive pattern group;

forming first to third contact holes for the lower gate pad electrode, the lower common pad electrode and the lower data pad electrode by patterning at least one of the protective film and the gate insulating film using a photo-resist pattern; and

forming a third conductive pattern group including an upper gate pad electrode, an upper common pad electrode and an upper data pad electrode by depositing a third conductive layer on the photo-resist pattern and then by lifting-off the photo-resist pattern, the upper gate pad electrode, the upper common pad electrode and the upper data pad electrode connected to the lower gate pad electrode, the lower common pad electrode and the lower data pad electrode, respectively, via the first to third contact holes.

10. The method according to claim **9**, further comprising:

forming a stripper penetration path hole on at least one of the gate line, the data line, the common line, the pixel electrode and the common electrode in the pixel area, and at the same time

11. The method according to claim **10**, wherein the stripper penetration path hole facilitates the lifting off process of the photo-resist pattern.

12. The method according to claim **11**, wherein the photo-resist pattern has protrusions in an interface with the protective film.

13. The method according to claim **10**, wherein the stripper penetration path hole is formed to have a shape of a slit or a plurality of holes.

14. The method according to claim **9**, further comprising:

forming an upper storage electrode overlapping a portion of the gate line and a portion of the common line adjacent to the gate line with the gate insulating film and the semiconductor pattern therebetween and electrically connected to the pixel electrode.

15. The method according to claim **10**, wherein the stripper penetration path is formed in such a manner to go through until the gate insulating film under the protective film.

16. The method according to claim **10**, wherein the stripper penetration path includes any at least one of a slit and a plurality of holes provided along any at least one of said plurality of signal lines and electrodes.

17. The method according to claim **10**, wherein the stripper penetration path is provided on any at least one of a common electrode and a pixel electrode.

18. The method according to claim **10**, wherein said third conductive layer contains any one of a transparent conductive layer, titanium and tungsten.

19. A method of fabricating a thin film transistor substrate of horizontal electric field applying type, said method comprising:

a first mask process of forming a gate line, a gate electrode and a lower gate pad electrode connected to the gate line, a common line parallel to the gate line, a lower common pad electrode connected to the common line and a common electrode extended from the common line into a pixel area on a substrate from a first conductive layer;

a second mask process of entirely coating a gate insulating film, and forming a semiconductor pattern at a desired area of the gate insulating film and forming a data line crossing the gate line and the common line, a source electrode and a lower data pad electrode connected to the data line, a drain electrode opposed to the source electrode and a pixel electrode connected to the drain electrode to form a horizontal electric field along with the common electrode on said semiconductor pattern from a second conductive layer; and

a third mask process of entirely coating the protective film, patterning the protective film along with the gate insulating film to define first to fourth contact holes for exposing the lower gate pad electrode, the lower common pad electrode and a lower data pad electrode, and forming an upper gate pad electrode, an upper common pad electrode and an upper data pad electrode from a third conductive layer within the first to fourth contact holes.

20. The method according to claim **19**, wherein said third mask process includes:

entirely coating the protective film;

forming a photo-resist pattern on the protective film using a mask;

patterning the protective film and the gate insulating film by the photo-resist pattern;

entirely coating a transparent conductive film onto the photo-resist pattern; and

removing the photo-resist pattern covered with the transparent conductive film to pattern the transparent conductive film.

21. The method according to claim **19**, wherein said third mask process further comprises:

providing a penetration path of a stripper going through a protective film on any at least one of a plurality of signal lines and electrodes formed from said first and second conductive layers in order to remove said photo-resist pattern.

22. The method according to claim **21**, wherein the stripper penetration path is formed in such a manner to go through until the gate insulating film under the protective film.

23. The method according to claim **21**, wherein the stripper penetration path includes any at least one of a slit and a plurality of holes provided along any at least one of said plurality of signal lines and electrodes.

24. The method according to claim **21**, wherein the stripper penetration path is provided on any at least one of a common electrode and a pixel electrode.

25. The method according to claim **24**, wherein said third conductive layer making an interface with the patterned protective film is left within the stripper penetration path.

26. The method according to claim **25**, wherein the first to third contact holes are used as the stripper penetration path.

27. The method according to claim **19**, wherein said second mask process further comprises:

forming an upper storage electrode overlapping with a portion of the gate line and a portion of the common line adjacent to the gate line with having the gate insulating film and the semiconductor pattern therebetween and connected to the pixel electrode from said second conductive layer.

28. The method according to claim **19**, wherein said third conductive layer contains any one of a transparent conductive layer, titanium and tungsten.

* * * * *

patsnap

专利名称(译)	水平电场施加型液晶显示器及其制作方法		
公开(公告)号	US20130295701A1	公开(公告)日	2013-11-07
申请号	US13/933837	申请日	2013-07-02
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. LTD.		
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IPC分类号	G02F1/1333 G02F1/1343 G02F1/1362		
CPC分类号	G02F1/1333 G02F1/134363 G02F1/13458 G02F1/136227		
优先权	1020030077658 2003-11-04 KR		
其他公开文献	US8830437		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种水平电场型液晶显示（LCD）装置。 LCD器件通过三掩模工艺制造，并具有栅极焊盘，公共焊盘和数据焊盘电极，每个都包括由透明导电材料形成的上电极。通过剥离工艺，这些上电极形成在接触孔内。