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Kajita et al.

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(45) **Date of Patent: Dec. 17, 2019**

(54) **LIQUID CRYSTAL DISPLAY DEVICE WITH OVERLAPPING SEMICONDUCTOR LAYERS**

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(73) Assignee: **Panasonic Liquid Crystal Display Co., Ltd.**, Hyogo (JP)

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(22) Filed: **Mar. 8, 2018**

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(30) **Foreign Application Priority Data**

Mar. 9, 2017 (JP) 2017-044784

(51) **Int. Cl.**

G02F 1/1368 (2006.01)
G02F 1/1362 (2006.01)
G02F 1/1333 (2006.01)
G02F 1/1347 (2006.01)
(Continued)

(52) **U.S. Cl.**

CPC ***G02F 1/1368*** (2013.01); ***G02F 1/13471*** (2013.01); ***G02F 1/133345*** (2013.01); ***G02F 1/136209*** (2013.01); *G02F 1/133512* (2013.01); *G02F 2001/133562* (2013.01); *G02F 2001/133567* (2013.01); *G02F 2001/133601* (2013.01); *G02F 2001/134372* (2013.01); *G02F 2201/40* (2013.01); *G02F 2202/103* (2013.01); *G02F 2202/28* (2013.01)

(58) **Field of Classification Search**

CPC G02F 2201/52; G02F 1/1347; G02F 1/13471; G02F 2001/133567; G02F 2001/133562; G02F 2202/103; H01L 29/78669

See application file for complete search history.

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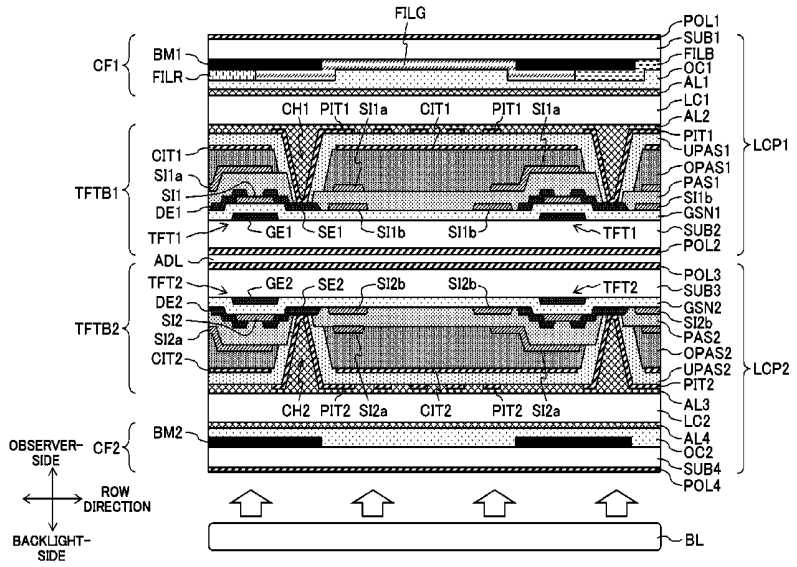
(57) **ABSTRACT**

A liquid crystal display device includes a first substrate formed with a first gate line, a first source line, a first thin film transistor including a first channel region and a first semiconductor layer, and a second semiconductor layer electrically insulated from the first semiconductor layer, a second substrate disposed opposite to the first substrate, and a first liquid crystal layer disposed between the first substrate and the second substrate. The second semiconductor layer is disposed between the first thin film transistor and the first liquid crystal layer, and overlaps at least a part of the first channel region of the first thin film transistor in planar view.

16 Claims, 22 Drawing Sheets



(51) **Int. Cl.**
G02F 1/1335 (2006.01)
G02F 1/1343 (2006.01)

(56) **References Cited**

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FIG.1

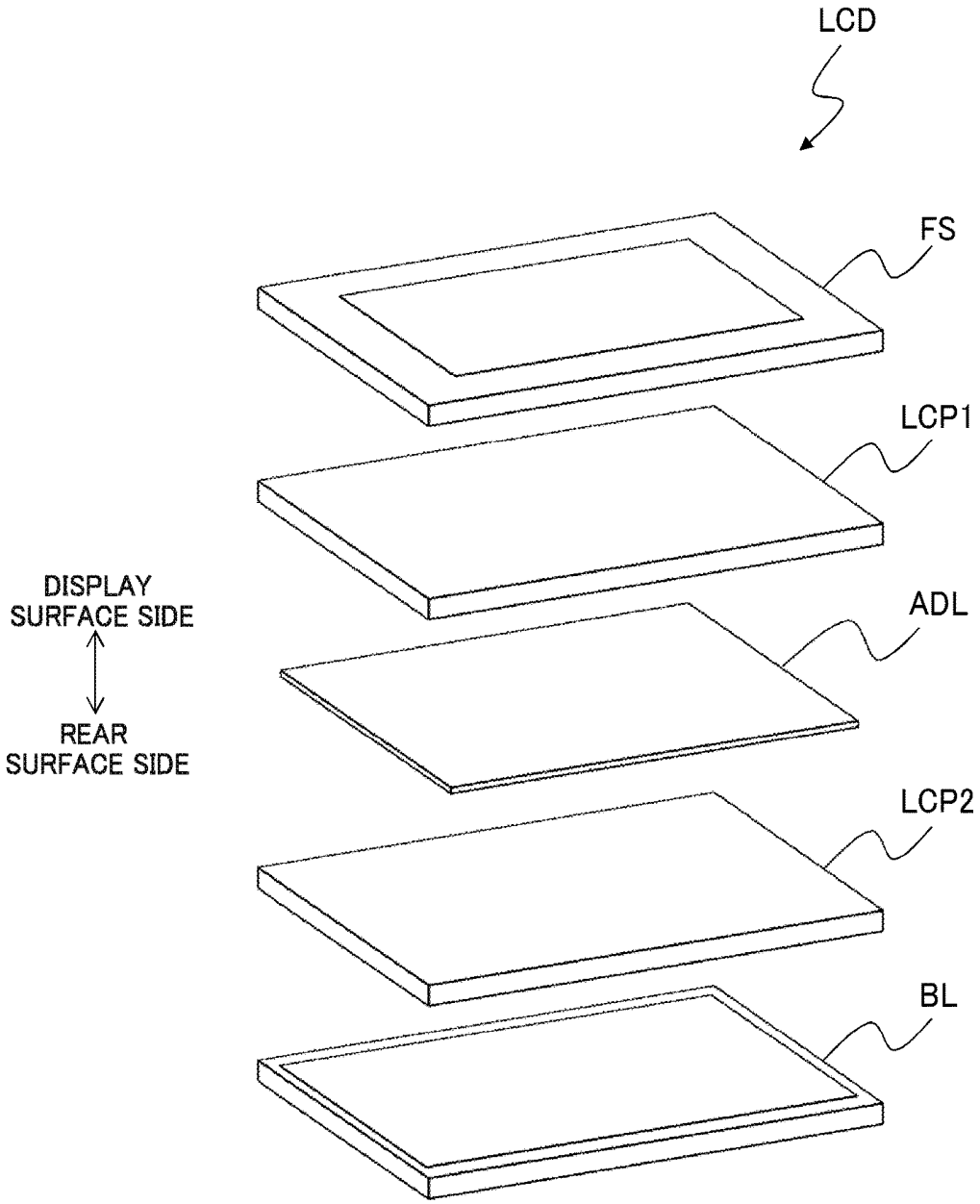

LCD
FS
LCP1
ADL
LCP2
BL
DISPLAY SURFACE SIDE
REAR SURFACE SIDE

FIG.2

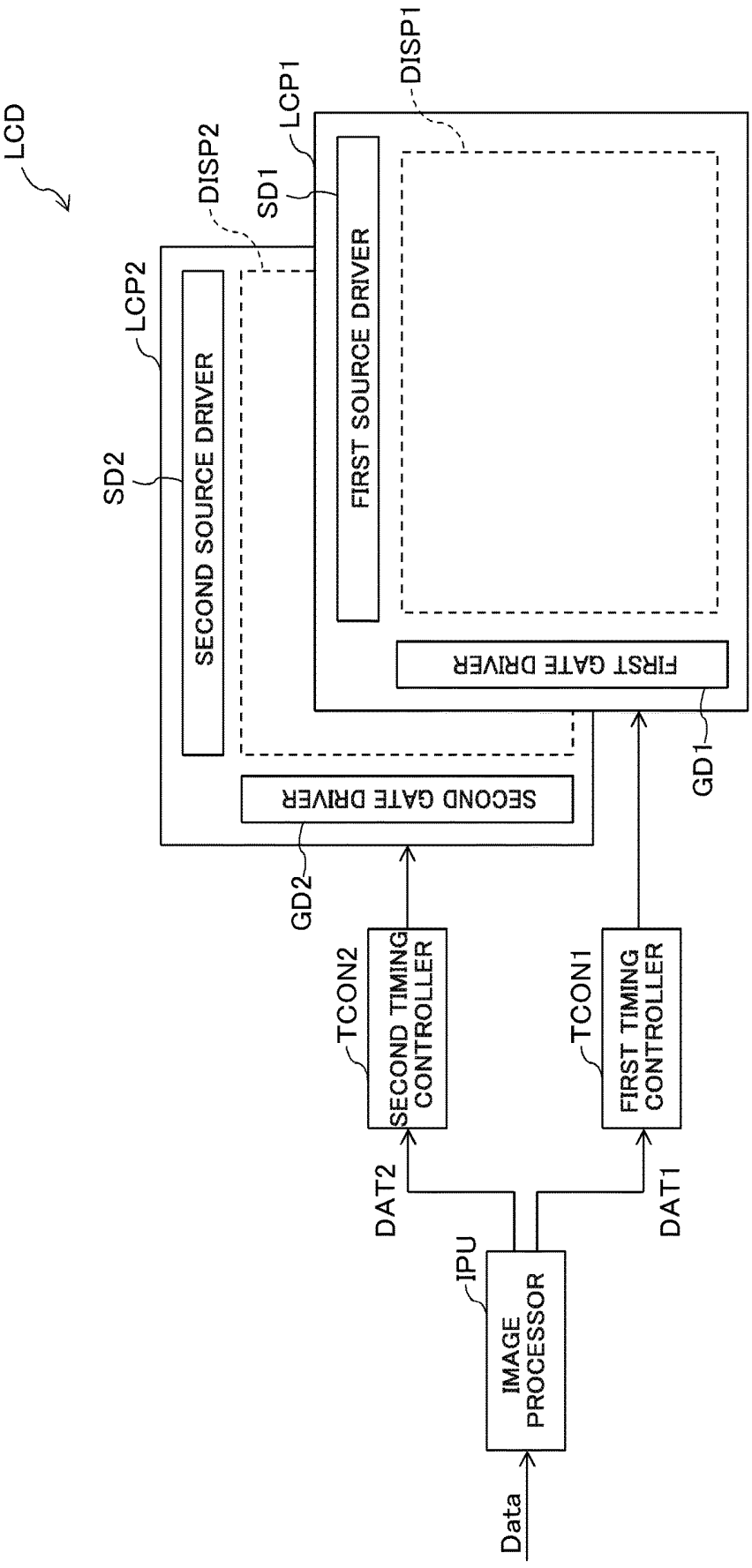

LCD
DISP1
LCP1
SD1
FIRST SOURCE DRIVER
FIRST GATE DRIVER
GD1
DISP2
LCP2
SD2
SECOND SOURCE DRIVER
SECOND GATE DRIVER
GD2
TCON2
SECOND TIMING CONTROLLER
TCON1
FIRST TIMING CONTROLLER
DAT2
DAT1
IPU
IMAGE PROCESSOR
Data

FIG.3

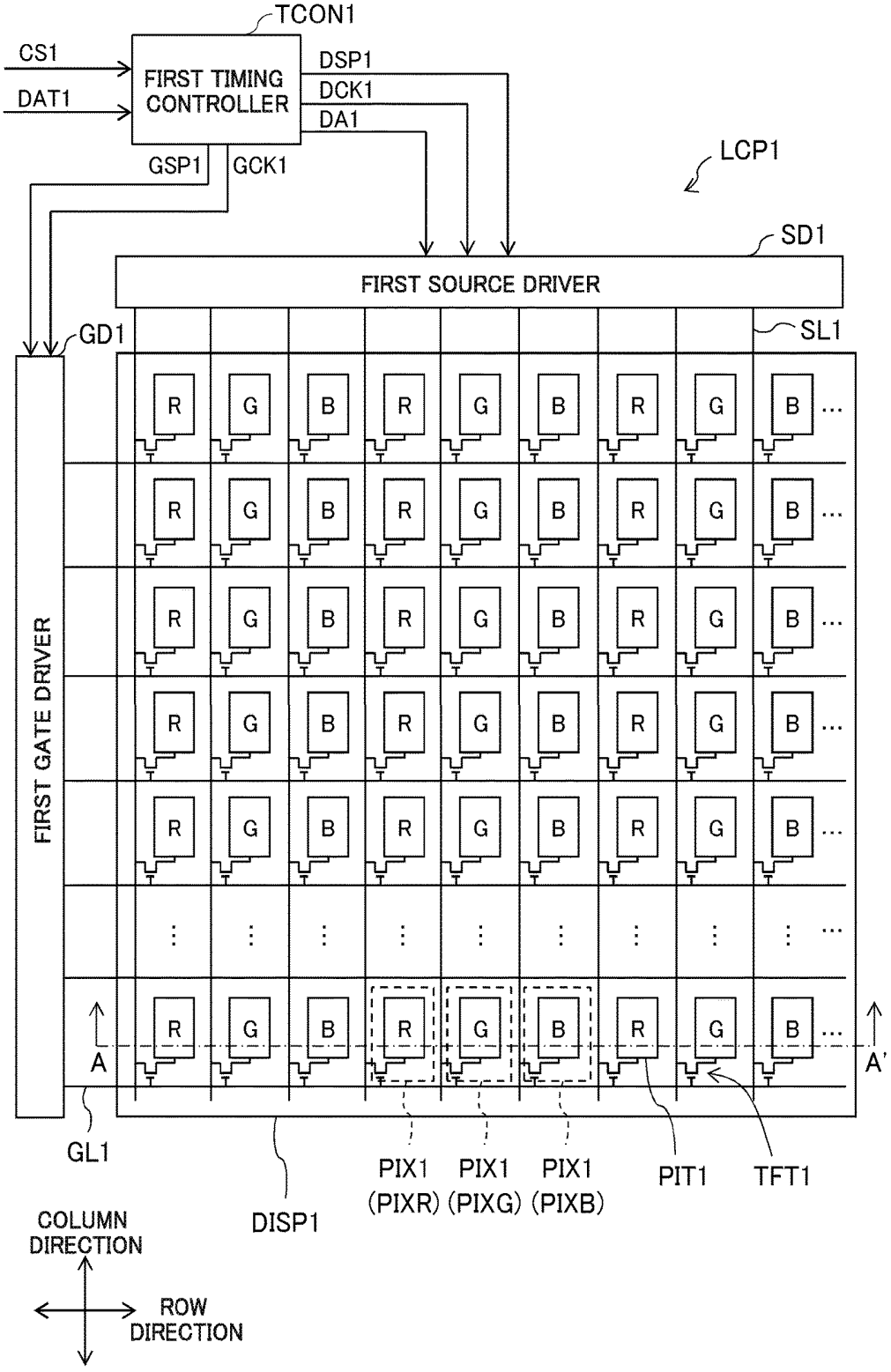

TCON1
CS1
DAT1
FIRST TIMING CONTROLLER
DSP1
DCK1
DA1
GSP1
GCK1
LCP1
SD1
FIRST SOURCE DRIVER
GD1
SL1
FIRST GATE DRIVER
R
G
B
A
A'
GL1
DISP1
PIX1 (PIXR)
PIX1 (PIXG)
PIX1 (PIXB)
PIT1
TFT1
COLUMN DIRECTION
ROW DIRECTION

FIG.4

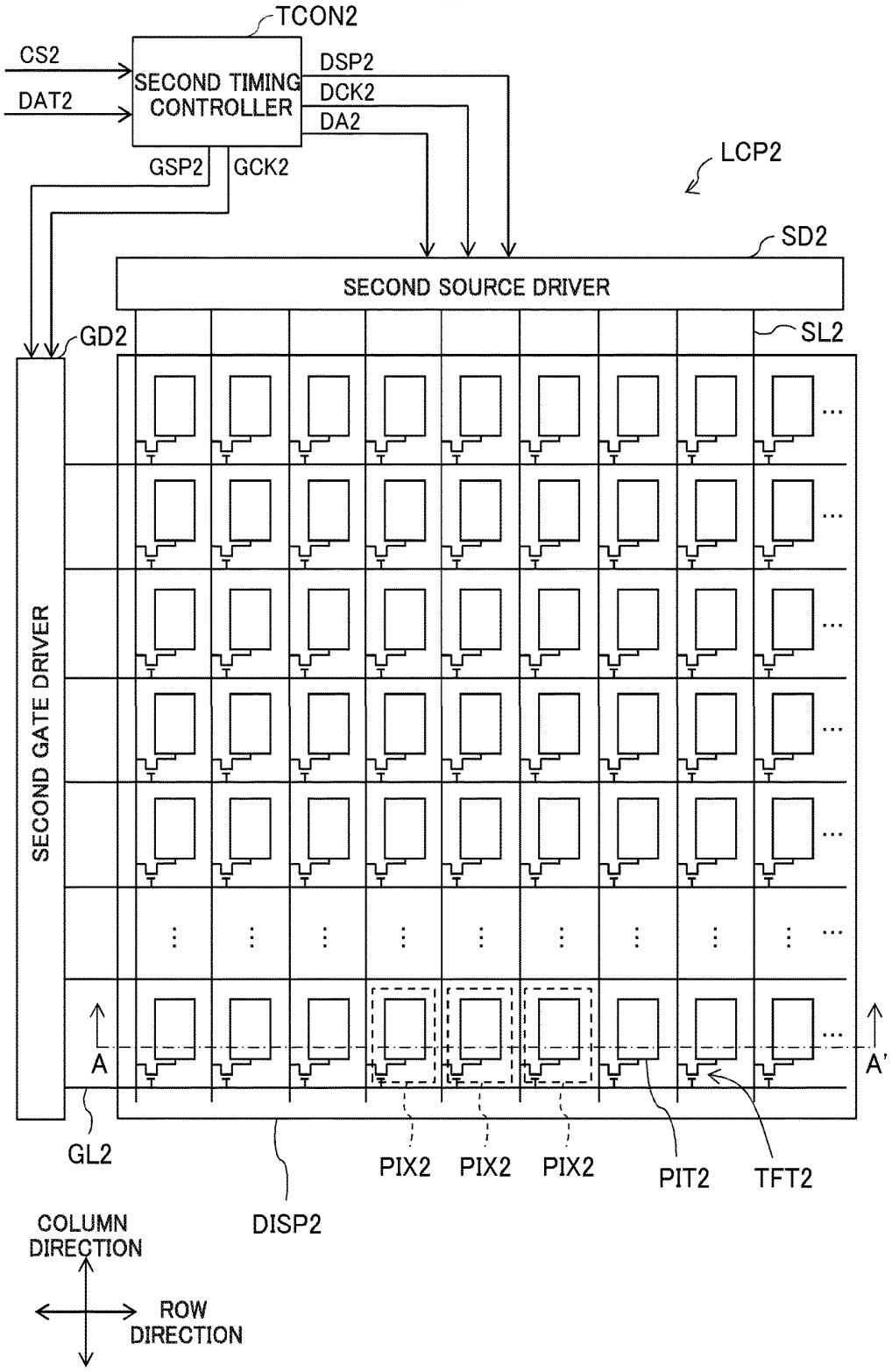

TCON2
CS2
DAT2
SECOND TIMING CONTROLLER
DSP2
DCK2
DA2
GSP2
GCK2
LCP2
SD2
SECOND SOURCE DRIVER
GD2
SL2
SECOND GATE DRIVER
A
A'
GL2
DISP2
PIX2
PIX2
PIX2
PIT2
TFT2
COLUMN DIRECTION
ROW DIRECTION

FIG.5

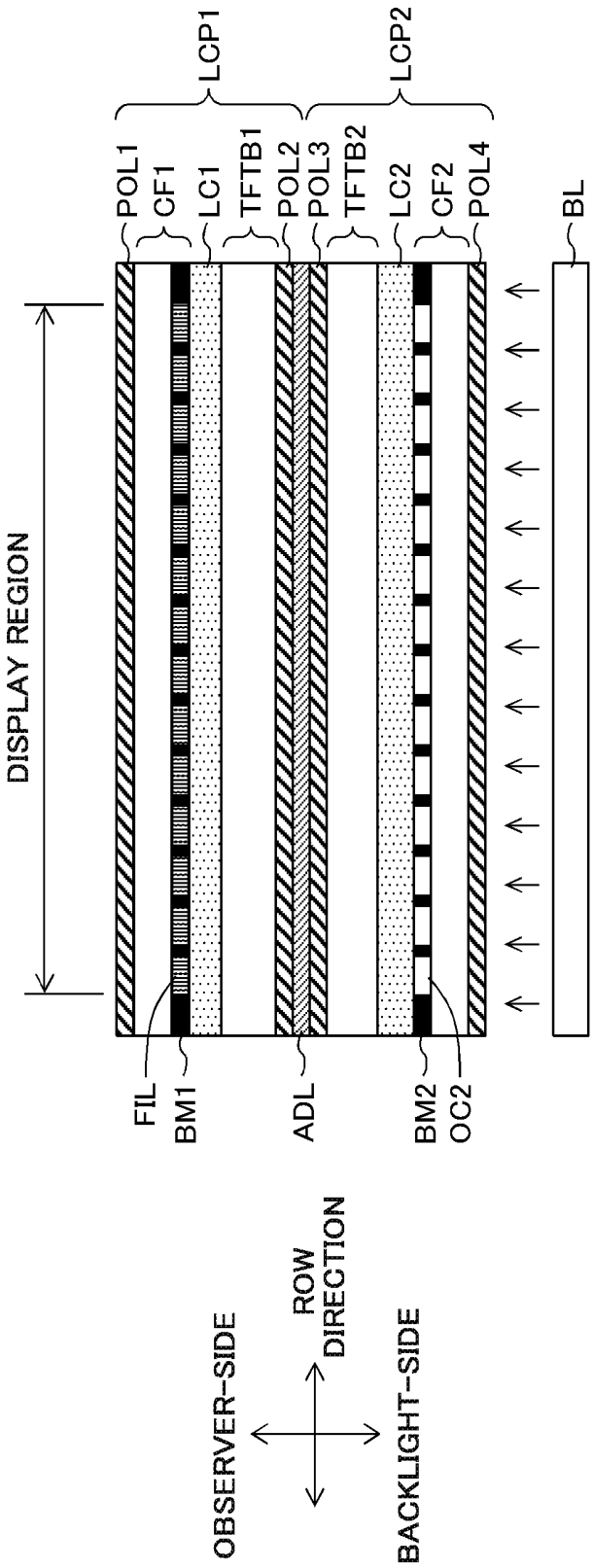

LCP1
LCP2
POL1
CF1
LC1
TFTB1
POL2
POL3
TFTB2
LC2
CF2
POL4
BL
DISPLAY REGION
FIL
BM1
ADL
BM2
OC2
OBSERVER-SIDE
ROW DIRECTION
BACKLIGHT-SIDE

FIG.6A

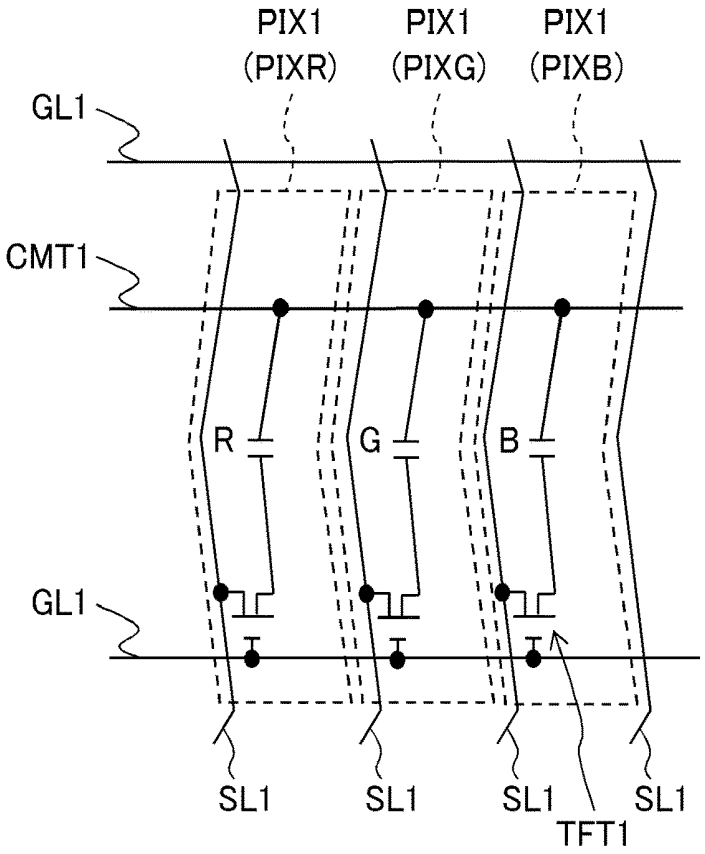

PIX1
(PIXR)
PIX1
(PIXG)
PIX1
(PIXB)
GL1
CMT1
R
G
B
GL1
SL1
SL1
SL1
SL1
TFT1

FIG.6B

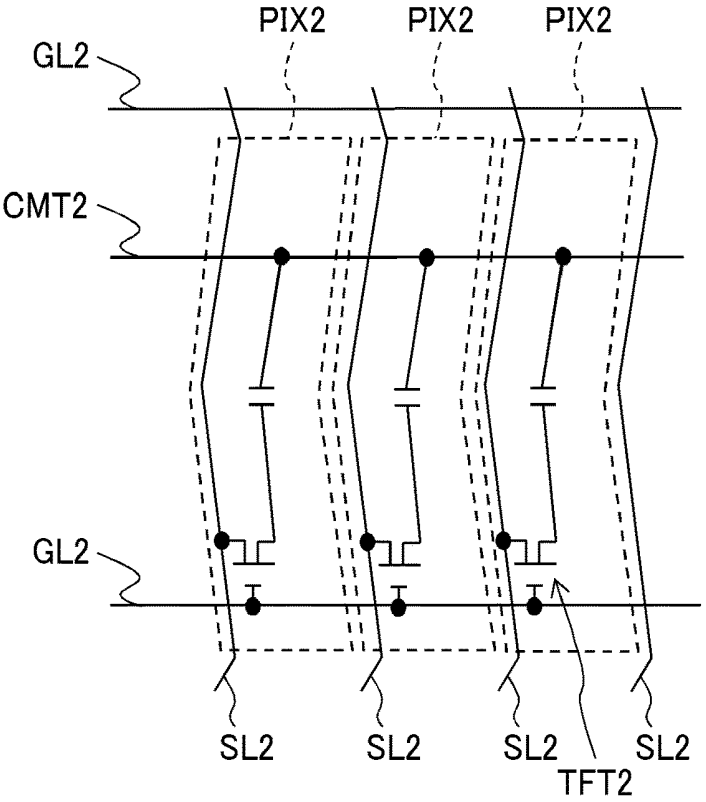

PIX2
PIX2
PIX2
GL2
CMT2
GL2
SL2
SL2
SL2
SL2
TFT2

FIG.7

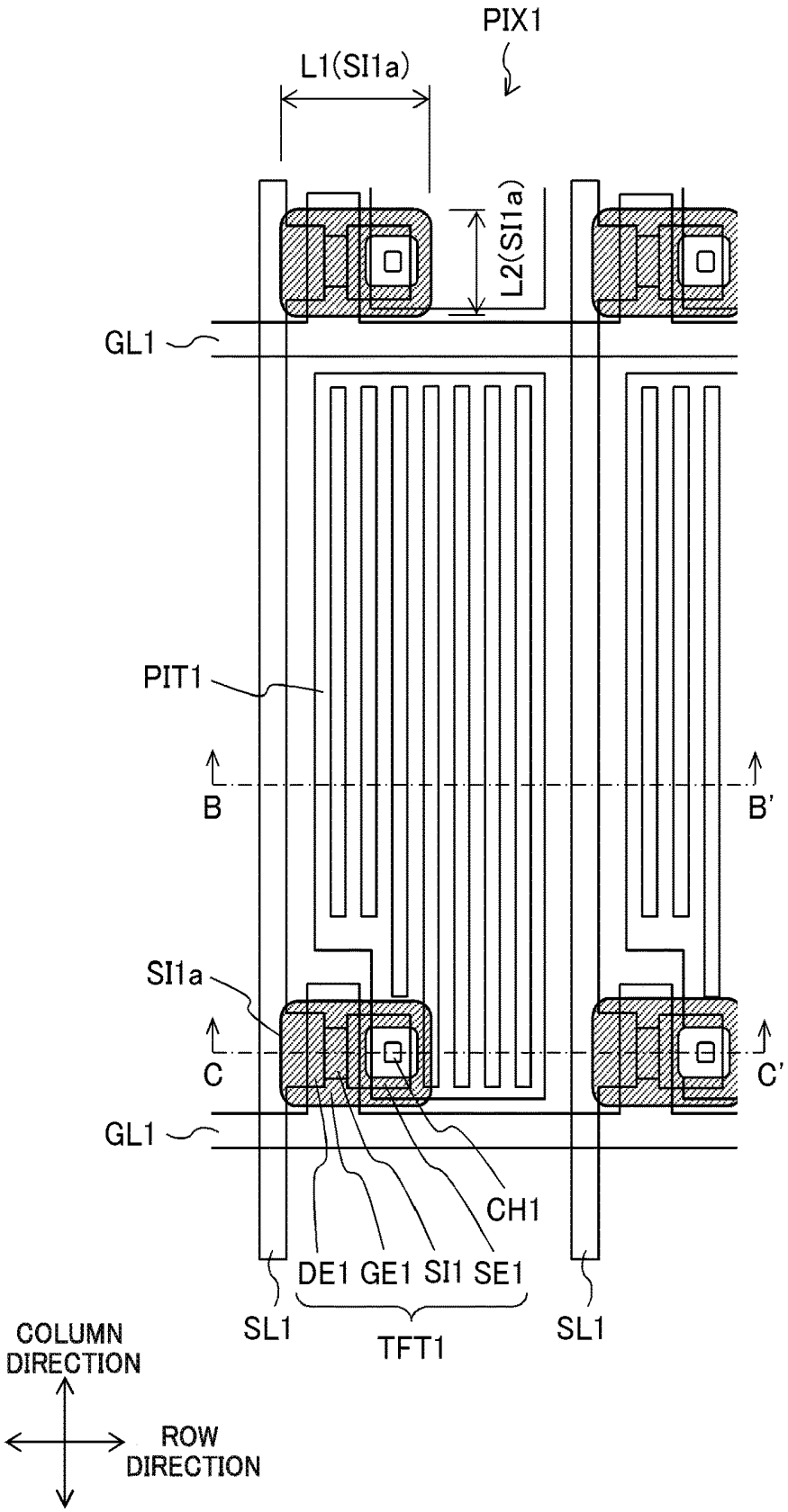

PIX1
L1(SI1a)
L2(SI1a)
GL1
PIT1
B
B'
SI1a
C
C'
GL1
CH1
DE1 GE1 SI1 SE1
SL1
TFT1
SL1
COLUMN DIRECTION
ROW DIRECTION

FIG.8

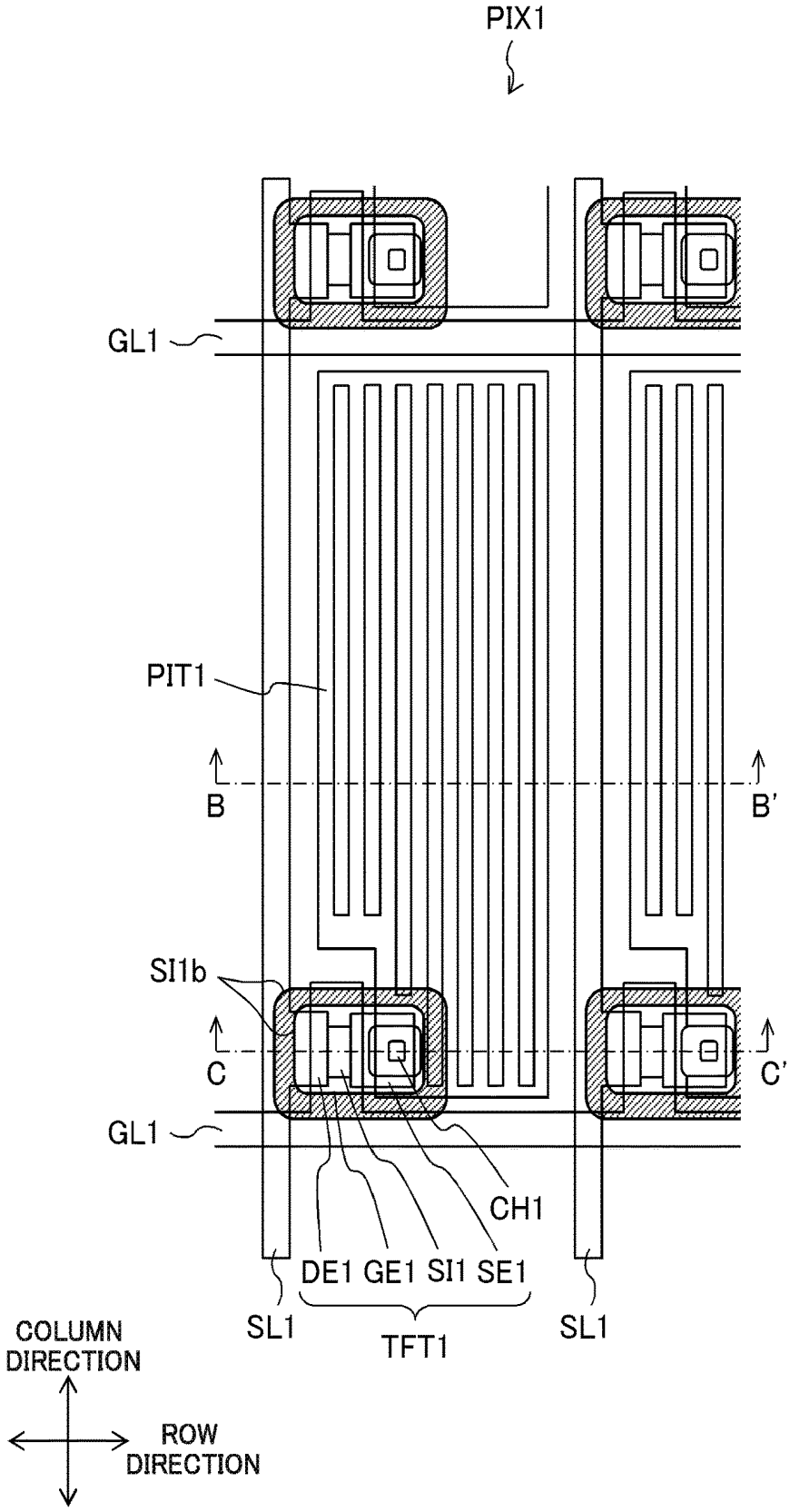

PIX1
GL1
PIT1
B
B'
SI1b
C
C'
GL1
CH1
DE1 GE1 SI1 SE1
SL1
TFT1
SL1
COLUMN DIRECTION
ROW DIRECTION

FIG.9

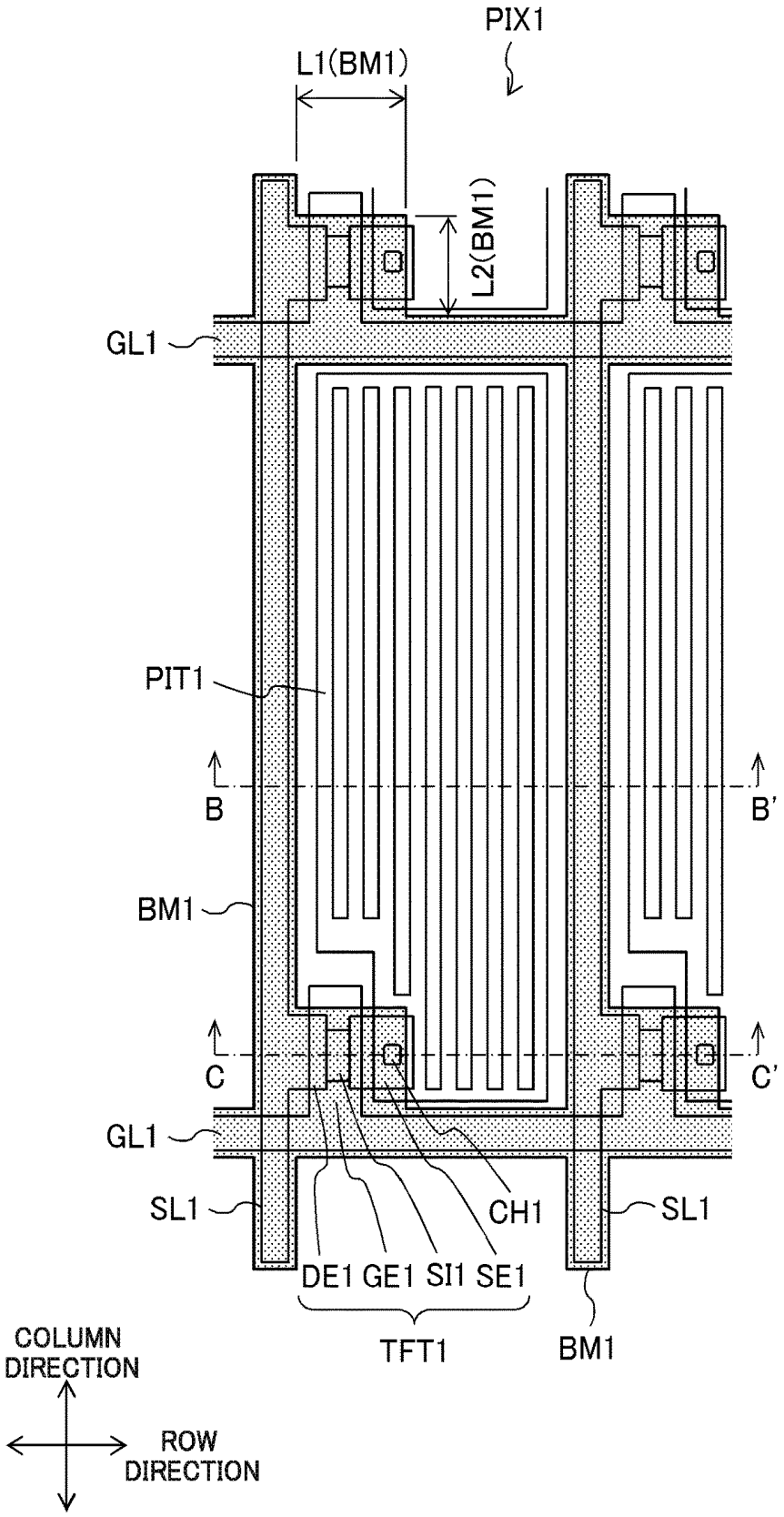

PIX1
L1(BM1)
L2(BM1)
GL1
PIT1
B
B'
BM1
C
C'
GL1
SL1
CH1
SL1
DE1 GE1 SI1 SE1
TFT1
BM1
COLUMN DIRECTION
ROW DIRECTION

FIG.10

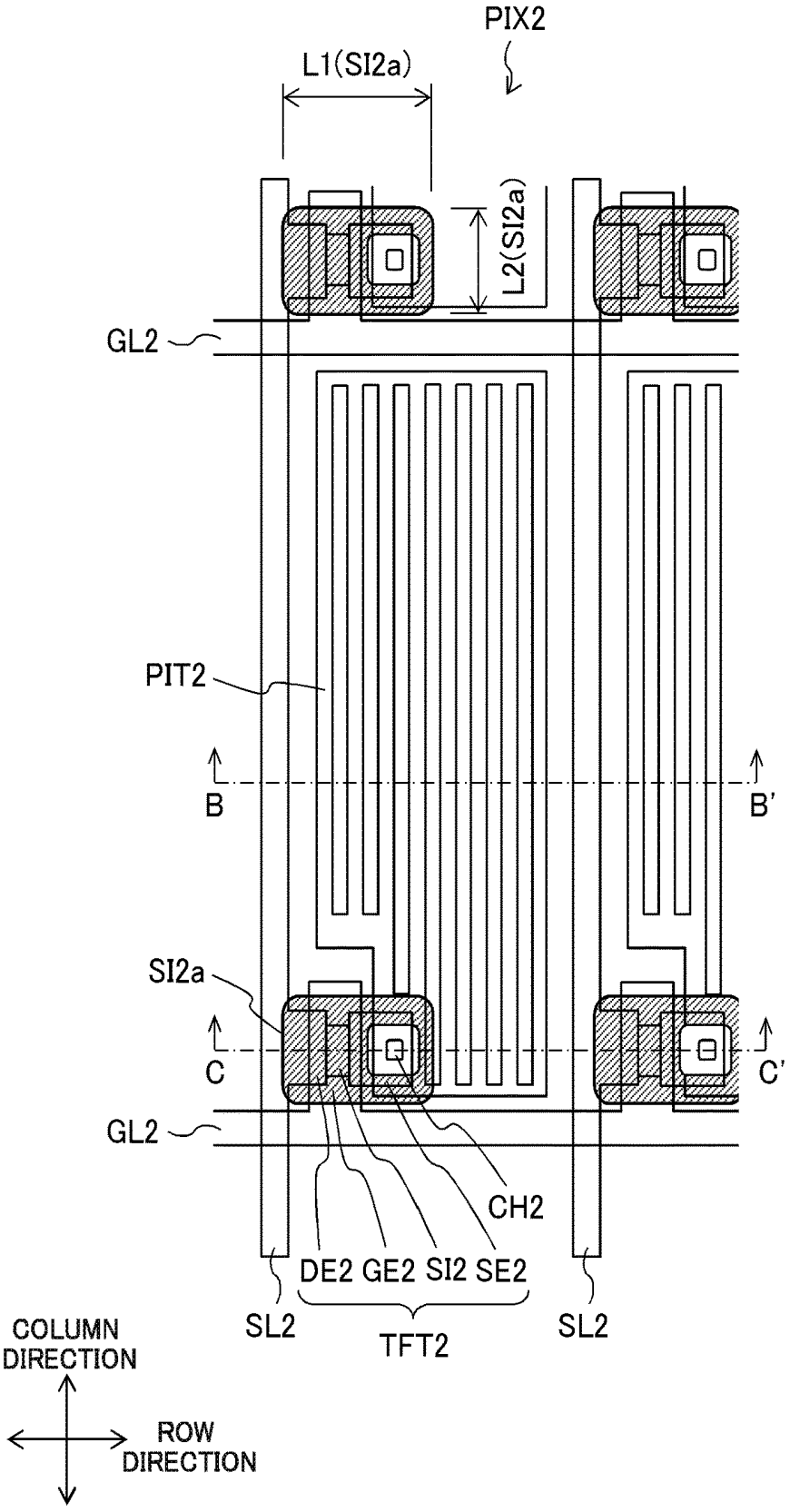

PIX2
L1(SI2a)
L2(SI2a)
GL2
PIT2
B
B'
SI2a
C
C'
GL2
CH2
DE2 GE2 SI2 SE2
SL2
TFT2
SL2
COLUMN DIRECTION
ROW DIRECTION

FIG.11

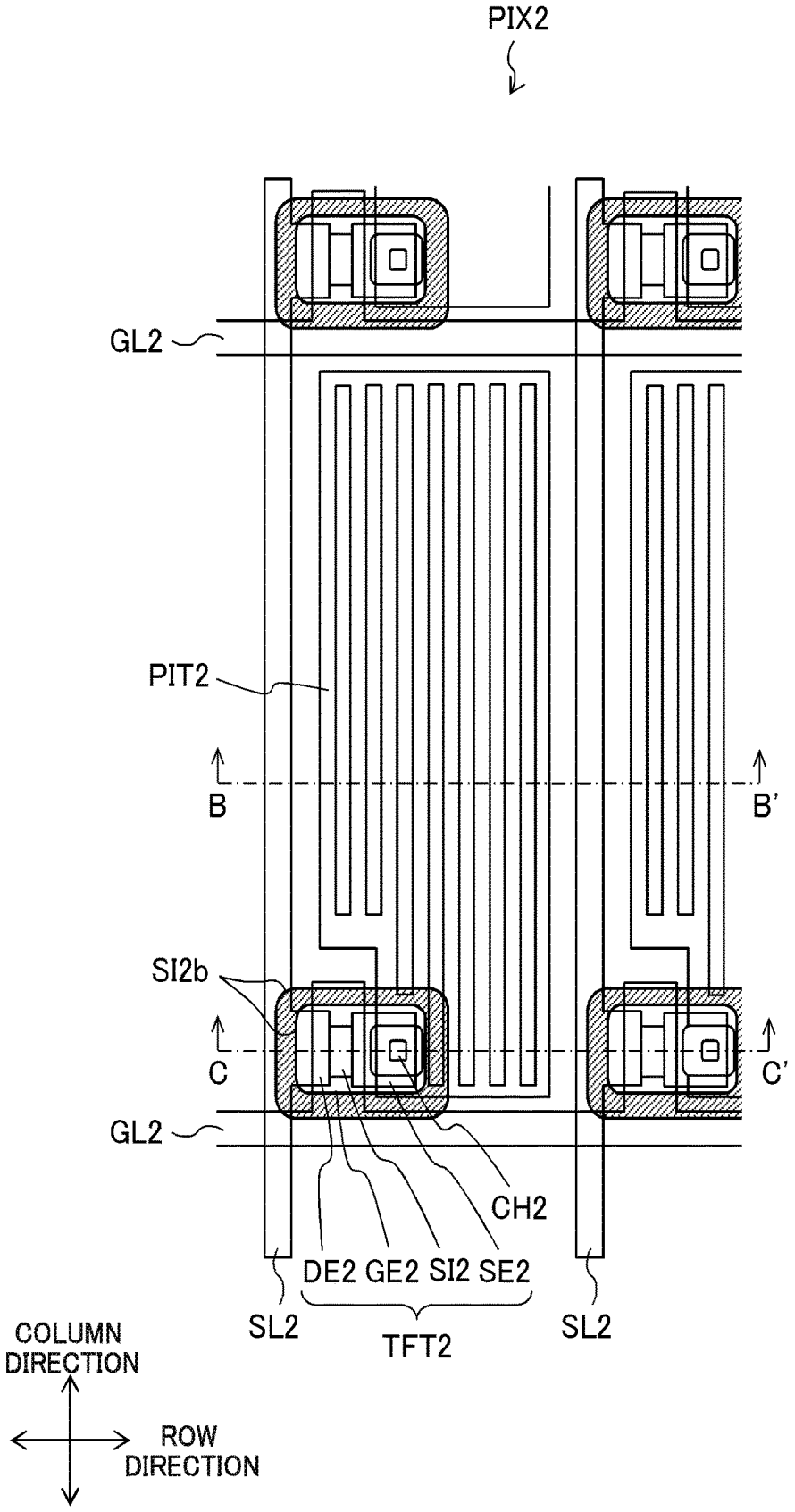

PIX2
GL2
PIT2
B
B'
SI2b
C
C'
GL2
CH2
DE2 GE2 SI2 SE2
SL2
TFT2
SL2
COLUMN DIRECTION
ROW DIRECTION

FIG.12

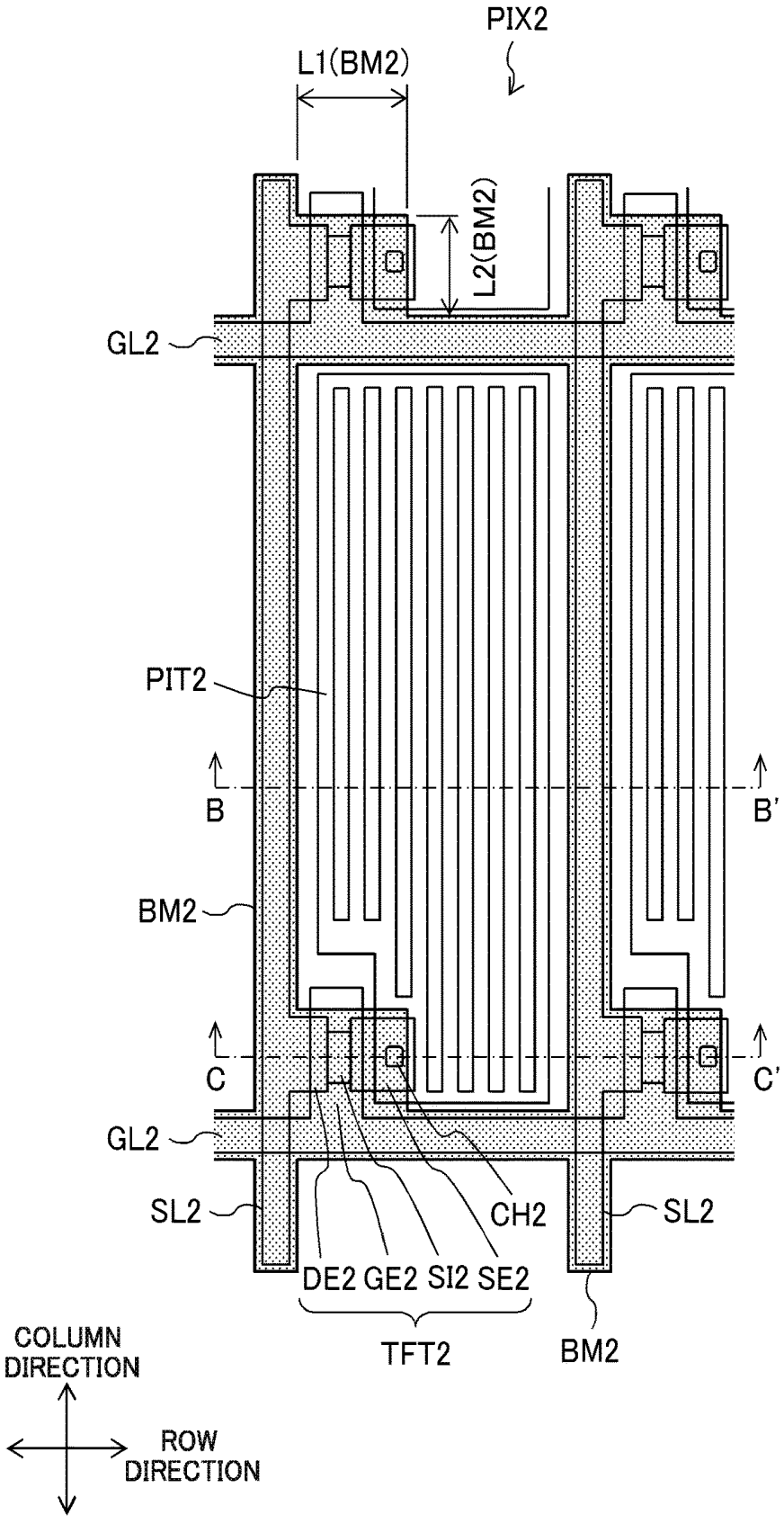

PIX2
L1(BM2)
L2(BM2)
GL2
PIT2
B
B'
BM2
C
C'
GL2
SL2
CH2
SL2
DE2 GE2 SI2 SE2
TFT2
BM2
COLUMN DIRECTION
ROW DIRECTION

FIG.13

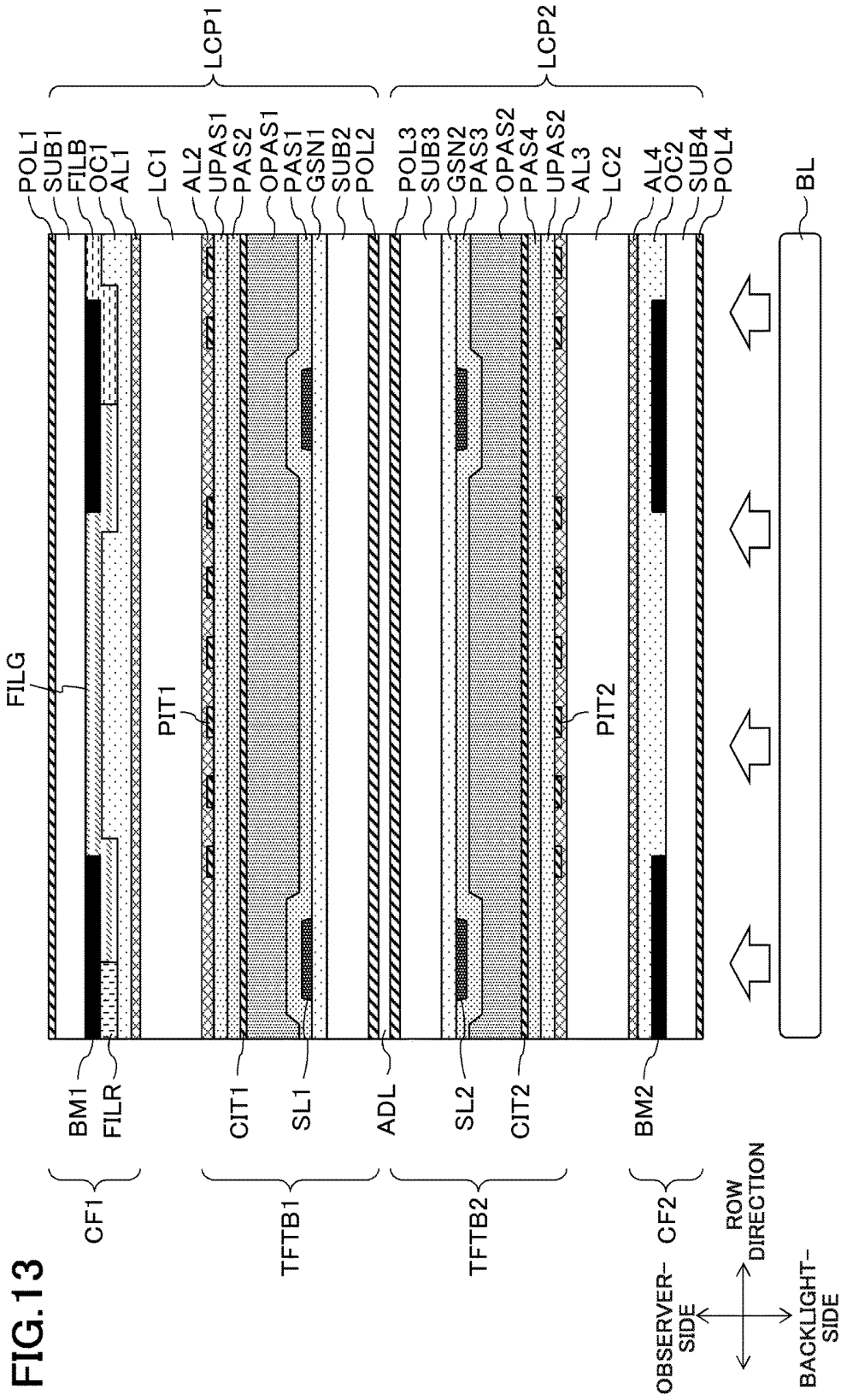

LCP1
LCP2
POL1
SUB1
FILB
OC1
AL1
LC1
AL2
UPAS1
PAS2
OPAS1
PAS1
GSN1
SUB2
POL2
POL3
SUB3
GSN2
PAS3
OPAS2
PAS4
UPAS2
AL3
LC2
AL4
OC2
SUB4
POL4
BL
FILG
PIT1
PIT2
BM1
FILR
CIT1
SL1
ADL
SL2
CIT2
BM2
CF1
TFTB1
TFTB2
CF2
OBSERVER-SIDE
ROW DIRECTION
BACKLIGHT-SIDE

FIG.14

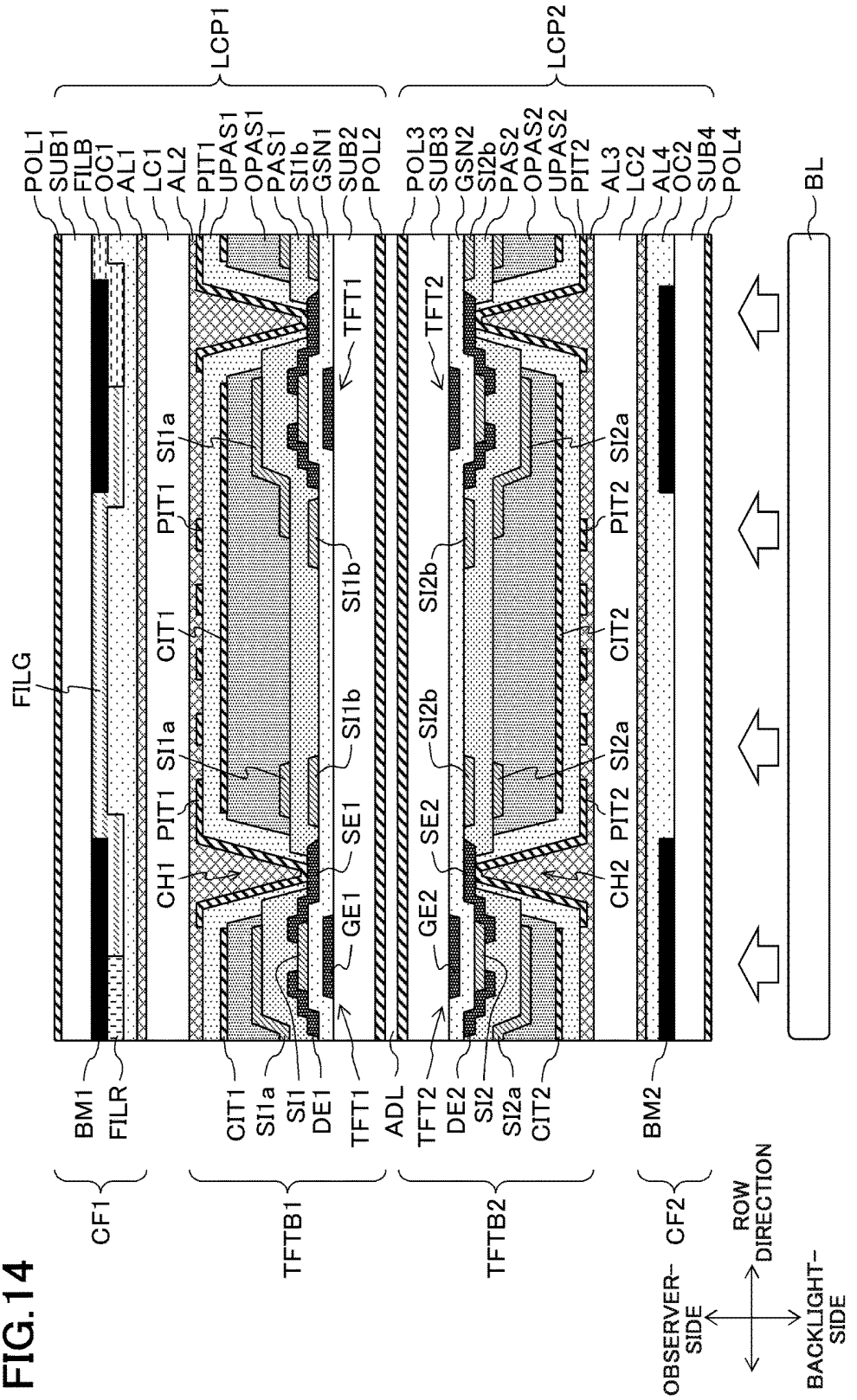

LCP1
LCP2
POL1
SUB1
FILB
OC1
AL1
LC1
AL2
PIT1
UPAS1
OPAS1
PAS1
SI1b
GSN1
SUB2
POL2
POL3
SUB3
GSN2
SI2b
PAS2
OPAS2
UPAS2
PIT2
AL3
LC2
AL4
OC2
SUB4
POL4
BL
FILG
TFT1
TFT2
SI1a
PIT1
CIT1
SI1b
SE1
CH1
GE1
SI2b
SE2
GE2
SI2a
PIT2
CIT2
CH2
BM1
FILR
CIT1
SI1a
SI1
DE1
TFT1
ADL
TFT2
DE2
SI2
SI2a
CIT2
BM2
CF1
TFTB1
TFTB2
CF2
ROW DIRECTION
OBSERVER-SIDE
BACKLIGHT-SIDE

FIG.15

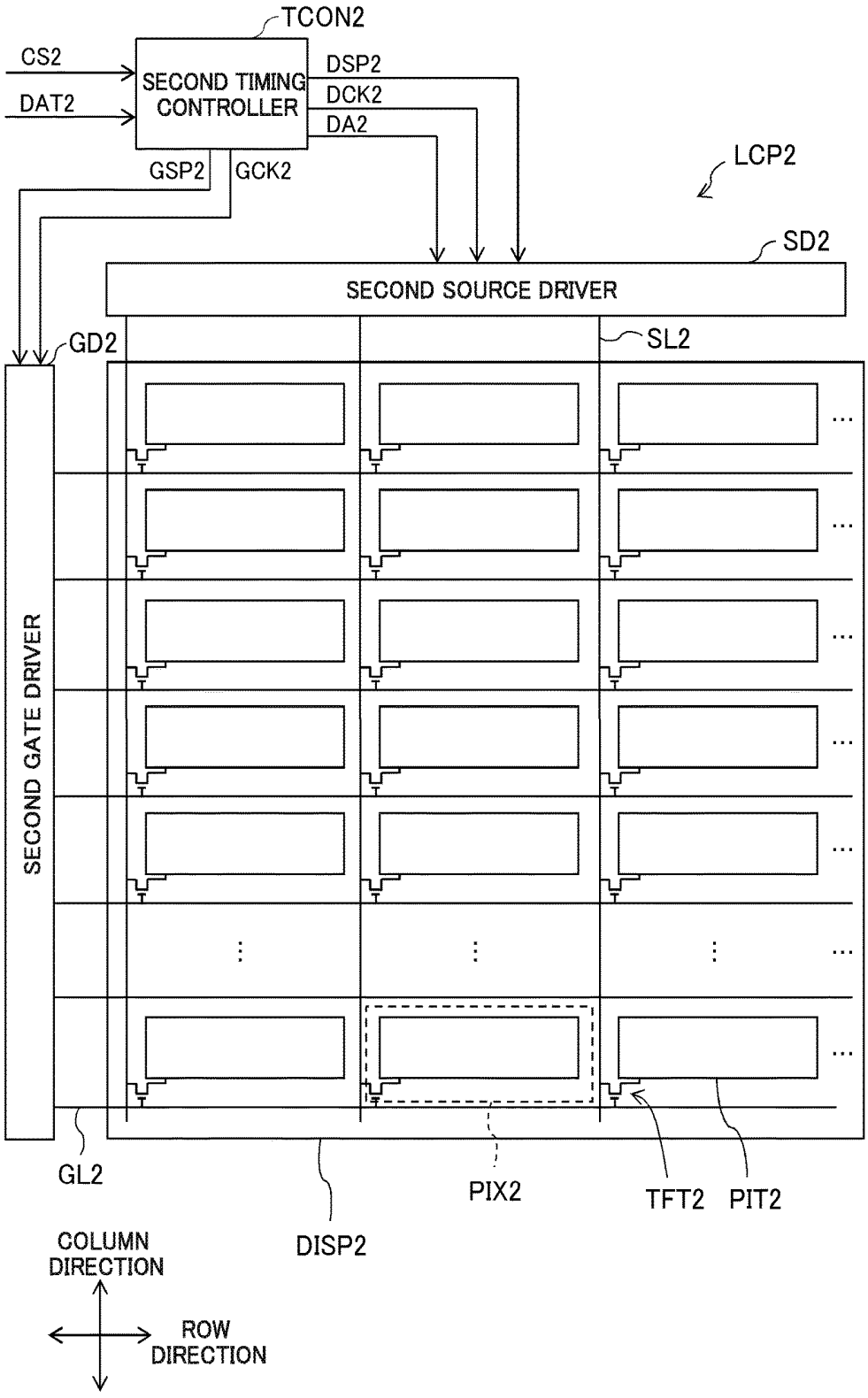

TCON2
CS2
DAT2
SECOND TIMING CONTROLLER
DSP2
DCK2
DA2
GSP2
GCK2
LCP2
SD2
SECOND SOURCE DRIVER
GD2
SL2
SECOND GATE DRIVER
GL2
DISP2
PIX2
TFT2
PIT2
COLUMN DIRECTION
ROW DIRECTION

FIG.16A

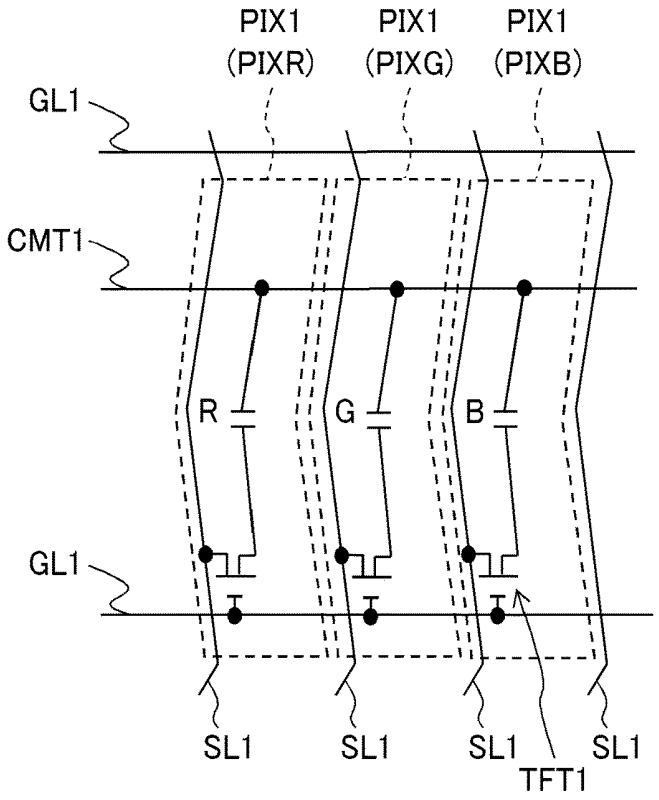


FIG.16B

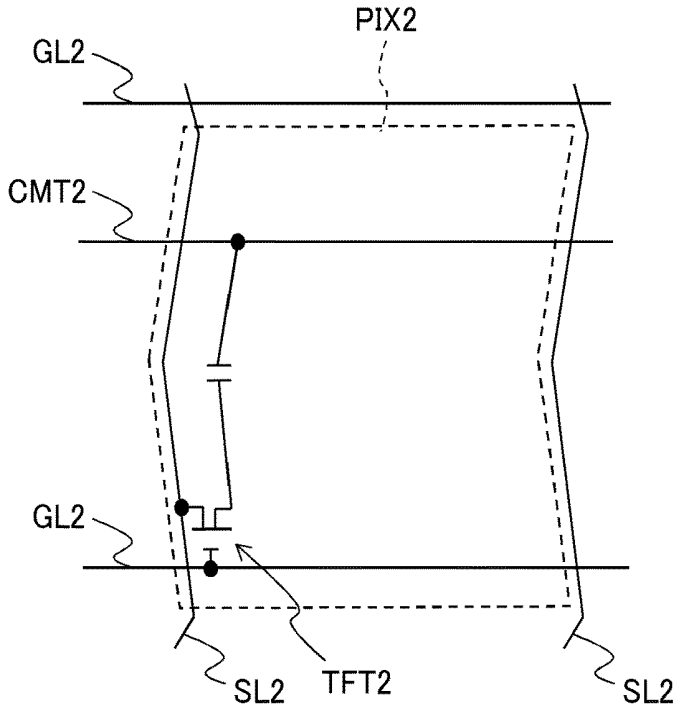
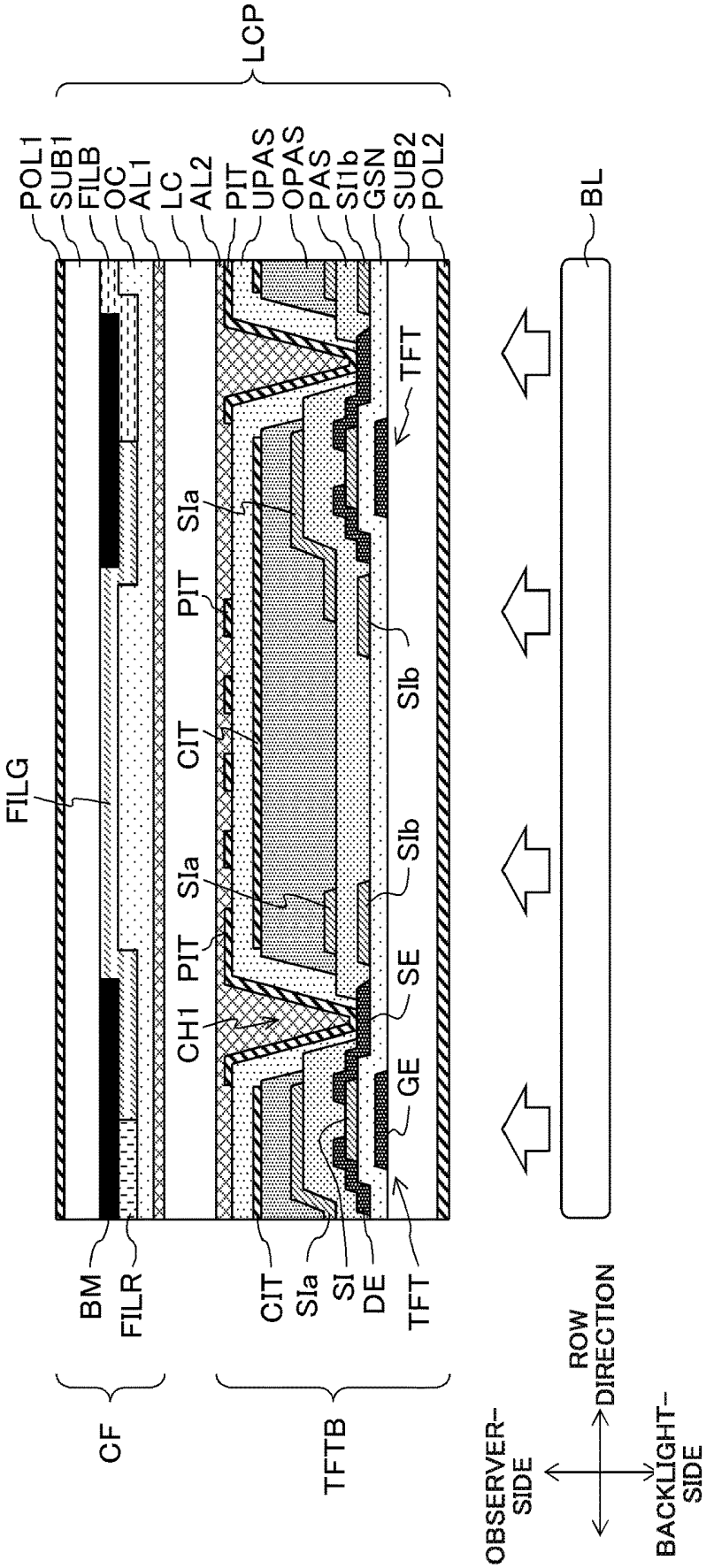


FIG.17


LCP
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SUB1
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OC
AL1
LC
AL2
PIT
UPAS
OPAS
PAS
SI1b
GSN
SUB2
POL2
BL
TFT
SIa
PIT
CIT
SIb
FILG
SIa
SIb
CH1
PIT
SE
GE
BM
FILR
CIT
SIa
SI
DE
TFT
CF
TFTB
ROW DIRECTION
OBSERVER-SIDE
BACKLIGHT-SIDE

FIG.18

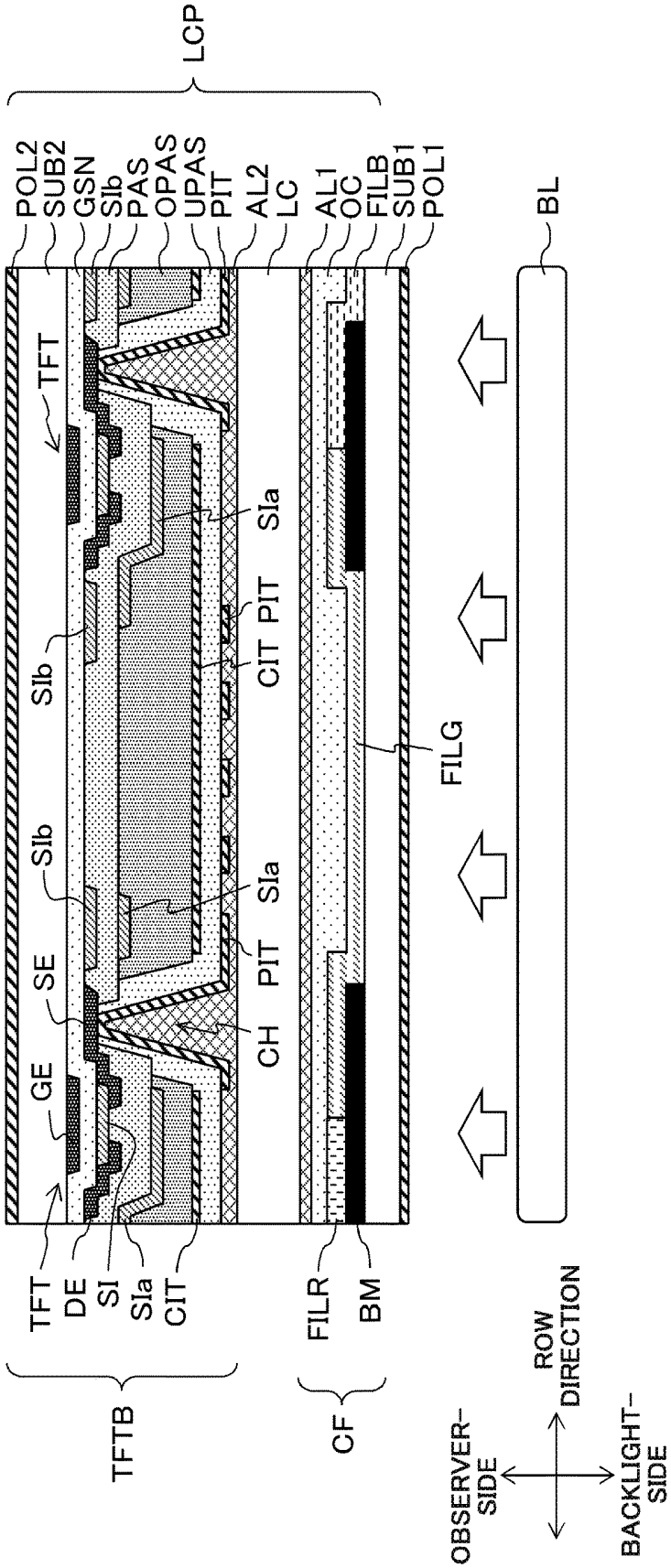

LCP
POL2
SUB2
GSN
SIb
PAS
OPAS
UPAS
PIT
AL2
LC
AL1
OC
FILB
SUB1
POL1
BL
TFT
SIa
SIb
CIT
PIT
FILG
SIb
SIa
SE
PIT
CH
GE
TFT
DE
SI
SIa
CIT
FILR
BM
TFTB
CF
ROW DIRECTION
OBSERVER-SIDE
BACKLIGHT-SIDE

FIG.19

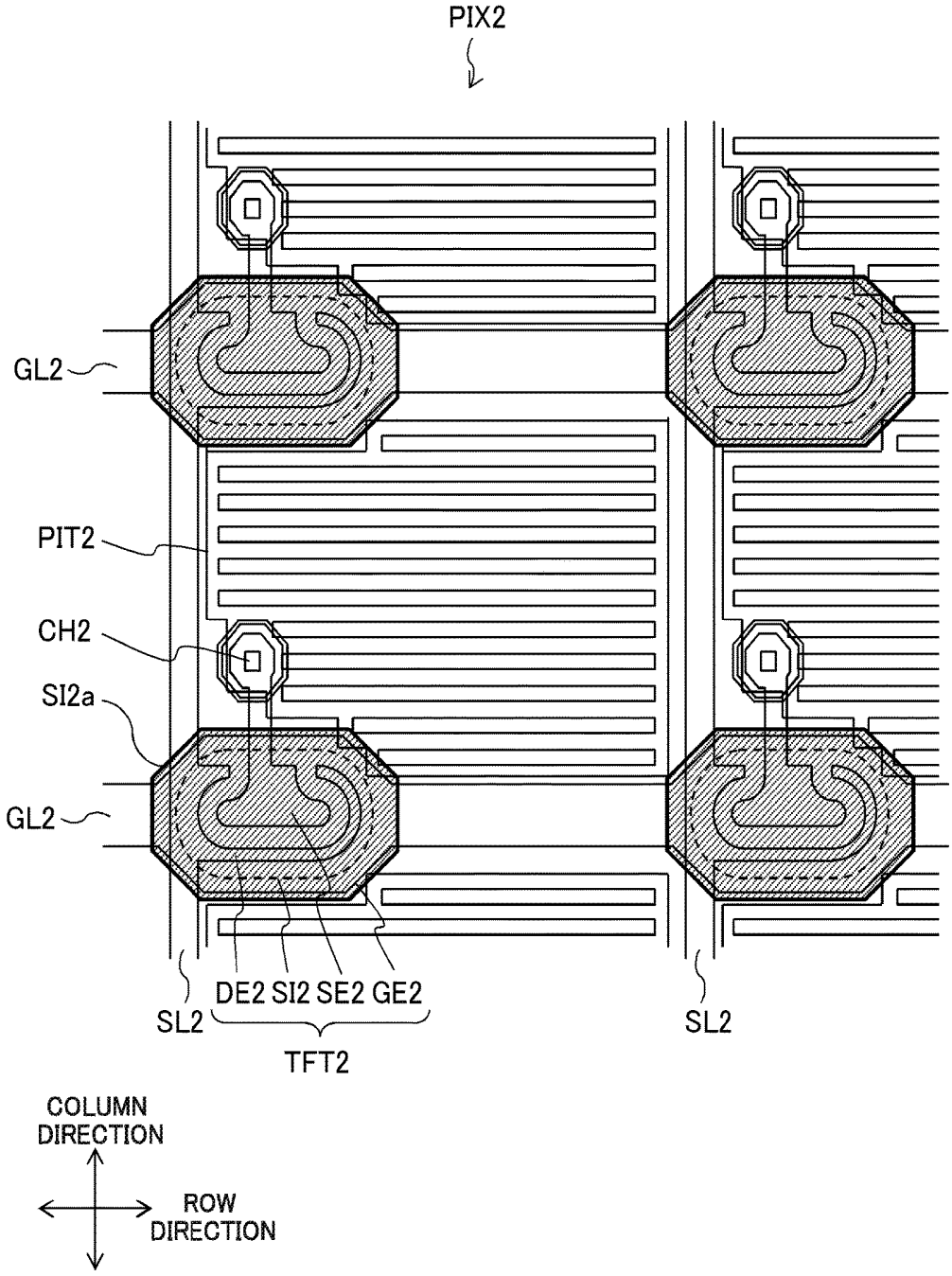

PIX2
GL2
PIT2
CH2
SI2a
GL2
SL2
DE2 SI2 SE2 GE2
TFT2
SL2
COLUMN DIRECTION
ROW DIRECTION

FIG.20

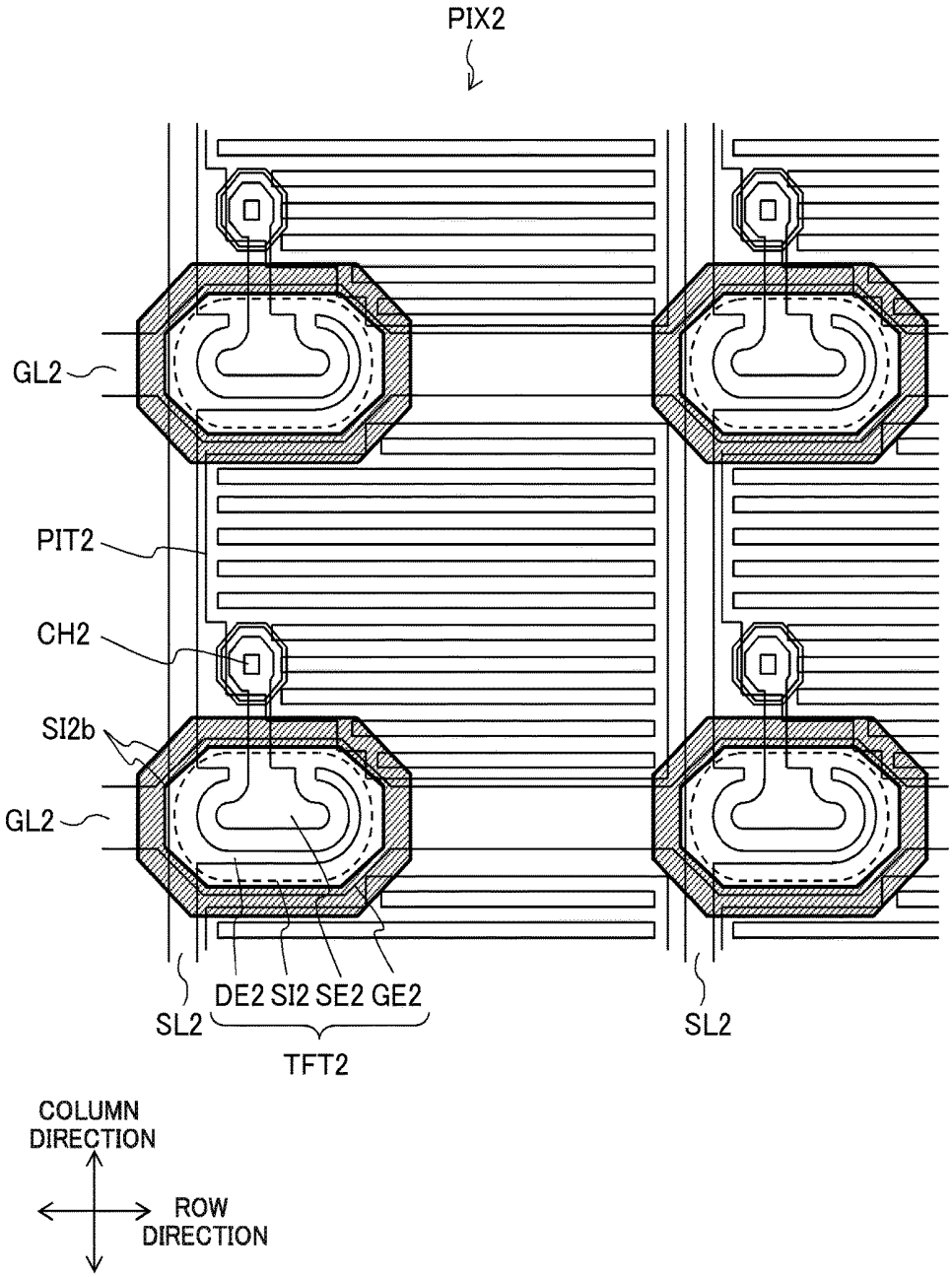

PIX2
GL2
PIT2
CH2
SI2b
GL2
SL2
DE2 SI2 SE2 GE2
TFT2
SL2
COLUMN DIRECTION
ROW DIRECTION

FIG.21

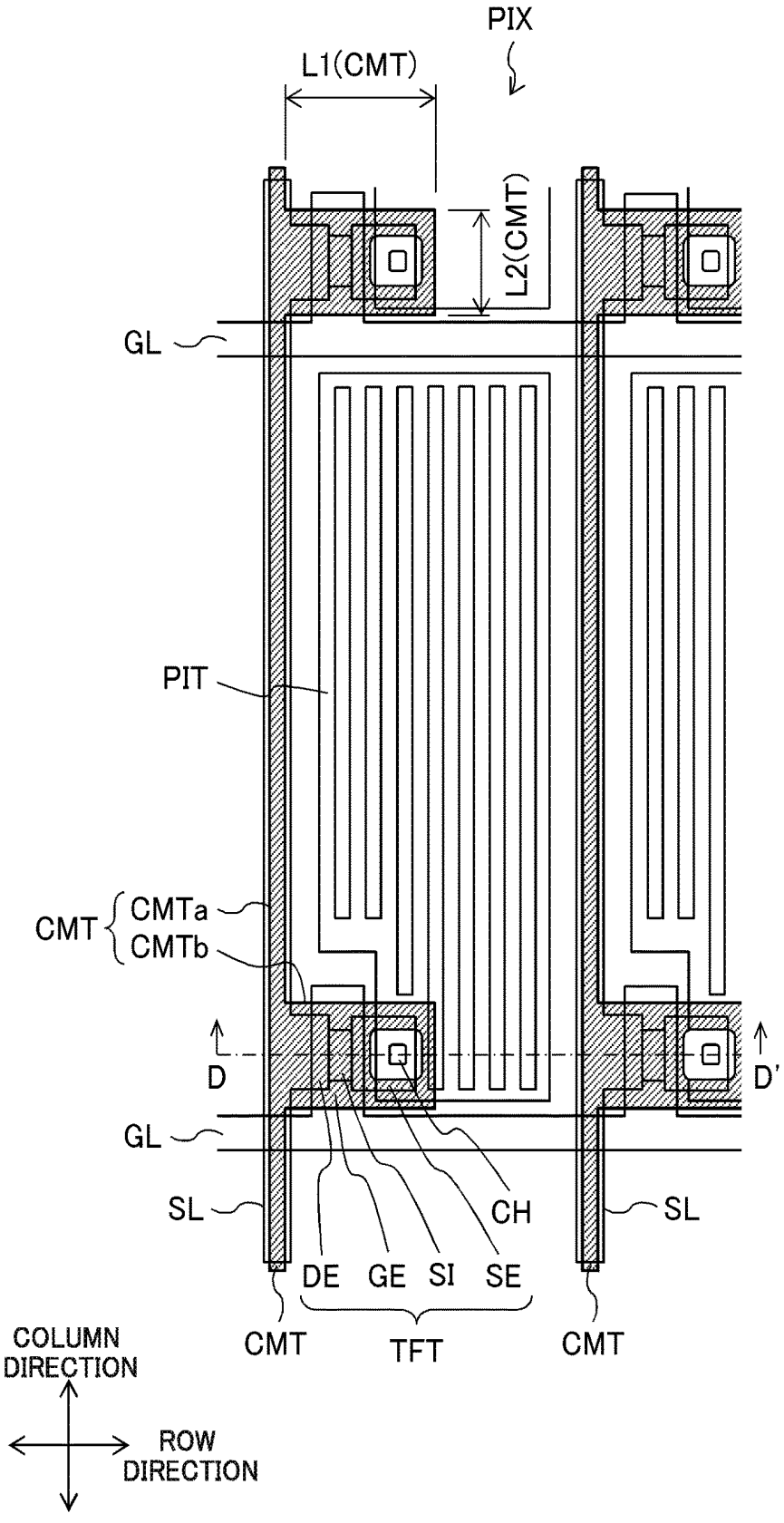
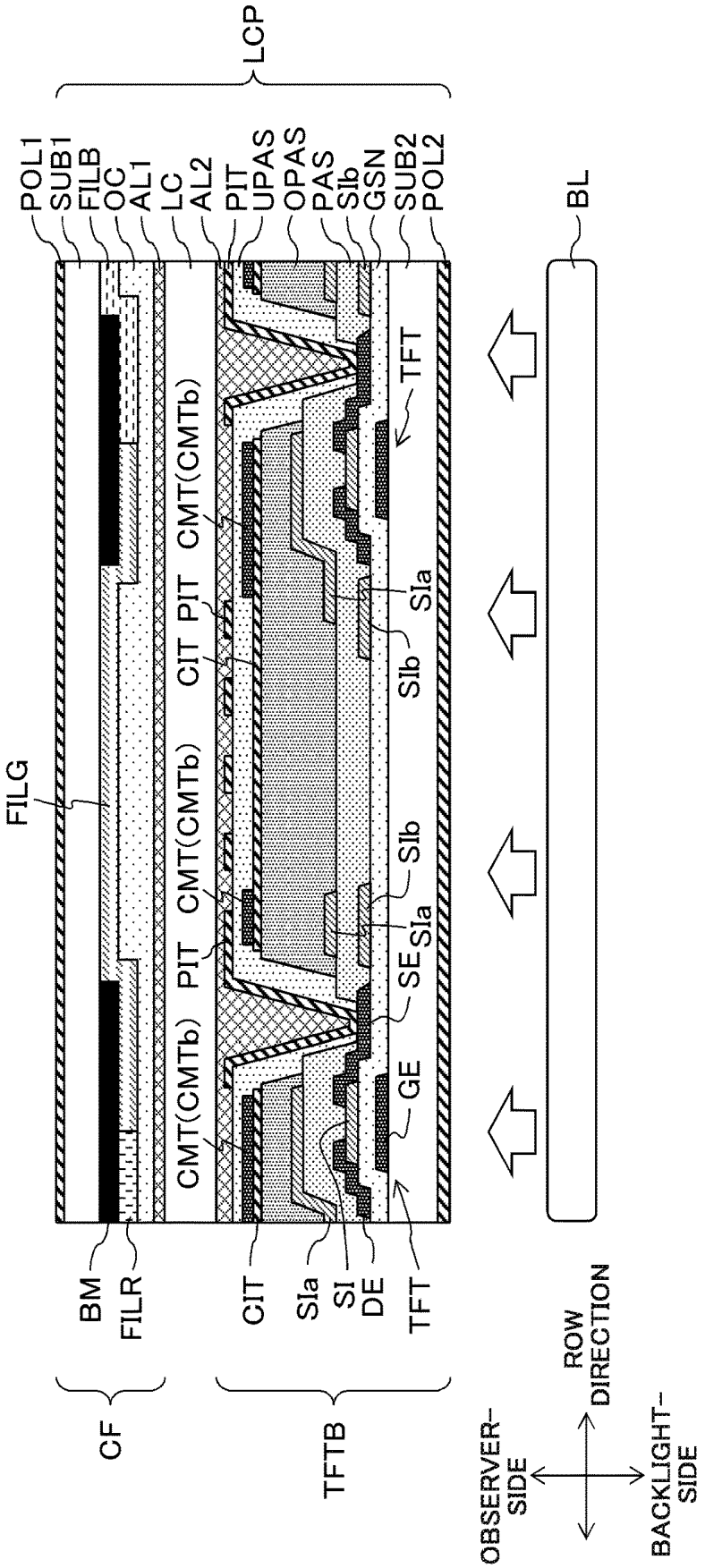

PIX
L1(CMT)
L2(CMT)
GL
PIT
CMT
CMTa
CMTb
D
D'
GL
SL
CH
SL
DE
GE
SI
SE
CMT
TFT
CMT
COLUMN DIRECTION
ROW DIRECTION

FIG.22


LCP
POL1
SUB1
FILB
OC
AL1
LC
AL2
PIT
UPAS
OPAS
PAS
SIb
GSN
SUB2
POL2
BL
TFT
CMT(CMTb)
CIT
PIT
SIa
SIb
SE
GE
FILG
BM
FILR
CIT
SIa
SI
DE
TFT
CF
TFTB
ROW DIRECTION
OBSERVER-SIDE
BACKLIGHT-SIDE

LIQUID CRYSTAL DISPLAY DEVICE WITH OVERLAPPING SEMICONDUCTOR LAYERS

CROSS-REFERENCE TO RELATED APPLICATION

The present application claims priority from Japanese application JP 2017-044784 filed on Mar. 9, 2017, the contents of which are hereby incorporated by reference into this application.

TECHNICAL FIELD

The present invention relates to a liquid crystal display device, and, more particularly to a liquid crystal display device with improved contrast.

BACKGROUND

In a liquid crystal display device, when light from a backlight, light from an outside (natural light), or light in which the light from the backlight and the natural light is scattered by a liquid crystal layer (scattered light) is incident on a channel region of a thin film transistor, a characteristic of the thin film transistor generally changes, which results in degradation of display quality. For example, a method for enlarging a region of a black matrix or a method for providing a light shielding layer on a backlight side of the thin film transistor is conceivable as a method for solving the problem. However, in these methods, an opening ratio of a pixel is degraded, or a configuration becomes complicated.

A technique, in which two display panels overlap each other and an image is displayed on each display panel based on an input video signal, is conventionally proposed to improve contrast of a liquid crystal display device (for example, see International Publication WO2007/040127). Specifically, for example, a color image is displayed on a front-side (observer-side) display panel in two display panels disposed back and forth, and a black-and-white image is displayed on a rear-side (backlight-side) display panel, thereby improving contrast. In a liquid crystal display device including two display panels, the display panel disposed on the backlight side is easily influenced by the back light or the scattered light, and the characteristic of the thin film transistor is easy to change.

Thus, in the conventional liquid crystal display device, the display quality is degraded due to the light incident on the channel region of the thin film transistor.

The present disclosure is made in view of the above situation, and an object of the present disclosure is to provide a liquid crystal display device that can prevent the degradation of the display quality due to the light incident on the channel region of the thin film transistor.

SUMMARY

In one general aspect, the instant application describes a liquid crystal display device includes a first substrate formed with a first gate line, a first source line, a first thin film transistor including a first channel region and a first semiconductor layer, and a second semiconductor layer electrically insulated from the first semiconductor layer, a second substrate disposed opposite to the first substrate, and a first liquid crystal layer disposed between the first substrate and the second substrate. The second semiconductor layer is disposed between the first thin film transistor and the first liquid crystal layer, and overlaps at least a part of the first channel region of the first thin film transistor in planar view.

The above general aspect may include one or more of the following features. The first semiconductor layer and the second semiconductor layer may be made of amorphous silicon.

Only an inorganic insulator film may be disposed between the first thin film transistor and the second semiconductor layer.

A thickness of the second semiconductor layer may be larger than a thickness of the first semiconductor layer.

The first semiconductor layer may be higher than the second semiconductor layer in density of at least one of boron and phosphorus.

The liquid crystal display device may further include a backlight. The first liquid crystal layer may be disposed between the backlight and the first substrate.

The second substrate may include a black matrix. At least a part of the second semiconductor layer may not overlap the black matrix in planar view.

The liquid crystal display device may further include a third substrate formed with a second gate line, a second source line, and a second thin film transistor, a fourth substrate disposed opposite to the third substrate, and a second liquid crystal layer disposed between the third substrate and the fourth substrate. The second substrate may be disposed between the first liquid crystal layer and the second liquid crystal layer.

The liquid crystal display device may further include a backlight. The first liquid crystal layer may be disposed between the backlight and the second substrate.

The liquid crystal display device may further include a third substrate formed with a second gate line, a second source line, and a second thin film transistor, a fourth substrate disposed opposite to the third substrate, and a second liquid crystal layer disposed between the third substrate and the fourth substrate. The first substrate may be disposed between the first liquid crystal layer and the second liquid crystal layer.

The liquid crystal display device may further include a backlight. The first liquid crystal layer may be disposed between the backlight and the first substrate.

A third semiconductor layer may be further formed on the third substrate. The third semiconductor layer may be disposed between the second thin film transistor and the second liquid crystal layer, and may overlap at least a part of a second channel region of the second thin film transistor in planar view.

In another general aspect, a display device of the instant application includes a first substrate formed with a first gate line, a first source line, a first thin film transistor including a first channel region and a first semiconductor layer, and a second semiconductor layer electrically insulated from the first semiconductor layer; a second substrate disposed opposite to the first substrate; and a first liquid crystal layer disposed between the first substrate and the second substrate. The second semiconductor layer is disposed in a layer identical to the first semiconductor layer, and disposed away from the first thin film transistor.

The above general aspect may include one or more of the following features. The second semiconductor layer may have a ring shape, and may be disposed so as to surround the first channel region in planar view.

The first semiconductor layer and the second semiconductor layer may include an amorphous silicon layer including an impurity layer containing at least one of boron and phosphorus.

The second substrate may include a black matrix. At least a part of the second semiconductor layer may overlap the black matrix in planar view.

In the liquid crystal display device of the present disclosure, the degradation of the display quality due to the light incident on the channel region of the thin film transistor can be prevented.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a perspective view illustrating a schematic configuration of liquid crystal display device of a first exemplary embodiment;

FIG. **2** is a view illustrating a schematic configuration of liquid crystal display device of the first exemplary embodiment;

FIG. **3** is a plan view illustrating a schematic configuration of display panel LCP**1** of the first exemplary embodiment;

FIG. **4** is a plan view illustrating a schematic configuration of display panel LCP**2** of the first exemplary embodiment;

FIG. **5** is a sectional view taken along line A-A in FIGS. **3** and **4**;

FIGS. **6**A and **6**B are plan views each illustrating a disposition relationship between pixel of display panel LCP**1** and pixel of display panel LCP**2**;

FIG. **7** is a plan view illustrating a configuration of pixel of display panel LCP**1**;

FIG. **8** is a plan view illustrating a configuration of pixel of display panel LCP**1**;

FIG. **9** is a plan view illustrating a configuration of pixel of display panel LCP**1**;

FIG. **10** is a plan view illustrating a configuration of pixel of display panel LCP**2**;

FIG. **11** is a plan view illustrating a configuration of pixel of display panel LCP**2**;

FIG. **12** is a plan view illustrating a configuration of pixel of display panel LCP**2**;

FIG. **13** is a sectional view taken along line B-B' in FIGS. **7** to **12**;

FIG. **14** is a sectional view taken along line C-C' in FIGS. **7** to **12**;

FIG. **15** is a plan view illustrating another schematic configuration of display panel LCP**2** of the first exemplary embodiment;

FIGS. **16**A and **16**B are plan views each illustrating a disposition relationship between pixel of display panel LCP**1** and pixel of display panel LCP**2** of the first exemplary embodiment;

FIG. **17** is a sectional view illustrating a configuration of pixel of display panel of s second exemplary embodiment;

FIG. **18** is a sectional view illustrating another configuration of pixel of display panel of the second exemplary embodiment;

FIG. **19** is a plan view illustrating another configuration of pixel of display panel of the first exemplary embodiment;

FIG. **20** is a plan view illustrating another configuration of pixel of display panel of the first exemplary embodiment;

FIG. **21** is a plan view illustrating another configuration of pixel of display panel LCP of the second exemplary embodiment; and

FIG. **22** is a sectional view taken along line D-D' in FIG. **21**.

DETAILED DESCRIPTION

Hereinafter, an exemplary embodiment of the present disclosure will be described with reference to the drawings.

A liquid crystal display device according to one exemplary embodiment includes a plurality of display panels that display images, a plurality of driving circuits (a plurality of source drivers and a plurality of gate drivers) that drive the display panels, a plurality of timing controllers that control the driving circuits, an image processor that performs image processing on an input video signal input from an outside and outputs image data to each of the timing controllers, and a backlight that irradiates the plurality of display panels with light from a rear surface side. A number of the plurality of display panels is not limited to two, and may be more When viewed from the observer side, the plurality of display panels are disposed while overlapping each other in a front-back direction. An image is displayed on each of the display panels. A liquid crystal display device LCD of a first exemplary embodiment including two display panels will be described below by way of example, and a liquid crystal display device LCD of a second exemplary embodiment including a one display panels will be described below by way of example.

First Exemplary Embodiment

FIG. **1** is a perspective view illustrating a schematic configuration of liquid crystal display device LCD of the exemplary embodiment. As illustrated in FIG. **1**, liquid crystal display device LCD includes display panel LCP**1** disposed at a position (front side) closer to an observer, display panel LCP**2** disposed at a position (rear side) farther away from the observer with respect to display panel LCP**1**, adhesive layer ADL in which display panel LCP**1** and display panel LCP**2** adhere to each other, backlight BL disposed on the rear surface side of display panel LCP**2**, and front chassis FS that covers display panel LCP**1** and display panel LCP**2** from the display surface side.

FIG. **2** is a view illustrating the schematic configuration of liquid crystal display device LCD of the exemplary embodiment. As illustrated in FIG. **2**, display panel LCP**1** includes first source driver SD**1** and first gate driver GD**1**, and display panel LCP**2** includes second source driver SD**2** and second gate driver GD**2**. Liquid crystal display device LCD also includes first timing controller TCON**1** that controls first source driver SD**1** and first gate driver GD**1**, second timing controller TCON**2** that controls second source driver SD**2** and second gate driver GD**2**, and image processor IPU that outputs image data to first timing controller TCON**1** and second timing controller TCON**2**. For example, display panel LCP**1** displays a color image in first image display region DISP**1** according to the input video signal, and display panel LCP**2** displays a black-and-white image in second image display region DISP**2** according to the input video signal. Image processor IPU receives input video signal Data transmitted from an external system (not illustrated), performs known image processing on input video signal Data, and then outputs first image data DAT**1** to first timing controller TCON**1** and outputs second image data DAT**2** to second timing controller TCON**2**. Image processor IPU also outputs a control signal (not illustrated in FIG. **2**) such as a synchronizing signal to first timing controller TCON**1** and second timing controller TCON**2**. For example, first image data DAT**1** is image data for displaying the color image, and second image data DAT**2** is image data for displaying the monochrome image.

FIG. **3** is a plan view illustrating a schematic configuration of display panel LCP**1** of the first exemplary embodiment, and FIG. **4** is a plan view illustrating a schematic

configuration of display panel LCP2 of the first exemplary embodiment. FIG. 5 is a sectional view taken along line A-A in FIGS. 3 and 4.

The schematic configuration of display panel LCP1 will be described with reference to FIGS. 3 and 5. As illustrated in FIG. 5, display panel LCP1 includes thin film transistor substrate TFTB1 disposed on the side of backlight BL, counter substrate CF1, which is disposed on the observer side while being opposite to thin film transistor substrate TFTB1, and liquid crystal layer LC1 disposed between thin film transistor substrate TFTB1 and counter substrate CF1. Polarizing plate POL2 is disposed on the side of backlight BL of display panel LCP1, and polarizing plate POL1 is disposed on the observer side.

In thin film transistor substrate TFTB1, as illustrated in FIG. 3, a plurality of source lines SL1 extending in a first direction (for example, a column direction), and a plurality of gate lines GL1 extending in a second direction (for example, a row direction) different from the first direction are formed, and thin film transistor TFT1 is formed close to an intersection between each of the plurality of source lines SL1 and each of the plurality of gate lines GL1. In plan view of display panel LCP1, a region surrounded by two source lines SL1 adjacent to each other and two gate lines GL1 adjacent to each other is defined as one pixel PIX1, and a plurality of pixels PIX1 are disposed in a matrix form (the row direction and the column direction). The plurality of source lines SL1 are disposed at equal intervals in the row direction, and the plurality of gate lines GL1 are disposed at equal intervals in the column direction. In thin film transistor substrate TFTB1, pixel electrode PIT1 is formed in each pixel PIX1, and one common electrode CIT1 (see FIG. 14) common to the plurality of pixels PIX1 is formed. Drain electrode DE1 (see FIG. 14) constituting thin film transistor TFT1 is electrically connected to source line SL1, source electrode SE1 (see FIG. 14) is electrically connected to pixel electrode PIT1 through contact hole CH1 (see FIG. 14), and gate electrode GE1 (see FIG. 14) is electrically connected to gate line GL1.

As illustrated in FIG. 5, a light transmission unit that transmits light and black matrix BM1 (a light shielding unit) that obstructs the light transmission are formed in counter substrate CF1. A plurality of color filters FIL (colored layer) are formed in the light transmission unit according to each pixel PIX1. The light transmission unit is surrounded by black matrix BM. For example, the light transmission unit is formed into a rectangular shape. The plurality of color filters FIL include red color filters FILR (red layer) made of a red (R color) material to transmit red light, green color filters FILG (green layer) made of a green (G color) material to transmit green light, and blue color filters FILB (blue layer) made of a blue (B color) material to transmit blue light. Red color filters FILR, green color filters FILG, and blue color filters FILB are repeatedly arrayed in the row direction in this order, identical-color filters FIL are arrayed in the column direction, and black matrix BM1 is formed at a boundary between color filters FIL adjacent to each other in the row direction and the column direction. According to each color filter FIL, as illustrated in FIG. 3, the plurality of pixels PIX1 include red pixels PIXR corresponding to red color filter FILR, green pixels PIXG corresponding to green color filter FILG, and blue pixels PIXB corresponding to blue color filter FILB. In display panel LCP1, red pixels PIXR, green pixels PIXG, and blue pixels PIXB are repeatedly arrayed in the row direction in this order, and pixels PIX1 having the identical color are arrayed in the column direction.

First timing controller TCON1 has a known configuration. For example, based on first image data DAT1 and first control signal CS1 (such as a clock signal, a vertical synchronizing signal, and a horizontal synchronizing signal), which are output from image processor IPU, first timing controller TCON1 generates various timing signals (data start pulse DSP1, data clock DCK1, gate start pulse GSP1, and gate clock GCK1) to control first image data DA1 and drive of first source driver SD1 and first gate driver GD1 (see FIG. 3). First timing controller TCON1 outputs first image data DA1, data start pulse DSP1, and data clock DCK1 to first source driver SD1, and outputs gate start pulse GSP1 and gate clock GCK1 to first gate driver GD1.

First source driver SD1 outputs a data signal (data voltage) corresponding to first image data DA1 to source line SL1 based on data start pulse DSP1 and data clock DCK1. First gate driver GD1 outputs a gate signal (gate voltage) to gate lines GL1 based on gate start pulse GSP1 and gate clock GCK1.

First source driver SD1 supplies the data voltage to each source line SL1, and first gate driver GD1 supplies the gate voltage to each gate line GL1. Common voltage Vcom is supplied from a common driver (not illustrated) to common electrode CIT1 through a common wiring CMT1 (see FIG. 6). When the gate voltage (gate-on voltage) is supplied to gate line GL1, thin film transistor TFT1 connected to gate line GL1 is turned on, and the data voltage is supplied to pixel electrode PIT1 through source line SL1 connected to thin film transistor TFT1. An electric field is generated by a difference between the data voltage supplied to pixel electrode PIT1 and common voltage Vcom supplied to common electrode CIT1. The liquid crystal is driven by the electric field, and transmittance of the light emitted from backlight BL is controlled, thereby displaying an image. In display panel LCP1, a color image is displayed by the supply of a desired data voltage to source line SL1 connected to pixel electrode PIT1 of each of pixel PIX1.

The configuration of display panel LCP2 will be described below with reference to FIGS. 4 and 5. As illustrated in FIG. 5, display panel LCP2 includes thin film transistor substrate TFTB2 disposed on the side of backlight BL, counter substrate CF2, which is disposed on the observer side while being opposite to thin film transistor substrate TFTB2, and liquid crystal layer LC2 disposed between thin film transistor substrate TFTB2 and counter substrate CF2. Polarizing plate POL4 is disposed on the side of backlight BL of display panel LCP2, and polarizing plate POL3 is disposed on the observer side. Adhesive layer ADL is disposed between polarizing plate POL2 of display panel LCP1 and polarizing plate POL3 of display panel LCP2.

In thin film transistor substrate TFTB2, as illustrated in FIG. 4, a plurality of source lines SL2 extending in the column direction, and a plurality of gate lines GL2 extending in the row direction are formed, and thin film transistor TFT2 is formed close to the intersection between each of the plurality of source lines SL2 and each of the plurality of gate lines GL2. In plan view of display panel LCP2, a region surrounded by two source lines SL2 adjacent to each other and two gate lines GL2 adjacent to each other is defined as one pixel PIX2, and a plurality of pixels PIX2 are disposed in a matrix form (the row direction and the column direction). The plurality of source lines SL2 are disposed at equal intervals in the row direction, and the plurality of gate lines GL2 are disposed at equal intervals in the column direction. In thin film transistor substrate TFTB2, pixel electrode PIT2 is formed in each pixel PIX2, and one common electrode CIT2 (see FIG. 14) common to the plurality of pixels PIX2

is formed. Drain electrode DE2 constituting thin film transistor TFT2 is electrically connected to source line SL2, source electrode SE2 (see FIG. 14) is electrically connected to pixel electrode PIT2 through contact hole CH2 (see FIG. 14), and gate electrode GE2 (see FIG. 14) is electrically connected to gate line GL2.

In counter substrate CF2 (See FIG. 5), the light transmission unit that transmits light is formed. The color filter (colored portion) is not formed in the light transmission unit, but overcoat film OC2 is formed in the light transmission unit.

Second timing controller TCON2 has a known configuration. For example, based on second image data DAT2 and second control signal CS2 (such as a clock signal, a vertical synchronizing signal, and a horizontal synchronizing signal), which are output from image processor IPU, second timing controller TCON2 generates various timing signals (data start pulse DSP2, data clock DCK2, gate start pulse GSP2, and gate clock GCK2) to control second image data DA2 and drive of second source driver SD2 and second gate driver GD2 (see FIG. 4). Second timing controller TCON2 outputs second image data DA2, data start pulse DSP2, and data clock DCK2 to second source driver SD2, and outputs gate start pulse GSP2 and gate clock GCK2 to second gate driver GD2.

Second source driver SD2 outputs the data voltage corresponding to second image data DA2 to source line SL2 based on data start pulse DSP2 and data clock DCK2. Second gate driver GD2 outputs the gate voltage to gate lines GL2 based on gate start pulse GSP2 and gate clock GCK2.

Second source driver SD2 supplies the data voltage to each source line SL2, and second gate driver GD2 supplies the gate voltage to each gate line GL2. The common driver supplies common voltage Vcom to common electrode CIT2 through a common wiring CMT1 (see FIG. 6). When the gate voltage (gate-on voltage) is supplied to gate line GL2, thin film transistor TFT2 connected to gate line GL2 is turned on, and the data voltage is supplied to pixel electrode PIT2 through source line SL2 connected to thin film transistor TFT2. An electric field is generated by a difference between the data voltage supplied to pixel electrode PIT2 and common voltage Vcom supplied to common electrode CIT2. The liquid crystal is driven by the electric field, and transmittance of the light emitted from backlight BL is controlled, thereby displaying an image. In display panel LCP2, a color image is displayed by the supply of a desired data voltage to source line SL1 connected to pixel electrode PIT1 of each of red pixel PIXR, green pixel PIXG, and blue pixel PIXB.

FIGS. 6A and 6B are plan views each illustrating a disposition relationship between pixel PIX1 of display panel LCP1 and pixel PIX2 of display panel LCP2. Liquid crystal display device LCD is configured such that a number of pixels PIX1 (a number of pixel electrodes PIX1) per unit area of display panel LCP1 is equal to a number of pixels PIX2 (a number of pixel electrodes PIX2) per unit area of display panel LCP2. An area of one pixel PIX1 is equal to an area of one pixel PIX2.

Each of FIGS. 7 to 9 is a plan view illustrating a configuration of pixel PIX1 of display panel LCP1. FIGS. 7 and 8 illustrate a state in which counter substrate CF1 is seen through, and FIG. 9 illustrates thin film transistor substrate TFTB1 while black matrix BM1 of counter substrate CF1 overlaps thin film transistor substrate TFTB1.

As illustrated in FIG. 7, in thin film transistor TFT1, drain electrode DE1 is electrically connected to source line SL1, a part of drain electrode DE1 overlaps semiconductor layer SI1 (first semiconductor layer), source electrode SE1 is electrically connected to pixel electrode PIT1 through contact hole CH1, and a part of source electrode SE1 overlaps semiconductor layer SI1. Gate electrode GE1 is electrically connected to gate line GL1, and a part of gate electrode GE1 overlaps semiconductor layer SI1. Light absorption layers SI1*a* (second semiconductor layer), SI1*b* are disposed close to thin film transistor TFT1. For convenience, FIG. 7 illustrates light absorption layer SI1*a* while light absorption layer SI1*b* is omitted, and FIG. 8 illustrates light absorption layer SI1*b* while light absorption layer SI1*a* is omitted. Light absorption layer SI1*a* (a region (hatched portion) surrounded by a solid line in FIG. 7) overlaps at least a part of a channel region of thin film transistor TFT1 in planar view. Light absorption layer SI1*a* may overlap the whole channel region of thin film transistor TFT1 or a whole region where thin film transistor TFT1 is formed in planar view. Light absorption layer SI1*b* (a region (hatched portion) surrounded by a solid line in FIG. 8) is formed into a ring shape, and disposed so as to surround the channel region of thin film transistor TFT1 in planar view. Light absorption layer SI1*b* may overlap a part of gate electrode GE1 of thin film transistor TFT1 in planar view. Light absorption layers SI1*a*, SI1*b* are made of the same material as semiconductor layer SI1, for example, amorphous silicon (a-Si). Because amorphous silicon generally has a property of high light absorptivity in a long wavelength region, light absorption layers SI1*a*, SI1*b* absorb back light, natural light, scattered light, and the like. At least one of light absorption layers SI1*a*, SI1*b* may be made of the same material (for example, a black resin composition) as black matrix BM1. Each of light absorption layers SI1*a*, SI1*b* is electrically separated (insulated) from another component, and disposed in a floating state.

As illustrated in FIG. 9, in black matrix BM1 (a half tone portion in FIG. 9), a portion extending in the column direction overlaps source line SL1 in planar view, and a portion extending in the row direction overlaps gate line GL1 in planar view. Apart of black matrix BM1 overlaps a part of the channel region of thin film transistor TFT1 in planar view. Lengths L1 (SI1*a*), L2 (SI1*a*) (see FIG. 7) of light absorption layer SI1*a* overlapping the channel region of thin film transistor TFT1 are larger than lengths L1 (BM1), L2 (BM1) (see FIG. 9) of black matrix BM1 overlapping the channel region of thin film transistor TFT1, respectively. At least a part of light absorption layer SI1*a* needs not to overlap black matrix BM1 in planar view.

Each of FIGS. 10 to 12 is a plan view illustrating a configuration of pixel PIX2 of display panel LCP2. FIGS. 10 and 11 illustrate a state in which counter substrate CF2 is seen through, and FIG. 12 illustrates thin film transistor substrate TFTB2 while black matrix BM2 of counter substrate CF2 overlaps thin film transistor substrate TFTB2.

As illustrated in FIG. 10, in thin film transistor TFT2, drain electrode DE2 is electrically connected to source line SL2, a part of drain electrode DE2 overlaps semiconductor layer SI2, source electrode SE2 is electrically connected to pixel electrode PIT2 through contact hole CH2, and a part of source electrode SE2 overlaps semiconductor layer SI2. Gate electrode GE2 is electrically connected to gate line GL2, and a part of gate electrode GE2 overlaps semiconductor layer SI2. Light absorption layers SI2*a* (third semiconductor layer), SI2*b* are disposed close to thin film transistor TFT2. For convenience, FIG. 10 illustrates light absorption layer SI2*a* while light absorption layer SI2*b* is omitted, and FIG. 11 illustrates light absorption layer SI2*b* while light absorption layer SI2*a* is omitted. Light absorp-

tion layer SI2*a* (a region (hatched portion) surrounded by a solid line in FIG. **10**) overlaps at least a part of a channel region of thin film transistor TFT**2** in planar view. Light absorption layer SI2*a* may overlap the whole channel region of thin film transistor TFT**2** or a whole region where thin film transistor TFT**2** is formed in planar view. Light absorption layer SI2*b* (a region (hatched portion) surrounded by a solid line in FIG. **11**) is formed into a ring shape, and disposed so as to surround the channel region of thin film transistor TFT**2** in planar view. Light absorption layer SI2*b* may overlap a part of gate electrode GE**2** of thin film transistor TFT**2** in planar view. Light absorption layers SI2*a*, SI2*b* are made of the same material as semiconductor layer SI**2**, for example, amorphous silicon (a-Si), and light absorption layers SI2*a*, SI2*b* absorb back light, natural light, scattered light, and the like similarly to light absorption layers SI1*a*, SI1*b*. At least one of light absorption layers SI2*a*, SI2*b* may be made of the same material (for example, a black resin composition) as black matrix BM**2**. Each of light absorption layers SI2*a*, SI2*b* is electrically separated (insulated) from another component, and disposed in a floating state.

As illustrated in FIG. **12**, in black matrix BM**2** (a half tone portion in FIG. **12**), a portion extending in the column direction overlaps source line SL**2** in planar view, and a portion extending in the row direction overlaps gate line GL**2** in planar view. Apart of black matrix BM**2** overlaps a part of the channel region of thin film transistor TFT**2** in planar view. Lengths L**1** (SI2*a*), L**2** (SI2*a*) (see FIG. **10**) of light absorption layer SI2*a* overlapping the channel region of thin film transistor TFT**2** are larger than lengths L**1** (BM**2**), L**2** (BM**2**) (see FIG. **12**) of black matrix BM**2** overlapping the channel region of thin film transistor TFT**2**, respectively. At least a part of light absorption layer SI2*a* needs not to overlap black matrix BM**2** in planar view.

FIG. **13** is a sectional view taken along line B-B' in FIGS. **7** to **12**, and FIG. **14** is a sectional view taken along line C-C' in FIGS. **7** to **12**. Sectional structures of pixels PIX**1**, PIX**2** will be described below with reference to FIGS. **13** and **14**. In display panel LCP**1**, thin film transistor substrate TFTB**1** is disposed on the side of backlight BL, and counter substrate CF**1** is disposed on the observer side. In display panel LCP**2**, thin film transistor substrate TFTB**2** is disposed on the observer side, and counter substrate CF**2** is disposed on the side of backlight BL. That is, thin film transistor substrate TFTB**1** and thin film transistor substrate TFTB**2** are disposed opposite to each other.

In thin film transistor substrate TFTB**1** constituting pixel PIX**1** of display panel LCP**1**, gate line GL**1** and gate electrode GE**1** are formed on transparent substrate SUB**2** (glass substrate), and gate insulator film GSN**1** is formed so as to cover gate line GL**1** and gate electrode GE**1**. Source line SL**1**, drain electrode DE**1**, source electrode SE**1**, semiconductor layer SI**1**, and light absorption layer SI1*b* are formed on gate insulator film GSN**1**, and inorganic insulator film PAS**1** is formed so as to cover source line SL**1**, drain electrode DE**1**, source electrode SE**1**, semiconductor layer SI**1**, and light absorption layer SI1*b*. Semiconductor layer SI**1** and light absorption layer SI1*b* are made of the same material, and formed through the same process. In the same layer as semiconductor layer SI**1**, light absorption layer SI1*b* is disposed away from thin film transistor TFT**1**. Specifically, light absorption layer SI1*b* is electrically separated (isolated) from semiconductor layer SI**1**, gate electrode GE**1**, drain electrode DE**1**, and source electrode SE**1** around thin film transistor TFT**1**, and formed in the floating state. Light absorption layer SI1*a* is formed on inorganic insulator film PAS**1**. Light absorption layer SI1*a* is made of the same material as semiconductor layer SI**1**. A thickness of light absorption layer SI1*a* may be equal to or larger than thicknesses of semiconductor layer SI**1** and light absorption layer SI1*b*. Light absorption layer SI1*a* overlaps the region where thin film transistor TFT**1** is formed in planar view. A pixel-center-side end (contour end) of light absorption layer SI1*b* is located closer to a pixel center than a pixel-center-side end (contour end) of light absorption layer SI1*a*. Organic insulator film OPAS**1** is formed so as to cover light absorption layer SI1*a*.

Common electrode CIT**1** is formed on organic insulator film OPAS**1**, and common wiring CMT**1** (not illustrated) is formed on common electrode CIT**1**. Upper insulator film UPAS**1** is form so as to cover common electrode CIT**1** and common wiring CMT**1**, pixel electrode PIT**1** is formed on upper insulator film UPAS**1**, and alignment film AL**2** is formed so as to cover pixel electrode PIT**1**. Inorganic insulator film PAS**1**, light absorption layer SI1*a*, organic insulator film OPAS**1**, common electrode CIT**1**, and upper insulator film UPAS**1** are partially bored to make contact hole CH**1**. A part of pixel electrode PIT**1** is electrically connected to source electrode SE**1** through contact hole CH**1**.

In counter substrate CF**1**, black matrix BM**1** and color filter FIL (red color filter FILR, green color filter FILG, and blue color filter FILB) are formed on transparent substrate SUB**1** (glass substrate). Overcoat film OC**1** is coated on a surface of color filter FIL, and alignment film AL**1** is formed on overcoat film OC**1**.

In thin film transistor substrate TFTB**2** constituting pixel PIX**2** of display panel LCP**2**, gate line GL**2** and gate electrode GE**2** are formed on transparent substrate SUB**3** (glass substrate), and gate insulator film GSN**2** is formed so as to cover gate line GL**2** and gate electrode GE**2**. Source line SL**2**, drain electrode DE**2**, source electrode SE**2**, semiconductor layer SI**2**, and light absorption layer SI2*b* are formed on gate insulator film GSN**2**, and inorganic insulator film PAS**2** is formed so as to cover source line SL**2**, drain electrode DE**2**, source electrode SE**2**, semiconductor layer SI**2**, and light absorption layer SI2*b*. Semiconductor layer SI**2** and light absorption layer SI2*b* are made of the same material, and formed through the same process. In the same layer as semiconductor layer SI**2**, light absorption layer SI2*b* is disposed away from thin film transistor TFT**2**. Specifically, light absorption layer SI2*b* is electrically separated (isolated) from semiconductor layer SI**2**, gate electrode GE**2**, drain electrode DE**2**, and source electrode SE**2** around thin film transistor TFT**2**, and formed in the floating state. Light absorption layer SI2*a* is formed on inorganic insulator film PAS**2**. Light absorption layer SI2*a* is made of the same material as semiconductor layer SI**2**. A thickness of light absorption layer SI2*a* may be equal to or larger than thicknesses of semiconductor layer SI**2** and light absorption layer SI2*b*. Light absorption layer SI2*a* overlaps the region where thin film transistor TFT**2** is formed in planar view. A pixel-center-side end (contour end) of light absorption layer SI2*b* is located closer to a pixel center than a pixel-center-side end (contour end) of light absorption layer SI2*a*. Organic insulator film OPAS**2** is formed so as to cover light absorption layer SI2*a*.

Common electrode CIT**2** is formed on organic insulator film OPAS**2**, and common wiring CMT**2** (not illustrated) is formed on common electrode CIT**2**. Upper insulator film UPAS**2** is form so as to cover common electrode CIT**2** and common wiring CMT**2**, pixel electrode PIT**2** is formed on upper insulator film UPAS**2**, and alignment film AL**3** is

formed so as to cover pixel electrode PIT2. Inorganic insulator film PAS2, light absorption layer SI2*a*, organic insulator film OPAS2, common electrode CIT2, and upper insulator UPAS2 are partially bored to make contact hole CH2. A part of pixel electrode PIT2 is electrically connected to source electrode SE2 through contact hole CH2.

In counter substrate CF2, lattice-shape black matrix BM2 is formed on transparent substrate SUB4 (glass substrate), an opening (light transmission unit) of black matrix BM2 and black matrix BM2 are coated with overcoat film OC2, and alignment film AL4 is formed on overcoat film OC2.

In liquid crystal display device LCD of the first exemplary embodiment, light absorption layers SI1*a*, SI1*b* are disposed close to thin film transistor TFT1 in display panel LCP1, and light absorption layers SI2*a*, SI2*b* are disposed close to thin film transistor TFT2 in display panel LCP2, so that an amount of light incident on the channel regions of thin film transistors TFT1, TFT2 can be decreased. For example, in display panel LCP1, the amount of natural light incident on the channel region of thin film transistor TFT1 can be decreased because light absorption layer SI1*a* is disposed so as to overlap thin film transistor TFT1 in planar view, and the amount of scattered light incident on the channel region of thin film transistor TFT1 can be decreased because light absorption layer SI1*b* is formed in the same layer as semiconductor layer SI1. In display panel LCP2, the amount of back light incident on the channel region of thin film transistor TFT2 can be decreased because light absorption layer SI2*a* is disposed between thin film transistor TFT2 and backlight BL while disposed so as to overlap thin film transistor TFT2 in planar view, and the amount of scattered light (such as light reflected from display panel LCP1) incident on the channel region of thin film transistor TFT1 can be decreased because light absorption layer SI2*b* is formed in the same layer as semiconductor layer SI2. In the region overlapping the channel region, areas of light absorption layers SI1*a*, SI2*a* are larger than areas of black matrices BM1, BM2, respectively, and light absorption layers SI1*a*, SI2*a* are disposed close to the channel regions. Therefore light absorption layers SI1*a*, SI2*a* can shield light that is not completely shielded by black matrices BM1, BM2. Because light absorption layers SI1*b*, SI2*b* have the function of shielding the light of the black matrix, widths of black matrices BM1, BM2 can be decreased, and an influence due to a misalignment between thin film transistor substrate TFTB and counter substrate CF can be decreased. Light absorption layers SI1*b*, SI2*b* are made of the same materials as semiconductor layers SI1, SI2, formed in the same layers, and formed through the same processes as semiconductor layers SI1, SI2, so that a manufacturing process does not become complicated.

Thus, light absorption layers SI1*a*, SI1*b*, SI2*a*, SI2*b* act as a light shielding unit that shields light incident on the channel region of the thin film transistor. Consequently, a characteristic change of the thin film transistor due to the light incidence is prevented, so that the degradation of the display quality can be prevented.

Liquid crystal display device LCD of the first exemplary embodiment is not limited to the above configuration. For example, as illustrated in FIGS. **3**, **15**, and **16**, liquid crystal display device LCD of the first exemplary embodiment may be configured such that a number of pixels PIX2 (a number of pixel electrodes PIT2) per unit area of display panel LCP2 is smaller than a number of pixels PIX1 (a number of pixel electrodes PIT1) per unit area of display panel LCP1. Specifically, in the configuration of FIG. **16**, pixels PIX1 of display panel LCP1 and pixels PIX2 of display panel LCP2 are disposed such that a ratio of the number of pixels PIX1 to the number of pixels PIX2 is 3:1. Three pixels PIX1 (red pixel PIXR, green pixel PIXG, blue pixel PIXB) of display panel LCP1 and one pixel PIX2 of display panel LCP2 are displayed so as to overlap each other in planar view.

In liquid crystal display device LCD, display panel LCP1 may be disposed on the side of backlight BL, and display panel LCP2 may be disposed on the observer side.

Light absorption layers SI1*a*, SI1*b* may be eliminated in the display panel (display panel LCP1 in FIG. **14** and the like) disposed on the observer side. One of light absorption layers SI2*a*, SI2*b* may be eliminated in the display panel (display panel LCP2 in FIG. **14** and the like) disposed on the backlight side. Thus, in liquid crystal display device LCD of the first exemplary embodiment, it is only necessary to provide light absorption layer SI2*a* or light absorption layer SI2*b* in the display panel (display panel LCP2 in FIG. **14** and the like) disposed on the side of backlight BL. Therefore, at least the light from backlight BL having the largest light amount can be shielded.

Second Exemplary Embodiment

Liquid crystal display device LCD according to a second exemplary embodiment is constructed with display panel LCP1 (see FIG. **3** and the like) of the first exemplary embodiment while display panel LCP2 of liquid crystal display device LCD of the first exemplary embodiment is eliminated. FIG. **17** is a sectional view illustrating display panel LCP of the second exemplary embodiment. FIG. **17** illustrates the sectional portion taken along line B-B' in FIGS. **7** to **9**. In display panel LCP of the second exemplary embodiment, thin film transistor substrate TFTB is disposed on the side of backlight BL, and counter substrate CF is disposed on the observer side. Light absorption layer SIa (second semiconductor layer) overlaps at least a part of the channel region of thin film transistor TFT in planar view. Light absorption layer SIa may overlap the whole channel region of thin film transistor TFT or the whole region where thin film transistor TFT is formed in planar view. Light absorption layer SIb is formed into a ring shape, and disposed so as to surround the channel region of thin film transistor TFT in planar view. Light absorption layer SIb may overlap a part of gate electrode GE of thin film transistor TFT in planar view. Consequently, the light incident on the channel region of thin film transistor TFT can be shielded.

Liquid crystal display device LCD of the second exemplary embodiment is not limited to the above configuration. For example, as illustrated in FIG. **18**, thin film transistor substrate TFTB may be disposed on the observer side, and counter substrate CF may be disposed on the side of backlight BL. In the configuration of FIG. **18**, light absorption layer SIa is disposed between thin film transistor TFT and backlight BL and close to the channel region, so that the light incident on the channel region from backlight BL can be shielded.

The configuration of the pixel in liquid crystal display device LCD of the present disclosure is not limited to the configurations of the first and second exemplary embodiments. For example, in each exemplary embodiment, the thin film transistor and the light absorption layer may be made of oxide semiconductor. For example, in display panel LCP of FIG. **17**, light absorption layer SIa may be disposed between pixel electrode PIT and common electrode CIT.

Each of FIGS. **19** and **20** is a plan view illustrating another pixel configuration of display panel LCP2 of the first exem-

plary embodiment. As illustrated in FIG. **19**, light absorption layer SI**2***a* (a region (hatched portion) surrounded by a solid line in FIG. **19**) is disposed so as to overlap the channel region of thin film transistor TFT**2** in planar view. As illustrated in FIG. **20**, light absorption layer SI**2***b* (a region (hatched portion) surrounded by a solid line in FIG. **20**) is formed into a ring shape, disposed so as to surround the channel region of thin film transistor TFT**1** in planar view, and overlaps an outer peripheral end of gate electrode GE**1** of thin film transistor TFT**1** in planar view. Contact hole CH**2** may be made outside the region of light absorption layers SI**2***a*, SI**2***b* in planar view. The configuration of the pixel in FIGS. **19** and **20** can also be applied to display panel LCP**1** of the first exemplary embodiment and display panel LCP of the second exemplary embodiment.

FIG. **21** is a plan view illustrating another pixel configuration of display panel LCP of the second exemplary embodiment. FIG. **22** is a sectional view taken along line D-D' in FIG. **21**. In the display panel of FIG. **21**, common wiring CMT (a half tone portion in FIG. **21**) includes a portion (first portion CMTa) extending in the column direction and a portion (second portion CMTb) extending in the row direction, first portion CMTa overlaps source line SL in planar view, and second portion CMTb overlaps at least a part of the channel region of thin film transistor TFT in planar view. Second portion CMTb may overlap the whole channel region of thin film transistor TFT or the whole region where thin film transistor TFT is formed in planar view. Common wiring CMT is made of a metallic material (such as copper (Cu), molybdenum (Mo), or aluminum (Al)), and electrically connected to common electrode CIT. First portion CMTa and second portion CMTb may integrally be formed, or separately be formed while electrically connected to each other. In the configuration of FIGS. **19** and **20**, the amount of light incident on the channel region from the outside (for example, the observer side) can be decreased. Light absorption layer SIb is disposed on the side of backlight BL with respect to second portion CMTb, so that the back light can be prevented from being reflected by second portion CMTb to be incident on the channel region. Second portion CMTb is integral with common wiring CMT, and formed through the same process as common wiring CMT, so that the manufacturing process does not become complicated. In the configuration of FIGS. **19** and **20**, light absorption layer SIa may be eliminated. The configuration of FIGS. **19** and **20** can also be applied to display panels LCP**1**, LCP**2** of the first exemplary embodiment.

In the display panel of each exemplary embodiment described above, the semiconductor layer of the thin film transistor may be higher than the light absorption layer in density of at least one of boron and phosphorus. The semiconductor layer and the light absorption layer may be configured to include an amorphous silicon layer including an impurity layer containing at least one of boron and phosphorus.

Although exemplary embodiments of the present disclosure are described above, the present disclosure is not limited to these exemplary embodiments. It is noted that exemplary embodiments properly changed from the exemplary embodiments described above by those skilled in the art without departing from the scope of the present disclosure are included in the present disclosure.

What is claimed is:

1. A liquid crystal display device comprising:

a first substrate formed with a first gate line, a first source line, a first thin film transistor including a first channel region and a first semiconductor layer, a second semiconductor layer electrically insulated from the first semiconductor layer, and a third semiconductor layer electrically insulated from both of the first semiconductor layer and the second semiconductor layer;

a second substrate disposed opposite to the first substrate; and

a first liquid crystal layer disposed between the first substrate and the second substrate, wherein the second semiconductor layer is disposed between the first thin film transistor and the first liquid crystal layer, and overlaps at least a part of the first channel region of the first thin film transistor in planar view,

the third semiconductor layer is disposed in a layer identical to the first semiconductor layer, and disposed away from the first thin film transistor, and

the second semiconductor layer at least partially overlaps with the third semiconductor layer in planar view.

2. The liquid crystal display device according to claim **1**, wherein the first semiconductor layer and the second semiconductor layer are made of amorphous silicon.

3. The liquid crystal display device according to claim **1**, wherein only an inorganic insulator film is disposed between the first thin film transistor and the second semiconductor layer.

4. The liquid crystal display device according to claim **1**, wherein a thickness of the second semiconductor layer is larger than a thickness of the first semiconductor layer.

5. The liquid crystal display device according to claim **1**, wherein the first semiconductor layer is higher than the second semiconductor layer in density of at least one of boron and phosphorus.

6. The liquid crystal display device according to claim **1**, further comprising a backlight, wherein the first liquid crystal layer is disposed between the backlight and the first substrate.

7. The liquid crystal display device according to claim **1**, wherein

the second substrate includes a black matrix, and

at least a part of the second semiconductor layer does not overlap the black matrix in planar view.

8. The liquid crystal display device according to claim **1**, further comprising:

a third substrate formed with a second gate line, a second source line, and a second thin film transistor;

a fourth substrate disposed opposite to the third substrate; and

a second liquid crystal layer disposed between the third substrate and the fourth substrate, wherein the second substrate is disposed between the first liquid crystal layer and the second liquid crystal layer.

9. The liquid crystal display device according to claim **8**, further comprising a backlight, wherein the first liquid crystal layer is disposed between the backlight and the second substrate.

10. The liquid crystal display device according to claim **1**, further comprising:

a third substrate formed with a second gate line, a second source line, and a second thin film transistor;

a fourth substrate disposed opposite to the third substrate; and

a second liquid crystal layer disposed between the third substrate and the fourth substrate, wherein the first substrate is disposed between the first liquid crystal layer and the second liquid crystal layer.

11. The liquid crystal display device according to claim 10, further comprising a backlight, wherein the first liquid crystal layer is disposed between the backlight and the first substrate.

12. The liquid crystal display device according to claim 10, wherein

a fourth semiconductor layer is further formed on the third substrate, and

the fourth semiconductor layer is disposed between the second thin film transistor and the second liquid crystal layer, and overlaps at least a part of a second channel region of the second thin film transistor in planar view.

13. The liquid crystal display device according to claim 1, wherein the second semiconductor layer has a first hole,

the third semiconductor layer has a second hole, and

the first hole overlaps with the second hole in planar view.

14. The liquid crystal display device according to claim 12, wherein a fifth semiconductor layer is further formed on the third substrate, the fifth semiconductor layer is disposed in a layer identical to a semiconductor layer of the second thin film transistor, and disposed away from the first thin film transistor, and

the fifth semiconductor layer overlaps with the fourth semiconductor layer in planar view.

15. The liquid crystal display device according to claim 8, wherein the second substrate includes a color filter.

16. The liquid crystal display device according to claim 10, wherein the second substrate includes a color filter.

* * * * *

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摘要(译)

液晶显示装置包括形成有第一栅极线，第一源极线，包括第一沟道区和第一半导体层的第一薄膜晶体管，以及与第一半导体层电绝缘的第二半导体层的第一基板，与第一基板相对的第二基板，和位于第一基板和第二基板之间的第一液晶层。第二半导体层设置在第一薄膜晶体管和第一液晶层之间，并且在平面图中与第一薄膜晶体管的第一沟道区的至少一部分重叠。