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(54) **PIXEL CIRCUIT AND LIQUID CRYSTAL DISPLAY CIRCUIT**

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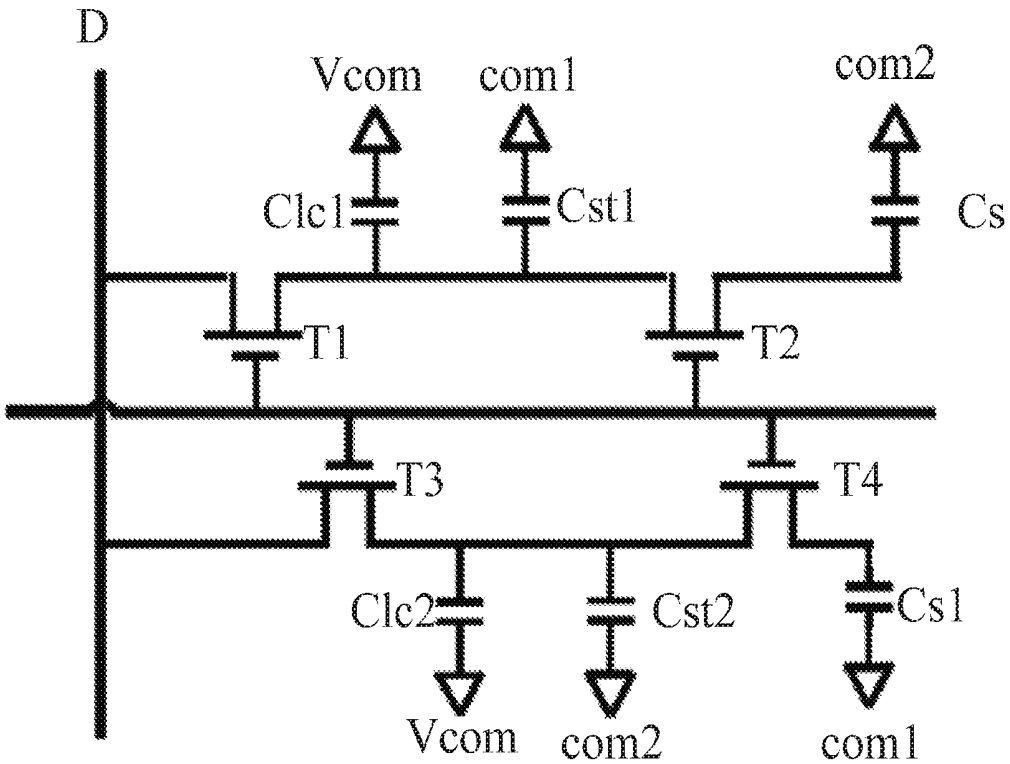
(57) **ABSTRACT**

The present disclosure provides a pixel circuit and a liquid crystal display circuit. The pixel circuit comprises a gate line, a data line, a first common line, a second common line, a first primary field-effect transistor (FET), a second primary FET, a first secondary FET, and a second secondary FET. A voltage of the first common line is different from a voltage of the second common line.



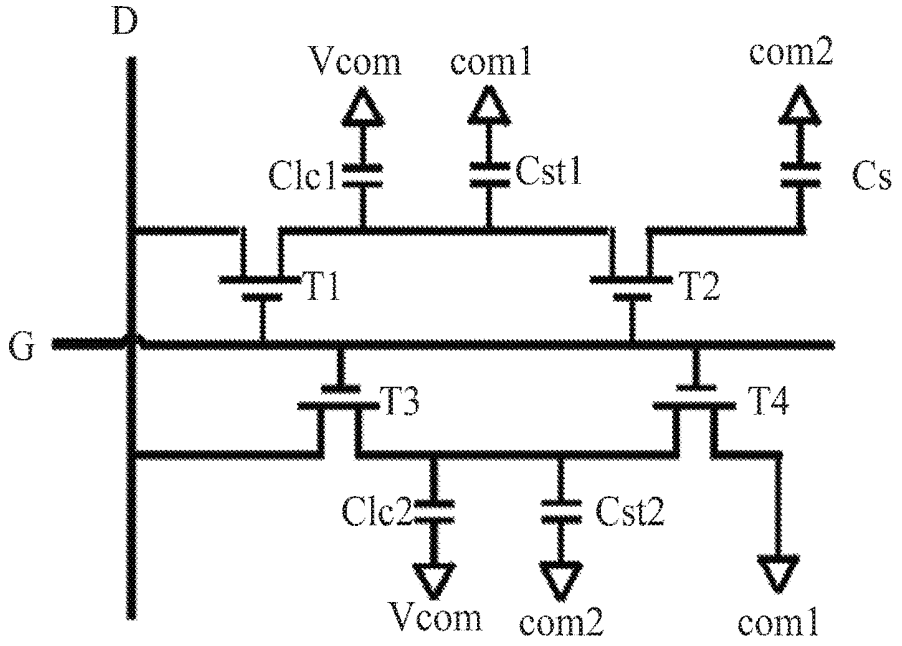

D
Vcom
com1
com2
Clc1
Cst1
Cs
T1
T2
G
T3
T4
Clc2
Cst2
Vcom
com2
com1

FIG. 1

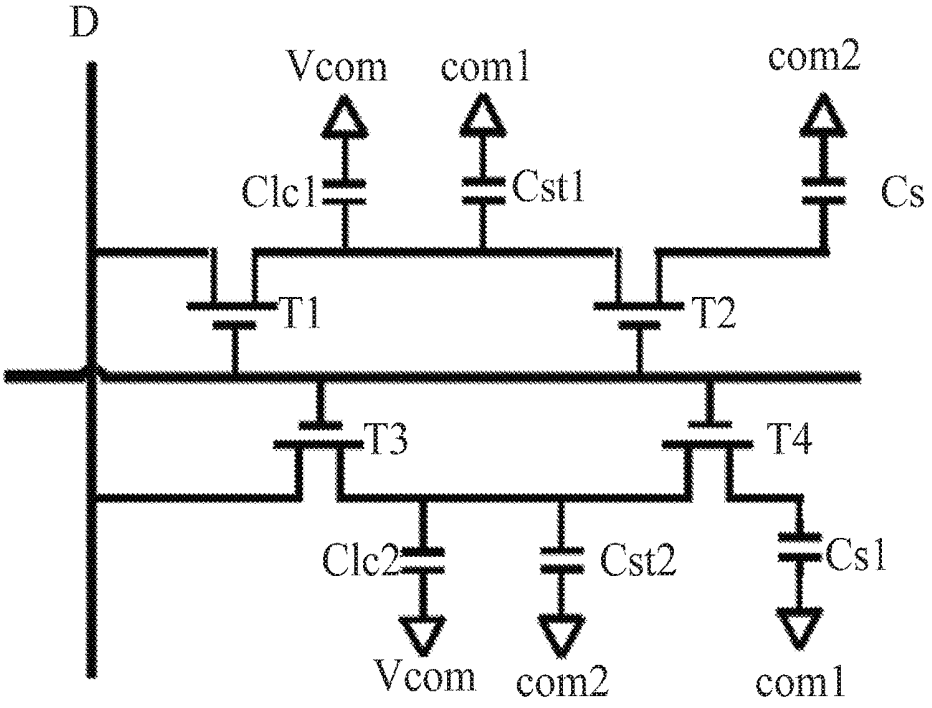

D
Vcom
com1
com2
Clc1
Cst1
Cs
T1
T2
T3
T4
Clc2
Cst2
Cs1
Vcom
com2
com1

FIG. 2

PIXEL CIRCUIT AND LIQUID CRYSTAL DISPLAY CIRCUIT

FIELD OF INVENTION

[0001] The present disclosure relates to the field of liquid crystal displays, and more particularly to a pixel circuit and a liquid display panel circuit.

BACKGROUND OF INVENTION

[0002] Eight-domain pixel structures lead the design trend for large dimension TVs. An eight-domain pixel is composed of a primary display area (primary area), a secondary display area (secondary area), and four different types of directing film. However, balance of a common voltage between the primary area and the secondary area becomes a dilemma due to high display resolution and high refresh rate. It becomes a problem when utilizing three transistor (3T) pixels.

[0003] The common voltage in the secondary area will be pulled down because in the present 3T pixel circuit structure, only the secondary area has a discharging path for a common electrode. Therefore, it is nearly impossible for the common voltage in the secondary area to reach an ideal level.

[0004] Therefore, defects of present technology urgently require improvement.

SUMMARY OF INVENTION

[0005] The object of this disclosure is to provide a pixel circuit and a liquid crystal display circuit to enhance the balance of common voltage between the primary area and the secondary area.

[0006] To solve the above-mentioned technical problems, the techniques that present disclosure provides are as follows.

[0007] The present disclosure provides a pixel circuit comprising:

[0008] a gate line configured to transmit a gate voltage;

[0009] a data line configured to transmit a data voltage;

[0010] a first common line configured to transmit a first common voltage;

[0011] a second common line configured to transmit a second common voltage;

[0012] a first primary field effect transistor (FET) comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a pixel capacitor;

[0013] a second primary FET comprising a source coupled to the drain of the first primary FET and coupled to the first common line through a primary storage capacitor, a gate coupled to the gate line, and a drain coupled to the second common line through a primary shared capacitor;

[0014] a first secondary FET comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a secondary pixel capacitor;

[0015] a second secondary FET comprising a source coupled to the drain of the first secondary FET and coupled to the second common line through a secondary storage capacitor, a gate coupled to the gate line, and a drain coupled to the first common line;

[0016] wherein a voltage of the first common line is different from a voltage of the second common line; and

[0017] the pixel circuit further comprises:

[0018] a first primary pixel electrode coupled to the source of the second primary FET; and

[0019] a first primary common electrode coupled to the first common line;

[0020] wherein the first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor; and

[0021] the first primary FET, the second primary FET, the first secondary FET, and the second secondary FET are thin film transistors.

[0022] The pixel circuit of present disclosure further comprises a first secondary common electrode coupled to the second common line and a first secondary pixel electrode coupled to the drain of the second secondary FET;

[0023] wherein the first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor.

[0024] The pixel circuit of present disclosure further comprises a primary metal layer coupled to the drain of the second primary FET, wherein the primary metal layer and the first secondary common electrode compose the primary shared capacitor.

[0025] In the pixel circuit of present disclosure, the drain of the second primary FET is coupled to the first common line through a secondary shared capacitor.

[0026] The pixel circuit of present disclosure further comprises a secondary metal layer coupled to the drain of the second secondary FET, wherein the secondary metal layer and the first primary common electrode compose the secondary shared capacitor.

[0027] The present disclosure further provides a pixel circuit which comprises:

[0028] a gate line configured to transmit a gate voltage;

[0029] a data line configured to transmit a data voltage;

[0030] a first common line configured to transmit a first common voltage;

[0031] a second common line configured to transmit a second common voltage;

[0032] a first primary field effect transistor (FET) comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a pixel capacitor;

[0033] a second primary FET comprising a source coupled to the drain of the first primary FET and coupled to the first common line through a storage capacitor, a gate coupled to the gate line, and a drain coupled to the second common line through a primary shared capacitor;

[0034] a first secondary FET comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a secondary pixel capacitor;

[0035] a second secondary FET comprising a source coupled to the drain of the first secondary FET and coupled to the second common line through a secondary storage capacitor, a gate coupled to the gate line, and a drain coupled to the first common line; wherein

[0036] a voltage of the first common line is different from a voltage of the second common line.

[0037] The pixel circuit of present disclosure further comprises a first primary pixel electrode coupled to the source of the second primary FET and a first primary common electrode coupled to the first common line. Wherein the first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor.

[0038] The pixel circuit of present disclosure further comprises a first secondary common electrode coupled to the second common line and a first secondary pixel electrode coupled to the drain of the second primary FET, wherein the first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor.

[0039] The pixel circuit of present disclosure further comprises a primary metal layer coupled to the drain of the second primary FET, wherein the primary metal layer and the first secondary common electrode compose the primary shared capacitor.

[0040] In the pixel circuit of present disclosure, the drain of the second primary FET is coupled to the first common line through a secondary shared capacitor.

[0041] The pixel circuit of present disclosure further comprises a secondary metal layer coupled to the drain of the second secondary FET, wherein the secondary metal layer and the first primary common electrode compose the secondary shared capacitor.

[0042] In the pixel circuit of present disclosure, the first primary FET, the second primary FET, the first secondary FET, and the second secondary FET are thin film transistors.

[0043] The present disclosure further comprises a liquid crystal display circuit comprising a pixel circuit, wherein the pixel circuit further comprises:

[0044] a gate line configured to transmit a gate voltage;

[0045] a data line configured to transmit a data voltage;

[0046] a first common line configured to transmit a first common voltage;

[0047] a second common line configured to transmit a second common voltage;

[0048] a first primary field effect transistor (FET) comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a pixel capacitor;

[0049] a second primary FET comprising a source coupled to the drain of the first primary FET and coupled to the first common line through a storage capacitor, a gate coupled to the gate line, and a drain coupled to the second common line through a primary shared capacitor;

[0050] a first secondary FET comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a secondary pixel capacitor;

[0051] a second secondary FET comprising a source coupled to the drain of the first secondary FET and coupled to the second common line through a secondary storage capacitor, a gate coupled to the gate line, and a drain coupled to the first common line; wherein

[0052] a voltage of the first common line is different from a voltage of the second common line.

[0053] The liquid display panel circuit of present disclosure further comprises a first primary pixel electrode coupled to the source of the second primary FET and a first primary common electrode coupled to the first common line, wherein the first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor.

[0054] The liquid display panel circuit of present disclosure further comprises a first secondary common electrode coupled to the second common line and a first secondary pixel electrode coupled to the drain of the second primary FET, wherein the first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor.

[0055] In the liquid display panel circuit of present disclosure, the pixel circuit further comprises a primary metal layer coupled to the drain of the second primary FET, wherein the primary metal layer and the first secondary common electrode compose the primary shared capacitor.

[0056] In the liquid display panel circuit of present disclosure, the drain of the second primary FET is coupled to the first common line through a secondary shared capacitor.

[0057] In the liquid display panel circuit of present disclosure, the pixel circuit further comprises a secondary metal layer coupled to the drain of the second secondary FET, wherein the secondary metal layer and the first primary common electrode compose the secondary shared capacitor.

[0058] In the liquid display panel circuit of present disclosure, the first primary FET, the second primary FET, the first secondary FET, and the second secondary FET are thin film transistors.

[0059] In the pixel circuit and the liquid display panel circuit of present disclosure, the ratio of voltages in the primary area to voltages in the secondary area can be maintained by disposing a primary shared capacitor. The primary shared capacitor is utilized to control the variation between the first common voltage of the first common line in the primary area and the second common voltage of the second common line in the secondary area. Therefore, the balance of common voltage between the primary area and secondary area can be improved.

DESCRIPTION OF THE DRAWINGS

[0060] FIG. **1** illustrates a structure of a preferable embodiment of a pixel circuit.

[0061] FIG. **2** illustrates another structure of a preferable embodiment of a pixel circuit.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0062] The illustrations of the following embodiments take the attached drawings as reference to indicate the applicable specific examples of the present disclosure. The mentioned directional terms, such as upper, lower, front, back, left, right, inner, outer, side, etc., are only directions by referring to the accompanying drawings, and thus the used directional terms are used to describe and understand the present invention, but the present invention is not limited thereto.

[0063] In the drawings, the similar modules are numbered with the same reference numbers.

[0064] Please refer to FIG. **1** which illustrates a preferable embodiment of a pixel circuit. The pixel circuit comprises a gate line G, a data line D, a first common line com**1**, a second common line com**2**, a first primary field-effect transistor (FET) T**1**, a second primary FET T**2**, a first secondary FET T**3**, and a second secondary FET T**4**.

[0065] The gate line G is utilized to transmit a gate voltage, in order to control the first primary FET T**1**, the second primary FET T**2**, the first secondary FET T**3**, and the second secondary FET T**4** to be in conduction or saturation mode.

[0066] The data line D is utilized to transmit a data voltage to the first primary FET T**1** and the first secondary FET T**3**.

[0067] The first common line com**1** is utilized to transmit a first common voltage Vcom**1**, and is coupled to the first primary common electrode com**1**.

[0068] The second common line com**2** is utilized to transmit a second common voltage Vcom**2**.

[0069] A source of the first primary FET T**1** is coupled to the data line D. A gate of the first primary FET T**1** is coupled to the gate line G. A drain of the first primary FET T**1** is coupled to a primary pixel capacitor Clc**1**. Another side of the primary pixel capacitor Clc**1** receives a common voltage Vcom.

[0070] A source of the second primary FET T**2** is coupled to the drain of the first primary FET T**1**. The source of the second primary FET T**2** is also coupled to the first common line com**1** through a primary storage capacitor Cst**1**. A gate of the second primary FET T**2** is coupled to the gate line G. A drain of the second primary FET T**2** is coupled to the second common line com**2**.

[0071] A source of the first secondary FET T**3** is coupled to the data line D. A gate of the first secondary FET T**3** is coupled to the gate line G. A drain of the first secondary FET T**3** is coupled to a secondary capacitor Clc**2**. Another side of the secondary capacitor Clc**2** receives the common voltage Vcom.

[0072] A source of the second secondary FET T**4** is coupled to the drain of the first secondary FET T**3**. The source of the second secondary FET T**4** is also coupled to the second common line com**2** through a primary storage capacitor Cst**2**. A gate of the second secondary FET T**4** is coupled to the gate line G. A drain of the second secondary FET T**4** is coupled to the first common line com**1**.

[0073] In practical application, the pixel circuit comprises a first primary pixel electrode, a first primary common electrode, a primary metal layer, a first secondary electrode, and a first secondary pixel electrode.

[0074] The first primary pixel electrode is coupled to the source of the second primary FET T**2**. The first primary common electrode is coupled to the first common line com**1**. The first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor Cst**1**.

[0075] The first secondary common electrode is coupled to the second common line com**2**. The first secondary pixel electrode is coupled to the source of the second secondary FET T**4**. The first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor Cst**2**.

[0076] The primary metal layer is coupled to the drain of the second primary FET T**2**. The primary metal layer and the first secondary common electrode compose the shared capacitor Cs.

[0077] Please refer to FIG. **2**. In another embodiment, the pixel circuit comprises a secondary shared capacitor Cs**1**. A drain of the second primary FET T**4** is coupled to the first common line cord through the secondary shared capacitor Cs**1**.

[0078] In practical application, the pixel circuit further comprises a secondary metal layer. The secondary metal layer is coupled to the drain of the second secondary FET T**4**. The secondary metal layer and the first primary common electrode compose the secondary shared capacitor Cs**1**.

[0079] Present disclosure further provides a liquid display circuit which comprises the above-mentioned pixel circuit. The plurality of pixel circuits is arranged in array. Pixel circuits of the same row are connected one by one through their gate lines. Pixel circuits of the same column are connected one by one through their data lines. That is, pixel circuits of the same row share the same gate line, and pixel circuits of the same column share the same data line.

[0080] In the pixel circuit and liquid crystal display circuit provided in the present disclosure, the ratio of voltages in primary area to voltages in secondary area can be maintained by disposing a primary shared capacitor. The primary shared capacitor is utilized to control the variation between the first common voltage of the first common line in primary area and the second common voltage of the second common line secondary area. Therefore, the balance of common voltage between primary area and secondary area can be improved.

[0081] In conclusion, although this disclosure has been disclosed through the preferable embodiments above, the preferable embodiments above are not utilized to limit this disclosure. One having ordinary skills can change and modify without violating the concepts and scope of this disclosure. Therefore, the scope that this disclosure protects is based on the scope defined by the claims.

What is claimed is:

1. A pixel circuit, comprising:

a gate line configured to transmit a gate voltage;

a data line configured to transmit a data voltage;

a first common line configured to transmit a first common voltage;

a second common line configured to transmit a second common voltage;

a first primary field effect transistor (FET) comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a pixel capacitor;

a second primary FET comprising a source coupled to the drain of the first primary FET and coupled to the first common line through a primary storage capacitor, a gate coupled to the gate line, and a drain coupled to the second common line through a primary shared capacitor;

a first secondary FET comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a secondary pixel capacitor;

a second secondary FET comprising a source coupled to the drain of the first secondary FET and coupled to the second common line through a secondary storage capacitor, a gate coupled to the gate line, and a drain coupled to the first common line;

wherein a voltage of the first common line is different from a voltage of the second common line;

the pixel circuit further comprises:

a first primary pixel electrode coupled to the source of the second primary FET; and

a first primary common electrode coupled to the first common line;

wherein the first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor; and

the first primary FET, the second primary FET, the first secondary FET, and the second secondary FET are thin film transistors.

2. The pixel circuit according to claim **1**, further comprising:

a first secondary common electrode coupled to the second common line; and

a first secondary pixel electrode coupled to the drain of the second secondary FET;

wherein the first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor.

3. The pixel circuit according to claim **2**, further comprising:

a primary metal layer coupled to the drain of the second primary FET, wherein the primary metal layer and the first secondary common electrode compose the primary shared capacitor.

4. The pixel circuit according to claim **2**, wherein the drain of the second primary FET is coupled to the first common line through a secondary shared capacitor.

5. The pixel circuit according to claim **4**, further comprising: a secondary metal layer coupled to the drain of the second secondary FET, wherein the secondary metal layer and the first primary common electrode compose the secondary shared capacitor.

6. A pixel circuit, comprising:

a gate line configured to transmit a gate voltage;

a data line configured to transmit a data voltage;

a first common line configured to transmit a first common voltage;

a second common line configured to transmit a second common voltage;

a first primary field effect transistor (FET) comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a pixel capacitor;

a second primary FET comprising a source coupled to the drain of the first primary FET and coupled to the first common line through a storage capacitor, a gate coupled to the gate line, and a drain coupled to the second common line through a primary shared capacitor;

a first secondary FET comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a secondary pixel capacitor;

a second secondary FET comprising a source coupled to the drain of the first secondary FET and coupled to the second common line through a secondary storage capacitor, a gate coupled to the gate line, and a drain coupled to the first common line;

wherein a voltage of the first common line is different from a voltage of the second common line.

7. The pixel circuit according to claim **6**, further comprising:

a first primary pixel electrode coupled to the source of the second primary FET; and

a first primary common electrode coupled to the first common line;

wherein the first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor.

8. The pixel circuit according to claim **7**, further comprising:

a first secondary common electrode coupled to the second common line; and

a first secondary pixel electrode coupled to the drain of the second primary FET;

wherein the first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor.

9. The pixel circuit according to claim **8**, further comprising: a primary metal layer coupled to the drain of the second primary FET, wherein the primary metal layer and the first secondary common electrode compose the primary shared capacitor.

10. The pixel circuit according to claim **8**, wherein the drain of the second primary FET is coupled to the first common line through a secondary shared capacitor.

11. The pixel circuit according to claim **10**, further comprising: a secondary metal layer coupled to the drain of the second secondary FET, wherein the secondary metal layer and the first primary common electrode compose the secondary shared capacitor.

12. The pixel circuit according to claim **6**, wherein the first primary FET, the second primary FET, the first secondary FET, and the second secondary FET are thin film transistors.

13. A liquid crystal display circuit, comprising: a pixel circuit comprising:

a gate line configured to transmit a gate voltage;

a data line configured to transmit a data voltage;

a first common line configured to transmit a first common voltage;

a second common line configured to transmit a second common voltage;

a first primary field effect transistor (FET) comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a pixel capacitor;

a second primary FET comprising a source coupled to the drain of the first primary FET and coupled to the first common line through a storage capacitor, a gate coupled to the gate line, and a drain coupled to the second common line through a primary shared capacitor;

a first secondary FET comprising a source coupled to the data line, a gate coupled to the gate line, and a drain coupled to a secondary pixel capacitor;

a second secondary FET comprising a source coupled to the drain of the first secondary FET and coupled to the second common line through a secondary storage capacitor, a gate coupled to the gate line, and a drain coupled to the first common line; wherein

a voltage of the first common line is different from a voltage of the second common line.

14. The liquid crystal display circuit according to claim **13**, wherein the pixel circuit further comprises:

a first primary pixel electrode coupled to the source of the second primary FET; and

a first primary common electrode coupled to the first common line;

wherein the first primary pixel electrode and the first primary pixel electrode compose the primary storage capacitor.

15. The liquid crystal display circuit according to claim **14**, wherein the pixel circuit further comprises:

a first secondary common electrode coupled to the second common line; and

a first secondary pixel electrode coupled to the drain of the second primary FET;

wherein the first secondary common electrode and the first secondary pixel electrode compose the secondary storage capacitor.

16. The liquid crystal display circuit according to claim **15**, wherein the pixel circuit further comprises: a primary metal layer coupled to the drain of the second primary FET,

wherein the primary metal layer and the first secondary common electrode compose the primary shared capacitor.

17. The liquid crystal display circuit according to claim **15**, wherein the drain of the second primary FET is coupled to the first common line through a secondary shared capacitor of the pixel circuit.

18. The liquid crystal display circuit according to claim **17**, wherein the pixel circuit further comprises: a secondary metal layer coupled to the drain of the second secondary FET, wherein the secondary metal layer and the first primary common electrode compose the secondary shared capacitor.

19. The liquid crystal display circuit according to claim **13**, wherein the first primary FET, the second primary FET, the first secondary FET, and the second secondary FET are thin film transistors.

* * * * *

专利名称(译)	像素电路和液晶显示电路		
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[标]发明人	GAN QIMING		
发明人	GAN, QIMING		
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优先权	201711041093.2 2017-10-30 CN		
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外部链接	Espacenet USPTO		

摘要(译)

本公开提供了一种像素电路和液晶显示电路。像素电路包括栅极线，数据线，第一公共线，第二公共线，第一主场效应晶体管（FET），第二主FET，第一次级FET和第二次级FET。第一公共线的电压不同于第二公共线的电压。