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(19) **United States**(12) **Patent Application Publication**
Sun(10) **Pub. No.: US 2013/0120680 A1**(43) **Pub. Date: May 16, 2013**(54) **TFT ARRAY SUBSTRATE AND DISPLAY
DEVICE****Publication Classification**(71) Applicant: **Rongge Sun**, Beijing (CN)(72) Inventor: **Rongge Sun**, Beijing (CN)(73) Assignees: **HEFEI XINSHENG
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Beijing (CN)(51) **Int. Cl.**
G02F 1/1368 (2006.01)(52) **U.S. Cl.**
CPC **G02F 1/1368** (2013.01)
USPC **349/43**(57) **ABSTRACT**

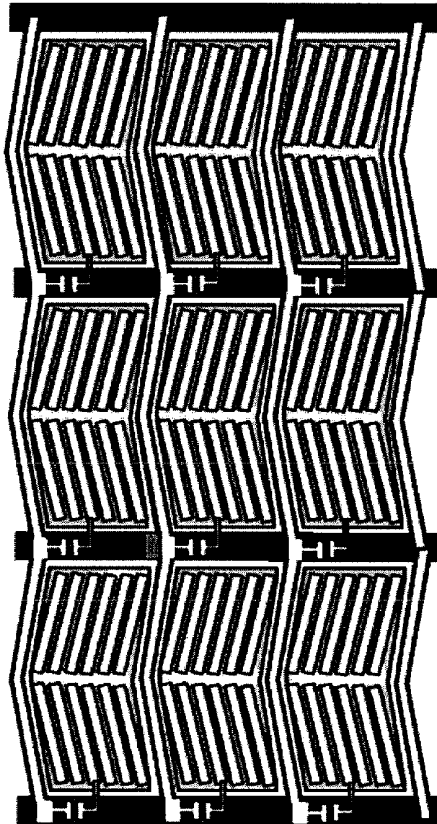
According to an embodiment of the present invention, there is disclosed a thin film transistor (TFT) array substrate comprising a sub-pixel units the sub-pixel unit comprises a thin film transistor device, a common electrode, a first pixel electrode layer and a second pixel electrode layer; one of the first pixel electrode layer and the second pixel electrode layer is connected to the common electrode, the other one is connected to a source electrode or a drain electrode of the thin film transistor, and the first and second pixel electrode layers are separated by an insulating layer; the second pixel electrode layer is located over the first pixel electrode layer; and the strip-like pixel electrodes make a tilt angle with an initial orientation of liquid crystals, and a gate line or a data line is parallel to the strip-like pixel electrodes close to itself. According to the embodiment, a phenomenon of orientation disorder of liquid crystals will not occur at an edge of pixel from influence of disordered electric fields.

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§ 371 (c)(1),

(2), (4) Date: **Dec. 17, 2012**(30) **Foreign Application Priority Data**

Nov. 15, 2011 (CN) 201110362219.2



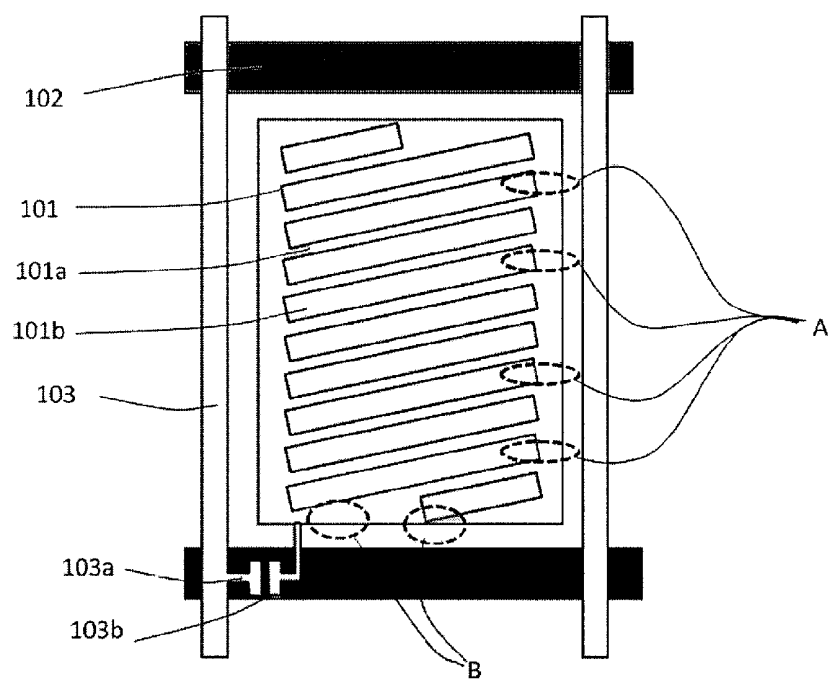


FIG.1

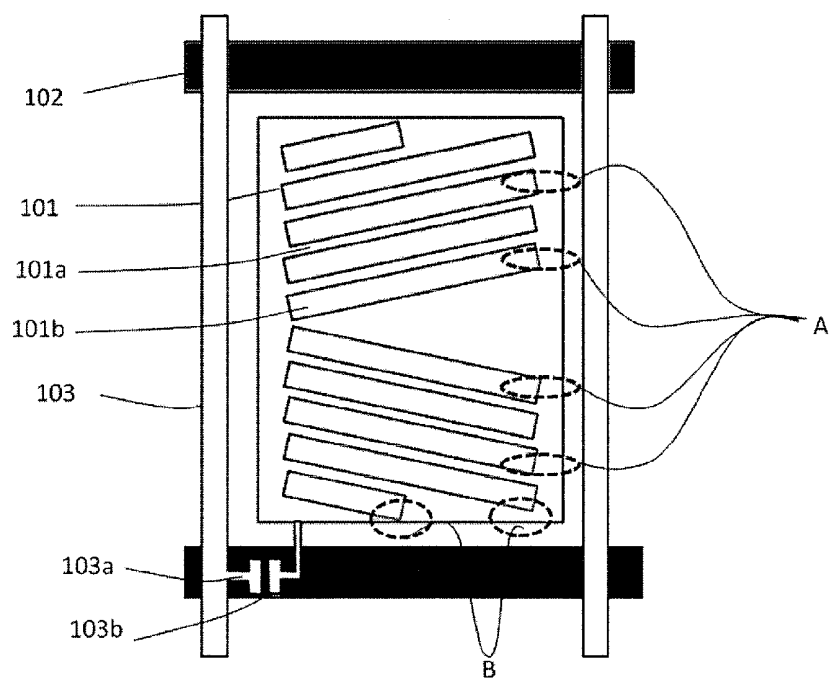


FIG.2

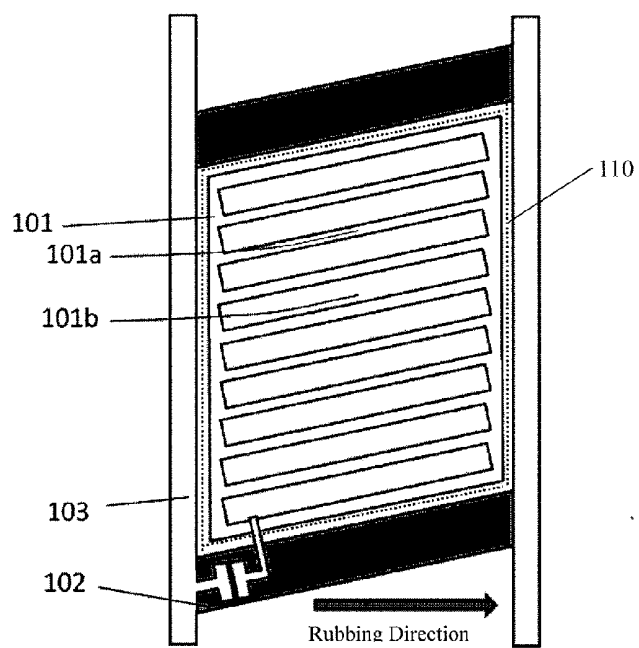


FIG.3

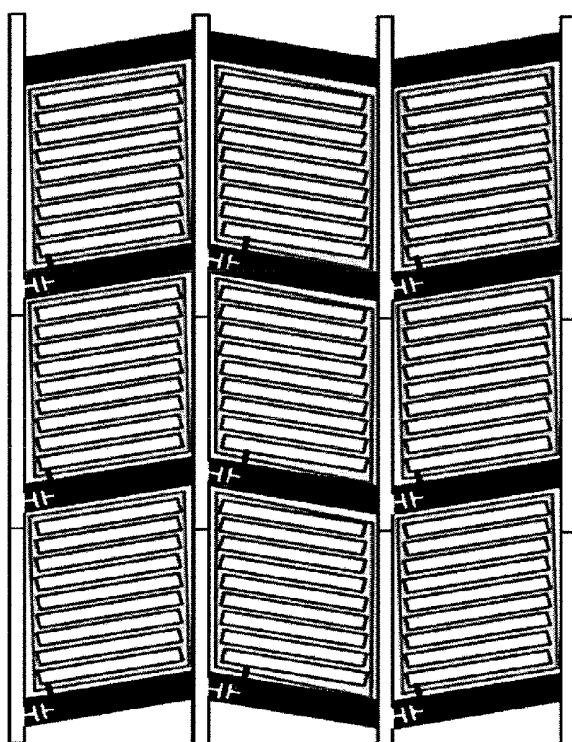


FIG.4

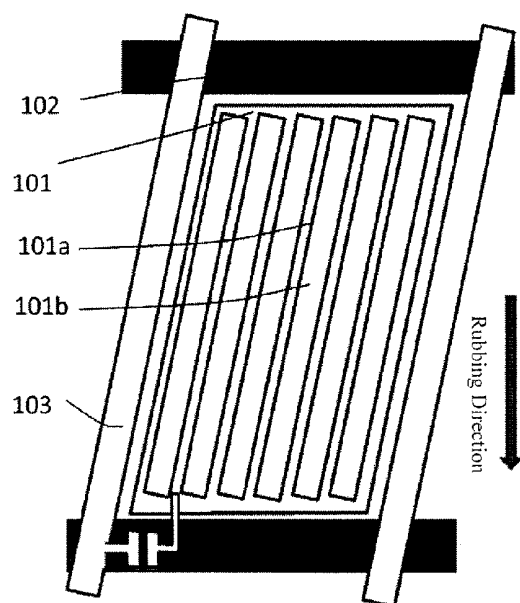


FIG.5

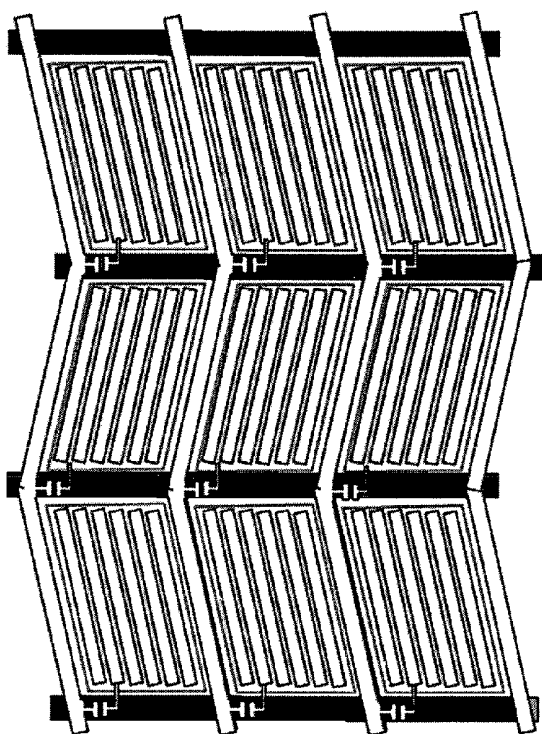


FIG.6

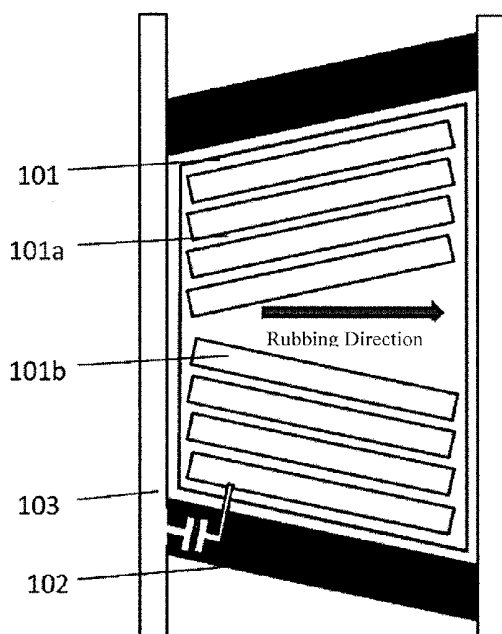


FIG. 7

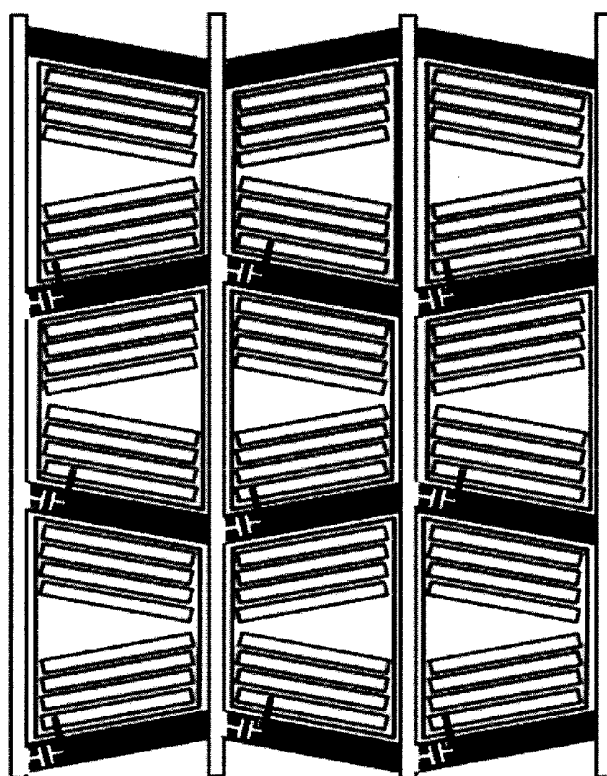


FIG. 8

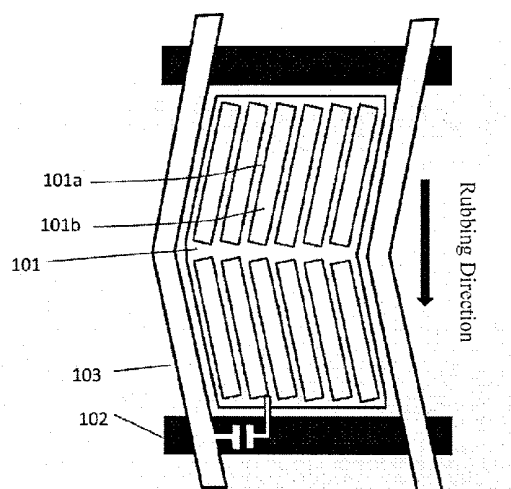


FIG.9

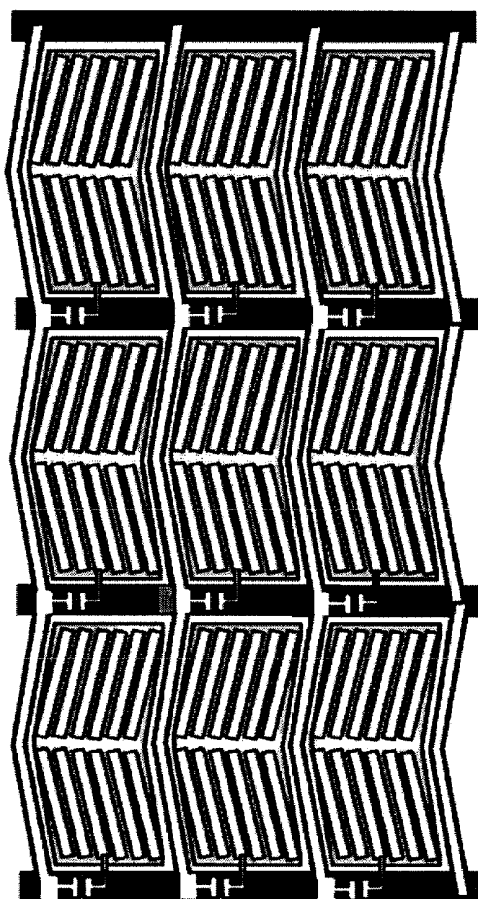


FIG.10

TFT ARRAY SUBSTRATE AND DISPLAY DEVICE

TECHNICAL FIELD

[0001] Embodiments of the present invention relate to a thin film transistor (TFT) array substrate and display device.

BACKGROUND

[0002] TN, IPS, VA and ADS are several modes of liquid crystal display. ADS is the abbreviation for Advanced Super Dimension Switch (ADSDS), i.e., an advanced super dimension switch technology, in which a multi-dimensional electric field is formed by an electric field produced at edges of slit electrodes on a same plane and an electric field produced between a layer of the slit electrodes and a layer of a plate-like electrode, and allows liquid crystal molecules in all orientations in a liquid crystal cell, which are located directly above the electrode and between the slit electrodes, to be rotated, thereby enhancing the work efficiency of liquid crystals and increasing the transmissive efficiency. The Advanced Super Dimensional Switch technology can improve the picture quality of TFT products, and has advantages of high resolution, high transmittance, low power consumption, wide viewing angle, high aperture ratio, low chromatic aberration, and push Mura-free, etc.

[0003] In manufacturing an array substrate of a TFT liquid crystal display in an ADS mode, the first layer is a transparent pixel electrode layer (usually indium tin oxide (ITO)), i.e., the above plate-like electrode; subsequently, a gate metal layer, a source-drain metal electrode layer and a second pixel electrode layer (usually also ITO) are formed in sequence, and the second pixel electrode layer is the above slit-like electrode. For the sake of illustrative convenience, a plurality of strip-like structures with a certain width and interval in the second pixel electrode layer are called as strip-like pixel electrodes. These strip-like structures and openings between the strip-like structures form the slit-like electrodes.

[0004] The TFT pixel structure in the ADS mode has ever been in evolving. An early stage structure was a single domain structure, as shown in FIG. 1. The single domain pixel structure comprises: a gate line 102, a data line 103, a second pixel electrode layer 101, and strip-like pixel electrodes 101a located on the second pixel electrode layer 101 and openings 101b of the second pixel electrode layer. The gate line 102 and the data line 103 intersect each other to define a sub-pixel unit. The data line 103 is connected to a drain electrode 103a of a TFT, and a source electrode 103b of the TFT is connected to the second pixel electrode layer 101. Strip-like pixel electrodes within the same sub-pixel have a same direction in the figure.

[0005] Later, a two domain structure was proposed. In the two domain structure, a sub-pixel can be divided into two parts of left and right, and strip-like pixel electrodes for the two parts are bilaterally symmetric, so that chromatic aberration can be further decreased. However, black vertical stripes occur at the junction of two domains at the center of the sub-pixel.

[0006] Later, a pixel structure design was proposed by US Patent Application Publication No. US 2002/0041354, as shown in FIG. 2. The pixel unit also has a two domain structure and is divided into two parts of upper and lower, and strip-like pixel electrodes for the two parts are longitudinally symmetric, so that an effect of low chromatic aberration is

obtained, and at the same time, a black-stripe region at the junction of domains is reduced and the transmissive characteristic is enhanced.

[0007] However, the forgoing existing technologies did not resolve black stripes at edges of pixels. At an edge of a pixel unit in the ADS mode, due to a disturbed electric field produced by a gate line or a data line and an influence brought by a pixel-electrode edge per se, the electric field direction in this place is inconsistent with direction of the fringe field for driving liquid crystals inside the pixel unit, so that an orientation disorder of liquid crystals occurs at the edge of the pixel unit. A, B shown in FIGS. 1 and 2 are regions of the orientation disorder of liquid crystals in the neighborhood of data lines and gate lines, respectively. Presence of the black stripes will affect transmittance and response speed of the display panel. For improving the display effect, a wider black matrix is usually prepared on an opposed color filter substrate so as to shield the regions of the orientation disorder, which causes degradation of the aperture ratio. Thus, transmittance is reduced.

SUMMARY

[0008] Embodiments of the present invention can overcome the defect that there are too many black-stripe regions at edges of pixels, thereby enhancing aperture ratio and transmittance.

[0009] In one aspect of the present invention, there is provided a TFT array substrate, comprising: a gate line and a data line, which are formed on a substrate, and a sub-pixel unit defined by intersecting of the gate line and the data line, wherein the sub-pixel unit comprises a thin film transistor device, a common electrode, a first pixel electrode layer and a second pixel electrode layer; wherein one of the first pixel electrode layer and the second pixel electrode layer is connected to the common electrode, the other one of the pixel electrode layers is connected to a source electrode or a drain electrode of the thin film transistor, and the first pixel electrode layer and the second pixel electrode layer are separated by an insulating layer; the second pixel electrode layer is located over the first pixel electrode layer, and the pattern of strip-like pixel electrodes of the second pixel electrode layer overlap up-and-down with the pattern of the first pixel electrode layer; and the strip-like pixel electrodes make a tilt angle with an initial orientation of liquid crystals, and a gate line or a data line is parallel to the strip-like pixel electrodes close to the gate line or the data line.

[0010] As to the TFT array substrate, for example, the tilt angle is 3°~15°.

[0011] As to the TFT array substrate, for example, the tilt angle is 7°~12°.

[0012] As to the TFT array substrate, for example, the strip-like pixel electrodes of the second pixel electrode layer are parallel to each other. For example, the gate line is parallel to the strip-like pixel electrodes of the second pixel electrode layer, and the data line is perpendicular to the initial orientation of liquid crystals. Or, for example, the data line is parallel to the strip-like pixel electrodes of the second pixel electrode layer, and the gate line is perpendicular to the initial orientation of liquid crystals.

[0013] As to the TFT array substrate, for example, the strip-like pixel electrodes of the second pixel electrode layer are divided into two sets which are symmetric to each other. For example, the gate line is parallel to one of the sets of the strip-like pixel electrodes in the second pixel electrode layer,

which are close to the gate line, and the data line is perpendicular to the initial orientation of liquid crystals. Or, a first part of the data line is parallel to one set of the strip-like pixel electrodes in the second pixel electrode layer, which is close to the first part, a second part of the data lines are parallel to the other set of the strip-like pixel electrodes in the second pixel electrode layer, which is close to the second part, and the gate line is perpendicular to the initial orientation of liquid crystals.

[0014] For example, the TFT array substrate may comprise a plurality of gate lines, a plurality of data lines, and a plurality of sub-pixels defined by intersecting of the plurality of gate lines and the plurality of data lines, wherein along the direction of the initial orientation of liquid crystals, the strip-like pixel electrodes in two adjoining sub-pixel units are symmetric to each other with respect to a gate line or data line therebetween, and along a direction perpendicular to the initial orientation of liquid crystals, the strip-like pixel electrodes in two adjoining sub-pixel units, which adjoin, are parallel to each other.

[0015] As to the TFT array substrate, for example, the first pixel electrode layer comprises a plate-like electrode.

[0016] In another aspect of the invention, there is further provided a display device, an array substrate in the display device is the TFT array substrate as stated above.

[0017] According to embodiments of the invention, by means of making direction of the gate line or data line parallel to that of a neighbor pixel electrode, direction of a disturbed electric field for the gate line or data line are made to be consistent with direction of a fringe field within a pixel unit; and meanwhile, because the pixel-electrode edge in the neighborhood of the gate line or the data line is parallel to the inside strip-like pixel electrodes, the electric field direction at the edge of the pixel unit is made to be consistent with direction of the fringe field within the pixel unit. As such, regions of orientation disorder of liquid crystals at the edge of the pixel unit are reduced, and aperture ratio and transmissive characteristic of the pixel unit are improved. According to the embodiments of the invention, a higher aperture ratio and transmittance can be achieved without adding process steps, thereby enhancing optical utilization ratio, reducing costs and power consumption of a backlight source, and obtaining an effect of more green and environmental protection, compared with the prior art.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] To illustrate technical solutions in embodiments of the present invention more clearly, accompanied drawings will be briefly introduced below. Obviously, the accompanied drawings described below merely relate to some embodiments of the present invention, and are not limitation on the present invention.

[0019] FIG. 1 is a schematic view illustrating the structure of a TFT array substrate in prior art;

[0020] FIG. 2 is a schematic view illustrating the structure of another kind of TFT array substrate in prior art;

[0021] FIG. 3 is a schematic view illustrating a sub-pixel structure in a TFT array substrate according to an embodiment of the invention;

[0022] FIG. 4 is a schematic view illustrating an array substrate containing nine sub-pixel structures as shown in FIG. 3;

[0023] FIG. 5 is a schematic view illustrating a sub-pixel structure in another kind of TFT array substrate according to an embodiment of the invention;

[0024] FIG. 6 is a schematic view illustrating an array substrate containing nine sub-pixel structures as shown in FIG. 5;

[0025] FIG. 7 is a schematic view illustrating a sub-pixel structure in another kind of TFT array substrate according to an embodiment of the invention;

[0026] FIG. 8 is a schematic view illustrating an array substrate containing nine sub-pixel structures as shown in FIG. 7;

[0027] FIG. 9 is a schematic view illustrating a sub-pixel structure in another kind of TFT array substrate according to an embodiment of the invention;

[0028] FIG. 10 is a schematic view illustrating an array substrate containing nine sub-pixel structures as shown in FIG. 9.

DETAILED DESCRIPTION

[0029] In order to make objects, technical details and advantages of the embodiments of the invention apparent, hereinafter, technical solutions in embodiments of the present invention will be clearly and fully described in combination with the accompanied drawings in the embodiments of the present invention. Apparently, the embodiments to be described are merely a part but not all of embodiments of the present invention. Every other embodiment as would be obvious to those ordinarily skilled in the art on the basis of described embodiments in the present invention without creative work, comes within the protection scope of the present invention.

[0030] Unless otherwise defined, all the technical and scientific terms used herein have the same meanings as commonly understood by one of ordinary skill in the art to which the present invention belongs. The terms “first,” “second,” etc., which are used in the description and the claims of the present application for invention, are not intended to indicate any sequence, amount or importance, but distinguish various components. Also, the terms such as “a,” “an,” etc., are not intended to limit the amount, but indicate the existence of at least one. The terms “comprises,” “comprising,” “includes,” “including,” etc., are intended to specify that the elements or the objects stated before these terms encompass the elements or the objects and equivalents thereof listed after these terms, but do not preclude the other elements or objects. The phrases “connect,” “connected,” etc., are not intended to define a physical connection or mechanical connection, but may include an electrical connection, directly or indirectly. “On,” “under,” “right,” “left” and the like are only used to indicate relative position relationship, and when the position of the object which is described is changed, the relative position relationship may be changed accordingly.

[0031] The array substrate of the embodiment of the present invention includes a plurality of gate lines and a plurality of data lines which intersect each other to define a pixel units arranged in an array, each pixel unit comprising a thin film transistor as a switch element, and a pixel electrode and a common electrode for controlling orientation of liquid crystal. For example, a gate electrode of the thin film transistor in each pixel is electrically connected to or integrally formed with a corresponding gate line, a source electrode thereof is connected to or integrally formed with a corresponding data line, and a drain electrode thereof is connected to or integrally formed with a corresponding pixel electrode. The following description is mainly connected with one or more pixel units, but other pixel units can be formed similarly.

Embodiment 1

[0032] FIG. 3 is a schematic view illustrating the structure of a single sub-pixel in a TFT array substrate structure according to the invention. The array substrate comprises a plurality of gate lines 102 and a plurality of data lines 103 which are formed on a base substrate (not shown in the figure); and a plurality of sub-pixel units defined by intersecting each other of these gate lines 102 and data lines 103, each of the sub-pixel units comprising a thin film transistor device as a switching element and a common electrode, a first pixel electrode layer 110 and a second pixel electrode layer 101. The first pixel electrode layer 110, as shown by a broken-line in FIG. 3, comprises a plate-like electrode, for example. On the second pixel electrode layer 101, there are strip-like pixel electrodes 101a and openings 101b of the second pixel electrode layer 101. One of the first pixel electrode layer 110 and the second pixel electrode layer 101 is connected to the common electrode, the other one of the pixel electrode layers is connected to a source electrode or a drain electrode of the thin film transistor, and the first pixel electrode layer 110 and the second pixel electrode layer 101 are separated by an insulating layer. The second pixel electrode layer 101 is located over the first pixel electrode layer 110, and the pattern of the strip-like pixel electrodes 101a of the second pixel electrode layer 101 overlap up-and-down with the pattern of the first pixel electrode layer 110.

[0033] In the embodiment, an alignment layer located on the array substrate is, for example, rubbed in a horizontal direction as shown in FIG. 3, so that the initial orientation of liquid crystals is horizontal. A plurality of strip-like pixel electrodes 101a each are parallel to each other, the gate lines 102 are parallel to the strip-like pixel electrodes 101a, the direction of the data lines 103 is perpendicular to the initial orientation of liquid crystals, and the entire second pixel electrode layer 101 takes the shape of parallelogram. The strip-like pixel electrodes 101a make a tilt angle of 3°~15°, preferably 7°~12°, such as 9°, 10°, with respect to the initial orientation of liquid crystals.

[0034] Such a design makes direction of a disturbed electric field produced by the gate lines 102 consistent with direction of a fringe field for driving the liquid crystals within the pixel units, and meanwhile, pixel-electrode edges close to the gate lines 102 are parallel to the inside strip-like pixel electrodes 101a. This will not cause a phenomenon of orientation disorder of liquid crystals at edges of the pixel units due to influence of disordered electric fields, and will cause no black stripes to occur in the neighborhood of the gate lines 102. Accordingly, a width of a black matrix in a corresponding place on a color filter substrate can be decreased, and aperture ratio and transmittance are enhanced.

[0035] As shown in FIG. 4, it is a TFT array substrate produced by utilizing the TFT pixel structure shown in FIG. 3, and nine sub-pixel structures shown in FIG. 3 are presented in the figure. Along the direction of the initial orientation of liquid crystals (i.e., a horizontal direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are symmetric to each other with respect to a data line interposed therebetween; and along a direction perpendicular to the initial orientation of liquid crystals (i.e., a perpendicular direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are parallel to each other.

Embodiment 2

[0036] As shown in FIG. 5, it differs from Embodiment 1 in that: an alignment layer located on an array substrate is, for example, rubbed in a perpendicular direction as shown in FIG. 5, so that the initial orientation of liquid crystals is a vertical direction, data lines 103 are parallel to strip-like pixel electrodes 101a, the direction of gate lines 102 is perpendicular to the initial orientation of the liquid crystals, and entire second pixel electrode layer 101 takes the shape of parallelogram.

[0037] Such a design makes direction of a disturbed electric field produced by the data lines 103 consistent with direction of a fringe field for driving the liquid crystals within the pixel units, and meanwhile, pixel-electrode edges close to the data lines 103 are parallel to the inside strip-like pixel electrodes 101a. This will not cause a phenomenon of orientation disorder of liquid crystals at edges of the pixel units due to influence of disordered electric fields, and will cause no black stripe to occur in the neighborhood of the data lines 103. Accordingly, a width of a black matrix in a corresponding place on a color filter substrate can be decreased, and aperture ratio and transmittance are enhanced.

[0038] As shown in FIG. 6, it is an array substrate produced by utilizing the TFT pixel structure shown in FIG. 5, and nine sub-pixel structures shown in FIG. 5 are presented in the figure. Along the direction of the initial orientation of liquid crystals (i.e., a perpendicular direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are symmetric to each other with respect to a gate line interposed therebetween; and along a direction perpendicular to the initial orientation of liquid crystals (i.e., a horizontal direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are parallel to each other.

Embodiment 3

[0039] As shown in FIG. 7, it differs from Embodiment 1 in that: in each of sub-pixel units, the plurality of strip-like pixel electrodes 101a on the second pixel electrode layer 101 are divided into two sets which are symmetric to each other with respect to the central line of the sub-pixel unit for example, and respective strip-like pixel electrodes 101a in each of the sets are parallel to each other. Each of the two gate lines 102 surrounding the sub-pixel unit is parallel to the corresponding one of the sets of the strip-like pixel electrodes 101a close to the gate lines in the second pixel electrode layer, so that entire second pixel electrode layer 101 of the sub-pixel unit take the shape of trapezoid.

[0040] In the embodiment, an alignment layer located on an array substrate is, for example, rubbed in a horizontal direction as shown in FIG. 7, so that the initial orientation of liquid crystals is horizontal.

[0041] Such a design makes direction of a disturbed electric field produced by the gate lines 102 consistent with direction of a fringe field for driving the liquid crystals within the pixel units, and meanwhile, pixel-electrode edges close to the gate lines 102 are parallel to the inside strip-like pixel electrodes 101a. This will not cause a phenomenon of orientation disorder of liquid crystals at edges of the pixel units due to influence of disordered electric fields, and will cause no black stripe to occur in the neighborhood of the gate lines 102. Accordingly, width of a black matrix in a corresponding place on a color filter substrate can be decreased, and aperture ratio and transmittance are enhanced. As compared with Embodi-

ments 1 and 2, the strip-like pixel electrodes **101a** are divided into two sets, and an advantage of lower chromatic aberration is provided over one set of strip-like pixel electrodes **101a**.

[0042] As shown in FIG. 8, it is an array substrate produced by utilizing the TFT pixel structure shown in FIG. 7, and nine sub-pixel structures shown in FIG. 7 are shown in the figure. Along the direction of the initial orientation of liquid crystals (i.e., a horizontal direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are symmetric to each other with respect to a data line therebetween; and along a direction perpendicular to the initial orientation of liquid crystals (i.e., a perpendicular direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are parallel to each other.

Embodiment 4

[0043] As shown in FIG. 9, it differs from Embodiment 3 in that: an alignment layer located on an array substrate is, for example, rubbed in a perpendicular direction, so that the initial orientation of liquid crystals is a vertical direction. Data lines **103** are parallel to strip-like pixel electrodes **101a**, and the direction of gate lines **102** is perpendicular to the initial orientation of liquid crystals. Because two sets of the strip-like pixel electrodes **101a** are distributed symmetrically with respect to the central line of a sub-pixel unit in the perpendicular direction, the portions of two data lines **103** surrounding the sub-pixel unit on two sides, which correspond to the sub-pixel unit, are bent to be two sections, so that entire second pixel electrode layer **101** of the sub-pixel unit take the shape of hexagon.

[0044] Such a design makes direction of a disturbed electric field produced by the data lines **103** consistent with direction of a fringe field for driving the liquid crystals within the pixel units, and meanwhile, pixel-electrode edges close to the data lines **103** are parallel to the inside strip-like pixel electrodes **101a**. This will not cause a phenomenon of orientation disorder of liquid crystals at edges of the pixel units due to influence of disordered electric fields, and will cause no black stripe to occur in the neighborhood of the data lines **103**. Accordingly, a width of a black matrix in a corresponding place on a color filter substrate can be decreased, and aperture ratio and transmittance are enhanced.

[0045] As shown in FIG. 10, it is an array substrate produced by utilizing the TFT pixel structure shown in FIG. 9, and nine sub-pixel structures shown in FIG. 9 are shown in the figure. Along the direction of the initial orientation of liquid crystals (i.e., a perpendicular direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are symmetric to each other with respect to a gate line therebetween; and along a direction perpendicular to the initial orientation of liquid crystals (i.e., a horizontal direction in the figure), the strip-like pixel electrodes in two adjoining sub-pixel structures are parallel to each other.

Embodiment 5

[0046] According to the invention, there is further provided a display device, such as a liquid crystal panel, a liquid crystal television, a cell phone, a liquid crystal display, a digital photo frame, and so on, which further comprises an opposed substrate. An example of the opposed substrate is a color filter substrate, and color-filter sub-pixel units, which are useful for pixel points for displaying colors (such as red, green and blue), are formed on the color filter substrate in correspon-

dence to sub-pixel units on an array substrate. However, some display devices, such as electronic paper display devices, do not need a color filter substrate besides an array substrate, and the opposed substrate is for example a transparent glass or plastic substrate.

[0047] The array substrate in these display devices is any one of the TFT array substrates in the foregoing Embodiments 1~4.

[0048] Various modifications and variances can also be made by those ordinarily skilled in the related technical field without departing from the spirit and scope of the present invention, and thus all the equivalent technical solutions also come within the scope of the present invention. The patent protection scope of the present invention shall be defined by the following claims.

1. A thin film transistor (TFT) array substrate, comprising: a gate line and a data line, which are formed on a substrate, and a sub-pixel unit defined by intersecting of the gate line and the data line, wherein the sub-pixel unit comprises a thin film transistor device, a common electrode, a first pixel electrode layer and a second pixel electrode layer; wherein one of the first pixel electrode layer and the second pixel electrode layer is connected to the common electrode, the other one of the pixel electrode layers is connected to a source electrode or a drain electrode of the thin film transistor, and the first pixel electrode layer and the second pixel electrode layer are separated by an insulating layer; the second pixel electrode layer is located over the first pixel electrode layer, and the pattern of strip-like pixel electrodes of the second pixel electrode layer overlap up-and-down with the pattern of the first pixel electrode layer; and the strip-like pixel electrodes make a tilt angle with an initial orientation of liquid crystals, and a gate line or a data line is parallel to the strip-like pixel electrodes close to the gate line or the data line.
2. The TFT array substrate claimed as claim 1, wherein the tilt angle is $3^{\circ}\sim 15^{\circ}$.
3. The TFT array substrate claimed as claim 2, wherein the tilt angle is $7^{\circ}\sim 12^{\circ}$.
4. The TFT array substrate claimed as claim 1, wherein the strip-like pixel electrodes of the second pixel electrode layer are parallel to each other.
5. The TFT array substrate claimed as claim 4, wherein the gate line is parallel to the strip-like pixel electrodes of the second pixel electrode layer, and the data line is perpendicular to the initial orientation of liquid crystals.
6. The TFT array substrate claimed as claim 4, wherein the data line is parallel to the strip-like pixel electrodes of the second pixel electrode layer, and the gate line is perpendicular to the initial orientation of liquid crystals.
7. The TFT array substrate claimed as claim 1, wherein the strip-like pixel electrodes of the second pixel electrode layer are divided into two sets which are symmetric to each other.
8. The TFT array substrate claimed as claim 7, wherein the gate line is parallel to one of the sets of the strip-like pixel electrodes in the second pixel electrode layer, which are close to the gate line, and the data line is perpendicular to the initial orientation of liquid crystals.
9. The TFT array substrate claimed as claim 7, wherein a first part of the data line is parallel to one set of the strip-like pixel electrodes in the second pixel electrode layer, which is

close to the first part, a second part of the data lines are parallel to the other set of the strip-like pixel electrodes in the second pixel electrode layer, which is close to the second part, and the gate line is perpendicular to the initial orientation of liquid crystals.

10. The TFT array substrate claimed as claim **1**, comprising a plurality of gate lines, a plurality of data lines, and a plurality of sub-pixels defined by intersecting of the plurality of gate lines and the plurality of data lines, wherein along the direction of the initial orientation of liquid crystals, the strip-like pixel electrodes in two adjoining sub-pixel units are symmetric to each other with respect to the gate line or the data line interposed therebetween, and along a direction perpendicular to the initial orientation of liquid crystals, the strip-like pixel electrodes in two adjoining sub-pixel units are parallel to each other.

11. The TFT array substrate claimed as claim **1**, wherein the first pixel electrode layer comprises a plate-like electrode.

12. A display device, comprising the TFT array substrate claimed in claim **1**.

* * * * *

专利名称(译)	TFT阵列基板和显示装置		
公开(公告)号	US20130120680A1	公开(公告)日	2013-05-16
申请号	US13/704684	申请日	2012-11-08
[标]申请(专利权)人(译)	太阳荣格		
申请(专利权)人(译)	SUN , RONGGE		
当前申请(专利权)人(译)	京东方科技集团股份有限公司. 合肥新盛光电科技有限公司.		
[标]发明人	SUN RONGGE		
发明人	SUN, RONGGE		
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其他公开文献	US9557620		
外部链接	Espacenet USPTO		

摘要(译)

根据本发明的一个实施例，公开了一种薄膜晶体管（TFT）阵列基板，包括子像素单元，子像素单元包括薄膜晶体管器件，公共电极，第一像素电极层和第二像素电极层；第一像素电极层和第二像素电极层中的一个连接到公共电极，另一个连接到薄膜晶体管的源电极或漏电极，并且第一和第二像素电极层通过绝缘层；第二像素电极层位于第一像素电极层上方；条状像素电极与液晶的初始取向形成倾斜角，栅极线或数据线与靠近自身的条状像素电极平行。根据该实施例，由于无序电场的影响，在像素的边缘处不会发生液晶取向紊乱的现象。

