

10

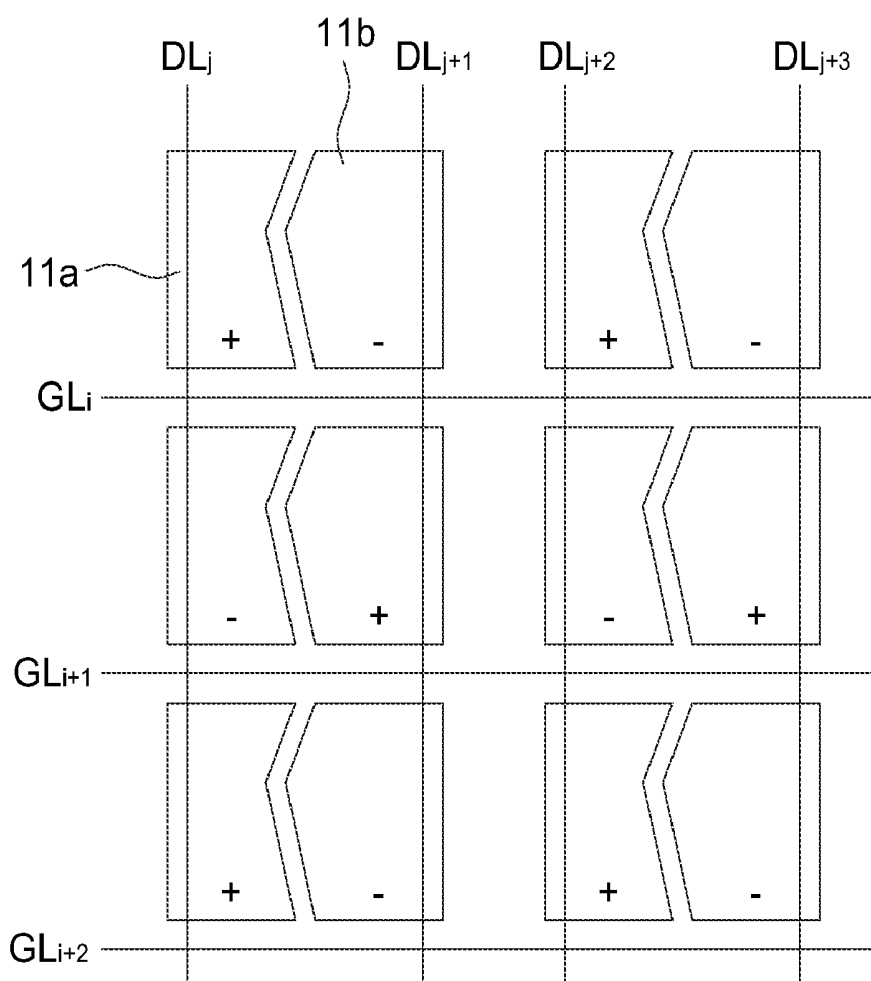


FIG. 1 (Related Art)

20

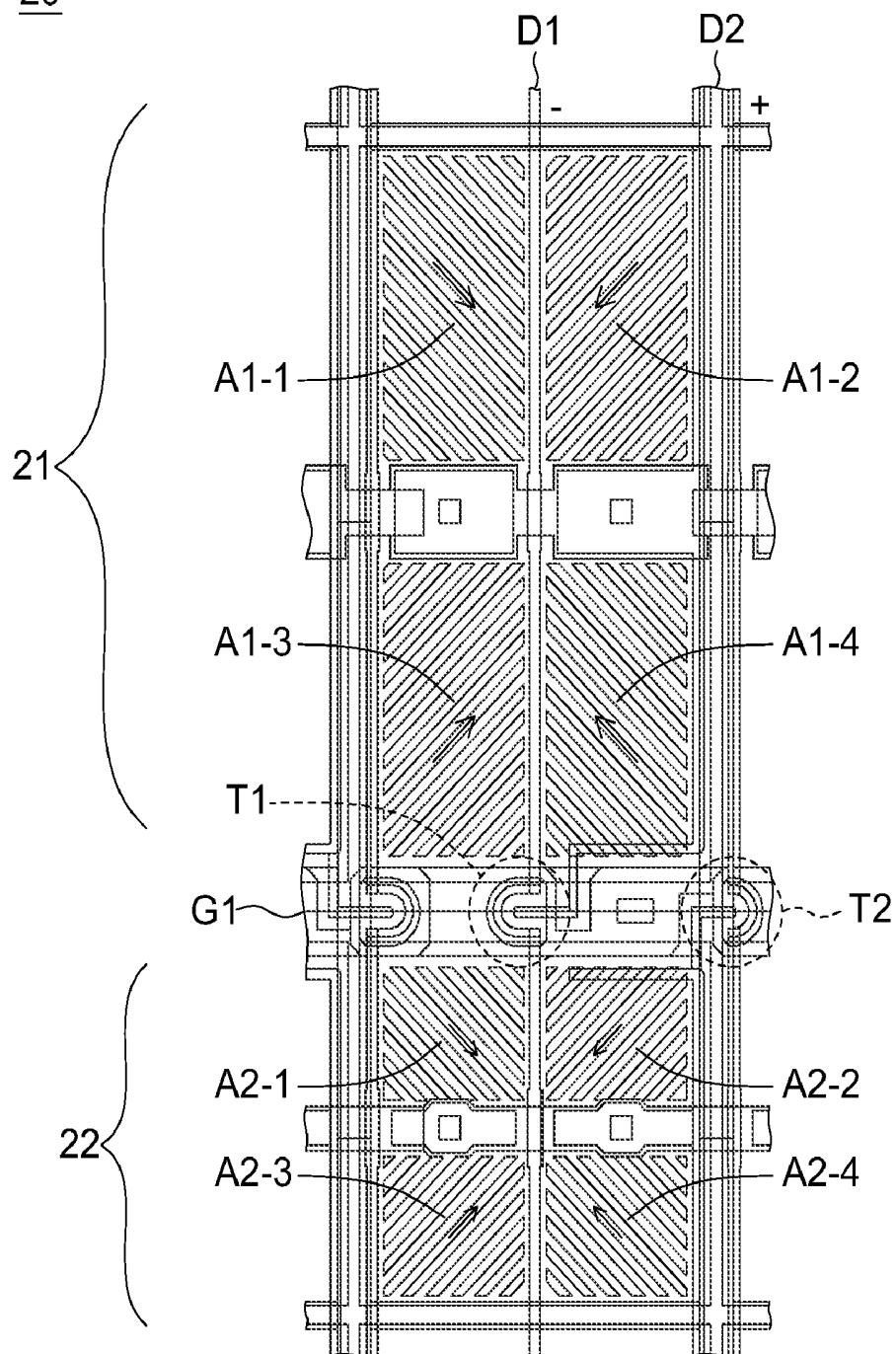


FIG. 2

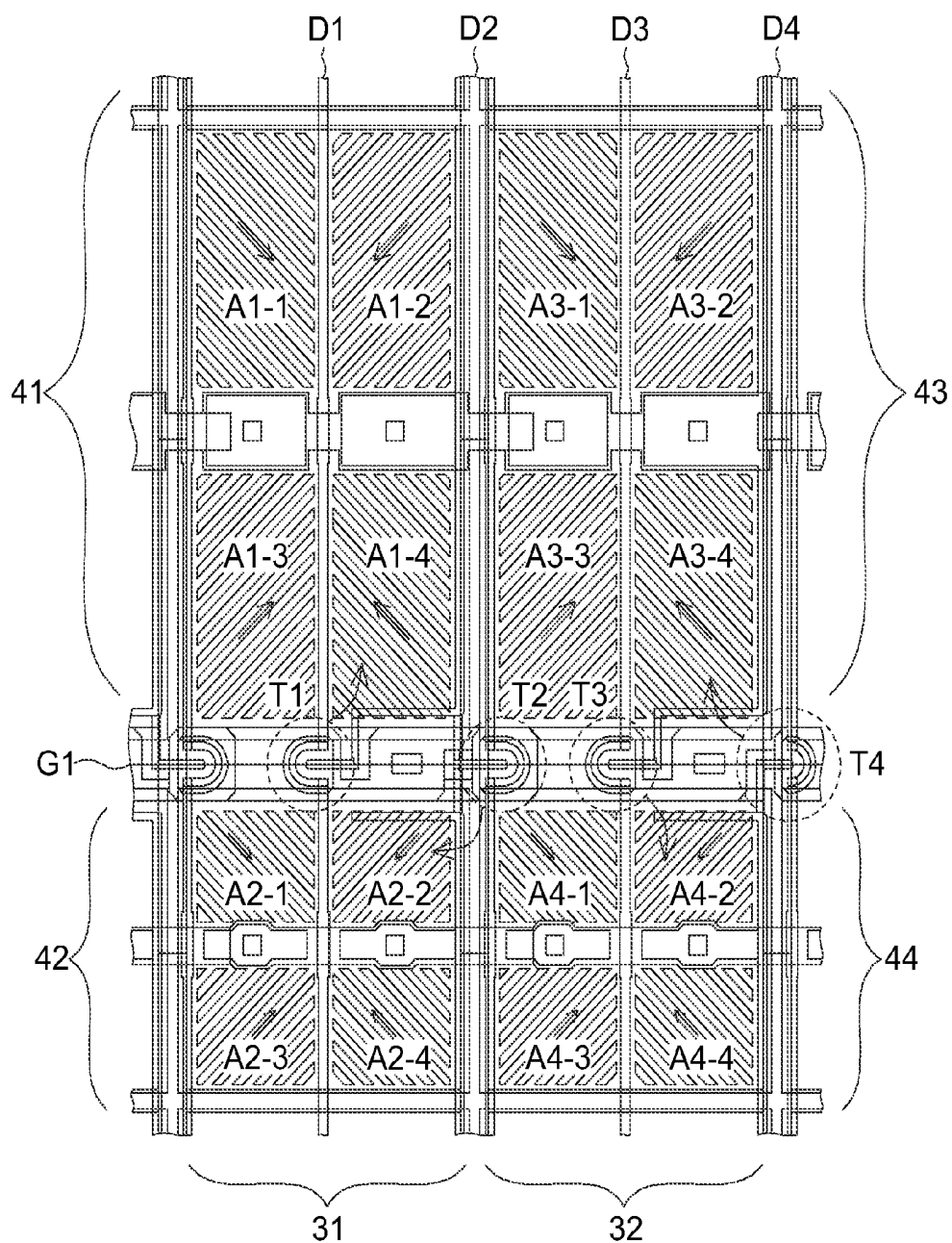


FIG. 3

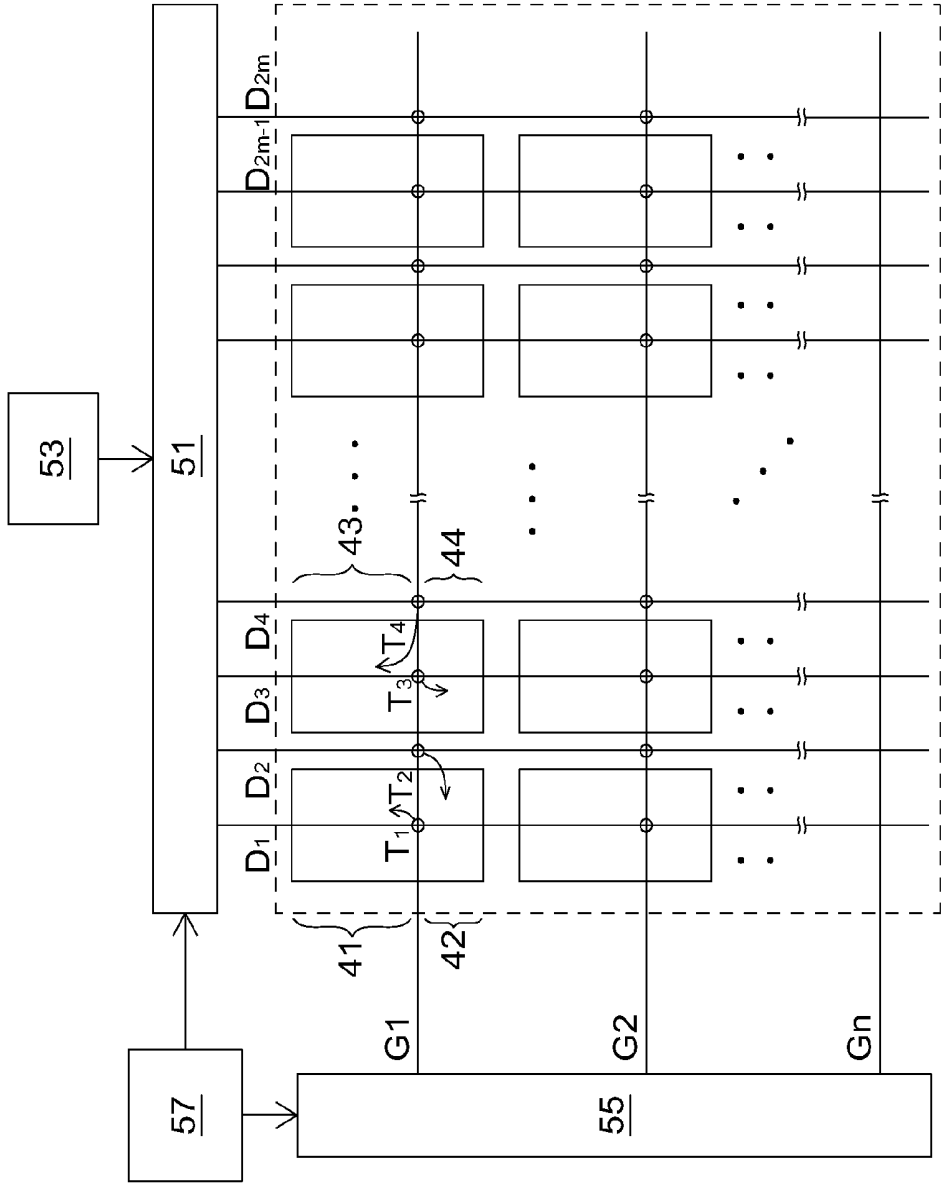


FIG. 4

LIQUID CRYSTAL DISPLAY ELEMENT AND PIXEL STRUCTURE

[0001] This application is a divisional of co-pending U.S. patent application Ser. No. 12/213,252, filed Jun. 17, 2008 and entitled "LIQUID CRYSTAL DISPLAY ELEMENT AND PIXEL STRUCTURE", now allowed. The prior application Ser. No. 12/213,252 claims the benefit of Taiwan application Serial No. 96145132, filed Nov. 28, 2007, the subject matter of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The invention relates in general to a pixel structure of liquid crystal display element, and more particularly to a pixel structure of a liquid crystal display element capable of reducing vertical crosstalk effect and having high transmittance.

[0004] 2. Description of the Related Art

[0005] Along with the rapid growth in the demand for portable products such as personal digital assistant (PDA), cellular phone, projector and large-sized projection TV, the demand for liquid crystal display (LCD) also grows, and consumers are requesting perfect display quality of the portable products. And how to improve product yield rate and make the quality meet consumers' request has become an essential factor in the design of display elements to manufacturers of LCD elements.

[0006] FIG. 1 is a diagram of a conventional pixel design of liquid crystal display element. In the design of the pixel of liquid crystal display element of FIG. 1, the data lines originally disposed at two sides of the pixel region are shifted to be at the inner side of each pixel region and under the transparent electrode (ITO). That is, the data lines are disposed within the transmitting area so as to achieve the effect of dot conversion.

[0007] Referring to FIG. 1. The liquid crystal display element 10 includes a plurality of gate lines $GL_i, GL_{i+1}, GL_{i+2}, \dots$ and data lines $DL_j, DL_{j+1}, DL_{j+2}, DL_{j+3}, \dots$, wherein i is a positive integer, j is a positive integer, the gate lines and the data lines are substantially criss-crossed in a matrix to define a plurality of pixel areas, and each pixel area includes a left sub-pixel area 11a and a right sub-pixel area 11b. The data lines are respectively disposed at the inner side of the left sub-pixel area 11a and the right sub-pixel area 11b of each pixel area and positioned under the transparent electrode (ITO). When the pixel areas of the liquid crystal display element 10 are driven, if the polarity of respective data voltage inputted to the data lines $DL_j, DL_{j+1}, DL_{j+2}, DL_{j+3}, \dots$ (j is a positive integer) is in the sequence of $+, -, +, -, +, -, \dots$, then voltages of opposite polarities are inputted to the left sub-pixel area 11a and the right sub-pixel area 11b in each pixel area.

[0008] However, there are many defects in the design of pixels as indicated in FIG. 1. When the data lines DL_j, DL_{j+1} provide a signal to the pixel area disposed between the data lines DL_j and DL_{j+1} and above the gate line GL_j , the adjacent pixel area next to it is not driven. Due to the capacitance coupling effect between the data lines and the transparent electrode, the pixel area that is not driven originally will be affected by the driving of neighboring pixel area and result in the problem of vertical crosstalk. Moreover, the design of disposing the data lines within the transmitting area will affect the aperture rate and decrease the transmittance.

[0009] Therefore, how to manufacture a high quality liquid crystal display element capable of reducing vertical crosstalk, maintaining pixel transmittance, preventing the display element from short-circuiting (for example, the metal lines will

be short-circuited if the data lines are too close in the manufacturing process), and improving the yield rate of manufacturing process has become a focus of considerations in the research and development.

SUMMARY OF THE INVENTION

[0010] The invention is directed to a liquid crystal display element capable of reducing vertical crosstalk of pixels and maintaining pixel transmittance and symmetry of view angle so that the manufactured element has high quality, the manufacturing process is free of metal line short-circuiting and has high yield rate due to the pixel design.

[0011] According to a first aspect of the present invention, a liquid crystal display element including a plurality of gate lines and data lines is provided. The gate lines and the data lines are substantially criss-crossed in a matrix to define a plurality of pixel areas, and each pixel area includes a first sub-pixel area and a second sub-pixel area.

[0012] The liquid crystal display element includes a first sub-pixel electrode and a second sub-pixel electrode, wherein each of the first sub-pixel electrode and the second sub-pixel electrode at least include two display domains at the left and the right.

[0013] The first data line is disposed at the interface between the two display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line is disposed at the edges of the pixel area.

[0014] The gate line is disposed between the second sub-pixel area and the first sub-pixel area. The liquid crystal display element includes a first transistor and a second transistor, wherein the first sub-pixel electrode and the second sub-pixel electrode are respectively controlled by the first data line and the second data line through the first transistor and the second transistor.

[0015] According to a second aspect of the present invention, a liquid crystal display element including at least two pixel areas is provided. The pixel areas is defined by a plurality of the gate lines and the data lines which are substantially criss-crossed in a matrix. Two pixel elements including a first pixel element and a second pixel element are respectively disposed in a first pixel area and a second pixel area, wherein the first pixel area includes a first sub-pixel area and a second sub-pixel area, and the second pixel area includes a third sub-pixel area and a fourth sub-pixel area.

[0016] The first pixel area includes a first sub-pixel area and a second sub-pixel area, and a first data line, a second data line and a gate line are disposed adjacently.

[0017] The first pixel element includes a first sub-pixel electrode and a second sub-pixel electrode respectively disposed in the first sub-pixel area and the second sub-pixel, wherein each of the first sub-pixel electrode and the second sub-pixel electrode at least includes two display domains at the left and the right.

[0018] The first data line is disposed at the interface between the two display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line is disposed at the edges of the first pixel area.

[0019] The gate line is disposed between the second sub-pixel electrode and the first sub-pixel electrode, and the first pixel element includes a first transistor and a second transistor, wherein the first sub-pixel electrode and the second sub-pixel electrode are respectively controlled by the first data line and the second data line through the first transistor and the second transistor.

[0020] The second pixel area includes a third sub-pixel area and a fourth sub-pixel area, and a third data line, a fourth data line and the gate line are disposed adjacently.

[0021] The second pixel element includes a third sub-pixel electrode and a fourth sub-pixel electrode respectively disposed in the third sub-pixel electrode and the fourth sub-pixel electrode, wherein each of the third sub-pixel electrode and the fourth sub-pixel electrode includes two display domains at the left and the right.

[0022] The third data line is disposed at the interface between the two display domains of the third sub-pixel electrode and the fourth sub-pixel electrode, and the fourth data line is disposed at the edges of the second pixel area.

[0023] The gate line is disposed between the third sub-pixel electrode and the fourth sub-pixel electrode, and the second pixel element includes a third transistor and a fourth transistor, wherein the fourth sub-pixel electrode and the third sub-pixel electrode are respectively controlled by the third data line and the fourth data line through the third transistor and the fourth transistor.

[0024] According to a third aspect of the present invention, a pixel structure of liquid crystal display including a first sub-pixel electrode and a second sub-pixel electrode, a first data line and a second data line, a gate line, and a first transistor and a second transistor is provided.

[0025] The first sub-pixel electrode and the second sub-pixel electrode are respectively disposed in a first sub-pixel area and a second sub-pixel area neighboring the first sub-pixel area, wherein each of the first sub-pixel electrode and the second sub-pixel electrode respectively includes two display domains at the left and the right.

[0026] The first data line is disposed under the interface between two display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line is disposed under the edges of the first sub-pixel electrode and the second sub-pixel electrode.

[0027] The gate line is disposed between the second sub-pixel area and the first sub-pixel area.

[0028] The first sub-pixel electrode is controlled by the gate line and the first data line through the first transistor, and the second sub-pixel electrode is controlled by the gate line and the second data line through the second transistor.

[0029] The invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. 1 is a diagram of a conventional pixel design of liquid crystal display element;

[0031] FIG. 2 is a structural diagram of a single pixel area according to a first embodiment of the present invention;

[0032] FIG. 3 is a structural diagram of two pixel areas according to a second embodiment of the present invention; and

[0033] FIG. 4 is a design diagram of a liquid crystal display of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0034] The invention provides a pixel structure of liquid crystal display element capable of reducing vertical crosstalk effect. A single pixel area is divided into two sub-pixel areas at the top and the bottom, and each of the two sub-pixel areas includes two display domains at the left and the right. The data line is disposed at the interface between the left display domain and the right display domain and positioned under the transparent electrode (ITO).

[0035] According to an embodiment of the invention, a single pixel area is divided into at least a first sub-pixel area

and a second sub-pixel area. The display element includes a first sub-pixel electrode and a second sub-pixel electrode respectively disposed in the first sub-pixel area and the second sub-pixel area, and each of the first sub-pixel electrode and the second sub-pixel electrode includes two display domains at the left and the right. The liquid crystal molecules in the display domain tilt in different directions and degrees (that is, a single pixel area at least includes four liquid crystal display domains with different tilting directions). In each pixel area, the first data line is disposed at the interface between two display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line is disposed at the edges of the pixel area. The gate line substantially criss-crossed with the first and the second data lines is disposed between the first sub-pixel area and the second sub-pixel area. The display element includes a first transistor and a second transistor. The first sub-pixel electrode and the second sub-pixel electrode are respectively controlled by the first data line and the second data line through the first transistor and the second transistor.

[0036] The invention is exemplified by a first embodiment and a second embodiment. In the two embodiments, each single pixel area includes eight display domains whose liquid crystal molecules are tilting at different directions. The first embodiment discloses the structure of a single pixel area, and the second embodiment discloses a pixel driving method of the invention. However, the embodiments disclosed herein are used for illustrating the present invention, but not for limiting the scope of the present invention. Besides, the drawings used for illustrating the embodiment and applications of the present invention only show the characteristic parts to avoid obscuring the invention.

First Embodiment

[0037] FIG. 2 is a structural diagram of a single pixel area according to a first embodiment of the present invention. As indicated in FIG. 2, the liquid crystal display element 20 includes a first data line D_1 , a second data line D_2 and a gate line G_1 substantially criss-crossed with the first data line D_1 and the second data line D_2 . Each pixel area includes a first sub-pixel area 21 and a second sub-pixel area 22 neighboring the first sub-pixel area 21, wherein the first sub-pixel electrode and the second sub-pixel electrode are respectively disposed in the first sub-pixel area 21 and the second sub-pixel area 22. The first sub-pixel electrode in the first sub-pixel area 21 and the second sub-pixel electrode in the second sub-pixel area 22 respectively correspond to four display domains. In the present embodiment of the invention, the area of the first sub-pixel area 21 is larger than that of the second sub-pixel area 22.

[0038] The first data line D_1 is disposed at the interface between the left and the right display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line D_2 is disposed under the edges of the first sub-pixel electrode and the second sub-pixel electrode.

[0039] The gate line G_1 disposed between the second sub-pixel area 22 and the first sub-pixel area 21. A first transistor T1 and a second transistor T2, wherein the first sub-pixel electrode and the second sub-pixel electrode are respectively controlled by the first data line D_1 and the second data line D_2 through the first transistor T1 and the second transistor T2.

[0040] Referring to FIG. 2. In the first sub-pixel area 21, the first display domain A1-1 and the third display domain A1-3 of the first sub-pixel electrode are disposed at the left of the first data line D_1 , the second display domain A1-2 and the fourth display domain A1-4 are disposed at the right of the first data line D_1 . The first data line D_1 is disposed at the

interface between the first display domain A1-1 and the second display domain A1-2 and also disposed at the interface between the third display domain A1-3 and the fourth display domain A1-4.

[0041] Likewise, in the second sub-pixel area 22, the first display domain A2-1 and the third display domain A2-3 of the first sub-pixel electrode are disposed at the left of the first data line D_1 , the second display domain A2-2 and the fourth display domain A2-4 are disposed at the right of the first data line D_1 . The first data line D_1 is disposed at the interface between the first display domain A2-1 and the second display domain A2-2 and also disposed at the interface between the third display domain A2-3 and the fourth display domain A2-4.

[0042] Moreover, the first sub-pixel electrode and the second sub-pixel electrode correspondingly control the tilting directions of the liquid crystal molecules in the eight display domains which form a contained angle with the first data line D_1 . For example, a contained angle of 45 degrees is formed.

[0043] When a single pixel electrode of FIG. 2 is driven, the first display domain A1-1, the second display domain A1-2, the third display domain A1-3, and the fourth display domain A1-4 of the first sub-pixel electrode are controlled by the first data line D_1 through the first transistor T1, and the first display domain A2-1, the second display domain A2-2, the third display domain A2-3, the fourth display domain A2-4 of the second sub-pixel electrode are controlled by the second data line D_2 through the second transistor T2.

[0044] When the display element is driven, the first sub-pixel electrode and the second sub-pixel electrode of the single pixel area could be driven by the first voltage and the second voltage of opposite polarities (such as the -polarity and the +polarity respectively), so that the four display domains in the first sub-pixel area 21 and the four display domains in the second sub-pixel area 22 would have opposite polarities. In practical application, the second voltage could be larger than the first voltage.

[0045] In the first embodiment of the invention, the first data line D_1 is disposed at the center of the transmitting area of the pixel. As such location having poor transmittance is exactly the interface between the display domains, the overall transmittance of the pixel and the symmetry of the display domain will not be significantly affected. Moreover, the second data line D_2 is disposed at the edge of the transmitting area of a neighboring pixel, so the overall transmittance and the symmetry of the display domain of the neighboring pixel either will not be significantly affected.

[0046] In practical application, when the panel is displaying uniform signals, the first data line D_1 and the second data line D_2 covered by the pixel electrodes can carry signals of opposite polarities but with the same amplitude, so the capacitance coupling between the first data line D_1 and the second data line D_2 and the pixel electrode will be offset, hence avoiding vertical crosstalk. Moreover, in the design of the pixel structure, there is still a certain distance between the first data line D_1 and the second data line D_2 , hence avoiding neighboring data lines being short-circuited.

Second Embodiment

[0047] In the second embodiment, it is exemplified by taking two neighboring pixel areas as a unit for constructing a display element. To drive the display element can be viewed as to operate pixel elements in these pixel areas. The structure and the operation of a pixel element are illustrated in details as below. Noted that the second embodiment is for illustrating one of the methods of driving the pixel elements of the invention not for limiting the scope of protection of the invention.

[0048] FIG. 3 is a structural diagram of two pixel areas according to a second embodiment of the present invention. The pixel elements are disposed in two neighboring pixel areas. As indicated in FIG. 3, a first pixel element and a second pixel element of the liquid crystal display element 30 are respectively disposed in a first pixel area 31 and a second pixel area 32, wherein the first pixel area 31 includes a first sub-pixel area 41 and a second sub-pixel area 42, and the second pixel area 32 includes a third sub-pixel area 43 and a fourth sub-pixel area 44.

[0049] In practical application, the area of the first sub-pixel area 41 is larger than that of the second sub-pixel area 42, and the area of the third sub-pixel area 43 is larger than that of the fourth sub-pixel area 44. The area of the first sub-pixel area 41 of the first pixel area 31 is substantially equal to that of the third sub-pixel area 43 of the second pixel area 32, and the area of the second sub-pixel area 42 of the first pixel area 31 is substantially equal to that of the fourth sub-pixel area 44 of the second pixel area 32.

[0050] <The Structure of the First Pixel Area 31>

[0051] The first pixel area 31 includes a first sub-pixel area 41 and a second sub-pixel area 42, wherein the first pixel element includes a first sub-pixel electrode and a second sub-pixel electrode. The first sub-pixel electrode in the first sub-pixel area 41 and the second sub-pixel electrode in the second sub-pixel area 42 respectively correspond to four display domains. In the first pixel area 31, the first data line D_1 and the second data line D_2 are substantially criss-crossed with the gate line G_1 . The first data line D_1 is disposed at the interface between the left and the right display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line D_2 is disposed at the edges of the first sub-pixel electrode and the second sub-pixel electrode.

[0052] The first sub-pixel area 41 of the first pixel area 31 has four display domains, including the first display domain A1-1 and the third display domain A1-3 both disposed at the left of the first data line D_1 , and the second display domain A1-2 and the fourth display domain A1-4 both disposed at the right of the first data line D_1 . The first data line D_1 is disposed at the interface between the first display domain A1-1 and the second display domain A1-2, and also disposed at the interface between the third display domain A1-3 and the fourth display domain A1-4.

[0053] Likewise, in the second sub-pixel area 42 of the first pixel area 31, the second sub-pixel electrode has four display domains including the first display domain A2-1 and the third display domain A2-3 both disposed at the left of the first data line D_1 , and the second display domain A2-2 and the fourth display domain A2-4 both disposed at the right of the first data line D_1 . The first data line D_1 is disposed at the interface between the first display domain A2-1 and the second display domain A2-2, and also at the interface between the third display domain A2-3 and the fourth display domain A2-4.

[0054] For the first pixel area 31, the gate line G_1 is disposed between the first sub-pixel area 41 and the second sub-pixel area 42, and the first pixel element includes a first transistor T1 and a second transistor T2. The four display domains of the first sub-pixel electrode and the four display domains of the second sub-pixel electrode are respectively controlled by the first data line D_1 and the second data line D_2 through the first transistor T1 and the second transistor T2.

[0055] Moreover, the tilting directions of the liquid crystal molecules in the eight display domains of the first sub-pixel electrode and the second sub-pixel electrode are correspondingly controlled to form a contained angle with the first data line D_1 . Examples of the contained angles include about 45 degrees as shown in FIG. 3.

[0056] <The Structure of the Second Pixel Area 32>

[0057] The second pixel area 32 includes a third sub-pixel area 43 and a fourth sub-pixel area 44, wherein the second pixel element includes a third sub-pixel electrode and a fourth sub-pixel electrode. The third sub-pixel electrode in the third sub-pixel area 43 and the fourth sub-pixel electrode in the fourth sub-pixel area 44 respectively correspond to four display domains. In the second pixel area 32, the third data line D_3 and the fourth data line D_4 are substantially criss-crossed with the gate line G_1 . The third data line D_3 is disposed at the interface between the left and the right display domains of the third sub-pixel electrode and the fourth sub-pixel electrode, and the fourth data line D_4 is disposed under the edges of the third sub-pixel electrode and the fourth sub-pixel electrode.

[0058] The third sub-pixel area 43 of the second pixel area 32 has four display domains including the first display domain A3-1 and the third display domain A3-3 both disposed at the left of the third data line D_3 , and the second display domain A3-2 and the fourth display domain A3-4 both disposed at the right of the third data line D_3 . The third data line D_3 is disposed at the interface between the first display domain A3-1 and the second display domain A3-2, and also at the interface between the third display domain A3-3 and the fourth display domain A3-4.

[0059] Likewise, in the fourth sub-pixel area 42 of the second pixel area 32, the second sub-pixel electrode has four display domains including the first display domain A4-1 and the third display domain A4-3 both disposed at the left of the third data line D_3 , and the second display domain A4-2 and the fourth display domain A4-4 both disposed at the right of the third data line D_3 . The third data line D_3 is disposed at the interface between the first display domain A4-1 and the second display domain A4-2, and also at the interface between the third display domain A4-3 and the fourth display domain A4-4.

[0060] For the second pixel area 32, the gate line G_1 is disposed between the third sub-pixel area 43 and the fourth sub-pixel area 44, and the second pixel element includes a third transistor T3 and a fourth transistor T4. The four display domains of the fourth sub-pixel electrode and the four display domains of third sub-pixel electrode are respectively controlled by the third data line D_3 and the fourth data line D_4 through the third transistor T3 and the fourth transistor T4.

[0061] Moreover, the tilting directions of the liquid crystal molecules in the eight display domains of the third sub-pixel electrode and the fourth sub-pixel electrode are correspondingly controlled to form a contained angle with the first data line D_3 . Examples of the contained angles include 45 degrees as shown in FIG. 3.

[0062] <Method of Driving Pixel Element>

[0063] One of the methods of driving the pixel of the invention is disclosed below, but the invention is not limited thereto. Any one who is skilled in the art related to the invention can make necessary adjustments and slight changes to fit actual needs.

[0064] Referring to FIG. 3 and FIG. 4. FIG. 4 is a design diagram of a pixel structure of a liquid crystal display element of the present invention. The liquid crystal display element 50 includes a plurality of gate lines $G_1, G_2, \dots, G_n$ and data lines $D_1, D_2, \dots, D_{2m}$, wherein both n and m are positive integers, and the gate lines $G_1, G_2, \dots, G_n$ are substantially criss-crossed with the data lines $D_1, D_2, \dots, D_{2m}$ in a matrix to define a plurality of pixel areas. Every pixel area is designed for one pixel element. In other words, each block in FIG. 4 denotes one pixel area, every pixel area has one pixel element of FIG. 3, and the entire display element includes a plurality of repeated pixel elements.

[0065] Besides, the data lines $D_1, D_2, D_3, D_4, \dots, D_{2m}$ are coupled to the data driver 51, and the data driver 51 is electrically connected to a voltage supplier 53. The gate lines $G_1, G_2, \dots, G_n$ are coupled to the gate driver 55. The data driver 51 and the gate driver 55 are electrically connected to a signal controller 57 respectively.

[0066] When the display element is driven, the four display domains (A1-1, A1-2, A1-3 and A1-4) of the first sub-pixel area 41 disposed in the upper part of the first pixel area 31 are controlled by the first data line D_1 through the first transistor T1, and the four display domains (A2-1, A2-2, A2-3 and A2-4) of the second sub-pixel area 42 disposed in the lower part of the first pixel area 31 are controlled by the second data line D_2 through the second transistor T2. The four display domains (A3-1, A3-2, A3-3 and A3-4) of the third sub-pixel area 43 disposed in the upper part of the second pixel area 32 are controlled by the fourth data line D_4 through the fourth transistor T4, and the four display domains (A4-1, A4-2, A4-3 and A4-4) of the fourth sub-pixel area 44 disposed in the lower part of the second pixel area 32 are controlled by the third data line D_3 through the third transistor T3.

[0067] When the display element is driven, the first sub-pixel electrode (disposed in the first sub-pixel area 41) and the second sub-pixel electrode (disposed in the second sub-pixel area 42) in the first pixel area 31 of a pixel element of FIG. 3 are respectively driven by a first voltage provided by the first data line D_1 and a second voltage provided by the second data line D_2 .

[0068] The first sub-pixel electrode and the second sub-pixel electrode are respectively driven by a first voltage and a second voltage, wherein the polarity of the first voltage (indicated such as “-” polarity) is opposite to the polarity (indicated such as “+” polarity) of the second voltage. Therefore, the negative polarity (“-” polarity) of the four display domains in the first sub-pixel area 41 is opposite to the positive polarity (“+” polarity) of the four display domains in the second sub-pixel area 42 when the display element is driven to achieve dot conversion. In practical application, the second voltage could be larger than the first voltage.

[0069] The third sub-pixel electrode (disposed in the third sub-pixel area 43) and the fourth sub-pixel electrode (disposed in the fourth sub-pixel area 44) in the second pixel area 32 are respectively driven by a fourth voltage provided by the fourth data line D_4 and a third voltage driven by the third data line D_3 . In practical application, the third voltage could be larger than the fourth voltage.

[0070] The third sub-pixel electrode and the fourth sub-pixel electrode are respectively driven by a third voltage and a fourth voltage, wherein the polarity (such as “-” polarity) of the third voltage is opposite to the polarity (such as “+” polarity) of the fourth voltage. Therefore, the positive polarity (such as +polarity) of the four display domains in the third sub-pixel area 43 is opposite to the negative polarity (such as -polarity) in the four display domains in the fourth sub-pixel area 44 when the display element is driven.

[0071] According to the disclosure in the second embodiment of the invention, the data lines $D_1, D_3, \dots, D_{2m-1}$ are disposed at the center of the transmitting area of the pixel, so the overall transmittance of the pixel and the symmetry of the display domain will not be significantly affected. Moreover, the data lines $D_2, D_4, \dots, D_{2m}$ are disposed at the edges of two neighboring pixel transmitting areas, so the overall transmittance of the neighboring pixel and the symmetry of the display domain will not be significantly affected.

[0072] In practical application, when the panel is displaying uniformed signals, the first data line D_1 and the second data line D_2 are preferably covered by the pixel electrode that

can carry signals of opposite polarities but with the same amplitude, (likewise, the third data line D_3 and the fourth data line D_4 carry signals of opposite polarities but with the same amplitude), so the capacitance coupling between the first data line D_1 and the second data line D_2 and the pixel electrode will be offset and balanced, hence avoiding vertical crosstalk. Moreover, in the design of the pixel, there is still a sufficient distance between the first data line D_1 and the second data line D_2 and between the third data line D_3 and the fourth data line D_4 , hence avoiding neighboring data lines being short-circuited without affecting the yield rate of the display element.

[0073] While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A liquid crystal display element disposed in a pixel area including a first sub-pixel area and a second sub-pixel area, comprising:

a first sub-pixel electrode and a second sub-pixel electrode disposed in the first sub-pixel area and the second sub-pixel area respectively, wherein each of the first sub-pixel electrode and the second sub-pixel electrode at least comprises at least two display domains at the left and the right;

a first data line and a second data line, wherein the first data line is disposed at an interface between the two display domains of the first sub-pixel electrode and the second sub-pixel electrode, and the second data line is disposed at the edges of the pixel area;

a gate line disposed between the second sub-pixel area and the first sub-pixel area; and

a first transistor and a second transistor, wherein the first sub-pixel electrode and the second sub-pixel electrode are respectively controlled by the first data line and the second data line through the first transistor and the second transistor;

wherein the first sub-pixel electrode and the second sub-pixel electrode in the first pixel element are respectively driven by a first voltage provided by the first data line and a second voltage provided by the second data line, and the first voltage and the second voltage have opposite polarities, and

wherein each of the first sub-pixel electrode and the second sub-pixel electrode is coupled with two data lines having opposite polarities.

2. The liquid crystal display element according to claim 1, wherein each two display domains of the first sub-pixel elec-

trode and the second sub-pixel electrode correspondingly control tilting directions of liquid crystal molecules which form a contained angle of about 45 degrees with the first data line.

3. The liquid crystal display element according to claim 1, wherein the first sub-pixel electrode and the second sub-pixel electrode are inputted voltages of opposite polarities.

4. The liquid crystal display element according to claim 1, wherein the first sub-pixel electrode and the second sub-pixel electrode are respectively driven by the first voltage and the second voltage, and the second voltage is larger than the first voltage.

5. The liquid crystal display element according to claim 1, wherein each of the first sub-pixel electrode and the second sub-pixel electrode comprises four display domains including a first display domain, a second display domain, a third display domain, and a fourth display domain.

6. The liquid crystal display element according to claim 5, wherein the first display domain and the third display domain of the first sub-pixel electrode are disposed at the left of the first data line, the second display domain and the fourth display domain of the first sub-pixel electrode are disposed at the right of the first data line, and the first data line is disposed at the interface between the first display domain and the second display domain and also disposed at the interface between the third display domain and the fourth display domain.

7. The liquid crystal display element according to claim 5, wherein the first display domain and the third display domain of the second sub-pixel electrode are disposed at the left of the first data line, the second display domain and the fourth display domain of the second sub-pixel electrode are disposed at the right of the first data line, and the first data line is disposed at the interface between the first display domain and the second display domain and also disposed at the interface between the third display domain and the fourth display domain.

8. The liquid crystal display element according to claim 5, wherein four display domains of the first sub-pixel electrode and the four display domains of the second sub-pixel electrode are respectively inputted voltages of opposite polarities.

9. The liquid crystal display element according to claim 5, wherein the total area of the four display domains of the first sub-pixel electrode is larger than that of the four display domains of the second sub-pixel electrode.

10. The liquid crystal display element according to claim 5, wherein the four display domains of the first sub-pixel electrode and that of the second sub-pixel electrode are respectively driven by the first voltage and the second voltage, and the second voltage is larger than the first voltage.

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[标]申请(专利权)人(译)	苏婷魏 廖培群 侯恐龙		
申请(专利权)人(译)	苏婷伟 廖PEI-CHUN 侯宏隆		
当前申请(专利权)人(译)	苏婷伟 廖PEI-CHUN 侯宏隆		
[标]发明人	SU TING WEI LIAO PEI CHUN HOU HUNG LUNG		
发明人	SU, TING-WEI LIAO, PEI-CHUN HOU, HUNG-LUNG		
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摘要(译)

液晶显示器的像素结构包括第一和第二子像素电极，第一和第二数据线，栅极线，以及第一和第二晶体管。设置在第一和第二子像素区域中的第一和第二子像素电极分别包括左右两个至少两个显示域。第一数据线设置在第一和第二子像素电极中的每一个的两个域之间的界面下方，第二数据线设置在第一和第二子像素电极的边缘下方。栅极线设置在第一和第二子像素区域之间。第一子像素电极由栅极线和第一数据线通过第一晶体管控制。第二子像素电极由栅极线控制，第二数据线通过第二晶体管控制。

