

FIG. 1
Related Art

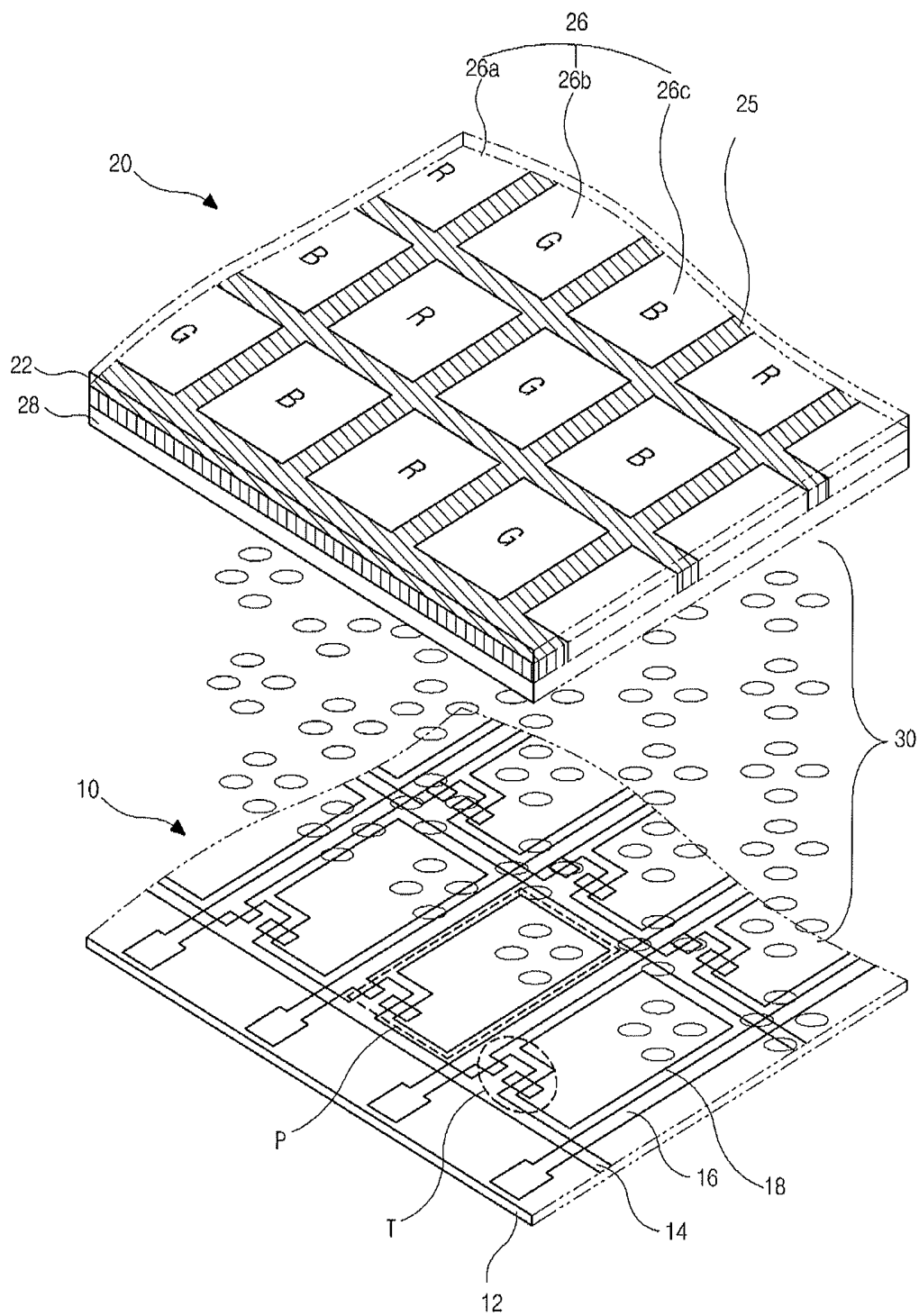


FIG. 2
Related Art

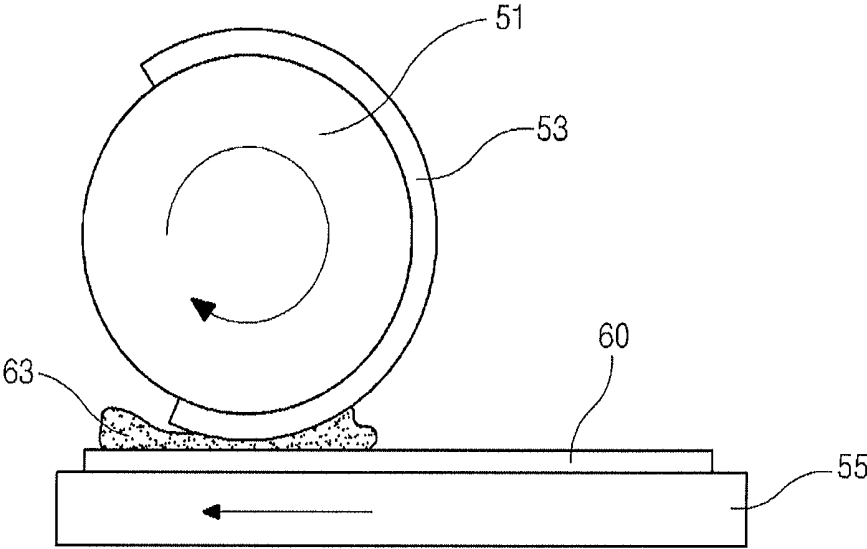


FIG. 3
Related Art

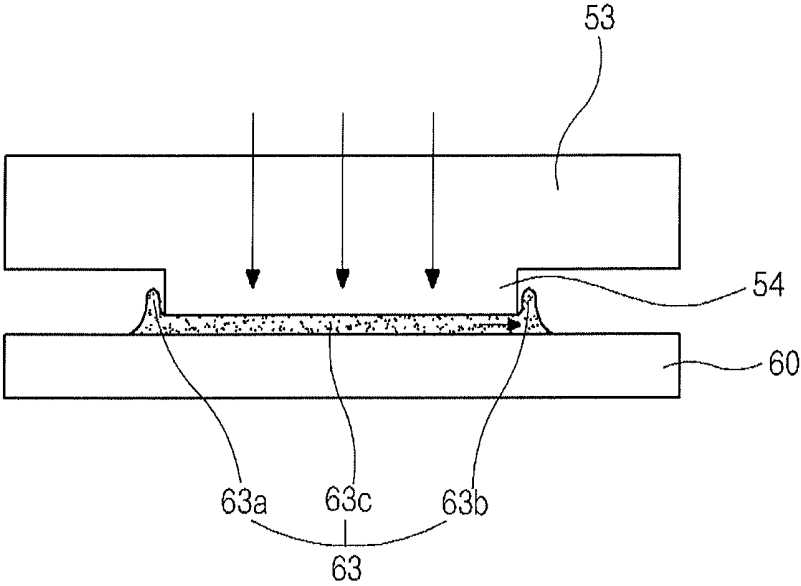


FIG. 4B

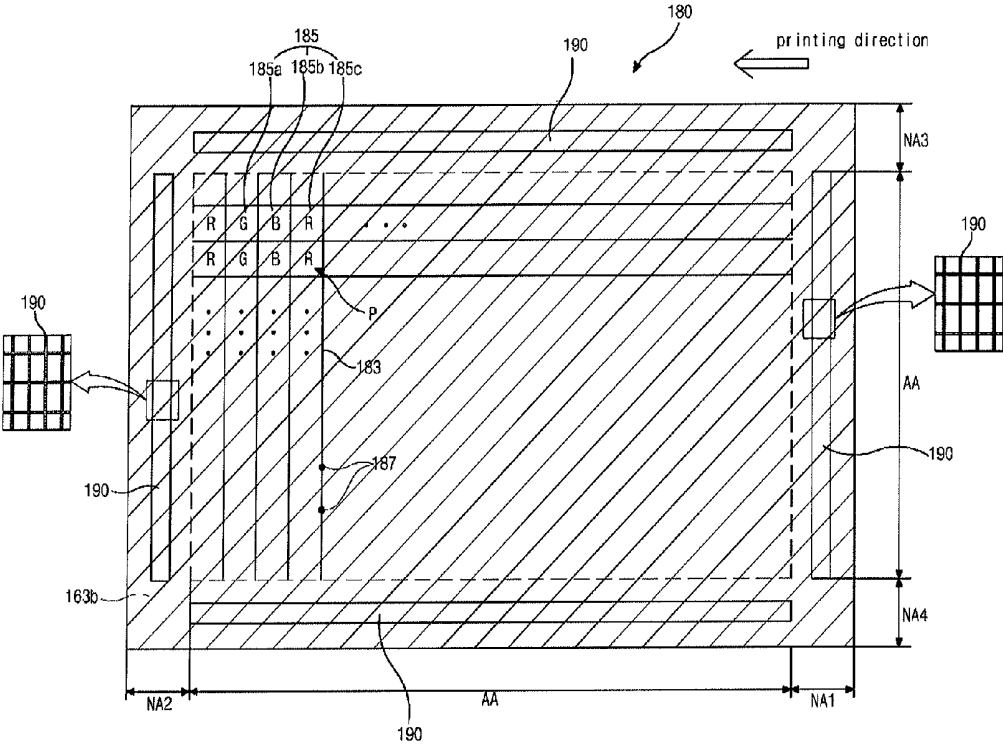
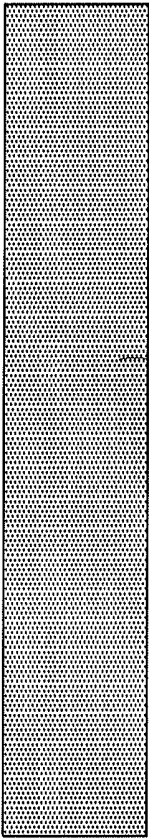


FIG. 5A



170

FIG. 5B

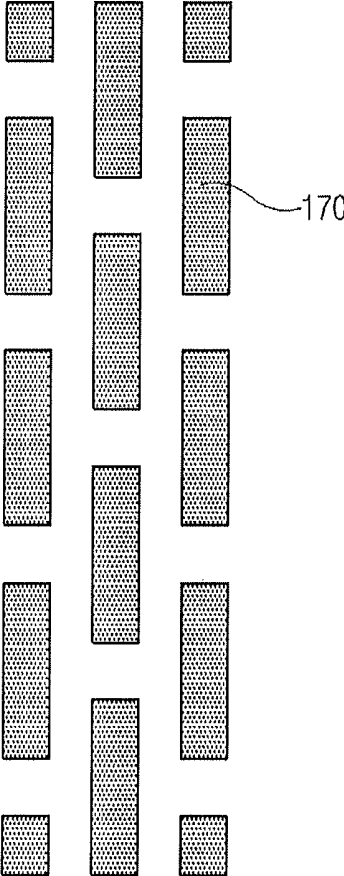


FIG. 5C

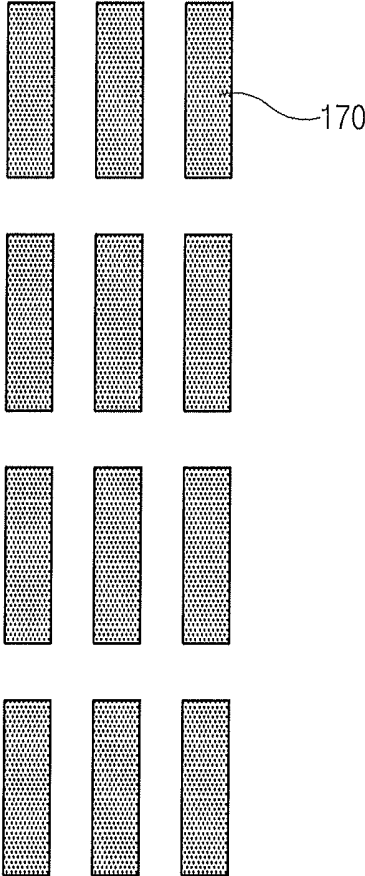


FIG. 5D

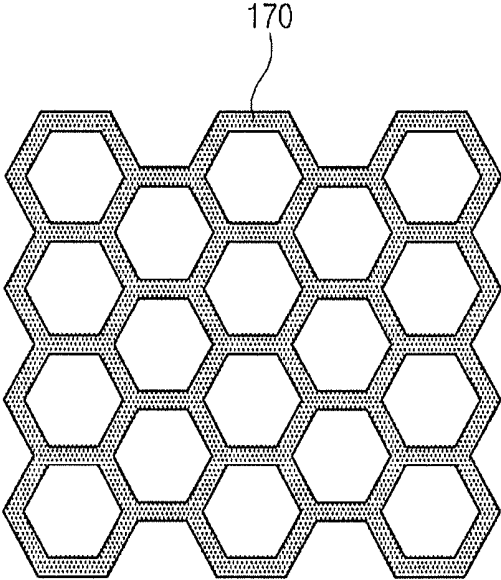


FIG. 5E

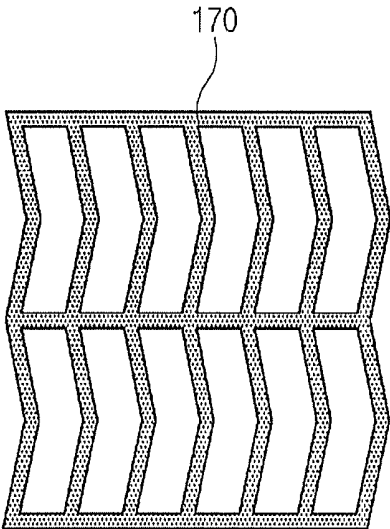


FIG. 5F

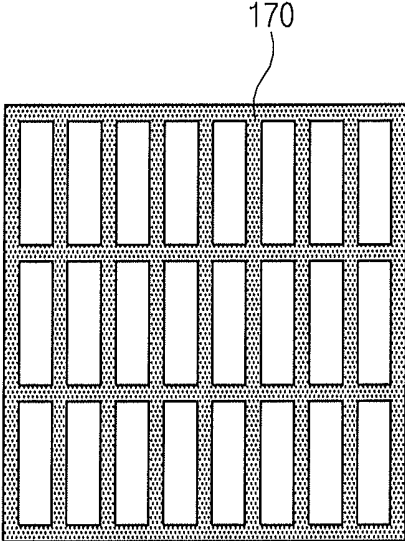


FIG. 5G

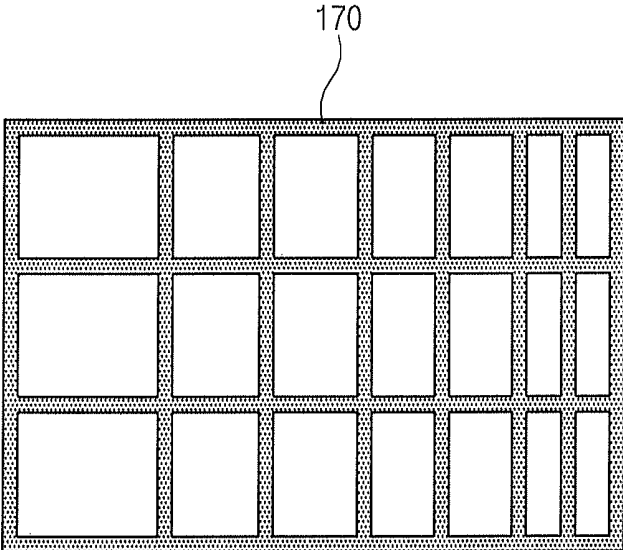


FIG. 6A

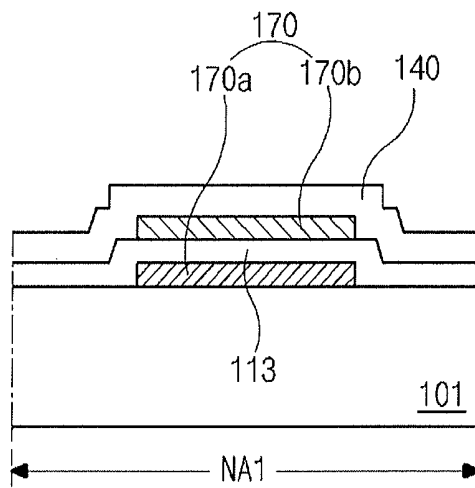


FIG. 6B

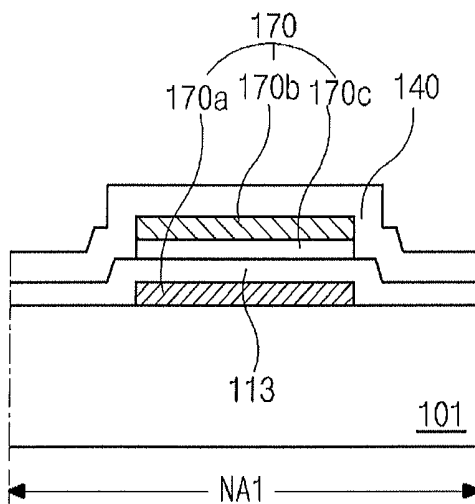


FIG. 6C

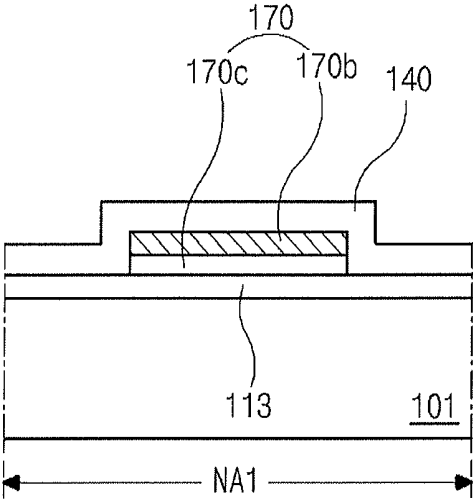


FIG. 6D

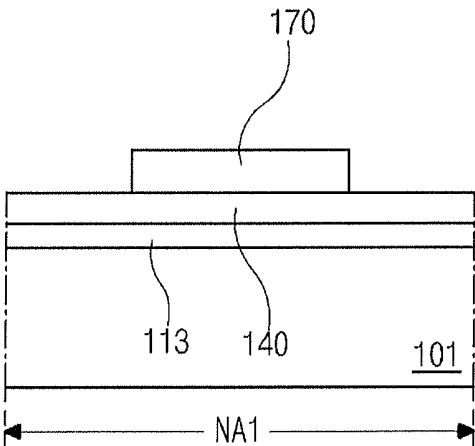


FIG. 7A

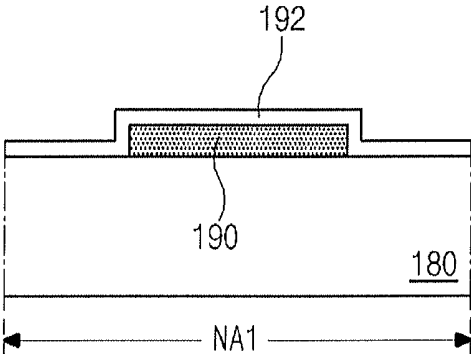
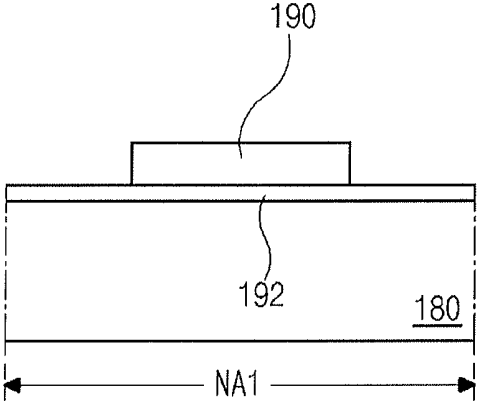


FIG. 7B



SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE INCLUDING THE SAME

This application claims the benefit of Korea Patent Application No. 10-2010-0101313, filed on Oct. 18, 2010, the entire contents of which is incorporated herein by reference for all purposes as if fully set forth herein.

BACKGROUND

1. Field of the Invention

The present disclosure relates to a liquid crystal display device, and more particularly, to a substrate having a means for preventing a mount of an orientation film and a liquid crystal display device including the substrate.

2. Discussion of the Related Art

Recently, a liquid crystal display (LCD) device has been in the spotlight as a next generation display device having high value added because of its low power consumption and good portability.

An active matrix liquid crystal display (AM-LCD) device, which includes thin film transistors as a switching device for a plurality of pixels, has been widely used due to its high resolution and superiority in displaying moving images.

In general, the LCD device is fabricated through an array substrate process for forming a thin film transistor and a pixel electrode on an array substrate, a color filter substrate process for forming a color filter layer and a common electrode on a color filter substrate and a cell process for forming a liquid crystal layer between the array substrate and a color filter substrate.

FIG. 1 is an exploded perspective view showing a liquid crystal display device according to the related art. In FIG. 1, the liquid crystal display (LCD) device includes an array substrate 10, a color filter substrate 20 and a liquid crystal layer 30 between the array substrate 10 and the color filter substrate 20. The array substrate 10 includes a first substrate 12, a gate line 14 on the first substrate 12, a data line 16 crossing the gate line 14 to define a pixel region P, a thin film transistor (TFT) T connected to the gate line 14 and the data line 16 and a pixel electrode 18 connected to the TFT T.

In addition, the color filter substrate 20 facing the array substrate 10 includes a second substrate 22, a black matrix 25 blocking a non-display area corresponding to the gate line 14, the data line 16 and the TFT T, a color filter layer 26 including red, green and blue color filters 26a, 26b and 26c each corresponding to the pixel region P and a common electrode 28 on an entire surface of the second substrate 22.

Although not shown in FIG. 1, a seal pattern may be formed in a boundary portion between the array substrate 10 and the color filter substrate 20 for preventing leakage of the liquid crystal layer 30. A lower orientation film may be formed between the array substrate 10 and the liquid crystal layer 30 and an upper orientation film may be formed between the color filter substrate 20 and the liquid crystal layer 30 for aligning the liquid crystal layer initially. Further, a polarizing plate may be formed on an outer surface of at least one of the first and second substrates 12 and 22.

A backlight unit may be disposed under the array substrate 10 to supply light. When a gate signal turning on the TFT T is sequentially supplied to the gate line 14, the TFT T is turned on and a data signal supplied to the data line 16 is applied to the pixel electrode 18 through the TFT T. As a result, a vertical electric field is generated between the pixel electrode 18 and the common electrode 28 and liquid crystal molecules in the liquid crystal layer 30 are re-aligned by the vertical electric

field, thereby the LCD device displaying images due to transmittance change of the liquid crystal layer 30.

The array substrate 10 is fabricated by forming the gate line 14, the data line 16, the TFT T and the pixel electrode 18 on the first substrate 12 through a depositing step, an exposing step, a developing step and an etching step for a source material. The color filter substrate is fabricated by forming the color filter layer 26 and the common electrode 28 on the second substrate 22. In addition, a liquid crystal panel is fabricated by attaching the array substrate 10 and the color filter substrate 12 with the liquid crystal layer 30 interposed therebetween and the LCD device is completed by attaching a driving circuit to the liquid crystal panel.

Since the LCD device uses an electro-optical effect of the liquid crystal that is determined by anisotropy and arrangement state of the liquid crystal molecules, adjustment of the arrangement state of the liquid crystal molecules influences stabilization in display quality of the LCD device. To obtain a uniform initial arrangement state of the liquid crystal molecules, an orientation process is performed.

In the orientation process, an orientation film is formed on each of the array substrate and the color filter substrate by printing a polymeric material such as polyimide and the orientation film is rubbed with a rubbing cloth along a predetermined direction. As a result, a polymer chain in the orientation film is aligned along the predetermined direction to have a directivity and the liquid crystal molecules have a uniform initial arrangement state due to the orientation film.

When the orientation film is formed to have a non-uniform thickness over a display area in the printing step, the orientation film is deteriorated in the subsequent rubbing step. Accordingly, the orientation film is required to have a uniform thickness.

FIG. 2 is a cross-sectional view showing a printing apparatus of an orientation film according to the related art, and FIG. 3 is a cross-sectional view showing a transferring plate and a substrate in a printing apparatus of an orientation film according to the related art. In FIG. 2, a plate cylinder 51 and a substrate 60 on a stage 55 contact each other with a transferring plate 53 interposed therebetween, and a polymeric material is transferred to the substrate 60 by adding a pressure to form an orientation film 63. Since the transferring plate 53 having the polymeric material contacts and is pressurized toward the substrate 60, the polymeric material transferred from the transferring plate 53 to the substrate 60 is spread out toward all directions. Although the orientation film 63 corresponding to a pattern region 54 (of FIG. 3) has a uniform thickness, the orientation film 63 corresponding to an outside of the pattern region 54 has a greater thickness because the orientation film 63 is not pressurized.

In FIG. 3, the orientation film 63 on the substrate 60 includes a starting portion 63a, an ending portion 63b and a central portion 63c. Due to rotation of the plate cylinder 51 (of FIG. 2), the pattern region 54 of the transferring plate 53 starts contacting the substrate 60 to form the starting portion 63a and stop contacting the substrate 60 to form the ending portion 63b. Since the polymeric material is pushed out from the central portion 63c to the starting and ending portions 63a and 63b, a thickness of each of the starting and ending portions 63a and 63b is three or four times as great as a thickness of the central portion 63c. The starting and ending portions 63a and 63b may be referred to as a mount of the orientation film 63.

The mount causes deterioration of the orientation film 63 in a subsequent rubbing step. In addition, since the starting and ending portions of the orientation film 63 have a zigzag line, the ending portion belonging to the non-display area is

designed to have a relatively great width. As a result, a bezel region corresponding to the non-display area is enlarged.

BRIEF SUMMARY

A substrate for a liquid crystal display device includes: a substrate including a display region displaying an image and a non-display region surrounding the display region; a dummy pattern in the non-display area over the substrate, the dummy pattern having a length that corresponds to a side of the display area; and an orientation film on the dummy pattern, the orientation film covering the non-display area and the whole display area.

In another aspect, a liquid crystal display device includes: first and second substrate facing and spaced apart from each other, the first and second substrates including a display region displaying an image and a non-display region surrounding the display region; a gate line and a data line over an inner surface of the first substrate, the gate line and the data line crossing each other to define a pixel region; a thin film transistor connected to the gate line and the data line; a pixel electrode connected to the thin film transistor; a first dummy pattern in the non-display area over the inner surface of the first substrate, the first dummy pattern having a length that corresponds to a side of the display area; a first orientation film on the pixel electrode and the first dummy pattern; a black matrix over an inner surface of the second substrate; a color filter layer in the pixel region, the color filter layer including red, green and blue color filters sequentially repeated in the pixel region; and a plurality of patterned spacers on the color filter layer, the plurality of patterned spacers spaced apart from each other and corresponding to the black matrix; a second dummy pattern in the non-display area over the inner surface of the second substrate, the second dummy pattern having a length that corresponds to the side of the display area; a second orientation film on the plurality of patterned spacers and the second dummy pattern; and a liquid crystal layer between the first and second orientation films.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

FIG. 1 is an exploded perspective view showing a liquid crystal display device according to the related art;

FIG. 2 is a cross-sectional view showing a printing apparatus of an orientation film according to the related art;

FIG. 3 is a cross-sectional view showing a transferring plate and a substrate in a printing apparatus of an orientation film according to the related art;

FIGS. 4A and 4B are plan views showing an array substrate and a color filter substrate, respectively, for a liquid crystal display device according to an embodiment of the present invention;

FIGS. 5A to 5G are plan views showing a first dummy pattern of a liquid crystal display device according to an embodiment of the present invention;

FIGS. 6A to 6D are cross-sectional views showing a first dummy pattern of a liquid crystal display device according to an embodiment of the present invention; and

FIGS. 7A and 7B are cross-sectional views showing a second dummy pattern of a liquid crystal display device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS AND THE PRESENTLY PREFERRED EMBODIMENTS

Reference will now be made in detail to the preferred embodiments, examples of which are illustrated in the accompanying drawings.

FIGS. 4A and 4B are plan views showing an array substrate and a color filter substrate, respectively, for a liquid crystal display device according to an embodiment of the present invention.

In FIG. 4A, an array substrate 101 for a liquid crystal display (LCD) device includes a display area AA displaying an image and first to fourth non-display areas NA1, NA2, NA3 and NA4 surrounding the display area AA. The first to fourth non-display areas NA1, NA2, NA3 and NA4 include first and second pad areas PA1 and PA2 where gate and data pads 112 and 137 are respectively formed.

A gate line 110 and a data line 130 that cross each other to define a pixel region P are formed in the display area AA. A thin film transistor (TFT) Tr connected to the gate line 110 and the data line 130 is formed in the pixel region P. Although not shown, the TFT Tr may include a gate electrode, a gate insulating layer, a semiconductor layer, a source electrode and a drain electrode. The gate-electrode is connected to the gate line 110. The gate insulating layer is formed on the gate electrode, and the semiconductor layer is formed on the gate insulating layer over the gate electrode. The semiconductor layer may include an active layer of intrinsic amorphous silicon and an ohmic contact layer of impurity-doped amorphous silicon. The source and drain electrodes are formed on the semiconductor layer and are spaced apart from each other. The source electrode is connected to the data line 130. In addition, a passivation layer is formed on the TFT Tr.

A pixel electrode 150 connected to the drain electrode of the TFT Tr is formed in the pixel region P. A common electrode may be formed in the pixel region P on the array substrate 101 according to a mode of the LCD device. For example, the pixel electrode 150 of a plate shape may be formed in the pixel region P on the array substrate 101 when the LCD device has a twisted nematic (TN) mode where a liquid crystal layer is driven by a vertical electric field. In addition, the pixel electrode and the common electrode that have a bar shape and alternate with each other may be formed in the pixel region P on the array substrate when the LCD device has an in-plane switching (IPS) mode where the liquid crystal layer is driven by a horizontal electric field. Further, a common line 114 parallel to and spaced apart from the gate line 110 may be formed on the array substrate 101 and the common electrode may be connected to the common line 114.

The gate pad 112 in the first pad area PA1 is connected to the gate line 110 and the data pad 137 in the second pad area PA2 is connected to the data line 130. In addition, a first dummy pattern 170 is formed in at least one of the first to fourth non-display area NA1, NA2, NA3 and NA4 on the array substrate 101. The first dummy pattern 170 may have a length corresponding to a side of the display area AA.

FIGS. 5A to 5G are plan views showing a first dummy pattern of a liquid crystal display device according to an embodiment of the present invention.

The first dummy pattern **170** may have a single bar pattern (dam shape) as shown in FIG. **5A**. In addition, the first dummy pattern **170** may have a plurality of bar patterns spaced apart from each other as shown in FIGS. **5B** and **5C**. In FIG. **5B**, the plurality of bar patterns are alternately disposed with each other such that ends of the adjacent bar patterns are not flush with each other. In FIG. **5C**, the plurality of bar patterns are disposed such that ends of the adjacent bar patterns are flush with each other. Although the adjacent bar patterns are spaced apart from each other by an equal distance in FIGS. **5B** and **5C**, the adjacent bar patterns may be spaced apart from each other by a gradually increasing or decreasing distance in another embodiment.

Further, the first dummy pattern **170** may have a lattice pattern as shown in FIGS. **5D** to **5G**. For example, the lattice pattern may include an opening having one of a hexagonal shape, a bent rectangular shape and a rectangular shape. In FIGS. **5D** to **5F**, the opening of the lattice pattern has an equal size (area). In FIG. **5E**, the opening of the lattice pattern has a gradually increasing or decreasing size (area).

Referring again to FIG. **4A**, the first dummy pattern **170** may have a height of about 0.5 μm to about 3 μm and a width of about 20 μm to about 200 μm . For example, the first dummy pattern **170** may have a width of about 50 μm to about 200 μm when the first dummy pattern **170** has the single bar pattern as shown in FIG. **5A**. In addition, the first dummy pattern **170** may have a width of about 20 μm to about 50 μm when the first dummy pattern **170** has one of the plurality of bar patterns as shown in FIGS. **5B** and **5C** and the lattice pattern as shown in FIGS. **5D** to **5G**.

The height of the first dummy pattern **170** may vary with a position of the first dummy pattern **170**. As the height of the first dummy pattern **170** increases, a thickness of the orientation film decreases. Accordingly, a mount of the orientation film is prevented by adjusting the height of the first dummy pattern **170**. For example, when the printing step for an orientation film starts at the first non-display area **NA1** and ends at the second non-display area **NA2**, a first height of the first dummy pattern **170** in the first non-display area **NA1** may be smaller than a second height of the first dummy pattern **170** in the second non-display area **NA2**.

In addition, when the first dummy pattern **170** has one of the plurality of bar patterns as shown in FIGS. **5B** and **5C** and the lattice pattern as shown in FIGS. **5D** to **5G**, the distance between the adjacent bar patterns or the size (area) of the opening of the lattice pattern (i.e., lattice density) may vary with a position of the first dummy pattern **170**. As the distance between the adjacent bar patterns or the size of the opening increases, a thickness of the orientation film decreases. Accordingly, a mount of the orientation film is prevented by adjusting the distance between adjacent bar patterns or the size of the opening of the lattice pattern of the first dummy pattern **170**. For example, when the printing step for an orientation film starts at the first non-display area **NA1** and ends at the second non-display area **NA2**, a first distance between the adjacent bar patterns of the first dummy pattern **170** in the first non-display area **NA1** may be smaller than a second distance between the adjacent bar patterns of the first dummy pattern **170** in the second non-display area **NA2** for the first dummy pattern **170** of the plurality of bar patterns as shown in FIGS. **5B** and **5C**. In addition, a first size (area) of the opening of the lattice pattern of the first dummy pattern **170** in the first non-display area **NA1** may be smaller than a second size (area) of the opening of the lattice pattern of the first dummy pattern **170** in the second non-display area **NA2** for the first dummy pattern **170** having the lattice pattern as shown in FIGS. **5D** to **5G**.

The first dummy pattern **170** may be formed of a multiple layer used for fabricating the array substrate **101**. FIGS. **6A** to **6D** are cross-sectional views showing a first dummy pattern of a liquid crystal display device according to an embodiment of the present invention.

In FIGS. **4A** and **6A**, the first dummy pattern **170** in the first and fourth non-display areas **NA1** and **NA4** may have a double-layered structure including a gate dummy layer **170a** and a data dummy layer **170b** over the array substrate **101**. Since the first and fourth non-display areas **NA1** and **NA4** do not include the first and second pad areas **PA1** and **PA2**, the gate dummy layer **170a** may include the same layer and the same material as the gate line **110** and the data dummy layer **170b** may include the same layer and the same material as the data line **130**. In addition, the first dummy pattern **170** may have at least one of the single bar pattern, a plurality of bar patterns and the lattice pattern as shown in FIGS. **5A** to **5G**. For example, the gate dummy layer **170a** and the data dummy layer **170b** may overlap each other with the same shape and the same area as each other. In addition, the gate dummy layer **170a** may be formed on the array substrate **101**, a gate insulating layer **113** may be formed between the gate dummy layer **170a** and the data dummy layer **170b**, and a passivation layer **140** may be formed on the data dummy layer **170b**.

In FIGS. **4A** and **6B**, the first dummy pattern **170** in the first and fourth non-display areas **NA1** and **NA4** may have a triple-layered structure including a gate dummy layer **170a**, a semiconductor dummy layer **170c** and a data dummy layer **170b** over the array substrate **101**. Since the first and fourth non-display areas **NA1** and **NA4** do not include the first and second pad areas **PA1** and **PA2**, the gate dummy layer **170a** may include the same layer and the same material as the gate line **110**, the semiconductor dummy layer **170c** may include the same layer and the same material as the semiconductor layer, and the data dummy layer **170b** may include the same layer and the same material as the data line **130**. In addition, the first dummy pattern **170** may have at least one of the single bar pattern, a plurality of bar patterns and the lattice pattern as shown in FIGS. **5A** to **5G**. For example, the gate dummy layer **170a**, the semiconductor dummy layer **170c** and the data dummy layer **170b** may overlap each other with the same shape and the same area as each other. Further, the gate dummy layer **170a** may be formed on the array substrate **101**, and a gate insulating layer **113** may be formed between the gate dummy layer **170a** and the semiconductor dummy layer **170c**. Moreover, the data dummy layer **170b** may be formed on the semiconductor dummy layer **170c**, and a passivation layer **140** may be formed on the data dummy layer **170b**.

In FIGS. **4A** and **6C**, the first dummy pattern **170** in the second non-display areas **NA2** may be disposed between the first pad area **PA1** and the display area **AA** and may have a double-layered structure including a semiconductor dummy layer **170c** and a data dummy layer **170b** over the array substrate **101**. Since the second non-display areas **NA2** includes the first pad area **PA1**, the semiconductor dummy layer **170c** may include the same layer and the same material as the semiconductor layer and the data dummy layer **170b** may include the same layer and the same material as the data line **130**. In addition, the first dummy pattern **170** may have at least one of the single bar pattern, a plurality of bar patterns and the lattice pattern as shown in FIGS. **5A** to **5G**. For example, the semiconductor dummy layer **170c** and the data dummy layer **170b** may overlap each other with the same shape and the same area as each other. Further, the semiconductor dummy layer **170c** and the data dummy layer **170b**

may be sequentially formed on a gate insulating layer **113**, and a passivation layer **140** may be formed on the data dummy layer **170b**.

Alternatively, the first dummy pattern **170** in the second non-display areas **NA2** may be disposed between the first pad area **PA1** and the display area **AA** and may have a triple-layered structure including a gate dummy layer **170a**, a semiconductor dummy layer **170c** and a data dummy layer **170b** over the array substrate **101**. Since the second non-display areas **NA2** includes the first pad area **PA1**, the first dummy pattern **170** may have a plurality of bar patterns as shown in FIG. **5C** such that the gate line **110** is disposed between adjacent bar patterns. For example, the gate dummy layer **170a**, the semiconductor dummy layer **170c** and the data dummy layer **170b** may overlap each other with the same shape and the same area as each other. Further, the gate dummy layer **170a** may include the same layer and the same material as the gate line **110**, the semiconductor dummy layer **170c** may include the same layer and the same material as the semiconductor layer, and the data dummy layer **170b** may include the same layer and the same material as the data line **130**.

Similarly, the first dummy pattern **170** in the third non-display areas **NA3** may be disposed between the second pad area **PA2** and the display area **AA** and may have a double-layered structure including a gate dummy layer **170a** and a semiconductor dummy layer **170c** over the array substrate **101** and may have at least one of the single bar pattern, a plurality of bar patterns and the lattice pattern as shown in FIGS. **5A** to **5G**. Alternatively, the first dummy pattern **170** in the third non-display areas **NA3** may be disposed between the second pad area **PA2** and the display area **AA** and may have a triple-layered structure including a gate dummy layer **170a**, a semiconductor dummy layer **170c** and a data dummy layer **170b** over the array substrate **101** and may have a plurality of bar patterns as shown in FIG. **5C**.

When the first dummy pattern **170** has one of a plurality of bar patterns as shown in FIGS. **5C** and **5C** and a lattice pattern as shown in FIGS. **5D** to **5G**, a distance between the adjacent bar patterns or a shape of an opening of the lattice pattern may be adjusted according to a position of the first dummy pattern **170**. In addition, a height of the first dummy pattern **170** may be adjusted by omitting at least one of the gate dummy layer **170a**, the semiconductor dummy layer **170c** and the data dummy layer **170b**.

The first dummy pattern **170** causes a step difference in the passivation layer **140** and the step difference of the passivation layer **140** prevents a mount of the orientation film and a zigzag line of the ending and starting portions of the orientation film. As a result, a bezel region of the LCD device is reduced.

Although the first dummy pattern **170** in the first to fourth non-display areas **NA1**, **NA2**, **NA3** and **NA4** is formed of the layers used for the TFT Tr (of FIG. **4A**) of the array substrate **101** in FIGS. **6A** to **6C**, the first dummy pattern **170** may be formed of an organic material as shown in FIG. **6D**. For example, the first dummy pattern **170** in the first to fourth non-display areas **NA1**, **NA2**, **NA3** and **NA4** may be formed on a passivation layer **140** by coating and patterning an organic material such as acrylic resin and benzocyclobutene (BCB).

In FIG. **4B**, a color filter substrate **180** for the LCD device also includes the display area **AA** and the first to fourth non-display areas **NA1**, **NA2**, **NA3** and **NA4** surrounding the display area **AA**. A black matrix **183** is formed along a boundary of the pixel region **P** in the display area **AA** and a color filter layer **185** is formed in the pixel region **P** exposed

through the black matrix **183**. The color filter layer **185** includes red, green and blue color filters **185a**, **185b** and **185c** sequentially repeated in the pixel regions **P**.

Although not shown, a common electrode may be formed on the color filter substrate **180** according to a mode of the LCD device. For example, the common electrode and an overcoat layer may be sequentially formed on an entire surface of the color filter layer **185** and the pixel electrode **150** (of FIG. **4A**) may be formed in the pixel region **P** on the array substrate **101** (of FIG. **4A**) when the LCD device has a TN mode. In addition, an overcoat layer may be formed on an entire surface of the color filter layer **185** and the pixel electrode and the common electrode of a bar shape may be formed in the pixel region **P** on the array substrate **101** when the LCD device has an IPS mode. The overcoat layer may be omitted. A plurality of patterned spacers **187** for maintaining a uniform cell gap may be formed on one of the common electrode and the overcoat layer. The plurality of patterned spacers **187** may be spaced apart from each other to correspond to the black matrix **183**.

A second dummy pattern **190** is formed in at least one of first to fourth non-display areas **NA1**, **NA2**, **NA3** and **NA4** on the color filter substrate **180**. The second dummy pattern **190** may have a length corresponding to a side of the display area **AA**. In addition, the second dummy pattern **190** may have a height of about 0.5 μm to about 3 μm and a width of about 20 μm to about 200 μm . In addition, the second dummy pattern **190** may have at least one of the single bar pattern similarly to FIG. **5A**, the plurality of bar patterns similarly to FIGS. **5B** and **5C** and the lattice pattern similarly to FIGS. **5D** to **5G**.

FIGS. **7A** and **7B** are cross-sectional views showing a second dummy pattern of a liquid crystal display device according to an embodiment of the present invention.

In FIGS. **4B** and **7A**, the second dummy pattern **190** in the first to fourth non-display areas **NA1**, **NA2**, **NA3** and **NA4** may have a single-layered structure over the color filter substrate **180**. The second dummy pattern **190** may include the same layer and the same material as the black matrix **183** and the common electrode **192** may be formed on the second dummy pattern **190**. The second dummy pattern **190** causes a step difference in the common electrode **192** and the step difference of the common electrode **192** prevents a mount of the orientation film and a zigzag line of the ending portion of the orientation film. As a result, a bezel region of the LCD device is reduced.

In FIGS. **4B** and **7B**, the second dummy pattern **190** in the first to fourth non-display areas **NA1**, **NA2**, **NA3** and **NA4** may have a single-layered structure over the color filter substrate **180**. The second dummy pattern **190** may include the same layer and the same material as the patterned spacer **187** and may be formed on one of the common electrode **192** and the overcoat layer. The second dummy pattern **190** generates a step difference that prevents a mount of the orientation film and a zigzag line of the ending and starting portions of the orientation film. As a result, a bezel region of the LCD device is reduced.

An orientation film **163a** and **163b** is formed on each of the array substrate **101** and the color filter substrate **180** by printing a polymeric material such as polyimide and the orientation film **163a** and **163b** is rubbed with a rubbing cloth without generation of a mount of the orientation film **163a** and **163b** due to the first and second dummy patterns **170** and **190**. The array substrate **101** and the color filter substrate **180** having the orientation film **163a** and **163b** are attached with a liquid crystal layer interposed therebetween by a seal pattern to complete the LCD device.

Consequently, in an LCD device according to the present disclosure, a dummy pattern that prevents a mount of an orientation film is formed in a non-display area surrounding a display area. As a result, a mount having a relatively great thickness at starting and ending portions of the orientation film is prevented. Since the mount of the orientation film is prevented, deterioration in a rubbing step is prevented. In addition, lifting of the orientation film due to contact with a seal pattern is prevented. Further, since the starting and ending portions of the orientation film have a straight line instead of a zigzag line due to the dummy pattern, a margin for an alignment error and a bezel region are reduced and the LCD device obtains a narrow bezel.

It will be apparent to those skilled in the art that various modifications and variations can be made in a substrate and a liquid crystal display device including the substrate of the present disclosure without departing from the spirit or scope of the invention. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

The invention claimed is:

1. A substrate for a liquid crystal display device, comprising:

a substrate body including a display region displaying an image and a non-display area surrounding the display area, the non-display area including a first non-display region and a second non-display region at opposing sides of the display area;

an orientation film for aligning a liquid crystal layer; and a dummy pattern for adjusting a thickness of the orientation film, the dummy pattern being formed in the non-display area and between the orientation film and the substrate body;

wherein the orientation film is formed on the dummy pattern and covers the non-display area and the whole display area,

wherein the dummy pattern includes a first pattern in the first non-display region and a second pattern in the second non-display region, the first pattern and the second pattern being one of a bar pattern and a lattice pattern, the bar pattern including a plurality of bars disconnected from each other and extending parallel to the opposing sides of the display area, the lattice pattern including a plurality of segments connected to each other to define a plurality of openings, and

wherein the first pattern in the first non-display region is different from the second pattern in the second non-display region of the non-display area.

2. The substrate according to claim 1, wherein each of the first pattern and the second pattern of the dummy pattern has one of a hexagonal shape, a bent rectangular shape and a rectangular shape.

3. The substrate according to claim 1, wherein each of the first and second pattern's is a bar pattern and the bars are aligned into a plurality of rows parallel to the opposing sides of the display area, the bars being spaced apart by a distance along a direction perpendicular to the opposing sides of the display area, the distance in the first non-display region is different from the distance in the second non-display region.

4. The substrate of claim 3, wherein the orientation film is formed on the display area and the non-display area of the substrate body by printing a material from the first non-display region towards the second non-display region of the non-display area, and wherein the distance in the first non-display region is smaller than the distance in the second non-display region.

5. The substrate according to claim 3, wherein the bars in the bar pattern are spaced apart from each other by one of a gradually increasing distance and a gradually decreasing distance, and the openings in the lattice pattern have one of a gradually increasing size and a gradually decreasing size.

6. The substrate according to claim 1, wherein that the bars in the bar pattern are not aligned along the direction perpendicular to the opposing sides of the display area.

7. The substrate according to claim 1, wherein the dummy pattern has a height of about 0.5 μm to about 3 μm and a width of about 20 μm to about 200 μm .

8. The substrate according to claim 1, wherein the display area comprises:

a gate line and a gate electrode on the substrate, the gate electrode connected to the gate line;

a gate insulating layer on the gate line and the gate electrode;

a semiconductor layer on the gate insulating layer over the gate electrode;

a source electrode and a drain electrode on the semiconductor layer, the gate electrode, the semiconductor layer, the source electrode and the drain electrode constituting a thin film transistor;

a data line crossing the gate line to define a pixel region, the data line connected to the source electrode;

a passivation layer on the thin film transistor; and

a pixel electrode on the passivation layer, the pixel electrode connected to the drain electrode, and

wherein a central portion of the orientation film is on the pixel electrode and an edge portion of the orientation film is on the dummy pattern.

9. The substrate according to claim 8, wherein the display area further comprises:

a common line parallel to and spaced apart from the gate line; and

a common electrode alternating with the pixel electrode, the common electrode connected to the common line.

10. The substrate according to claim 8, wherein the dummy pattern includes at least two of a gate dummy pattern, a semiconductor dummy pattern and a data dummy pattern overlapping each other, wherein the gate dummy pattern has a same layer and a same material as the gate line, wherein the semiconductor dummy pattern has a same layer and a same material as the semiconductor layer, and wherein the data dummy pattern has a same layer and a same material as the data line.

11. The substrate according to claim 8, wherein the dummy pattern includes an organic material layer on the passivation layer.

12. The substrate according to claim 1, wherein the display area comprises:

a black matrix along a boundary of a pixel region;

a color filter layer in the pixel region, the color filter layer including red, green and blue color filters sequentially repeated in the pixel region; and

a plurality of patterned spacers on the color filter layer, the plurality of patterned spacers spaced apart from each other and corresponding to the black matrix, and

wherein a central portion of the orientation film is on the plurality of patterned spacers and an edge portion of the orientation film is on the dummy pattern.

13. The substrate according to claim 12, wherein the dummy pattern includes at least one of a first layer that has a same layer and a same material as the black matrix and a second layer that has a same layer and a same material as the plurality of patterned spacers.

14. The substrate according to claim 13, wherein the display area further comprises a common electrode on the color filter layer and an overcoat layer on the common electrode, and wherein the plurality of patterned spacers are on the overcoat layer.

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15. The substrate of claim 1, wherein each of the first pattern and the second pattern is the lattice pattern and a size of the openings in the first non-display region is different from a size of the openings in the second non-display region.

16. The substrate of claim 15, wherein the orientation film is formed on the display area and the non-display area of the substrate body by printing a material from the first non-display region towards the second non-display region of the non-display area, wherein the size of the opening in the first non-display region is smaller than the size of the opening in the second non-display region.

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17. The substrate of claim 1, wherein a height of the first pattern is different from a height of the second pattern.

18. The substrate of claim 17, wherein the orientation film is formed on the display area and the non-display area of the substrate body by printing a material from the first non-display region towards the second non-display region of the non-display area, and wherein the height of the first pattern is smaller than the height of the second pattern.

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专利名称(译)	基板和包括其的液晶显示装置		
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[标]申请(专利权)人(译)	LEE JAE WON NOH这么年轻 KIM SUNG KI 金珍PIL SON KYUNG MO		
申请(专利权)人(译)	李在WON NOH SO-YOUNG KIM SUNG-KI KIM JIN-PIL SON KYUNG-MO		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD		
[标]发明人	LEE JAE WON NOH SO YOUNG KIM SUNG KI KIM JIN PIL SON KYUNG MO		
发明人	LEE, JAE-WON NOH, SO-YOUNG KIM, SUNG-KI KIM, JIN-PIL SON, KYUNG-MO		
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摘要(译)

一种用于液晶显示装置的基板，包括：基板，包括显示图像的显示区域和围绕显示区域的非显示区域;在基板上方的非显示区域中的虚设图案，虚设图案具有与显示区域的一侧相对应的长度;虚设图案上的取向膜，取向膜覆盖非显示区域和整个显示区域。

