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(54) **ARRAY SUBSTRATES AND DISPLAY PANELS**

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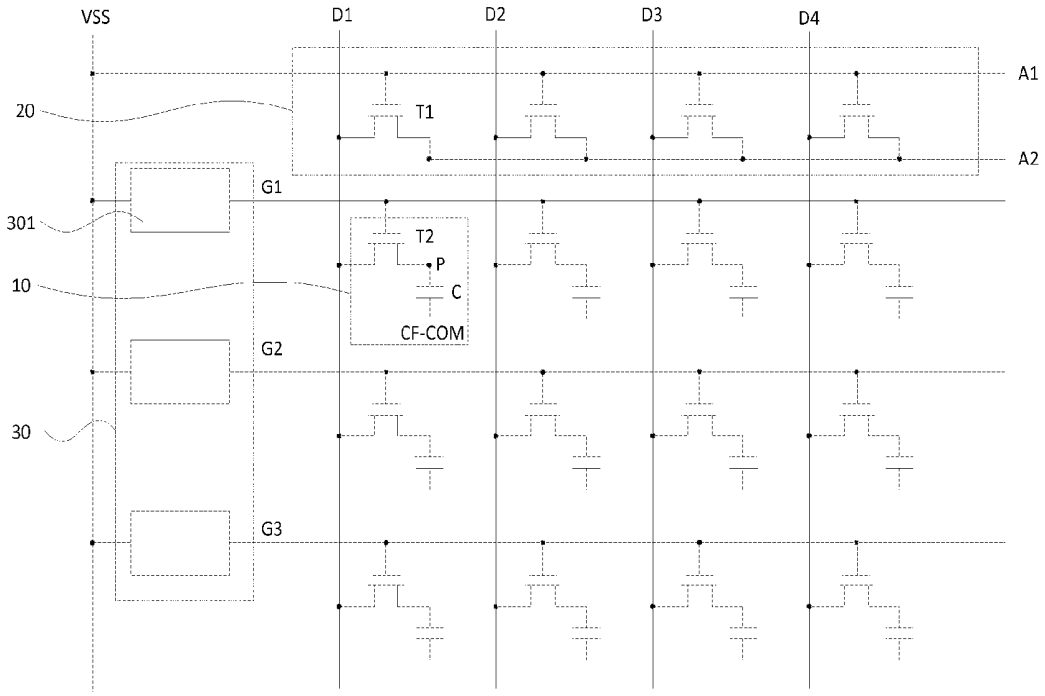
(57) **ABSTRACT**

The present disclosure relates to an array substrate and a display panel. The array substrate includes a plurality of scanning lines, and a plurality of data lines intersecting with the scanning lines to define a plurality of pixel areas. The array substrate further includes a control circuit connecting to the data lines. The control circuit is configured to maintain a voltage on the data lines to be the same with the voltage on a common electrode. The voltage of the pixel electrode within the pixel areas is the same with the voltages on the data lines so as to balance a voltage difference between the pixel electrode and the common electrode. In this way, the liquid crystal may not be twisted so as to avoid the white blur.



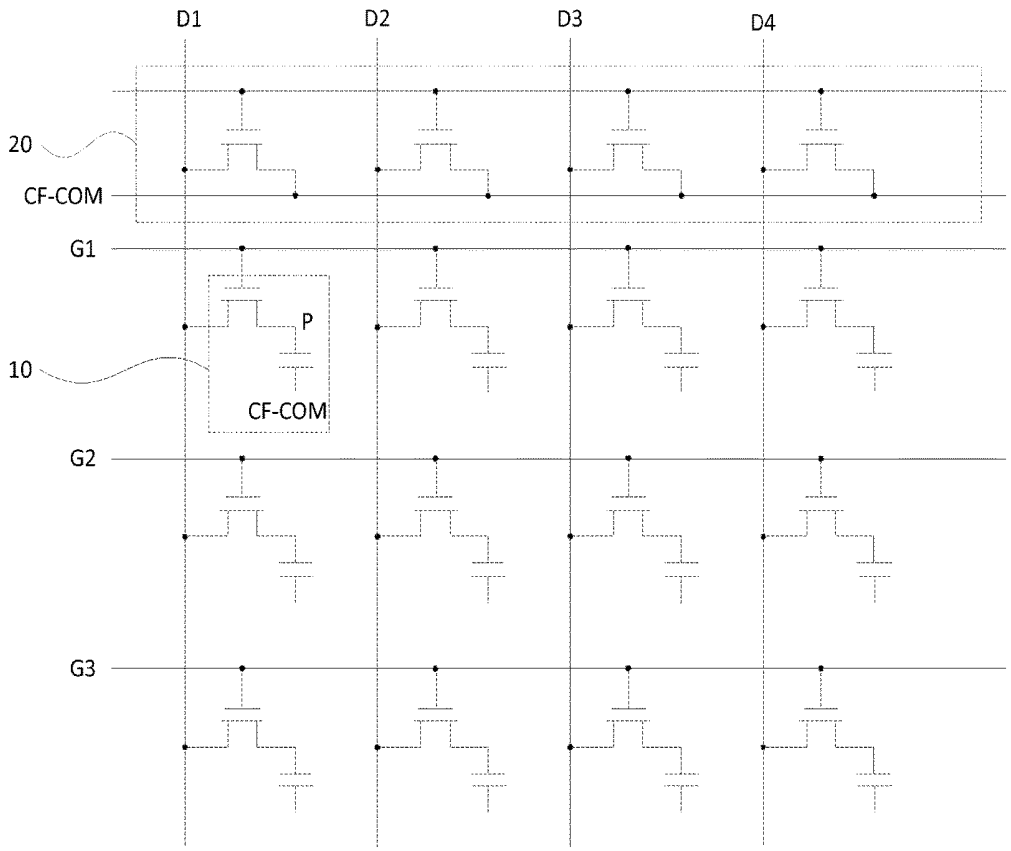


Fig.1

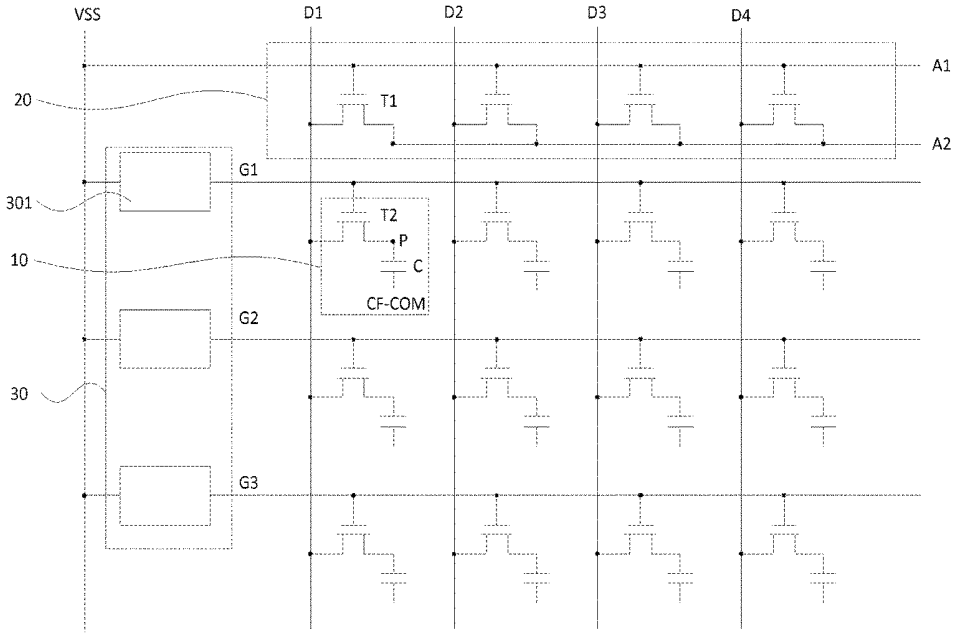


Fig.2

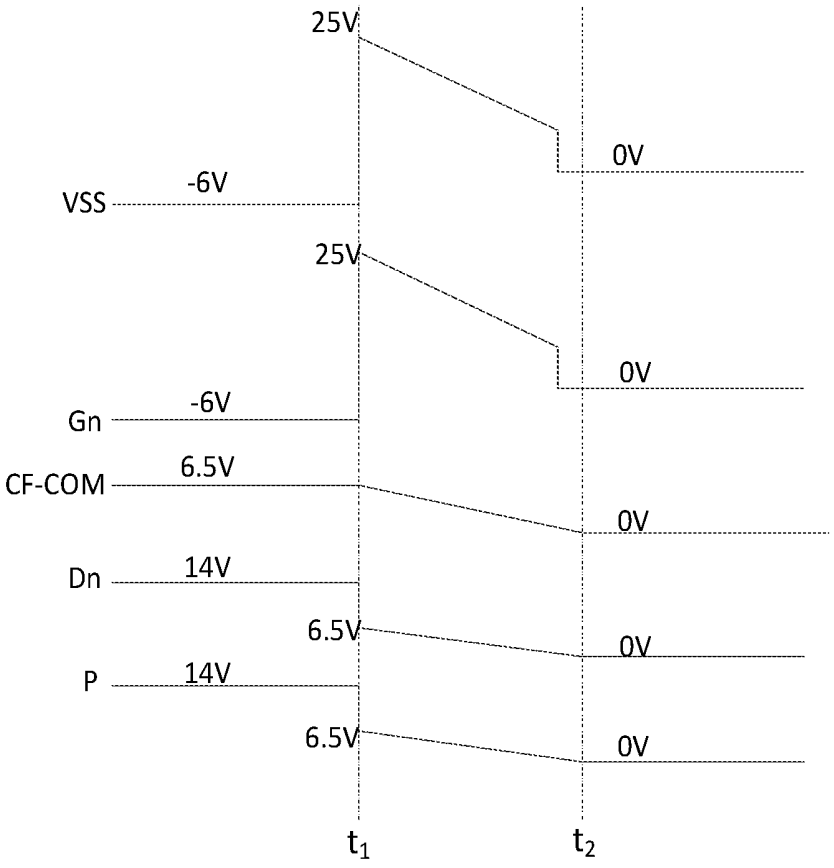

25V
0V
VSS
-6V
25V
0V
Gn
-6V
CF-COM
6.5V
0V
Dn
14V
6.5V
0V
P
14V
6.5V
0V
t1
t2

Fig.3

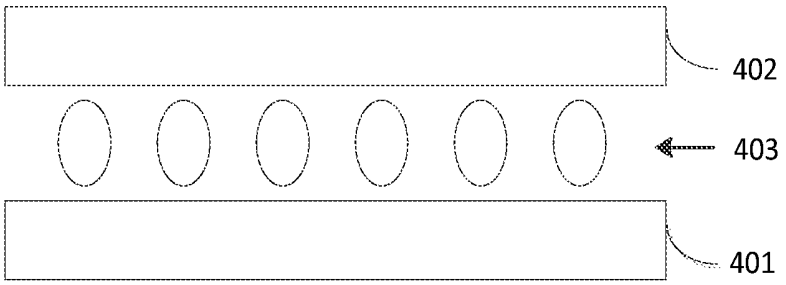

402
403
401

Fig.4

ARRAY SUBSTRATES AND DISPLAY PANELS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present disclosure relates to liquid crystal display technology, and more particularly to an array substrate and a display panel.

2. Discussion of the Related Art

[0002] Liquid crystal devices (LCDs) are characterized by attributes, such as small size, low power consumption, low radiation, and thus have been the major product in the flat display field. With the development of liquid crystal display technology, attributes including high resolution, high contrast, narrow borders, and thinner have become the trend of liquid crystal display. With respect to Gate Driver On Array (GOA), the driving circuits performing horizontal scanning may be manufactured in a rim of the display area of the substrate by the original manufacturing process, such that the original external Integrated Circuit (IC) may be replaced so as to complete the horizontal scanning. This not only reduces the manufacturing process of the external IC and the product costs, but may contribute to the narrow border design.

[0003] In the long-term research and development, it is found that the common electrode and the pixel electrode are provided on both sides of the liquid crystal layer in the liquid crystal display. When the GOA-LCD is turned off, the discharge of the common electrode is slow, When the pixel electrode is discharged to OV, the common electrode is maintained at a voltage greater than 3V, so that the common electrode and pixel electrode pressure is greater than 3V. This may result in liquid crystal deflection, and the screen may include white blur.

SUMMARY

[0004] The present disclosure relates to an array substrate and a display panel to resolve the white blue issue when the LCD is turned off.

[0005] In one aspect, an array substrate includes: a plurality of scanning lines; a plurality of data lines intersecting with the scanning lines to define a plurality of pixel areas; a control circuit connecting to the data lines, the control circuit being configured to maintain a voltage on the data lines to be the same with the voltage on a common electrode, and the voltage of the pixel electrode within the pixel areas being the same with the voltages on the data lines so as to balance a voltage difference between the pixel electrode and the common electrode.

[0006] In another aspect, a display panel includes: a first substrate, a second substrate, and a liquid crystal layer between the first substrate and the second substrate; wherein the first substrate is an array substrate includes: a plurality of scanning lines and data lines intersecting with each other so as to define a plurality of pixel areas; a control circuit connecting to the data lines for keeping the voltages on the data lines to be the same with the voltages of the common electrode when the display panel is turned off, and the voltage of the pixel electrode within the pixel areas being the same with the voltage on the data lines so as to balance a voltage difference between the pixel electrode and the common electrode.

[0007] In the present disclosure, the data lines connect to the control circuit. The voltage of the data lines is changed when the LCD is turned off, such that the voltage difference between the pixel electrode and the common electrode may be balanced. The liquid crystal are not twisted so as to reduce the white blur.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIG. **1** is a schematic view of the array substrate in accordance with one embodiment of the present disclosure.

[0009] FIG. **2** is a schematic view of the array substrate in accordance with another embodiment of the present disclosure.

[0010] FIG. **3** is a schematic view showing the voltage variation of each points of the array substrate in accordance with one embodiment of the present disclosure.

[0011] FIG. **4** is a schematic view of the display panel in accordance with one embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0012] Embodiments of the invention will now be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown.

[0013] Referring to FIG. **1**, the array substrate may include:

[0014] A plurality of scanning lines (Gn). In an example, the array substrate includes the scanning lines (G**1**-G**3**).

[0015] A plurality of data lines (Dn). In an example, the array substrate includes the data lines (D**1**-D**4**) intersecting with the scanning lines (Gn) to define a plurality of pixel areas **10**.

[0016] A control circuit **20** connecting to a plurality of data lines (Dn). When the LCD is turned off, the voltage of the data lines (Dn) are the same with the voltage of the common electrode (CF-COM). The voltage of the pixel electrode (P) within the pixel area **10** is the same with the voltage on the data lines (Dn) such that a voltage difference between the pixel electrode (P) and the common electrode (CF-COM) may be balanced.

[0017] In an example, the control circuit **20** may include at least one thin film transistor (TFT) and other components. With such configuration, when the LCD is turned off, the voltage of the data lines (Dn) and the voltage of the common electrode (P) within the pixel areas **10** are balanced. As such, the voltage difference between the common electrode (P) within the pixel areas **10** and the common electrode (CF-COM) are balanced, and the liquid crystal are not twisted.

[0018] In an example, the array substrate may be adopted by displays, such as LCD.

[0019] In the present disclosure, the data lines connect to the control circuit. The voltage of the data lines is changed when the LCD is turned off, such that the voltage difference between the pixel electrode and the common electrode may be balanced. The liquid crystal are not twisted so as to reduce the white blur.

[0020] Referring to FIGS. **2** and **3**, in one embodiment, the array substrate includes:

[0021] A plurality of scanning lines (Gn). In an example, the array substrate includes the scanning lines (G**1**-G**3**).

[0022] A plurality of data lines (Dn). In an example, the array substrate includes the data lines (D**1**-D**4**) intersecting with the scanning lines (Gn) to define a plurality of pixel areas **10**.

[0023] A control circuit **20** connecting to a plurality of data lines (Dn). When the LCD is turned off, the voltage of the data lines (Dn) are the same with the voltage of the common electrode (CF-COM). The voltage of the pixel electrode (P) within the pixel area **10** is the same with the voltage on the data lines (Dn) such that a voltage difference between the pixel electrode (P) and the common electrode (CF-COM) may be balanced.

[0024] The control circuit **20** includes a first control line (A**1**), a second control line (A**2**), and a plurality of TFTs (T**1**), wherein the first control line (A**1**) connects to a direct-current low voltage (VSS), the second control line (A**2**) connects to the common electrode (CF-COM), a gate of the TFTs (T**1**) connects to the al connects to the first control line (A**1**), a source of the second transistor (T**2**) connects to the data line (Dn), and a drain of the TFTs (T**1**) connects to the second control line (A**2**).

[0025] The pixel areas **10** includes a second TFT (T**2**). A gate of the second TFT (T**2**) connects to the scanning line (Gn), a source of the second TFT (T**2**) connects to the data lines (Dn), and a drain of the second TFT (T**2**) connects to the common electrode (P). The pixel areas **10** further includes a liquid crystal capacitor (C) equivalent to the liquid crystal layer. A first end of the liquid crystal capacitor (C) connects to the common electrode (P), and a second end of the liquid crystal capacitor (C) connects to the common electrode (CF-COM). The liquid crystals are controlled by the voltages at two ends of the liquid crystal capacitor (C), that is, the voltage between the common electrode (P) and the common electrode (CF-COM).

[0026] The liquid crystal panel **30** includes a plurality of driving units **301**. A first end of the driving unit **301** connects to the direct-current low voltage (VSS), and a second end of the driving unit **301** connects to a corresponding scanning line (Gn).

[0027] In an example, the liquid crystal panel **30** may be a GOA circuit.

[0028] In an example, the direct-current low voltage (VSS) may be a direct-current low voltage ranging from −14 V to −4 V.

[0029] In an example, the array substrate receives the turn-off signals at the moment (t**1**), the voltage on the first control line (A**1**) transits from −6 V to 25 V due to the inputted direct-current low voltage (VSS), such that the TFTs (T**1**) on the first control line (A**1**) are turned on. At this moment, the voltage on the data lines (Dn) transits from 14V to be the same with the voltage on the second control line (A**2**), that is, the voltage of the common electrode (CF-COM), i.e., 6.5V. At the same time, the voltage on the scanning lines (Gn) transits from −6V to 25V due to the inputted direct-current low voltage (VSS), such that the second TFTs (T**2**) on the scanning lines (Gn) are all turned on. At this moment, the voltage on the common electrode (P) transits from 14V to be the same with the voltage on the data lines (Dn), i.e., 6.5V. The voltages at two ends of the liquid crystal capacitor (C) are both 6.5V, and the voltage difference equals to zero. Afterward, the two ends of the liquid crystal capacitor (C) discharge at the same time. Until the moment (t**2**), the voltages at two ends of the liquid crystal capacitor (C) transits to be zero. As the voltages at two ends of the liquid crystal capacitor (C) are equal. Thus, the liquid crystal are not twisted, and the white blur may be avoided.

[0030] In the present disclosure, the data lines connect to the control circuit. The voltage of the data lines is changed when the LCD is turned off, such that the voltage difference between the pixel electrode and the common electrode may be balanced. The liquid crystal are not twisted so as to reduce the white blur.

[0031] Referring to FIG. **4**, the display panel may include:

[0032] A first substrate **401**, a second substrate **402**, and a liquid crystal layer between the first substrate **401** and the second substrate **402**, wherein the first substrate **401** is an array substrate includes: a plurality of scanning lines and data lines intersecting with each other so as to define a plurality of pixel areas; a control circuit connecting to the data lines for keeping the voltages on the data lines to be the same with the voltages of the common electrode when the LCD is turned off. In this way, the voltage difference between the pixel electrode and the common electrode may be balanced.

[0033] In one embodiment, the structure of the array substrate may be referenced in the above embodiments.

[0034] In the present disclosure, the data lines connect to the control circuit. The voltage of the data lines is changed when the LCD is turned off, such that the voltage difference between the pixel electrode and the common electrode may be balanced. The liquid crystal are not twisted so as to reduce the white blur.

[0035] It is believed that the present embodiments and their advantages will be understood from the foregoing description, and it will be apparent that various changes may be made thereto without departing from the spirit and scope of the invention or sacrificing all of its material advantages, the examples hereinbefore described merely being preferred or exemplary embodiments of the invention.

What is claimed is:

1. An array substrate, comprising:

a plurality of scanning lines;

a plurality of data lines intersecting with the scanning lines to define a plurality of pixel areas;

a control circuit connecting to the data lines, the control circuit being configured to maintain a voltage on the data lines to be the same with the voltage on a common electrode, and the voltage of the pixel electrode within the pixel areas being the same with the voltages on the data lines so as to balance a voltage difference between the pixel electrode and the common electrode;

wherein the control circuit comprises:

a first control line connecting to a direct-current low voltage;

a second control line connecting to the common electrode;

a plurality of first thin film transistors (TFTs), a gate of the first TFT connects to the first control line, a source of the first TFT connects to the data line, and a drain of the first TFT connects to the second control line;

the pixel area comprises a second TFT, a gate of the second TFT connects to the scanning line, a source of the second TFT connects to the data line, and a drain of the second TFT connects to the pixel electrode.

2. The array substrate as claimed in claim 1, wherein the array substrate further comprises:

a driving circuit comprising a plurality of driving units, first ends of the driving units connect to the direct-current low voltage, and second ends of the driving unit connect to the corresponding scanning line.

3. An array substrate, comprising:

a plurality of scanning lines;

a plurality of data lines intersecting with the scanning lines to define a plurality of pixel areas;

a control circuit connecting to the data lines, the control circuit being configured to maintain a voltage on the data lines to be the same with the voltage on a common electrode, and the voltage of the pixel electrode within the pixel areas being the same with the voltages on the data lines so as to balance a voltage difference between the pixel electrode and the common electrode.

4. The array substrate as claimed in claim 3, wherein the control circuit further comprises:

a first control line connecting to a direct-current low voltage;

a second control line connecting to the common electrode;

a plurality of first thin film transistors (TFTs), a gate of the first TFT connects to the first control line, a source of the first TFT connects to the data line, and a drain of the first TFT connects to the second control line.

5. The array substrate as claimed in claim 4, wherein the pixel area comprises a second TFT, a gate of the second TFT connects to the scanning line, a source of the second TFT connects to the data line, and a drain of the second TFT connects to the pixel electrode.

6. The array substrate as claimed in claim 4, wherein the array substrate further comprises:

a driving circuit comprising a plurality of driving units, first ends of the driving units connect to the direct-current low voltage, and second ends of the driving unit connect to the corresponding scanning line.

7. A display panel, comprising:

a first substrate, a second substrate, and a liquid crystal layer between the first substrate and the second substrate;

wherein the first substrate is an array substrate comprising:

a plurality of scanning lines and data lines intersecting with each other so as to define a plurality of pixel areas;

a control circuit connecting to the data lines for keeping the voltages on the data lines to be the same with the voltages of the common electrode when the display panel is turned off, and the voltage of the pixel electrode within the pixel areas being the same with the voltage on the data lines so as to balance a voltage difference between the pixel electrode and the common electrode.

8. The display panel as claimed in claim 7, wherein the control circuit comprises:

a first control line connecting to a direct-current low voltage;

a second control line connecting to the common electrode;

a plurality of first thin film transistors (TFTs), a gate of the first TFT connects to the first control line, a source of the first TFT connects to the data line, and a drain of the first TFT connects to the second control line.

9. The display panel as claimed in claim 8, wherein the pixel area comprises a second TFT, a gate of the second TFT connects to the scanning line, a source of the second TFT connects to the data line, and a drain of the second TFT connects to the pixel electrode.

10. The display panel as claimed in claim 8, wherein the array substrate further comprises:

a driving circuit comprising a plurality of driving units, first ends of the driving units connect to the direct-current low voltage, and second ends of the driving unit connect to the corresponding scanning line.

11. The display panel as claimed in claim 10, wherein the diving circuit is a gate driver on array (GOA) circuit.

12. The display panel as claimed in claim 10, wherein the direct-current low voltage is a direct-current low voltage ranging from −14 V to −4 V.

13. The display panel as claimed in claim 10, wherein the voltage of the common electrode is 6.5V when the display panel is turned off.

* * * * *

专利名称(译)	阵列基板和显示板		
公开(公告)号	US20190019468A1	公开(公告)日	2019-01-17
申请号	US15/577862	申请日	2017-08-18
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
[标]发明人	SHI LONGQIANG		
发明人	SHI, LONGQIANG		
IPC分类号	G09G3/36		
CPC分类号	G09G3/3655 G09G2320/0242 G09G2320/0204 G09G2310/0245 G09G2330/027		
优先权	201710582439.3 2017-07-17 CN		
外部链接	Espacenet USPTO		

摘要(译)

本公开涉及阵列基板和显示面板。阵列基板包括多条扫描线，以及与扫描线交叉的多条数据线，以限定多个像素区域。阵列基板还包括连接到数据线的控制电路。控制电路被配置为将数据线上的电压维持为与公共电极上的电压相同。像素区域内的像素电极的电压与数据线上的电压相同，以平衡像素电极和公共电极之间的电压差。以这种方式，液晶可以不被扭曲以避免白色模糊。