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CAO(10) **Pub. No.: US 2017/0212397 A1**(43) **Pub. Date: Jul. 27, 2017**(54) **ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY***H01L 27/12* (2006.01)*H01L 29/786* (2006.01)(71) Applicant: **Wuhan China Star Optoelectronics Technology Co., Ltd., Wuhan (CN)**(52) **U.S. Cl.**CPC *G02F 1/136213* (2013.01); *H01L 27/1222* (2013.01); *H01L 27/124* (2013.01); *H01L 27/1255* (2013.01); *H01L 27/1248* (2013.01); *H01L 29/78633* (2013.01); *G02F 1/1368* (2013.01); *G02F 1/13338* (2013.01); *G02F 1/13345* (2013.01); *G02F 1/136227* (2013.01); *G02F 1/133514* (2013.01)(72) Inventor: **Shangcao CAO, Shenzhen (CN)**(73) Assignee: **Wuhan China Star Optoelectronics Technology Co., L td., Wuhan (CN)**(21) Appl. No.: **15/075,188**

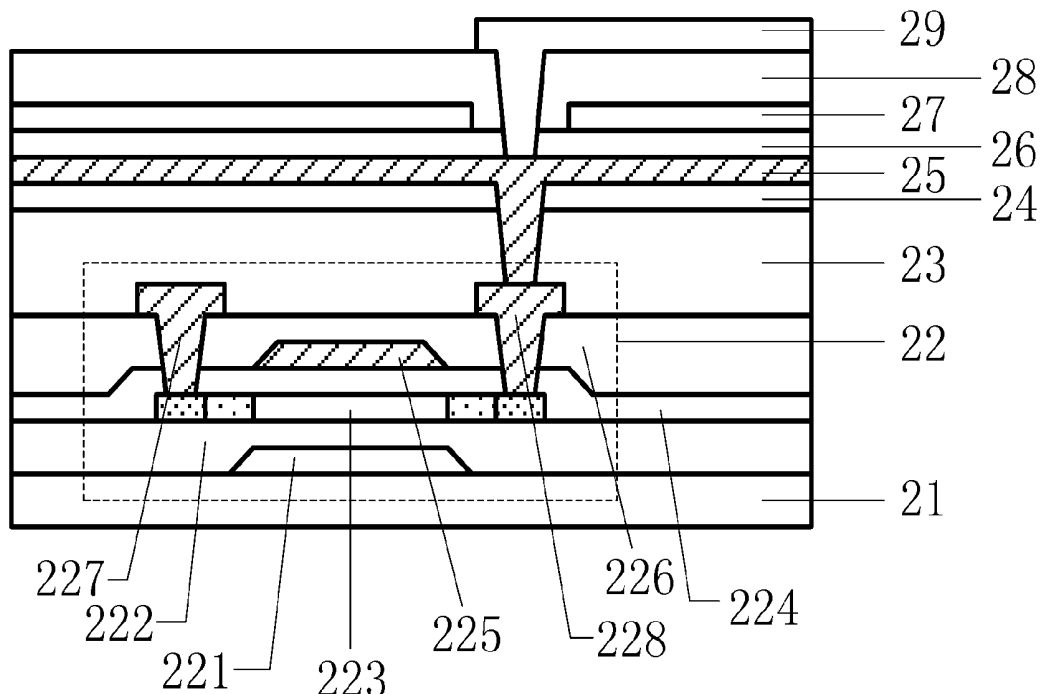
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The present disclosure discloses an array substrate and a liquid crystal display, the array substrate includes: a substrate; a thin film transistor disposed on the substrate; a conductive layer disposed on the thin film transistor and connected with a drain electrode of the thin film transistor; a common electrode disposed on the conductive layer and forming a first capacitor with the conductor layer; a pixel electrode disposed on the common electrode and connected with the conductive layer, the pixel electrode and the common electrode form a second capacitor. By the method above, the disclosure is capable of increasing capacitance of storage capacitors and improving optical performance of a display.



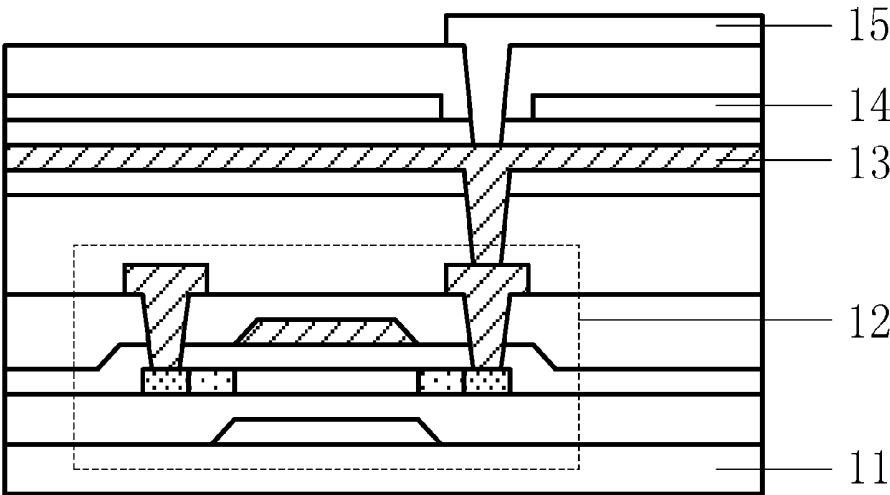


FIG. 1

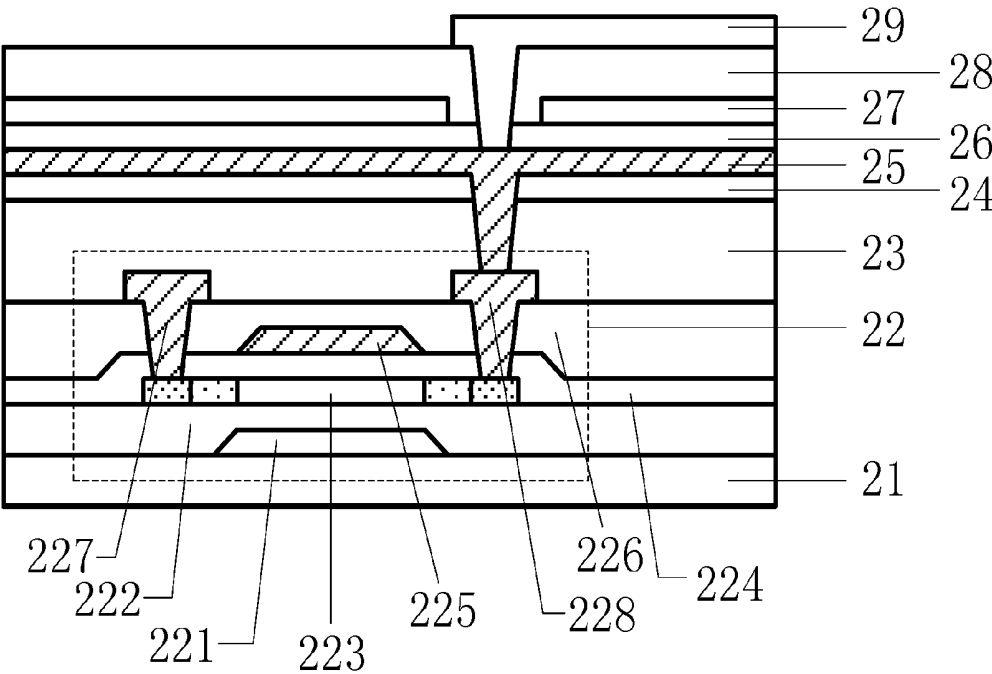


FIG. 2

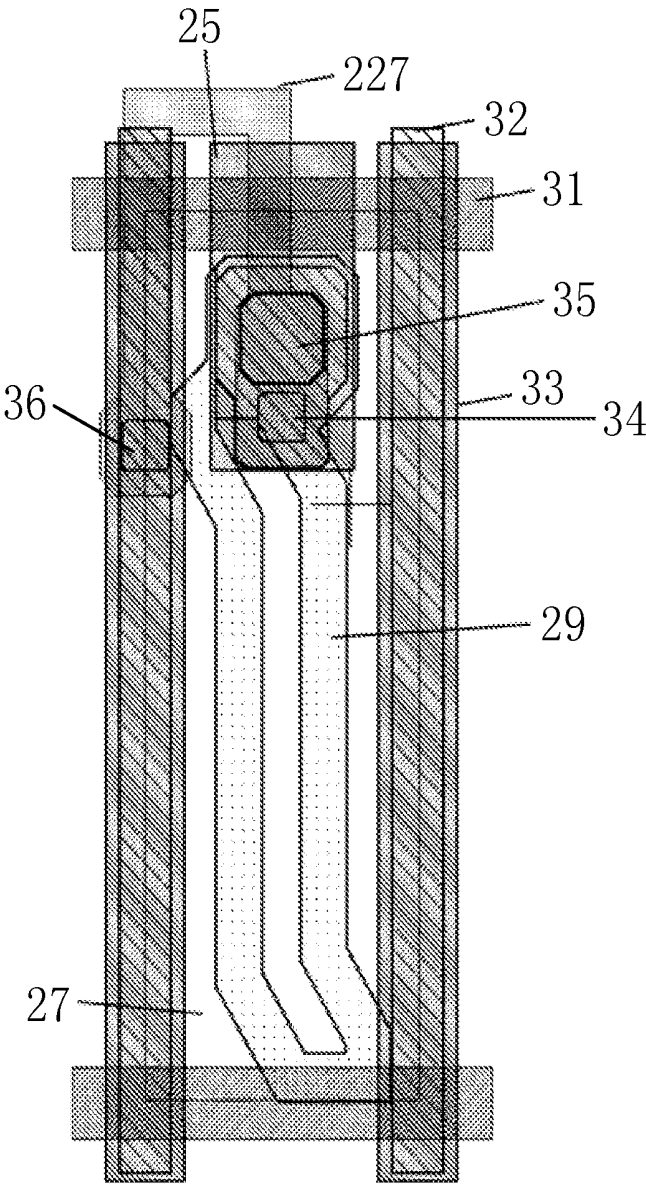


FIG. 3

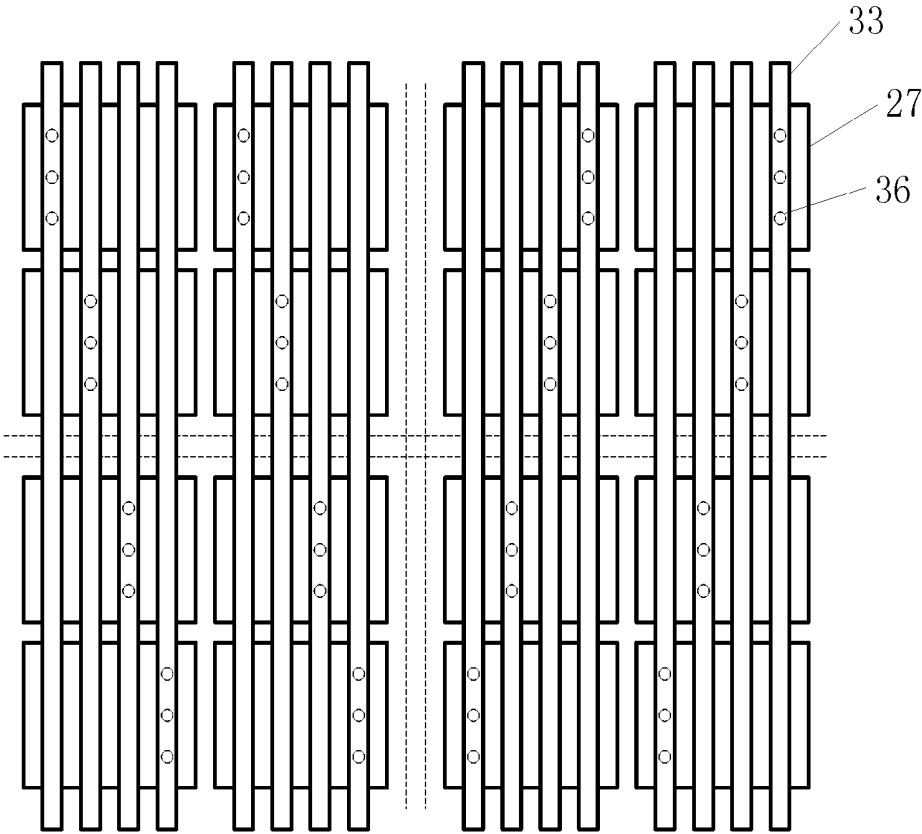


FIG. 4

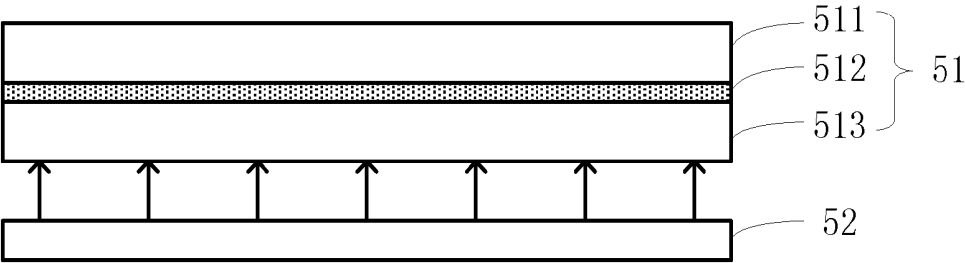


FIG. 5

ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates to a display technology field, and more particularly to an array substrate and a liquid crystal display.

BACKGROUND OF THE DISCLOSURE

[0002] A liquid crystal display (LCD) has a broad market prospect due to its good color display, wide angle of view and high contrast.

[0003] Time for opening each line of thin film transistors is short, which is hard to achieve the response time of liquid crystals, causing flash of a liquid crystal display. Therefore, a liquid crystal display can include a storage capacitor Cst to avoid the problem, a storage capacitor can be formed by a pixel electrode and a common electrode in some liquid crystal displays. Hence the storage capacitor can be applied to maintain the voltage of the pixel electrode after turning off the thin film transistor for a while, and supply longer response time for liquid crystals.

[0004] However, the size of a display needs to be reduced to meet the requirement of thinner, lighter of a liquid crystal display and lower energy consumption, which can cause decrease of a storage capacitor and increase of response time of liquid crystals, flashing in display as a result. Moreover, a display panel produced by fringe field switching (FFS) has a wider angle of view and is insensitive to slight width adjustment of a liquid crystal cell, also known as a hard panel. But a larger storage capacitor is necessary due to TFT in the liquid crystal panel is easily leaking electricity, which can prevent variation of a pixel gray scale in a frame time, the variation of a gray scale can reduce optical property of a liquid crystal panel, such as a cross display and flashing.

SUMMARY OF THE DISCLOSURE

[0005] The technical issue that the disclosure solves is to provide an array substrate and a liquid crystal display, which can increase the capacitance of a capacitor and improve optical property of a display.

[0006] A proposal offered by the present disclosure to solve the technical problem above is: providing an array substrate, the array substrate includes: a substrate; a thin film transistor disposed on the substrate; a conductive layer disposed on the thin film transistor and connected with a drain electrode of the thin film transistor; a common electrode disposed on the conductive layer and forming a first capacitor with the conductor layer; a pixel electrode disposed on the common electrode and connected with the conductive layer, the pixel electrode and the common electrode form a second capacitor.

[0007] An electrical conductivity of the conductive layer is higher than that of the pixel electrode.

[0008] It further includes a touch signal line, the touch signal line and the conductive layer are disposed on the same layer within a same process.

[0009] It further includes: a flat layer covering the thin film transistor; a first insulating layer disposed between the flat layer and the conductive layer; a second insulating layer disposed between the conductive layer and the common electrode; a third insulating layer disposed between the common electrode and the pixel electrode.

[0010] The conductive layer and the drain electrode of the thin film transistor are connected by through-holes of the first insulating layer and the flat layer.

[0011] The pixel electrode and the conductive layer are connected by through-holes of the second insulating layer and the third insulating layer.

[0012] The thin film transistor includes: a light shelter layer disposed on the substrate; a buffer layer covering the light shelter layer and the substrate; a source layer disposed on the buffer layer; a gate insulating layer covering the source layer, comprising a first source electrode through-hole and a first drain electrode through-hole; a gate disposed on the gate insulating layer; an interlayer dielectric layer covering the gate, comprising a second source electrode through-hole corresponding to the first source electrode through-hole and a second drain electrode through-hole corresponding to the first drain electrode through-hole; a source drain layer disposed on the interlayer dielectric layer, comprising a source electrode and a drain electrode, the source electrode and the source layer connected by the first source electrode through-hole and the second source electrode through-hole, the drain electrode and the source layer connected by the first drain electrode through-hole and the second drain electrode through-hole.

[0013] The gate and the source drain layer are metal electrodes.

[0014] The common electrode and the pixel electrode are transparent metallic oxide.

[0015] To solve the technical problem above, another proposal offered by the disclosure is: providing a liquid crystal display, the liquid crystal display includes a backlight and a display panel, the display panel includes an array substrate, a color film substrate and a liquid crystal layer between the array substrate and the color film substrate, the array substrate is the one above.

[0016] Merits of the disclosure: distinguishing from a conventional technique, a drain electrode of a thin film transistor and a pixel electrode are connected by a conductive layer; on one hand, the conductive layer and a common electrode form an extra capacitor, the extra capacitor and a capacitor formed by the original pixel electrode and the common electrode form a larger capacitor by parallel connection, which can increase capacitance of a pixel storage capacitor and voltage maintenance time of the pixel electrode, preventing appearance of flashing effectively and improving display effects; on the other hand, contact resistance between the conductive layer and the drain electrode of the thin film transistor can be reduced significantly, which can prevent errors in contact of the source electrode and the drain electrode of the thin film transistor caused by over etching when the conductive layer is etched.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] FIG. 1 is a structural diagram of an array substrate according to a first embodiment of the present disclosure;

[0018] FIG. 2 is a structural diagram of an array substrate according to a second embodiment of the present disclosure;

[0019] FIG. 3 is a top view of a pixel structure of the array substrate in the second embodiment of the disclosure;

[0020] FIG. 4 is a top view of an array substrate in the second embodiment of the disclosure;

[0021] FIG. 5 is a structural diagram of a liquid crystal display according to an embodiment of the disclosure.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0022] Referring to FIG. 1, a structural diagram of an array substrate according to a first embodiment of the present disclosure, the array substrate includes: a substrate 11; a thin film transistor 12 disposed on the substrate 11; a conductive layer 13 disposed on the thin film transistor 12 and connected with a drain electrode (not labelled) of the thin film transistor 12; a common electrode 14 disposed on the conductive layer 13 and forming a first capacitor Cst1 with the conductor layer 13; a pixel electrode 15 disposed on the common electrode 14 and connected with the conductive layer 13, the pixel electrode 15 and the common electrode 14 form a second capacitor Cst2.

[0023] The drain electrode of the thin film transistor 12 and the conductive layer 13 are metal or metallic oxide, the common electrode 14 and the pixel electrode 15 are transparent metallic oxide, such as indium tin oxide ITO.

[0024] Optionally, the substrate 11 is a transparent glass substrate, in other embodiments, it can also be a transparent plastic substrate.

[0025] Optionally, the thin film transistor 12 can be either a top gate type or a bottom gate type (as shown in FIG. 1), as well as other structures without limitation.

[0026] Specifically, the conductive layer 13 and the common electrode 14 have a corresponding section, a shape and an area of the corresponding section can be set according to practical circumstances. Furthermore, the common electrode 14 and the pixel electrode 15 likewise have a corresponding section, a shape and an area of the corresponding section can be set according to practical circumstances as well.

[0027] Based on a principle of a parallel plate capacitor C , which is $C \propto \epsilon S/d$, where ϵ is a dielectric constant, S is an area of an overlap section of two parallel plates, d is a distance between two parallel plates, the conductive layer 13 and the common electrode 14 can form a first capacitor Cst1, the common electrode 14 and the pixel electrode 15 can form a second capacitor Cst2. Meanwhile, as the conductive layer 13 and the pixel electrode 15 are connected electrically, therefore, the two capacitors Cst1 and Cst2 can be regarded as two parallel connected capacitors. According to a capacitance parallel connection formula: $C = Cst1 + Cst2$, a sum of capacitance of two parallel capacitors is larger than the capacitance of any one of them, therefore, capacitance of a double-layer capacitor formed by the conductive layer 13, the common electrode 14 and the pixel electrode 15 is larger, which can extend voltage maintenance time of the pixel electrode 15, when the size of a pixel is shrunk, flashing can be prevented effectively, which can improve display effects.

[0028] Meanwhile, in a conventional technique, the pixel electrode 15 and the drain electrode of the thin film transistor 12 can be connected electrically, when etching the conductive layer 13, the source electrode and the drain electrode of the thin film transistor 12 can be etched to decrease contact resistance between the pixel electrode 15 and the thin film transistor 12. But in the embodiment, the pixel electrode 15 is connected to the drain electrode of the thin film transistor 12 by the conductive layer 13, on one hand, the contact resistance between conductive layer 13 and the drain electrode of the thin film transistor 12 can be reduced significantly, on the other hand, a contact error can appear in the source electrode and the drain electrode of the thin film transistor 12 caused by over etching.

[0029] Furthermore, compared with the pixel electrode 15, the conductive layer 13 has larger electrical conductivity, which can reduce the connection resistance further.

[0030] Distinguishing from a conventional technique, a drain electrode of a thin film transistor and a pixel electrode are connected by a conductive layer; on one hand, the conductive layer and a common electrode form an extra capacitor, the extra capacitor and a capacitor formed by the original pixel electrode and the common electrode form a larger capacitor by parallel connection, which can increase capacitance of a pixel storage capacitor and voltage maintenance time of the pixel electrode, preventing appearance of flashing effectively and improving display effects; on the other hand, contact resistance between the conductive layer and the drain electrode of the thin film transistor can be reduced significantly, which can prevent errors in contact of the source electrode and the drain electrode of the thin film transistor caused by over etching when the conductive layer is etched.

[0031] Referring to FIG. 2, a structural diagram of an array substrate according to a second embodiment of the present disclosure, the array substrate includes: a substrate 21; a thin film transistor 22 disposed on the substrate 21.

[0032] The thin film transistor 22 includes: a light shelter layer 221 disposed on the substrate 21; a buffer layer 222 covering the light shelter layer 221 and the substrate 21; a source layer 223 disposed on the buffer layer 222; a gate insulating layer 224 covering the source layer 223, comprising a first source electrode through-hole (not labelled) and a first drain electrode through-hole (not labelled); a gate 225 disposed on the gate insulating layer 224; an interlayer dielectric layer 226 covering the gate 225, including a second source electrode through-hole (not labelled) corresponding to the first source electrode through-hole and a second drain electrode through-hole (not labelled) corresponding to the first drain electrode through-hole; a source drain layer disposed on the interlayer dielectric layer 226, including a source electrode 227 and a drain electrode 228, the source electrode 227 and the source layer 223 are connected by the first source electrode through-hole and the second source electrode through-hole, the drain electrode 228 and the source layer 223 are connected by the first drain electrode through-hole and the second drain electrode through-hole. The gate 225 and the source drain layer are metal or metallic oxide.

[0033] Optionally, the buffer layer 222, the gate insulating layer 224 and the interlayer dielectric layer 226 can be SiO_x , SiN_x or a mixture of SiO_x and SiN_x .

[0034] Optionally, the source layer 223 is amorphous silicon (a-Si) or polysilicon (p-Si), two sides of polysilicon contain a lightly doped region N- and a heavily doped region N+ respectively, the source electrode 227 and the heavily doped region of one side are connected, the drain electrode 228 and the heavily doped region of the other side are connected. Moreover, the source layer 223 can be metallic oxide semiconductor, such as indium gallium zinc oxide (IGZO).

[0035] Furthermore, the array substrate further includes: a flat layer 23 covering the thin film transistor 22; a first insulating layer 24 disposed on the flat layer 23; a conductive layer 25 disposed on the first insulating layer 24 and connected with the drain electrode 228 of the thin film transistor 22 by through-holes of the first insulating layer 24 and the flat layer 23; a second insulating layer 26 disposed

on the conductive layer 25; a common electrode 27 disposed on the second insulating layer 26 and forming a first capacitor Cst1 with the conductive layer 25; a third insulating layer 28 disposed on the common electrode 27; a pixel electrode 29 disposed on the third insulating layer 28 and connected with the conductive layer 25 by through-holes of the second insulating layer 26 and the third insulating layer 28, the pixel electrode 29 and the common electrode form a second capacitor Cst2.

[0036] Optionally, the flat layer 23 can be SiO_x , SiN_x or a mixture of SiO_x and SiN_x .

[0037] Optionally, the first insulating layer 24, the second insulating layer 27 and the third insulating layer 29 can be organic insulating layers manufactured by organic materials, for instance, benzocyclobutene.

[0038] Moreover, the array substrate further includes a touch signal line, the touch signal line and the conductive layer 25 are disposed on the same layer within a same process. That is, the touch signal line and the conductive layer 25 are formed in the same coating process, undergoing pattern composition respectively, and they are connected.

[0039] Each layer of the array substrate in the embodiments above can be filmed by physical vapor deposition or chemical vapor deposition without limitation.

[0040] Referring to FIG. 3 and FIG. 4 altogether, FIG. 3 is a top view of a pixel structure of the array substrate in the second embodiment of the disclosure, FIG. 4 is a top view of an array substrate in the second embodiment of the disclosure.

[0041] Besides structures same as ones marked in FIG. 2, others included are: a grid line 31, a data line 32, a touch signal line 33, a through-hole 34 of the interlayer dielectric layer 226, a through-hole 35 of the flat layer 23, through-holes 36 of the conductive layer 25 and the common electrode 27.

[0042] Specifically, during display, the thin film transistor 22 is turned on, since the data line 32 connected with the source electrode 227, data signals is transmitted to the drain electrode 228 by the thin film transistor 22, reaching the conductive layer 25 and the pixel electrode 29. At this time, the conductive layer 25 and the pixel electrode 29 respectively form capacitors with the common electrode 27, capacitance is enlarged by parallel connecting two capacitors and time for charging pixels is extend.

[0043] During touching, the thin film transistor 22 is turned off, touch signals are transmitted to the conductive layer and the pixel electrode 29 by the touch signal line 33. At this time, the conductive layer 25 and the pixel electrode 29 likewise form capacitors respectively with the common electrode 27, capacitance is enlarged by parallel connecting two capacitors and time for charging pixels is extend.

[0044] Distinguishing from a conventional technique, according to the disclosure, a drain electrode of a thin film transistor and a pixel electrode are connected by a conductive layer; on one hand, the conductive layer and a common electrode form an extra capacitor, the extra capacitor and a capacitor formed by the original pixel electrode and the common electrode form a larger capacitor by parallel connection, which can increase capacitance of a pixel storage capacitor and voltage maintenance time of the pixel electrode, preventing appearance of flashing effectively and improving display effects; on the other hand, contact resistance between the conductive layer and the drain electrode of the thin film transistor can be reduced significantly, which

can prevent errors in contact of the source electrode and the drain electrode of the thin film transistor caused by over etching when the conductive layer is etched.

[0045] Referring to FIG. 5, a structural diagram of a liquid crystal display according to an embodiment of the disclosure, the liquid crystal display includes a display panel 51 and a backlight 52, the display panel 51 includes an array substrate 513, a color film substrate 511 and a liquid crystal layer 512 between the array substrate 513 and the color film substrate 511.

[0046] The array substrate 513 is the array substrate in the embodiments above with the same structure. More details are glossed over.

[0047] Above are embodiments of the present disclosure, which does not limit the scope of the present disclosure. Any modifications, equivalent replacements or improvements within the spirit and principles of the embodiment described above should be covered by the protected scope of the disclosure.

What is claimed is:

1. An array substrate, wherein it comprises:
 - a substrate;
 - a thin film transistor disposed on the substrate;
 - a conductive layer disposed on the thin film transistor and connected with a drain electrode of the thin film transistor;
 - a common electrode disposed on the conductive layer and forming a first capacitor with the conductor layer;
 - a pixel electrode disposed on the common electrode and connected with the conductive layer, the pixel electrode and the common electrode forming a second capacitor.
2. The array substrate according to claim 1, wherein an electrical conductivity of the conductive layer is higher than that of the pixel electrode.
3. The array substrate according to claim 2, wherein it further comprises a touch signal line, the touch signal line and the conductive layer are disposed on the same layer within a same process.
4. The array substrate according to claim 1, wherein it further comprises:
 - a flat layer covering the thin film transistor;
 - a first insulating layer disposed between the flat layer and the conductive layer;
 - a second insulating layer disposed between the conductive layer and the common electrode;
 - a third insulating layer disposed between the common electrode and the pixel electrode.
5. The array substrate according to claim 4, wherein the conductive layer and the drain electrode of the thin film transistor are connected by through-holes of the first insulating layer and the flat layer.
6. The array substrate according to claim 4, wherein the pixel electrode and the conductive layer are connected by through-holes of the second insulating layer and the third insulating layer.
7. The array substrate according to claim 1, wherein the thin film transistor comprises:
 - a light shelter layer disposed on the substrate;
 - a buffer layer covering the light shelter layer and the substrate;
 - a source layer disposed on the buffer layer;
 - a gate insulating layer covering the source layer, comprising a first source electrode through-hole and a first drain electrode through-hole;

a gate disposed on the gate insulating layer;
an interlayer dielectric layer covering the gate, comprising a second source electrode through-hole corresponding to the first source electrode through-hole and a second drain electrode through-hole corresponding to the first drain electrode through-hole;

a source drain layer disposed on the interlayer dielectric layer, comprising a source electrode and a drain electrode, the source electrode and the source layer connected by the first source electrode through-hole and the second source electrode through-hole, the drain electrode and the source layer connected by the first drain electrode through-hole and the second drain electrode through-hole.

8. The array substrate according to claim 7, wherein the gate and the source drain layer are metal electrodes.

9. The array substrate according to claim 1, wherein the common electrode and the pixel electrode are transparent metallic oxide.

10. A liquid crystal display, comprising a backlight and a display panel, the display panel comprising an array substrate, a color film substrate and a liquid crystal layer between the array substrate and the color film substrate, wherein the array substrate is one of the array substrates in claim 1.

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专利名称(译)	阵列基板和液晶显示器		
公开(公告)号	US20170212397A1	公开(公告)日	2017-07-27
申请号	US15/075188	申请日	2016-03-20
[标]申请(专利权)人(译)	武汉华星光电技术有限公司		
申请(专利权)人(译)	中国武汉恒星光电科技有限公司.		
当前申请(专利权)人(译)	武汉中国光电科技有限公司		
[标]发明人	CAO SHANGCAO		
发明人	CAO, SHANGCAO		
IPC分类号	G02F1/1362 G02F1/1335 G02F1/1368 G02F1/1333 H01L27/12 H01L29/786		
CPC分类号	G02F1/136213 H01L27/1222 H01L27/124 H01L27/1255 H01L27/1248 G02F1/133514 G02F1/1368 G02F1/13338 G02F1/133345 G02F1/136227 H01L29/78633 G02F2001/134372		
优先权	201610049385.X 2016-01-25 CN		
外部链接	Espacenet USPTO		

摘要(译)

本发明公开了一种阵列基板和液晶显示器，该阵列基板包括：基板；薄膜晶体管设置在基板上；导电层，设置在薄膜晶体管上并与薄膜晶体管的漏极连接；公共电极设置在导电层上并与导电层形成第一电容器；像素电极设置在公共电极上并与导电层连接，像素电极和公共电极形成第二电容器。通过上述方法，本发明能够增加存储电容器的电容并改善显示器的光学性能。

