US 20150179121A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2015/0179121 A1**

(43) **Pub. Date: Jun. 25, 2015**

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(54) **LIQUID CRYSTAL DISPLAY DEVICE**

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(21) Appl. No.: **14/456,811**

(22) Filed: **Aug. 11, 2014**

(30) **Foreign Application Priority Data**

Dec. 20, 2013 (KR) 10-2013-0159949

Publication Classification

(51) **Int. Cl.**
G09G 3/36 (2006.01)

(52) **U.S. Cl.**
CPC ***G09G 3/3688*** (2013.01); ***G09G 3/3659*** (2013.01); *G09G 2310/0272* (2013.01)

(57) **ABSTRACT**

Disclosed is a liquid crystal display (LCD) device. The LCD device include first and second gate lines, data lines, a common electrode line formed between adjacent data lines and configured to perpendicularly cross the plurality of first and second gate lines and divide the plurality of pixel areas into first and second areas, first and second thin film transistors (TFTs) formed between a corresponding first gate line and a second gate line adjacent to the corresponding first gate line, a protective layer configured to include a first contact hole and a second contact hole, a common electrode formed on the protective layer and coupled to the common electrode line through the first contact hole, an insulation layer formed on the protective layer to cover the common electrode and a pixel electrode formed on the insulation layer.

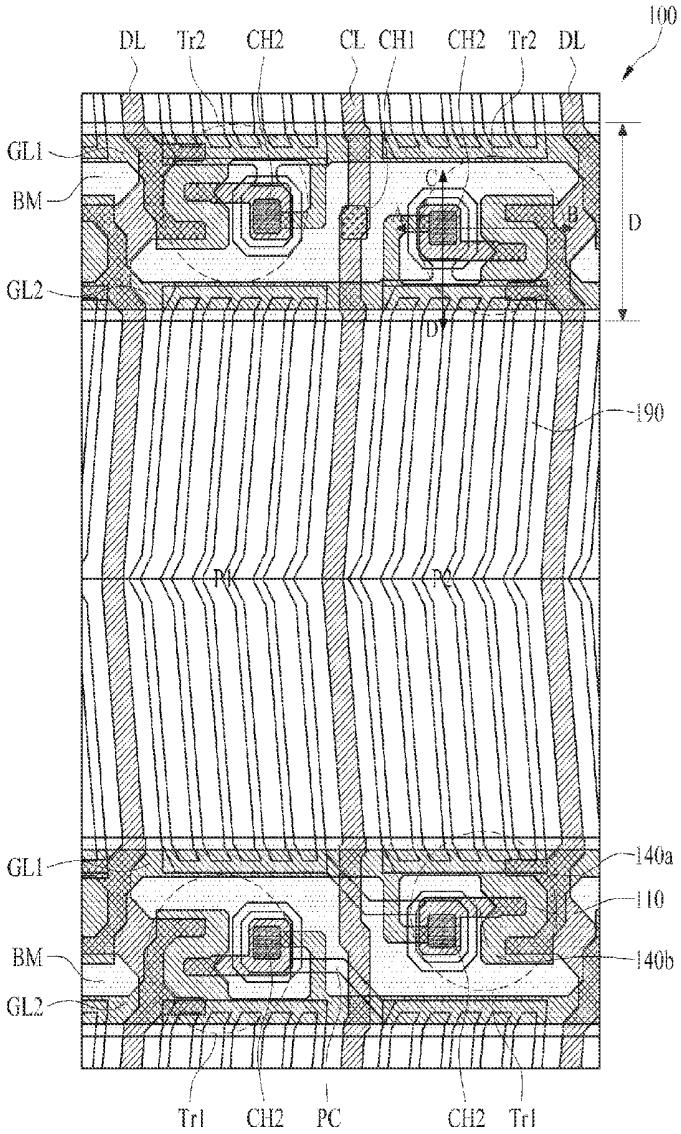


FIG. 1

Related Art

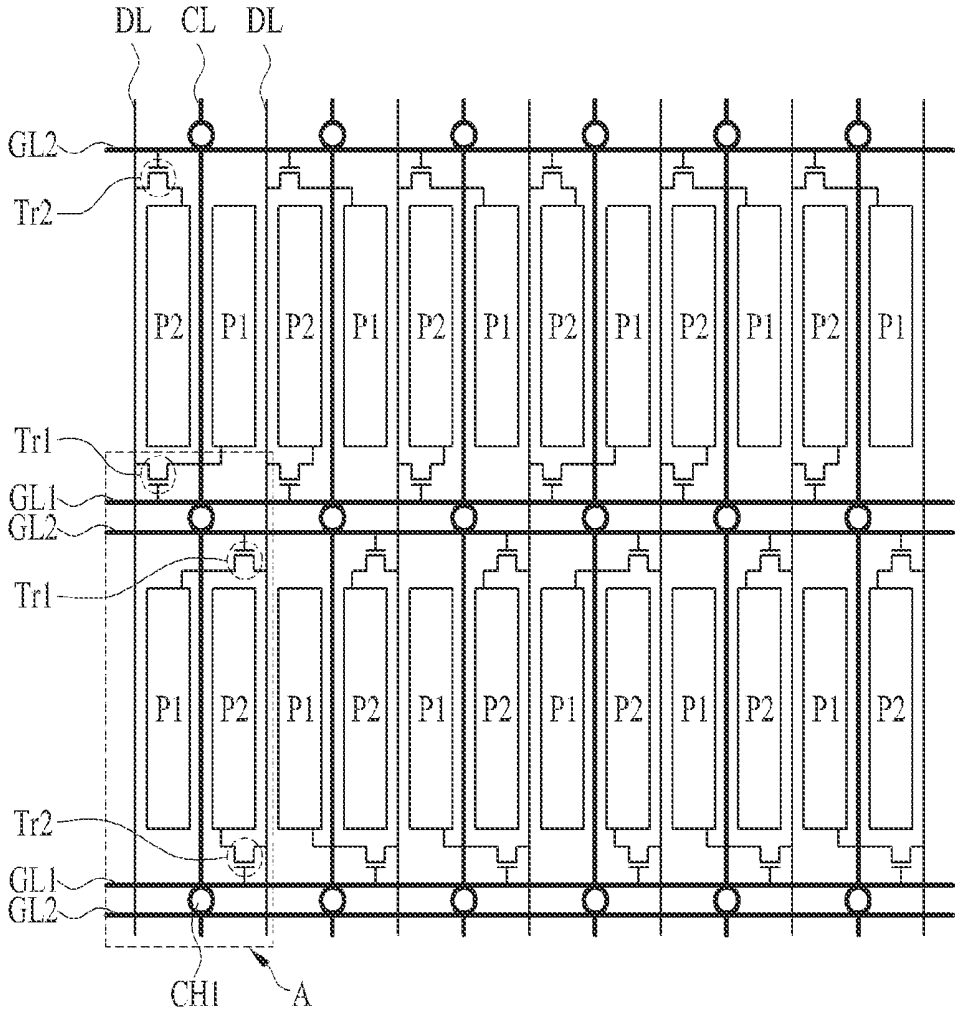


FIG. 2

Related Art

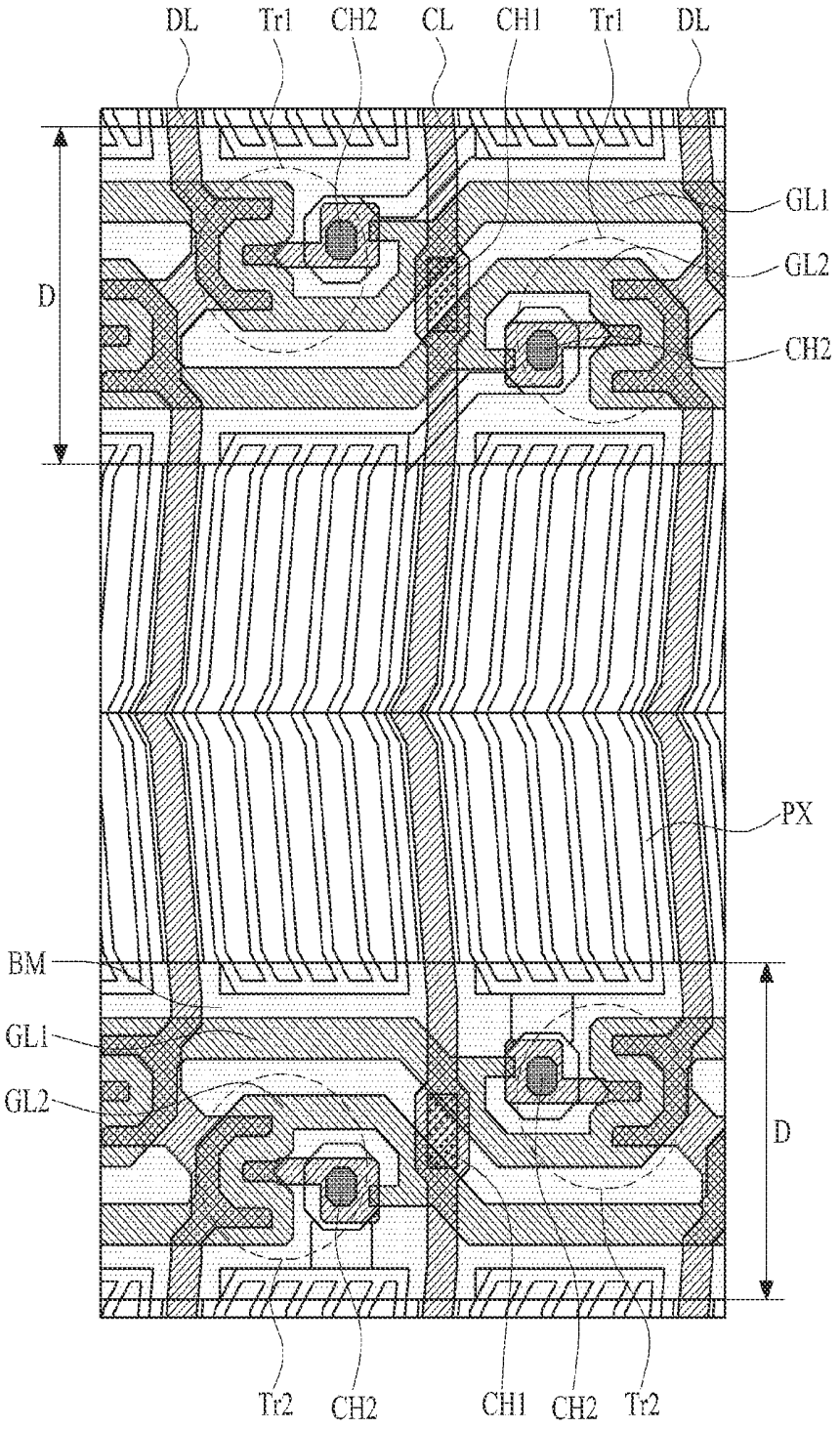


FIG. 3

Related Art

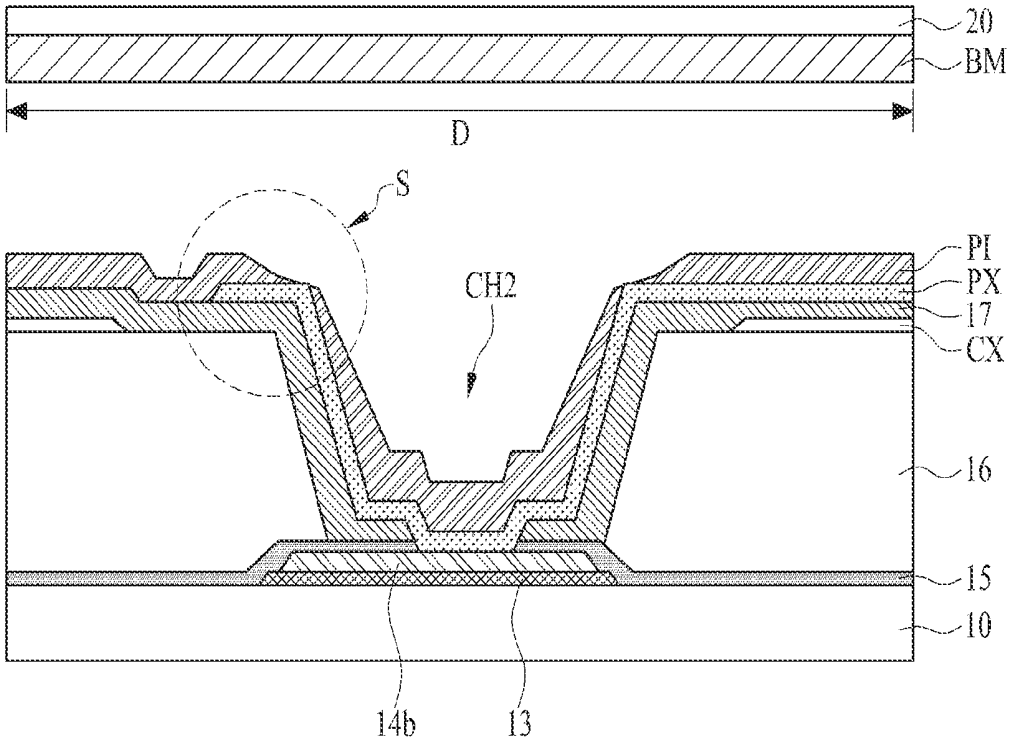


FIG. 4

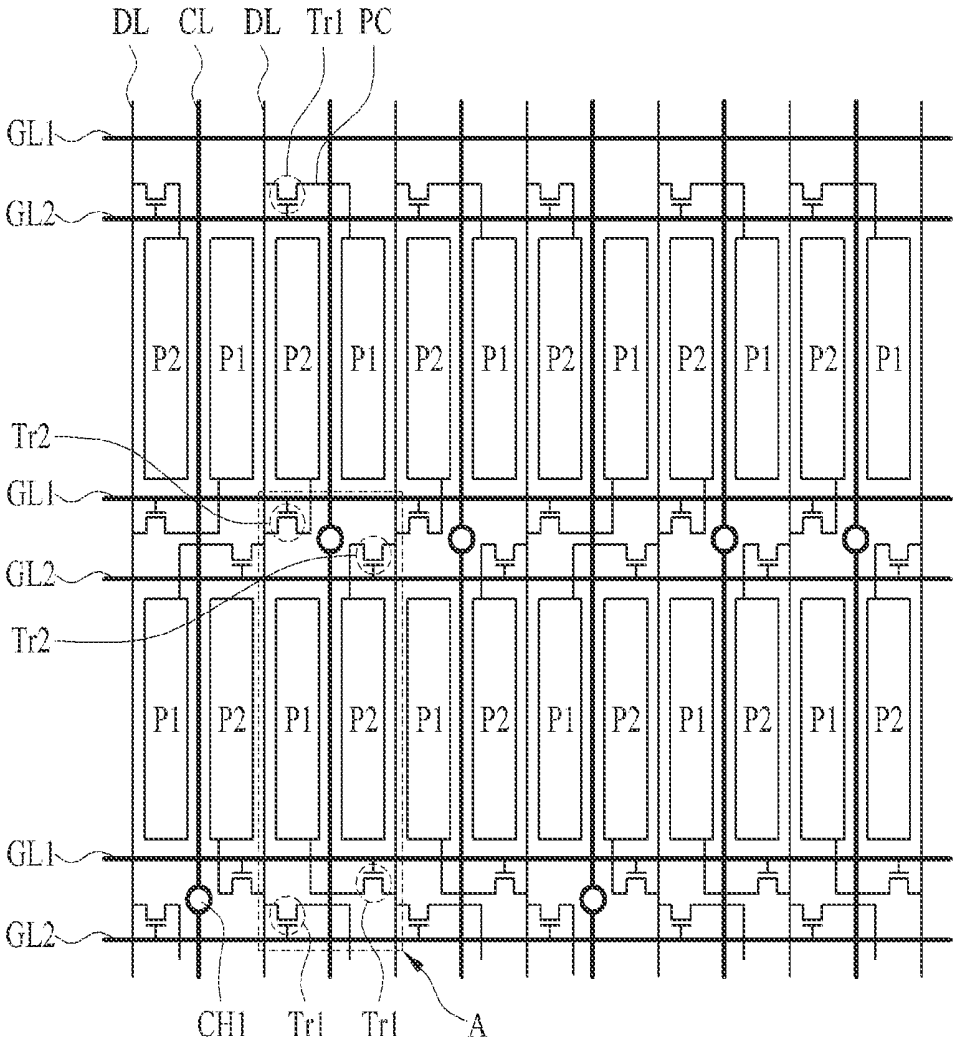

DL
CL
DL
Tr1
PC
GL1
GL2
P2
P1
Tr2
GL1
GL2
Tr2
P1
P2
GL1
GL2
CH1
Tr1
Tr1
A

FIG. 5

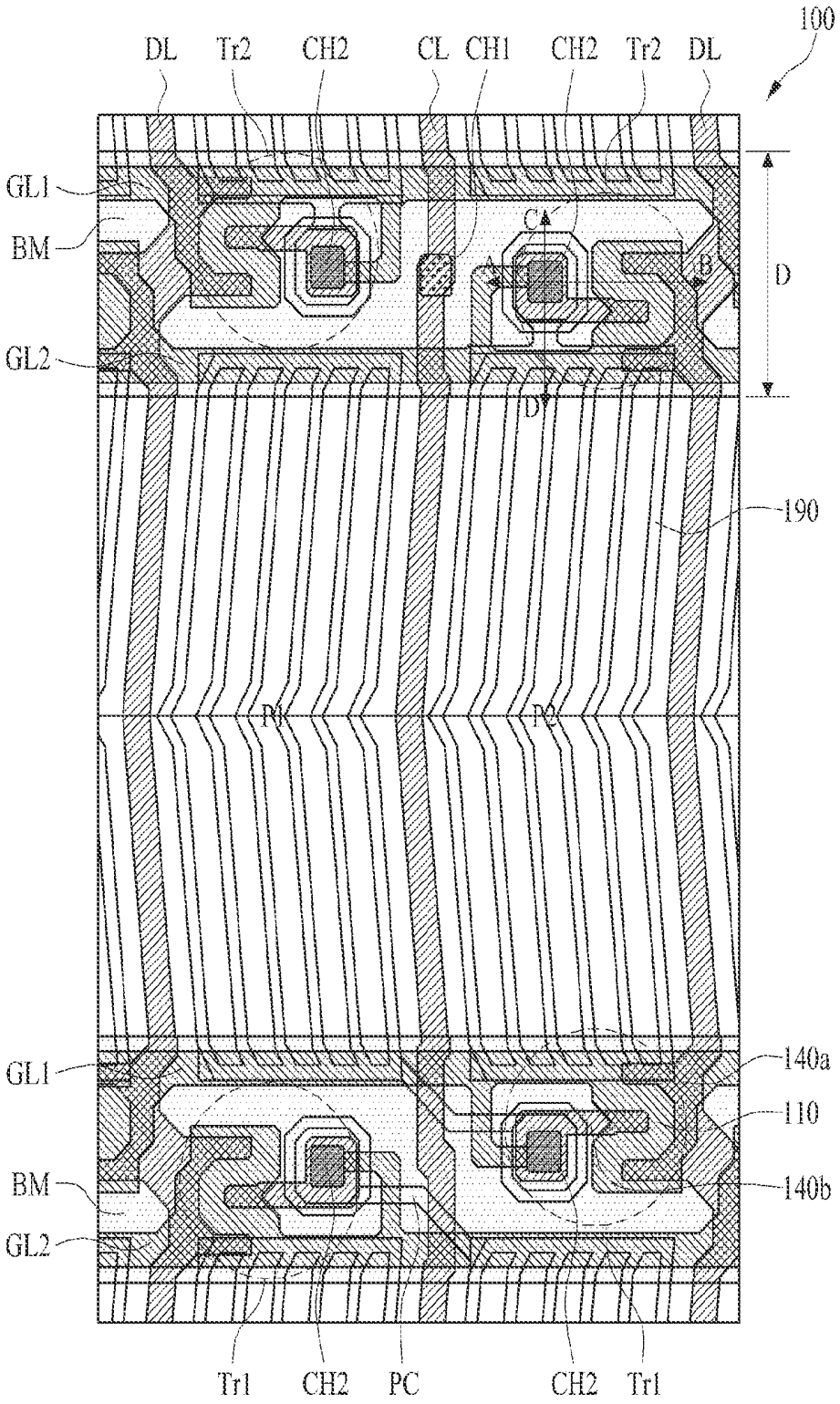

100
DL
Tr2
CH2
CL
CH1
CH2
Tr2
DL
GL1
BM
GL2
C
A
B
D
D'
190
PA
PC
GL1
BM
GL2
140a
110
140b
Tr1
CH2
PC
CH2
Tr1

FIG. 6

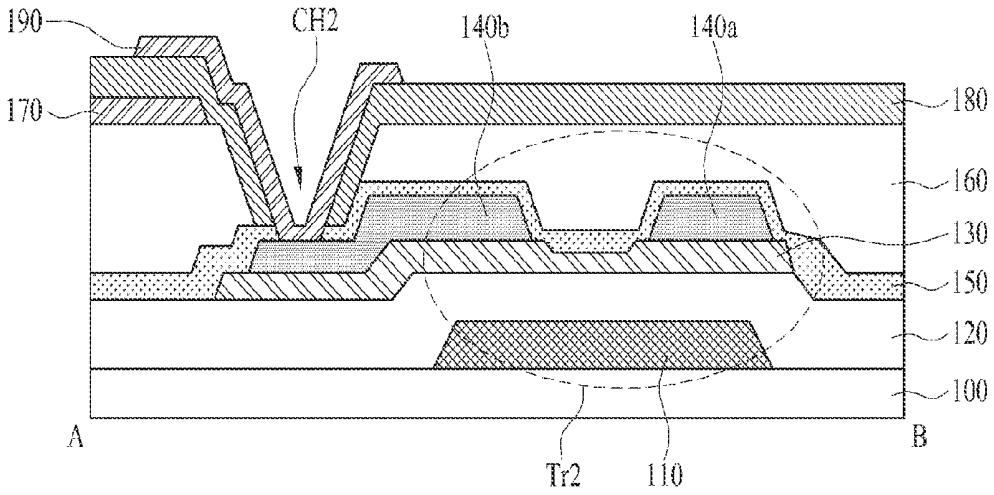
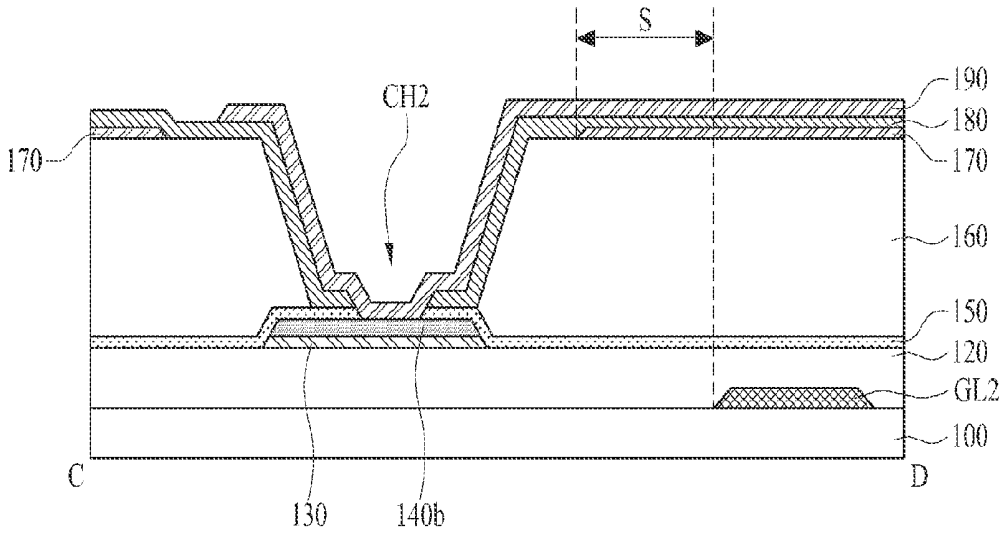

190
CH2
140b
140a
170
180
160
130
150
120
100
A
B
Tr2
110

FIG. 7


S
190
CH2
180
170
170
160
150
120
GL2
100
C
D
130
140b

LIQUID CRYSTAL DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of the Korean Patent Application No. 10-2013-0159949 filed on Dec. 20, 2013, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display (LCD) device, and more particularly, to an LCD device having a double reduced data (DRD) pixel structure for enhancing an aperture ratio.

[0004] 2. Discussion of the Related Art

[0005] In LCD devices, two substrates in which electric field generating electrodes are formed are disposed so that surfaces with the electrodes formed thereon face each other, liquid crystal molecules are injected between the two substrates, a voltage is applied to the electrodes, the liquid crystal molecules are driven by an electric field generated with the voltage, and an image is displayed based on a light transmittance which is changed according to movements of the liquid crystal molecules.

[0006] In the LCD devices, a twisted nematic (TN) mode or an in-plane switching (IPS) mode which is a driving mode of each of the LCD devices is determined depending on positions of a common electrode and pixel electrode of a liquid crystal panel. In particular, the IPS mode, in which the common electrode and the pixel electrode are arranged in parallel on one substrate to generate a lateral electric field, has a broader viewing angle than the TN mode that generates a vertical electrical field.

[0007] Recently, an advanced high-IPS (AH-IPS) mode which is improved from the IPS mode and increases luminance has been proposed. In the AH-IPS mode, the common electrode and the pixel electrode are alternately arranged on different layers on one substrate to generate a fringe field, thereby realizing improved image-quality characteristic over that of the IPS mode.

[0008] The LCD devices include a liquid crystal panel, a gate driving circuit for driving a plurality of gate lines which are formed in the liquid crystal panel, and a data driving circuit for driving a plurality of data lines which are formed in the liquid crystal panel. As sizes of the LCD devices are enlarged and a resolution becomes higher, the number of driving circuits increases.

[0009] However, since the data driving circuit is relatively more expensive than other elements, research and development are done on technology for reducing the number of driving circuits so as to reduce the manufacturing cost of each LCD device. As an example of the technology, a double rate driving (DDR) structure has been proposed. In the DDR structure, although the number of gate lines increase by two times, the number of data lines decreases by half (½), and thus, the number of driving circuits decreases by half, and a resolution is maintained.

[0010] Hereinafter, a related art LCD device having a DRD pixel structure will be described with reference to FIGS. **1** to **3**.

[0011] FIG. **1** is an equivalent circuit of the related art LCD device having the DRD pixel structure, and FIG. **2** is a plan view of the related art LCD device having the DRD pixel structure.

[0012] Referring to FIGS. **1** and **2**, the related art LCD device having the DRD pixel structure includes two gate lines GL**1** and GL**2** which are formed on a substrate, a data line DL which is formed to cross the gate lines GL**1** and GL**2**, and a common electrode line CL which is formed between adjacent data lines DL to cross the gate lines GL**1** and GL**2**.

[0013] A plurality of pixels P**1** and P**2** are defined by the gate lines GL**1** and GL**2**, the data line DL, and the common electrode line CL.

[0014] Each of the plurality of pixels P**1** and P**2** is coupled to the gate lines GL**1** and GL**2** and one data line DL.

[0015] In this case, first and second thin film transistors (TFTs) Tr**1** and Tr**2** which are coupled to the two gate lines GL**1** and GL**2** and the one data line DL are formed outside the two gate lines GL**1** and GL**2**, which are formed in an alternating pattern.

[0016] In detail, the first and second TFTs Tr**1** and Tr**2** are disposed outside the gate lines GL**1** and GL**2**, which are formed to be separated from each other and define pixel areas P**1** and P**2**. The first TFT Tr**1** is coupled to a first gate line GL**1** and a first pixel P**1**, and the second TFT Tr**2** is coupled to a second gate line GL**2** and a second pixel P**2**.

[0017] A first contact hole CH**1**, which connects the common electrode line CL and a common electrode (not shown), is formed between the gate lines GL**1** and GL**2** which are alternately formed. A second contact hole CH**2**, which connects the first and second TFTs Tr**1** and Tr**2** to a pixel electrode PX, is formed outside the gate lines GL**1** and GL**2** which are alternately formed.

[0018] In this case, in order to reduce light leaking around the first and second contact holes CH**1** and CH**2**, a black matrix BM having a certain length D is formed on an upper substrate (not shown) which is provided to face the substrate.

[0019] FIG. **3** is a cross-sectional view of the LCD device of FIG. **2**, and is a view illustrating light leakage which occurs around the second contact hole CH**2**.

[0020] Referring to FIG. **3**, the related art LCD device includes an active layer **13**, a drain electrode **14***b*, a protective layer **16** including the second contact hole CH**2** which exposes the drain electrode **14***b*, a common electrode CX, an insulation layer **17** including the second contact hole CH**2**, a pixel electrode PX which is coupled to the drain electrode **14***b* through the second contact hole CH**2**, and an alignment layer P**1**, which are sequentially formed on a substrate **10**.

[0021] In this case, the alignment layer P**1** flows down to the second contact hole CH**2** due to a flowability of the material forming the alignment layer P**1**, and is non-uniformly formed around the second contact hole CH**2** (see a circular block S). For this reason, light leakage occurs. To prevent the light leakage, the black matrix BM having the certain length D is formed on an upper substrate **20** which is provided to face the substrate **10**.

[0022] In the related art LCD device having the DRD pixel structure, the black matrix BM having the certain length D is formed and covers an opening through which light from a backlight (not shown) passes, causing a reduction in a transmittance of a liquid crystal panel.

SUMMARY

[0023] Accordingly, the present disclosure is directed to provide an LCD device that substantially obviates one or more problems due to limitations and disadvantages of the related art.

[0024] An aspect of the present disclosure is directed to provide an LCD device which has an improved DRD pixel structure and increases an aperture ratio of a liquid crystal panel.

[0025] Additional advantages and features will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the disclosure may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0026] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, there is provided a liquid crystal display (LCD) device including: a plurality of first and second gate lines alternately formed on a substrate in one direction; a plurality of data lines configured to perpendicularly cross the plurality of first and second gate lines to define a plurality of pixel areas; a common electrode line formed between adjacent data lines, the common electrode configured to perpendicularly cross the plurality of first and second gate lines and divide the plurality of pixel areas into first and second areas; first and second thin film transistors (TFTs) formed between a corresponding first gate line and a second gate line adjacent to the corresponding first gate line, the first and second TFTs each including a gate electrode, an active layer, a source electrode, and a drain electrode; a protective layer including a first contact hole exposing the common electrode line and a second contact hole exposing a portion of the drain electrode; a common electrode formed on the protective layer, and coupled to the common electrode line through the first contact hole; an insulation layer formed on the protective layer to cover the common electrode, the insulation layer including the second contact hole exposing the portion of the drain electrode; and a pixel electrode formed on the insulation layer, the pixel electrode coupled to the drain electrode line through the second contact hole.

[0027] A pixel electrode formed in the first area may be coupled to an adjacent first TFT, wherein the common electrode line is between the pixel electrode in the first area and the adjacent first TFT, and a pixel electrode formed in the second pixel area may be coupled to a second TFT formed on the same axis as the pixel electrode, wherein the common electrode line is between the pixel electrode in the second pixel area and the second TFT formed on the same axis.

[0028] The pixel electrode formed in the first area may be coupled to the first TFT by a pixel connection part.

[0029] The first contact hole may be formed in an area adjacent to two of the second TFTs, among a plurality of areas between the first and second gate lines.

[0030] The first and second gate lines are formed as straight lines.

[0031] The second contact hole may be formed between the first and second gate lines.

[0032] The pixel electrode may be formed to overlap the first and second gate lines adjacent to the pixel electrode.

[0033] The common electrode may be formed at a whole surface of each of the plurality of pixel areas except the first contact hole.

[0034] A gate line, a common electrode, and a pixel electrode may be sequentially formed to overlap each other in a peripheral area of the second contact hole, and the common electrode may be formed longer than the gate line in a direction of the second contact hole.

[0035] The common electrode may be formed longer than the gate line by at least 2 μm.

[0036] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiments of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0038] FIG. **1** is an equivalent circuit of the related art LCD device having the DRD pixel structure;

[0039] FIG. **2** is a plan view of the related art LCD device having the DRD pixel structure;

[0040] FIG. **3** is a cross-sectional view of the LCD device of FIG. **2**;

[0041] FIG. **4** is an equivalent circuit of an LCD device having a DRD pixel structure, according to one embodiment;

[0042] FIG. **5** is a plan view schematically illustrating an LCD device according to one embodiment;

[0043] FIG. **6** is a cross-sectional view taken along line A-B of the LCD device of FIG. **5**; and

[0044] FIG. **7** is a cross-sectional view taken along line C-D of the LCD device of FIG. **5**.

DETAILED DESCRIPTION OF THE INVENTION

[0045] Reference will now be made in detail to the exemplary embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0046] In the specification, in adding reference numerals for elements in each drawing, it should be noted that like reference numerals already used to denote like elements in other drawings are used for elements wherever possible.

[0047] The terms described in the specification should be understood as follows.

[0048] As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. The terms "first" and "second" are for differentiating one element from the other element, and these elements should not be limited by these terms.

[0049] It should be further understood that the terms "comprises", "comprising,", "has", "having", "includes" and/or "including", when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0050] The term "on" should be construed as including a case where one element is formed at a top of another element and moreover a case where a third element is disposed therebetween.

[0051] Hereinafter, embodiments of the present invention will be described in detail with reference to the accompanying drawings.

[0052] FIG. **4** is an equivalent circuit of an LCD device having a DRD pixel structure, according to one embodiment.

[0053] As seen in FIG. **4**, the LCD device having the DRD pixel structure according to one embodiment includes a plurality of first and second gate lines GL**1** and GL**2**, which are alternately formed as straight lines in one direction, and a plurality of data lines DL which perpendicularly cross the plurality of first and second gate lines GL**1** and GL**2** to define a plurality of pixel areas.

[0054] A common electrode line CL perpendicularly crosses the plurality of first and second gate lines GL**1** and GL**2**, and is formed between adjacent data lines DL. Also, the common electrode line CL divides the plurality of pixel areas into first and second areas.

[0055] Here, a pixel area formed in the first area is referred to as a first pixel area P**1**, and a pixel area formed in the second area is referred to as a second pixel area P**2**.

[0056] First and second TFTs Tr**1** and Tr**2** are coupled to one data line DL and two gate lines GL**1** and GL**2**.

[0057] Moreover, the first and second TFTs Tr**1** and Tr**2** are formed between two gate lines GL**1** and GL**2** which are alternately formed.

[0058] A pixel electrode formed in the first pixel area P**1** is coupled to an adjacent first TFT Tr**1** with the common electrode line CL between the pixel electrode formed in the first area and the adjacent first TFT TR**1**, and a pixel electrode formed in the second pixel area P**2** is coupled to the second TFT Tr**2**, which is formed on the same axis as that of the pixel electrode, with the common electrode line CL between the second TFT Tr**2** and the common electrode line CL.

[0059] In this case, the first TFT Tr**1** and the pixel electrode which is formed in the first pixel area P**1** are coupled to each other by a pixel connection part PC which is formed across the common electrode line CL.

[0060] That is, the LCD device according to one embodiment uses a DRD type in which liquid crystal cells formed in the pixel areas P**1** and P**2** are driven by using two gate lines GL**1** and GL**2** and one data line DL.

[0061] In this case, according to an embodiment, the first and second TFTs Tr**1** and Tr**2** are formed between the two gate lines GL**1** and GL**2** which are alternately formed as straight lines, thus enlarging each pixel area and increasing an aperture ratio.

[0062] A description of this will be made in detail with reference to FIG. **5**.

[0063] FIG. **5** is a plan view schematically illustrating an LCD device according to one embodiment, and is a plan view of an area A in the equivalent circuit of FIG. **4**. Therefore, like reference numerals refer to like elements throughout, and thus, a description on the same element is not repeated.

[0064] As seen in FIG. **5**, the first and second TFTs Tr**1** and Tr**2**, which each includes a gate electrode **110**, an active layer (not shown), a source electrode **140***a*, and a drain electrode **140***b*, are formed between a first gate line GL**1** and a second gate line GL**2** adjacent to the first gate line GL**1**.

[0065] In more detail, two gate lines GL**1** and GL**2** are formed as straight lines, and the first and second TFTs Tr**1** and Tr**2** are formed inside (i.e., between) the two gate lines GL**1** and GL**2**.

[0066] A contact hole CH**2**, which connects the first and second TFTs Tr**1** and Tr**2** to a pixel electrode **190**, is formed between the two gate lines GL**1** and GL**2**. The pixel electrode **190** is formed to overlap a first gate line GL**1**, which is formed on the pixel area, and a second gate line GL**2** formed under the pixel area.

[0067] In the LCD device according to one embodiment, a plurality of the second contact holes CH**2** may be formed in a direction parallel with each other, and thus, a black matrix BM for covering light leakage in the second contact hole CH**2** may be formed narrower than a related art second contact hole which is obliquely formed.

[0068] That is, a length D of the black matrix BM for covering the second contact hole CH**2** and the two gate lines GL**1** and GL**2** (which are alternately formed) is shorter than that of a related art black matrix, thereby increasing an aperture ratio.

[0069] The related art LCD device shows a transmittance of 3.37%, but the LCD device according to an embodiment of the present disclosure shows a transmittance of 4.41%. That is, according to one embodiment, a transmittance can increase by about 30%.

[0070] A common electrode (not shown) is coupled to the common electrode line CL through a first contact hole CH**1**, and is formed on a whole surface of a pixel area except the first contact hole CH**1**.

[0071] In this case, the first contact hole CH**1** is formed on the common electrode line CL, and particularly, is formed between first and second gate lines GL**1** and GL**2** with the second TFT Tr**2** formed therein. However, the first contact hole CH**1** is not formed between first and second gate lines GL**1** and GL**2** with the first TFT Tr**1** formed therein

[0072] That is, the first contact hole CH**1** is formed in only an area (to which two the second TFTs are adjacent) among a plurality of areas between the first and second gate lines, but is not formed in an area to which two the first TFTs are adjacent.

[0073] The first TFT Tr**1** is coupled to the pixel electrode **190** through a pixel connection part PC. The pixel electrode **190** is formed in the first pixel area P**1** adjacent to the first TFT Tr**1**, with the common electrode line CL between the first TFT Tr**1** and the pixel electrode **190**.

[0074] In this case, when the first contact hole CH**1** is formed between a plurality of the pixel connection parts PC, a distance between the pixel connection parts PC becomes narrow, causing a short-circuit defect. Therefore, the first contact hole CH**1** is not formed between the first and second gate lines GL**1** and GL**2** with the first TFT Tr**1** formed therein.

[0075] FIG. **6** is a cross-sectional view taken along line A-B of the LCD device of FIG. **5**. Like reference numerals refer to like elements throughout, and descriptions of elements described with respect to FIG. **5** are not repeated.

[0076] As seen in FIG. **6**, the LCD device according to an embodiment includes a second TFT Tr**2** formed on a substrate **100**, an inter-layer insulation layer **150** which includes the second TFT Tr**2** and is formed on the substrate **100**, a protective layer **160**, a common electrode **170** formed on the protective layer **160**, an insulation layer **180** which includes the

common electrode **170** and is formed on the protective layer **160**, and a pixel electrode **190** formed on the insulation layer **180**.

[0077] The substrate **100** mainly uses glass, but may use transparent plastic (for example, polyimide) which is bendable or flexible. Polyimide, which endures under a high temperature and has good heat-resistant properties, may be used in the case that a high-temperature deposition process is performed on the substrate **100**.

[0078] The second TFT Tr**2** includes a gate electrode **110**, an active layer **130**, a source electrode **140***a*, and a drain electrode **140***b*.

[0079] The gate electrode **110** is formed as a pattern on the substrate **100**.

[0080] The gate electrode **110** may be patterned simultaneously with the first and second gate lines GL**1** and GL**2**, and may be formed of molybdenum, aluminum, gold, titanium, neodymium, copper, or an alloy thereof. In addition, the gate electrode **110** may be formed of a single layer or multi-layer (which includes two or more layers) of the metal or alloy.

[0081] The gate insulation layer **120** may be formed of an inorganic-based insulating material such as silicon oxide or silicon nitride, but is not limited thereto. For example, the gate insulation layer **120** may be formed of an organic-based insulating material such as photo acryl or benzocyclobutene (BCB).

[0082] The active layer **150** overlaps the gate electrode **110**, and is formed as a pattern on the gate insulation layer **120**.

[0083] The active layer **150** may be formed of an oxide semiconductor such as In—Ga—Zn—O (IGZO), but is not limited thereto.

[0084] The source electrode **140***a* and the drain electrode **140***b* are separated from each other, and are formed as a pattern on the active layer **150** to face each other.

[0085] The inter-layer insulation layer **130**, the protective layer **160**, and the insulation layer **180** include a second contact hole CH**2** which exposes the drain electrode **140***b*.

[0086] The common electrode **170** is formed on the protective layer **160**, and the pixel electrode **190** coupled to the drain electrode **140***b* is formed on the insulation layer **180**.

[0087] FIG. **7** is a cross-sectional view taken along line C-D of the LCD device of FIG. **5**. Like reference numerals refer to like elements throughout, and descriptions of elements described with respect to FIG. **5** are not repeated.

[0088] As shown in FIG. **7**, the LCD device according to an embodiment includes a second gate line GL**2** formed on a substrate **100**, a gate insulation layer **120**, a second TFT Tr**2** including an active layer **130** and a drain electrode **140***b*, an inter-layer insulation layer **150** including a second contact hole CH**2**, a protective layer **160**, an insulation layer **180**, a common electrode **170** which is formed on the protective layer **160**, a common electrode **170** formed on the protective layer **160**, and a pixel electrode **190** which is formed on the insulation layer **180** and is coupled to the drain electrode **140***b*.

[0089] The second gate line GL**2**, the common electrode **170**, and the pixel electrode **190** are formed to overlap each other in a peripheral area of the second contact hole CH**2**, and the common electrode **170** is formed to be longer than the second gate line GL**2** in the second contact hole CH**2** direction.

[0090] In particular, the common electrode **170** may be formed to be longer than the second gate line GL**2** by 2 μm or more.

[0091] In this case, since the second gate line GL**2** and the pixel electrode **190** are formed to overlap each other, a parasitic capacitance is generated. However, since the common electrode **170** is formed between the second gate line GL**2** and the pixel electrode **190**, the parasitic capacitance is not generated.

[0092] However, an overlay of the second gate line GL**2** and the common electrode **170** is twisted, and for this reason, when the common electrode **170** does not cover the second gate line GL**2**, a parasitic capacitance is generated between the second gate line GL**2** and the pixel electrode **190**.

[0093] To prevent such a problem, the common electrode **170** according to an embodiment is formed to be longer than the second gate line GL**2** in the second contact hole CH**2** direction, and for example, may be formed to be longer than the second gate line GL**2** by 2 μm or more.

[0094] As described above, the two gate lines GL**1** and GL**2** are formed as straight lines, and the second contact hole CH**2** which exposes the drain electrode **140***b* is formed between the two gate lines GL**1** and GL**2**. Therefore, a length of the black matrix BM which is formed on the two gate lines GL**1** and GL**2** and the second contact hole CH**2** is reduced, and thus, the aperture ratio of the liquid crystal panel is increased, thereby enhancing a quality of an image produced by the liquid crystal panel.

[0095] Moreover, according to the embodiments of the present disclosure, the second gate line GL**2**, the common electrode **170**, and the pixel electrode **190** are sequentially formed in the peripheral area of the second contact hole CH**2** to overlap each other, and the common electrode **170** is formed to be longer than the second gate line GL**2** in the second contact hole CH**2** direction, thereby decreasing a parasitic capacitance generated between the second gate line GL**2** and the pixel electrode **190**.

[0096] In addition to the aforesaid features and effects, other features and effects of the present disclosure can be newly construed from the embodiments described herein.

[0097] It will be apparent to those skilled in the art that various modifications and variations can be made in the present disclosure without departing from the spirit or scope of the disclosure. Thus, it is intended that the present disclosure covers the modifications and variations of this disclosure provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A liquid crystal display (LCD) device comprising:

a plurality of first and second gate lines alternately formed on a substrate in one direction;

a plurality of data lines configured to perpendicularly cross the plurality of first and second gate lines to define a plurality of pixel areas;

a common electrode line formed between adjacent data lines, the common electrode line configured to perpendicularly cross the plurality of first and second gate lines and divide the plurality of pixel areas into first and second areas;

first and second thin film transistors (TFTs) formed between a corresponding first gate line and a second gate line adjacent to the corresponding first gate line, the first and second TFTs each including a gate electrode, an active layer, a source electrode, and a drain electrode;

a protective layer including a first contact hole exposing the common electrode line and a second contact hole exposing a portion of the drain electrode;

a common electrode formed on the protective layer, and coupled to the common electrode line through the first contact hole;

an insulation layer formed on the protective layer to cover the common electrode, the insulation layer including the second contact hole exposing the portion of the drain electrode; and

a pixel electrode formed on the insulation layer, the pixel electrode coupled to the drain electrode line through the second contact hole.

2. The LCD device of claim **1**, wherein,

a pixel electrode formed in the first area is coupled to an adjacent first TFT, wherein the common electrode line is between the pixel electrode in the first area and the adjacent first TFT, and

a pixel electrode formed in the second pixel area is coupled to a second TFT formed on the same axis as the pixel electrode, wherein the common electrode line is between the pixel electrode in the second area and the second TFT formed on the same axis.

3. The LCD device of claim **2**, wherein the pixel electrode formed in the first area is coupled to the first TFT by a pixel connection part.

4. The LCD device of claim **2**, wherein the first contact hole is formed in an area adjacent to two of the second TFTs, among a plurality of areas between the first and second gate lines.

5. The LCD device of claim **1**, wherein the first and second gate lines are formed as straight lines.

6. The LCD device of claim **1**, wherein the second contact hole is formed between the first and second gate lines.

7. The LCD device of claim **1**, wherein the pixel electrode is formed to overlap the first and second gate lines adjacent to the pixel electrode.

8. The LCD device of claim **1**, wherein the common electrode is formed at a whole surface of each of the plurality of pixel areas except the first contact hole.

9. The LCD device of claim **1**, wherein,

a gate line, a common electrode, and a pixel electrode are sequentially formed to overlap each other in a peripheral area of the second contact hole, and

the common electrode is formed longer than the gate line in a direction of the second contact hole.

10. The LCD device of claim **9**, wherein the common electrode is formed to be longer than the gate line by at least 2 μm.

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专利名称(译)	液晶显示装置		
公开(公告)号	US20150179121A1	公开(公告)日	2015-06-25
申请号	US14/456811	申请日	2014-08-11
[标]申请(专利权)人(译)	乐金显示有限公司		
申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
当前申请(专利权)人(译)	LG DISPLAY CO. , LTD.		
[标]发明人	LEE MIN JIC		
发明人	LEE, MIN JIC		
IPC分类号	G09G3/36		
CPC分类号	G09G3/3688 G09G2310/0272 G09G3/3659 G02F1/136227 G02F1/134363 G09G2300/0426 G09G2300/0434		
优先权	1020130159949 2013-12-20 KR		
其他公开文献	US9448452		
外部链接	Espacenet USPTO		

摘要(译)

公开了一种液晶显示（LCD）装置。 LCD装置包括第一和第二栅极线，数据线，形成在相邻数据线之间并且被配置为垂直地交叉多个第一和第二栅极线并且将多个像素区域划分为第一和第二区域的公共电极线，第一和第二栅极线。第二薄膜晶体管（TFT）形成在相应的第一栅极线和与相应的第一栅极线相邻的第二栅极线之间，保护层配置为包括第一接触孔和第二接触孔，公共电极形成在保护层上通过第一接触孔耦合到公共电极线的绝缘层，形成在保护层上以覆盖公共电极的绝缘层和形成在绝缘层上的像素电极。