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(54) **ARRAY SUBSTRATE AND DRIVING METHOD THEREOF AND LIQUID CRYSTAL PANEL**

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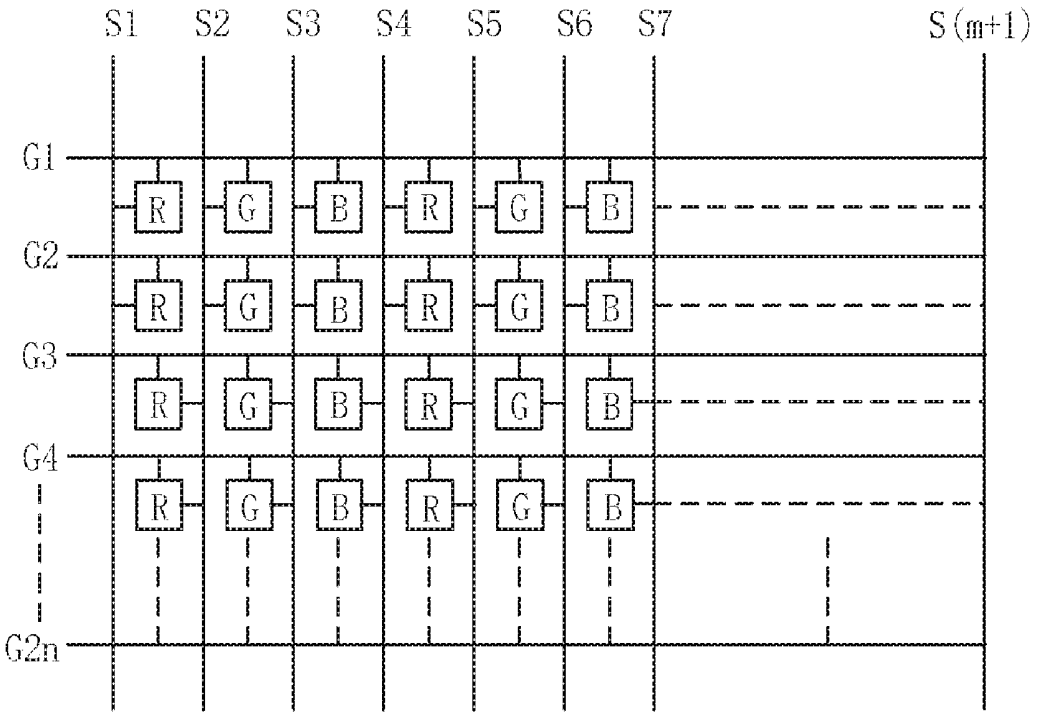
(57) **ABSTRACT**

An array substrate and a driving method thereof and a liquid crystal panel are provided. The array substrate includes plural scan lines, plural data lines and plural sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, in which every two rows of sub-pixels constitutes a unit, sub-pixels in the same column and in the same unit are connected to the same data line, sub-pixels in the same column but respectively in two adjacent units are connected to different data lines, two adjacent columns of sub-pixels in the same unit are connected to different data lines, and two scan lines in the same unit are conducted at the same time.



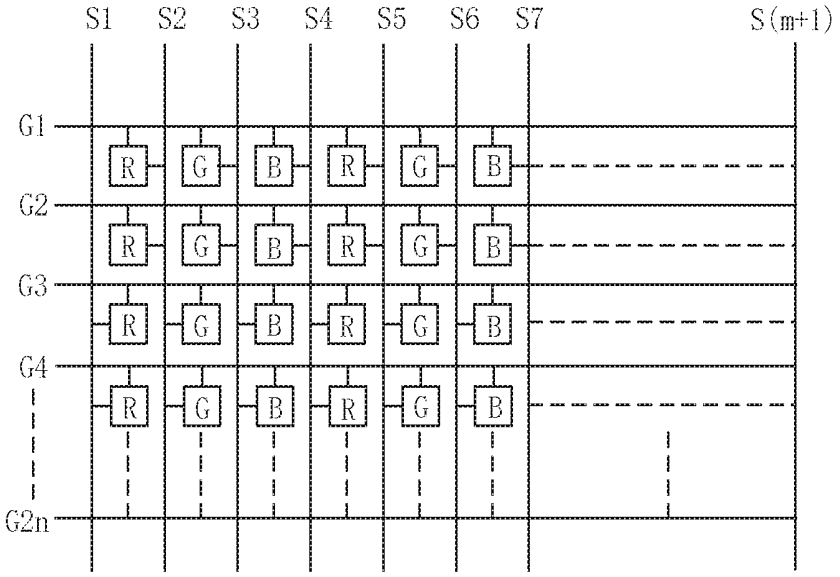

S1
S2
S3
S4
S5
S6
S7
S(m+1)
G1
G2
G3
G4
G2n
R
G
B

FIG. 1

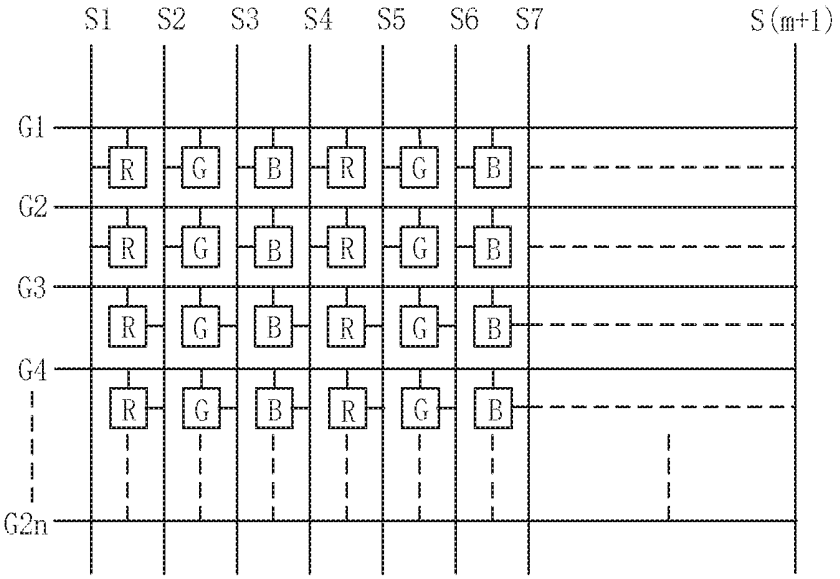

S1
S2
S3
S4
S5
S6
S7
S(m+1)
G1
G2
G3
G4
G2n
R
G
B

FIG. 2

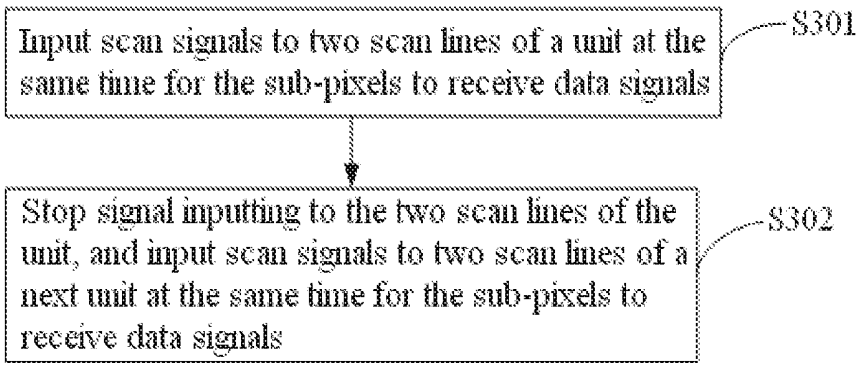

Input scan signals to two scan lines of a unit at the same time for the sub-pixels to receive data signals
S301
Stop signal inputting to the two scan lines of the unit, and input scan signals to two scan lines of a next unit at the same time for the sub-pixels to receive data signals
S302

FIG. 3

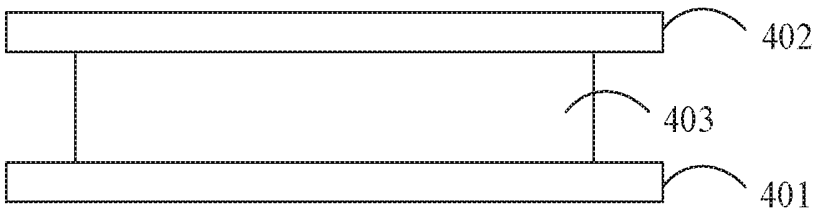

402
403
401

FIG. 4

ARRAY SUBSTRATE AND DRIVING METHOD THEREOF AND LIQUID CRYSTAL PANEL

RELATED APPLICATIONS

[0001] The present application is a National Phase of International Application Number PCT/CN2018/072075, filed Jan. 10,2018, and claims the priority of China Application No. 201711366972.2, filed Dec. 18, 2017.

FIELD OF THE DISCLOSURE

[0002] The present invention relates to a liquid crystal display field, and more particularly, to an array substrate and a driving method thereof and a liquid crystal panel.

BACKGROUND

[0003] Currently, display technology has been developed from two-dimensional (2D) display to three-dimensional (3D) display. A simplest method of the 3D display technology is that a left eye frame signal and a right eye frame signal are sequentially provided from the front end to the back end and a 3D eyeglass is in synchronization with the frame signals, such that the left lens opens when displaying an left eye image and the right lens opens when displaying a right eye image. In such a way, the human brain synthesizes the left eye image and the right eye image to achieve a 3D effect. To avoid any flicker in the screen, the frame rate should be increased to 120 Hz for each of the left eye frames and the right eye frames to have a frame rate of 60 Hz.

[0004] However, data lines of the prior art flip-pixel structure are designed by applying a z-shape layout, and such layout technique would result in transmitting the same data signal to two sub-pixels of different colors to produce cross interferences because the odd and even data lines are conducted simultaneously, which is non-beneficial to 3D display.

SUMMARY

[0005] To solve the aforementioned technical problems, the present invention provides an array substrate and a driving method thereof and a liquid crystal panel, which can solve the problems of cross interferences of data signals in the prior art technology and therefore achieve 3D display.

[0006] In order to solve the aforementioned technical problems, a first technical solution applied in the present disclosure is to provide an array substrate, which includes plural scan lines, plural data lines and plural sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, in which every two rows of sub-pixels constitutes a unit, sub-pixels in the same column and in the same unit are connected to the same data line, sub-pixels in the same column but respectively in two adjacent units are connected to different data lines, two adjacent columns of sub-pixels in the same unit are connected to different data lines, and two scan lines in the same unit are conducted at the same time.

[0007] In order to solve the aforementioned technical problems, a second technical solution applied in the present disclosure is to provide a method of driving an array substrate which includes plural scan lines, plural data lines and plural sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, in which every two rows of sub-pixels constitutes a unit, sub-pixels in the same column and in the same unit are connected to the same data line, sub-pixels in the same column but respectively in two adjacent units are connected to different data lines, and two adjacent columns of sub-pixels in the same unit connected to different data lines. The method includes simultaneously inputting scan signals to two scan lines corresponding to one unit for the sub-pixels to receive data signals, stopping signal inputting to the two scan lines corresponding to the one of the units, and simultaneously inputting scans signal to two scan lines corresponding to a next one unit for the sub-pixels to receive data signals.

[0008] In order to solve the aforementioned technical problems, a third technical solution applied in the present disclosure is to provide a liquid display panel that includes plural scan lines, plural data lines and plural sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, in which every two rows of sub-pixels constitutes a unit, sub-pixels in the same column and in the same unit are connected to the same data line, sub-pixels in the same column but respectively in two adjacent units are connected to different data lines, two adjacent columns of sub-pixels in the same unit are connected to different data lines, and two scan lines in the same unit are conducted at the same time.

[0009] Embodiments of the present invention have the following beneficial effects. In comparison with the prior art technology, in the array substrate according to the embodiments of the present invention, every two rows of sub-pixels constitutes a unit. By conducting two scan lines in a unit at the same time, disconnecting the two scan lines in the unit, and then conducting two scan lines in a next unit simultaneously, and by transmitting the same data signal to two sub-pixels in the same column and in the same unit according to the embodiments of the present invention, data signals can be correctly transmitted to the sub-pixels of the same color, thereby overcoming cross interferences and enhancing 3D display quality of the liquid crystal panel.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1** is a schematic structure diagram of an array substrate according to a first embodiment of the present invention.

[0011] FIG. **2** is a schematic structure diagram of an array substrate according to a second embodiment of the present invention.

[0012] FIG. **3** is a schematic flowchart of a driving method of an array substrate according to an embodiment of the present invention.

[0013] FIG. **4** is a schematic structure diagram of a liquid crystal panel according to an embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0014] A clear and complete description will be given to technical solutions of the embodiments of the present invention with reference to the attached drawings of the embodiments of the present invention. However, the embodiments so described are only some, but not all, of the embodiments of the present invention. Other embodiments that are available to those having ordinary skills of the art without the expense of creative effort and endeavor are considered belonging to the scope of protection of the present invention.

[0015] Please refer to FIG. **1**, FIG. **1** is a schematic structure diagram of an array substrate in accordance with a first embodiment of the present invention. As shown in FIG. **1**, the array substrate includes 2n scan lines G**1**, G**2**, G**3** . . . G**2***n*, m+1 data lines S**1**, S**2**, S**3** . . . S(m+1) and m columns of sub-pixels that are arranged in a matrix and are defined by the scan lines G**1**, G**2**, G**3** . . . G**2***n* and the data lines S**1**, S**2**, S**3** . . . S(m+1), where m and n are all integers larger than or equal to 2. The sub-pixels are divided into units each having two rows of sub-pixels; that is, a first row of sub-pixels and a second row of sub-pixels constitutes a first unit, and a third row of sub-pixels and a fourth row of sub-pixels constitutes a second unit, and so on, and a $(2n-1)^{th}$ row of sub-pixels and a $(2n)^{th}$ row of sub-pixels constitutes an n^{th} unit. Each unit includes two scan lines; that is, the first unit includes two scan lines G**1** and G**2**, and the second unit includes two scan lines G**3** and G**4**, and so on, and the n^{th} unit includes two scan lines G(2n−1) and G**2***n*. Two scan lines in the same unit are conducted simultaneously. Sub-pixels in the same column and in the same unit are connected to the same data line, while two adjacent columns of sub-pixels in the same unit are connected to different data lines. For example, the first column of sub-pixels in the first unit is connected to the same data line S**2**, the second column of sub-pixels in the first unit is connected to the same data line S**3**, the m^{th} column of sub-pixels in the first unit is connected to the same data line S(m+1), the first column of sub-pixels in the second unit is connected to the same data line S**1** the second column of sub-pixels in the second unit is connected to the same data line S**2**, and the m^{th} column of sub-pixels in the second unit is connected to the same data line Sm. Sub-pixels in the same column but respectively in two adjacent units are connected to different data lines. For example, the first column of sub-pixels in the first unit is connected to the data line S**2**, while the first column of sub-pixels in the second unit is connected to the data line S**1**. In the embodiment, scan signals are inputted to the scan lines G**1** and G**2** of the first unit at the same time, such that the first row of sub-pixels and the second row of sub-pixels are conducted to receive data signals from the data lines; then, signal inputting to the two scan lines G**1** and G**2** of the first unit is stopped, and scan signals are inputted to the scan lines G**3** and G**4** of the second unit at the same time, such that the third row of sub-pixels and the fourth row of sub-pixels are conducted to receive data signals from the data lines. In the embodiment, columns of sub-pixels of each odd-numbered unit among the n units are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line, and columns of sub-pixels of each even-numbered unit among the n units are sequentially electrically connected to a first data line through an m^{th} data line. When two scan lines in the same unit are conducted at the same time, data signals are inputted to the plural data lines S**1**, S**2**, S**3**, . . . , S(m+1) at the same time. In the n units, when the scan lines of an odd-numbered unit are conducted, a data signal with a gray level of **0** is inputted to the first data line S**1**; when the scan lines of an even-numbered unit are conducted, a data signal with a gray level of 0 is inputted to the $(m+1)^{th}$ data line S(m+1). The plural data lines S**1**, S**2**, S**3**, . . . S(m+1), the plural scan lines G**1**, G**2**, G**3**, G**2***n* and the plural sub-pixels are in the display area of the array substrate. In the embodiment, the plural sub-pixels includes red pixels (R), green pixels (G) and blue pixels (B), while in another embodiment, the plural sub-pixels may include red pixels (R), green pixels (G), blue pixels (B) and white pixels (W).

[0016] As can be seen from above, in the array substrate according to the embodiments of the present invention, every two rows of sub-pixels constitutes a unit. By conducting two scan lines in a unit at the same time, disconnecting the two scan lines in the unit, and then conducting two scan lines in a next unit at the same time, and by transmitting the same data signal to two sub-pixels in the same column and in the same unit according to the embodiments of the present invention, data signals can be correctly transmitted to the sub-pixels of the same color, thereby overcoming cross interferences and enhancing 3D display quality of the liquid crystal panel.

[0017] Please refer to FIG. **2**, FIG. **2** is a schematic structure diagram of an array substrate in accordance with a second embodiment of the present invention. As shown in FIG. **2**, the array substrate includes 2n scan lines G**1**, G**2**, G**3**, . . . G**2***n*, m+1 data lines S**1**, S**2**, S**3**, . . . , S(m+1) and m columns of sub-pixels that are arranged in a matrix and are defined by the scan lines G**1**, G**2**, G**3**, . . . , G**2***n* and the data lines S**1**, S**2**, S**3**, . . . S(m+1). The sub-pixels are divided into units each having two rows of sub-pixels; that is, a first row of sub-pixels and a second row of sub-pixels constitutes a first unit, and a third row of sub-pixels and a fourth row of sub-pixels constitutes a second unit, and so on, and a $(2n-1)^{th}$ row of sub-pixels and a $(2n)^{th}$ row of sub-pixels constitutes an n^{th} unit. Each unit includes two scan lines; that is, the first unit includes two scan lines G**1** and G**2**, and the second unit includes two scan lines G**3** and G**4**, and so on, and the n^{th} unit includes two scan lines G(2n−1) and G**2***n*. Two scan lines in the same unit are conducted at the same time. Sub-pixels in the same column and in the same unit are connected to the same data line. For example, the first column of sub-pixels in the first unit is connected to the same data line S**1**, the second column of sub-pixels in the first unit is connected to the same data line S**2**, the m^{th} column of sub-pixels in the first unit is connected to the same data line Sm, the first column of sub-pixels in the second unit is connected to the same data line S**2**, the second column of sub-pixels in the second unit is connected to the same data line S**3**, and the m^{th} column of sub-pixels in the second unit is connected to the same data line S(m+1). Sub-pixels in the same column but respectively in two adjacent units are connected to different data lines. For example, the second column of sub-pixels in the first unit is connected to the data line S**2**, while the second column of sub-pixels in the second unit is connected to the data line S**3**. In the embodiment, scan signals are inputted to the scan lines G**1** and G**2** of the first unit at the same time, such that the first row of sub-pixels and the second row of sub-pixels are conducted to receive data signals from the data lines; then, signal inputting to the two scan lines G**1** and G**2** of the first unit is stopped, and scan signals are inputted to the scan lines G**3** and G**4** of the second unit at the same time, such that the third row of sub-pixels and the fourth row of sub-pixels are conducted to receive data signals from the data lines. In the embodiment, columns of sub-pixels of each odd-numbered unit among the n units are sequentially electrically connected to a first data line through an m^{th} data line, and columns of sub-pixels of each even-numbered unit among the n units are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line. When two

scan lines corresponding to each unit are conducted at the same time, data signals are inputted to the plural data lines S1, S2, S3, . . . , S(m+1) at the same time. In the n units, when the scan lines of an odd-numbered unit are conducted, a data signal with a gray level of 0 is inputted to the $(m+1)^{th}$ data line S(m+1); when the scan lines corresponding to the even-numbered units are conducted, a data signal with a gray level of 0 is inputted to the first data line S1. The plural data lines S1, S2, S3, . . . , S(m+1), the plural scan lines G1, G2, G3, . . . G2*n* and the plural sub-pixels are in the display area of the array substrate. In the embodiment, the plural sub-pixels includes red pixels (R), green pixels (G) and blue pixels (B), while in another embodiment, the plural sub-pixels may include red pixels (R), green pixels (G), blue pixels (B) and white pixels (W).

[0018] As can be seen from the above, in the array substrate according to the embodiments of the present invention, every two rows of sub-pixels constitutes a unit. By conducting two scan lines in a unit at the same time, disconnecting the two scan lines in the unit, and then conducting two scan lines in a next unit at the same time, and by transmitting the same data signal to two sub-pixels in the same column and in the same unit according to the embodiments of the present invention, data signals can be correctly transmitted to the sub-pixels of the same color, thereby overcoming cross interferences and enhancing 3D display quality of the liquid crystal panel.

[0019] Please refer to FIG. **3**, FIG. **3** is a schematic flowchart of a method of driving an array substrate according to one embodiment of the present invention. In the following, the detailed process of the method is described in conjunction with FIGS. **1-3**.

[0020] In step S**301**, scan signals are simultaneously inputted to two scan lines of a unit for the sub-pixels to receive data signals.

[0021] In one particular embodiment, as shown in FIG. **1**, the sub-pixels of the array substrate sequentially form n units and are sequentially arranged into m rows, and the data lines are sequentially arranged into (m+1) rows, where m and n are all integers larger than or equal to 2. Scan signals are inputted to the two scan lines G**1** and G**2** of the first unit to conduct the scan lines G**1** and G**2** at the same time, and data signals are inputted to the plural data lines S**1**, S**2**, S**3**, . . . , S(m+1) at the same time. For example, the scan lines G**1** and G**2** are conducted at the same time, and data signals of gray levels respectively being 10, 8, 27, 16, are inputted to the data lines S**1**, S**2**, S**3**, S**4**, . . . at the same time, such that the first row of sub-pixels, the second row of sub-pixels, the third row of sub-pixels, . . . in the first unit respectively obtain the data signals of gray levels respectively being 8, 27, 16, ... The sub-pixels of each odd-numbered unit are neither connected with the first data line S**1**, and therefore, when the scan lines of an odd-numbered unit are conducted, the data signal with a gray level of 10 inputted to the first data line S**1** is not shown. In another particular embodiment, a data signal with a gray level from 0 to 255 and other than 10 may be inputted to the first data line S**1** before the scan lines of an odd-numbered unit are conducted.

[0022] In another particular embodiment, as shown in FIG. **2**, the sub-pixels of the array substrate sequentially form n units and are sequentially arranged into m rows, and the data lines are sequentially arranged into (m+1) rows, where m and n are all integers larger than or equal to 2. Scan signals are inputted to the two scan lines G**1** and G**2** of the first unit to conduct the scan lines G**1** and G**2** at the same time, and data signals are inputted to the plural data lines S**1**, S**2**, S**3**, . . . , S(m+1) at the same time. For example, the scan lines G**1** and G**2** are conducted at the same time, and data signals of gray levels respectively being 10, 8, 27, 16, . . . are inputted to the data lines S**1**, S**2**, S**3**, S**4**, . . . at the same time, such that the first row of sub-pixels, the second row of sub-pixels, the third row of sub-pixels, the fourth row of sub-pixels, in the first unit respectively obtain the data signals of gray levels respectively being 10, 8, 27, 16 . . . . In another particular embodiment, scan signals are inputted to the two scan lines G**1** and G**2** corresponding to the first unit simultaneously to conduct the scan lines G**1** and G**2** at the same time, and data signals of gray levels respectively being 10, 8, 27, 16, . . . are inputted to the data lines S(m+1), Sm, S(m−1), S(m−2), . . . at the same time, such that the $(m+1)^{th}$ column of sub-pixels, the m^{th} column of sub-pixels, the $(m-1)^{th}$ column of sub-pixels, the $(m-2)^{th}$ column of sub-pixels, . . . in the first unit respectively obtain the data signals of gray levels respectively being 10, 8, 27, 16, ... The sub-pixels of each odd-numbered unit are neither connected with the $(m+1)^{th}$ data line S(m+1), and therefore, when the scan lines of an odd-numbered unit are conducted, the data signal with a gray level of 10 inputted to the $(m+1)^{th}$ data line S(m+1) is not shown. In another particular embodiment, a data signal with a gray level from 0 to 255 and other than 10 may be inputted to the $(m+1)^{th}$ data line before the scan lines of an odd-numbered unit are conducted.

[0023] In step S**302**, signal inputting to the two scan lines corresponding to the unit is stopped, and scan signals are inputted to two scan lines of a next unit at the same time for the sub-pixels to receive data signals.

[0024] In one particular embodiment, as shown in FIG. **1**, in step S**301**, the scan lines G**1** and G**2** are conducted at the same time, and data signals of gray levels respectively being 10, 8, 27, 16, . . . are inputted to the data lines S**1**, S**2**, S**3**, S**4**, . . . at the same time, such that the first row of sub-pixels, the second row of sub-pixels, the third row of sub-pixels, . . . in the first unit respectively obtain the data signals of gray levels respectively being 8, 27, 16, ... In step S**302**, scan signal inputting to the two scan lines G**1** and G**2** of the first unit is stopped, i.e., the scan lines G**1** and G**2** are disconnected at the same time, and scan signals are inputted to the two scan lines G**3** and G**4** of the second unit to conduct the scan lines G**3** and G**4** at the same time, and data signals of gray levels respectively being 23, 57, 88, 99, . . . are inputted to the data lines S**1**, S**2**, S**3**, S**4**, . . . , such that the first row of sub-pixels, the second row of sub-pixels, the third row of sub-pixels, the fourth row of sub-pixels, . . . in the second unit respectively obtain the data signals of gray levels respectively being 23, 57, 88, 99, ... In another particular embodiment, the scan lines G**3** and G**4** are conducted at the same time, and data signals of gray levels respectively being **23**, **57**, **88**, **99**, . . . , are inputted to the data lines S(m+1), Sm, S(m−1), S(m−2), . . . at the same time, such that the $(m+1)^{th}$ column of sub-pixels, the m^{th} column of sub-pixels, the $(m-1)^{th}$ column of sub-pixels, the $(m-2)^{th}$ column of sub-pixels, . . . in the second unit respectively obtain the data signals of gray levels respectively being 23, 57, 88, 99, ... The sub-pixels of each even-numbered unit are neither connected with the $(m+1)^{th}$ data line S(m+1), and therefore, when the scan lines of an even-numbered unit are conducted, the data signal with a gray level of 23 inputted to the $(m+1)^{th}$ data line S(m+1) is not shown. In another particular embodi-

ment, a data signal with a gray level from 0 to 255 and other than 23 may be inputted to the $(m+1)^{th}$ data line S(m+1) before the scan lines of an even-numbered unit are conducted.

[0025] In another particular embodiment, as shown in FIG. **2**, in step S**301**, the scan lines G**1** and G**2** are conducted at the same time, and data signals of gray levels respectively being 10, 8, 27, 16, . . . are inputted to the data lines S**1**, S**2**, S**3**, S**4**, . . . at the same time, such that the first row of sub-pixels, the second row of sub-pixels, the third row of sub-pixels, . . . in the first unit respectively obtain the data signals of gray levels respectively being 8, 27, 16, ... In step S**302**, scan signal inputting to the two scan lines G**1** and G**2** of the first unit is stopped, i.e., the scan lines Gi and G**2** are disconnected at the same time, and scan signals are inputted to the two scan lines G**3** and G**4** of the second unit to conduct the scan lines G**3** and G**4** at the same time, and data signals of gray levels respectively being 23, 57, 88, 99, . . . are inputted to the data lines S**1**, S**2**, S**3**, S**4**, . . . , such that the first row of sub-pixels, the second row of sub-pixels, the third row of sub-pixels, . . . in the second unit respectively obtain the data signals of gray levels respectively being 57, 88, 99, ... The sub-pixels of each even-numbered unit are neither connected with the first data line S**1**, and therefore, when the scan lines of an even-numbered unit are conducted, the data signal with a gray level of 23 inputted to the first data line S**1** is not shown. In another particular embodiment, a data signal with a gray level from 0 to 255 and other than 23 may be inputted to the first data line S**1** before the scan lines of an even-numbered unit are conducted.

[0026] The above steps are repeated to sequentially input data signals to the sub-pixels in each unit, thereby achieving the goal of 3D display.

[0027] Please refer to FIG. **4**, FIG. **4** is a schematic structure diagram of a liquid crystal panel according to one embodiments of the present invention. As shown in FIG. **4**, the liquid crystal panel includes an array substrate **401**, a color filter substrate **402** and a liquid crystal layer **403** that is disposed between the array substrate **401** and the color filter substrate **402**, in which the array substrate **401** is the array substrate of any embodiment mentioned above.

[0028] In comparison with the prior art technology, in the array substrate according to the embodiments of the present invention, every two rows of sub-pixels constitutes a unit. By conducting two scan lines in a unit at the same time, disconnecting the two scan lines in the unit, and then conducting two scan lines in a next unit at the same time, and by transmitting the same data signal to two sub-pixels in the same column and in the same unit according to the embodiments of the present invention, data signals can be correctly transmitted to the sub-pixels of the same color, thereby overcoming cross interferences and enhancing 3D display quality of the liquid crystal panel.

[0029] It is believed that the present embodiments and their advantages will be understood from the foregoing description, and it will be apparent that various changes may be made thereto without departing from the spirit and scope of the invention or sacrificing all of its material advantages, the examples hereinbefore described merely being preferred or exemplary embodiments of the invention.

What is claimed is:

1. An array substrate comprising a plurality of scan lines, a plurality of data lines and a plurality of sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, wherein every two rows of sub-pixels constitutes a unit, sub-pixels in the same column and in the same unit are connected to the same data line, sub-pixels in the same column but respectively in two adjacent units are connected to different data lines, two adjacent columns of sub-pixels in the same unit are connected to different data lines, and two scan lines in the same unit are conducted at the same time.

2. The array substrate according to claim **1**, wherein the sub-pixels sequentially form n units, and the sub-pixels are sequentially arranged in m columns, and the data lines are sequentially arranged in m+1 columns, wherein each of m and n is an integer larger than or equal to 2.

3. The array substrate according to claim **2**, wherein in the n units, columns of sub-pixels of each odd-numbered unit are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line, and columns of sub-pixels of each even-numbered unit are sequentially electrically connected to a first data line through an m^{th} data line.

4. The array substrate according to claim **3**, wherein in the n units, when the scan lines of one of the odd-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the first data line, and when the scan lines of one of the even-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the $(m+1)^{th}$ data line.

5. The array substrate according to claim **2**, wherein in the n units, columns of sub-pixels of each odd-numbered unit are sequentially electrically connected to a first data line through an m^{th} data line, and columns of sub-pixels of each even-numbered unit are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line.

6. The array substrate according to claim **5**, wherein in the n units, when the scan lines of one of the odd-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the $(m+1)^{th}$ data line, and when the scan lines of one of the even-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the first data line.

7. The array substrate according to claim **1**, wherein the sub-pixels comprise red pixels, green pixels and blue pixels.

8. The array substrate according to claim **1**, wherein the sub-pixels comprise red pixels, green pixels, blue pixels and white pixels.

9. A method of driving an array substrate, the array substrate having a plurality of scan lines, a plurality of data lines and a plurality of sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, every two rows of sub-pixels constituting a unit, sub-pixels in the same column and in the same unit connected to the same data line, sub-pixels in the same column but respectively in two adjacent units connected to different data lines, and two adjacent columns of sub-pixels in the same unit connected to different data lines, wherein the method comprises:

inputting scan signals to two scan lines of one of the units at the same time for the sub-pixels to receive data signals; and

stopping signal inputting to the two scan lines of the one of the units, and inputting scan signals to two scan lines of a next one of the units at the same time for the sub-pixels to receive data signals.

10. The method according to claim **9**, wherein the sub-pixels sequentially form n units, and the sub-pixels are

sequentially arranged in m columns, and the data lines are sequentially arranged in m+1 columns, wherein each of m and n is an integer larger than or equal to 2.

11. The method according to claim **10**, wherein in the n units, columns of sub-pixels of each odd-numbered unit are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line, and columns of sub-pixels of each even-numbered unit are sequentially electrically connected to a first data line through an m^{th} data line.

12. The method according to claim **11**, wherein in the n units, when the scan lines corresponding to one of the odd-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the first data line, and when the scan lines corresponding to one of the even-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the $(m+1)^{th}$ data line.

13. The method according to claim **10**, wherein in the n number of units, columns of sub-pixels of each odd-numbered unit are sequentially electrically connected to a first data line through an m^{th} data line, and columns of sub-pixels of each even-numbered unit are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line.

14. The method according to claim **13**, wherein in the n number of units, when the scan lines corresponding to one of the odd-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the $(m+1)^{th}$ data line, and when the scan lines corresponding to one of the even-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the first data line.

15. A liquid crystal panel comprising an array substrate that comprises a plurality of scan lines, a plurality of data lines and a plurality of sub-pixels that are arranged in a matrix and are defined by the scan lines and the data lines, wherein every two rows of sub-pixels constitutes a unit, sub-pixels in the same column and in the same unit are connected to the same data line, sub-pixels in the same column but respectively in two adjacent units are connected to different data lines, two adjacent columns of sub-pixels in the same unit are connected to different data lines, and two scan lines in the same unit are conducted at the same time.

16. The liquid crystal panel according to claim **15**, wherein the sub-pixels sequentially form n units, and the sub-pixels are sequentially arranged in m columns, and the data lines are sequentially arranged in m+1 columns, wherein each of m and n is an integer larger than or equal to 2.

17. The liquid crystal panel according to claim **16**, wherein in the n units, columns of sub-pixels of each odd-numbered unit are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line, and columns of sub-pixels of each even-numbered unit are sequentially electrically connected to a first data line through an m^{th} data line.

18. The liquid crystal panel according to claim **17**, wherein in the n units, when the scan lines of one of the odd-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the first data line, and when the scan lines of one of the even-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the $(m+1)^{th}$ data line.

19. The liquid crystal panel according to claim **16**, wherein in the n number of units, columns of sub-pixels of each odd-numbered unit are sequentially electrically connected to a first data line through an m^{th} data line, and columns of sub-pixels of each even-numbered unit are sequentially electrically connected to a second data line through an $(m+1)^{th}$ data line.

20. The liquid crystal panel according to claim **19**, wherein in the n number of units, when the scan lines of one of the odd-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the $(m+1)^{th}$ data line, and when the scan lines of one of the even-numbered units are conducted, a data signal with a gray level from 0 to 255 is inputted to the first data line.

* * * * *

专利名称(译)	阵列基板及其驱动方法和液晶面板		
公开(公告)号	US20190187526A1	公开(公告)日	2019-06-20
申请号	US15/748780	申请日	2018-01-10
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
[标]发明人	WU YU		
发明人	WU, YU		
IPC分类号	G02F1/1362 G09G3/36		
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优先权	201711366972.2 2017-12-18 CN		
其他公开文献	US10690980		
外部链接	Espacenet USPTO		

摘要(译)

提供一种阵列基板及其驱动方法和液晶面板。阵列基板包括多条扫描线，多条数据线和多个子像素，它们以矩阵排列并由扫描线和数据线限定，其中每两行子像素构成一个单位子像素在同一列和同一单元中连接到同一数据线，同一列中的子像素但分别在两个相邻单元中连接到不同的数据线，同一单元中的两个相邻列的子像素连接对于不同的数据线，同一单元中的两条扫描线同时进行。