



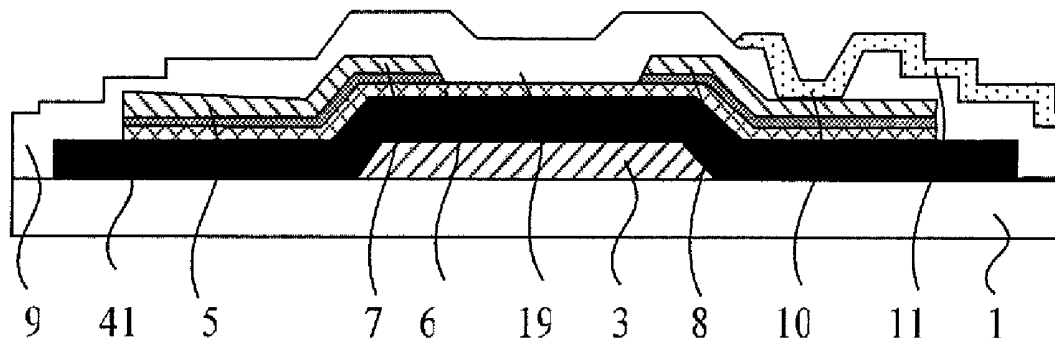
US 20120113366A1

(19) **United States**(12) **Patent Application Publication**
XIE(10) **Pub. No.: US 2012/0113366 A1**(43) **Pub. Date: May 10, 2012**(54) **ARRAY SUBSTRATE AND LIQUID CRYSTAL
DISPLAY****Publication Classification**(75) Inventor: **Zhenyu XIE**, Beijing (CN)(73) Assignee: **BEIJING BOE
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TECHNOLOGY CO., LTD.**,
Beijing (CN)(21) Appl. No.: **13/291,253**(22) Filed: **Nov. 8, 2011**(30) **Foreign Application Priority Data**

Nov. 9, 2010 (CN) 201020601738.0

(51) **Int. Cl.****G02F 1/1335** (2006.01)**G02F 1/1343** (2006.01)**H01L 29/786** (2006.01)(52) **U.S. Cl. 349/106; 257/59; 349/139; 257/E29.273**(57) **ABSTRACT**

An array substrate is provided and it comprises a base substrate and data lines and gate lines that crossed with one another to define pixel units on the base substrate. Each pixel unit comprises a pixel electrode and a thin film transistor (TFT) switch, and the TFT switch comprises a gate electrode, a source electrode, a drain electrode and an active layer. A gate insulation layer is provided between the gate electrode and the active layer, and the gate insulation layer comprises a nontransparent insulation layer.



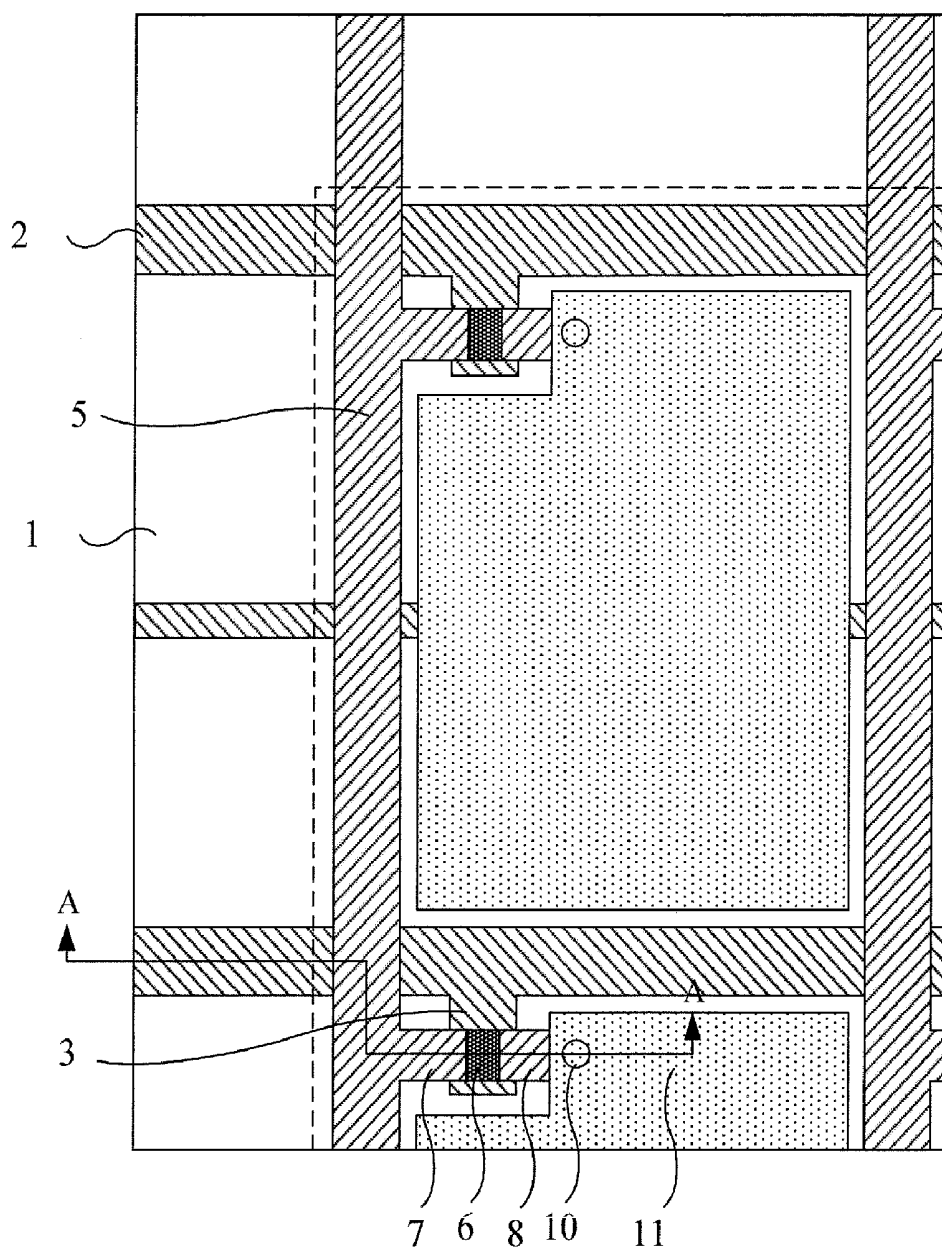


FIG.1A

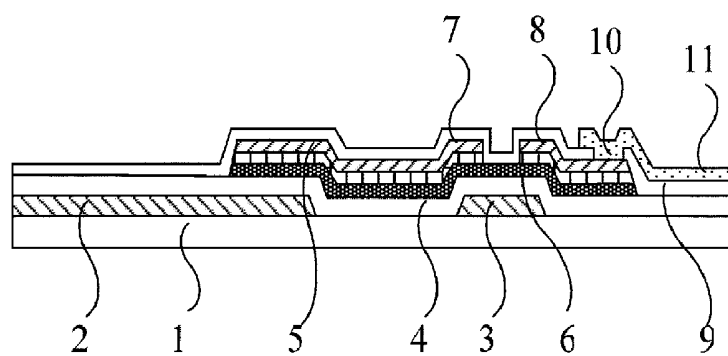


FIG.1B

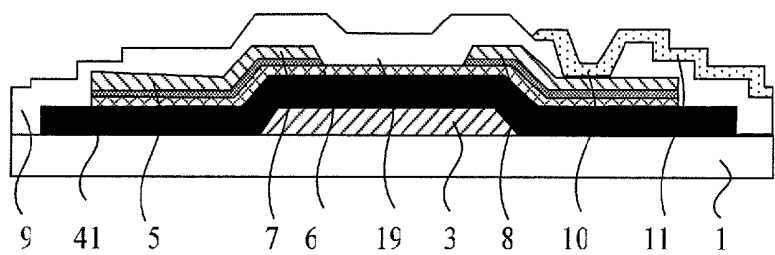


FIG. 2

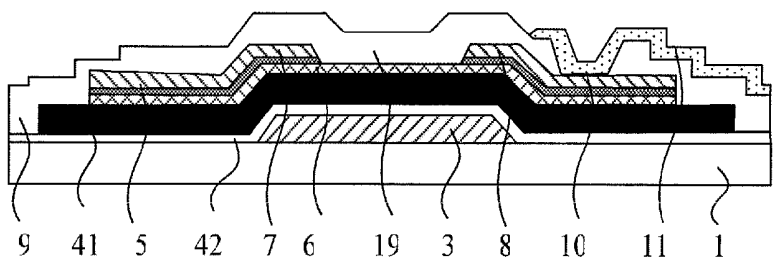


FIG. 3

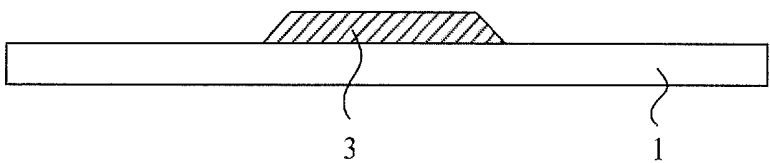


FIG. 4A

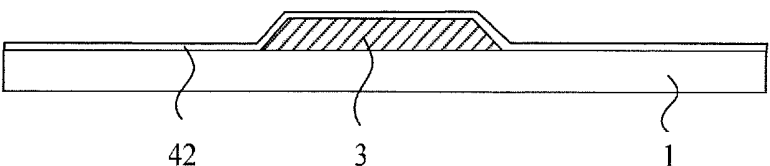


FIG. 4B

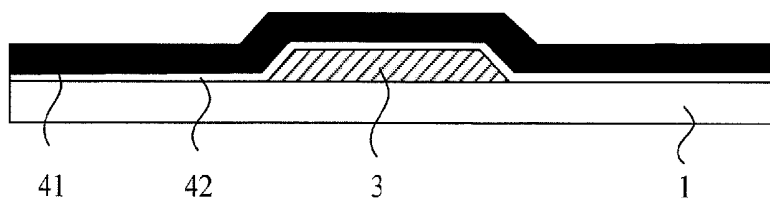


FIG. 4C

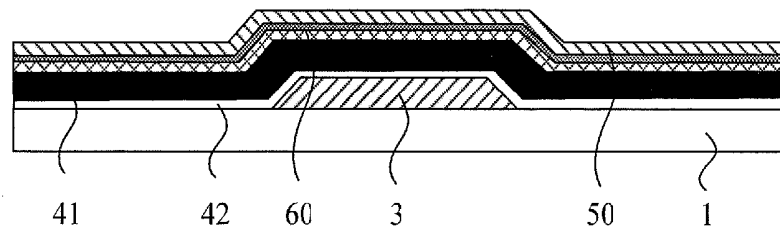


FIG. 4D

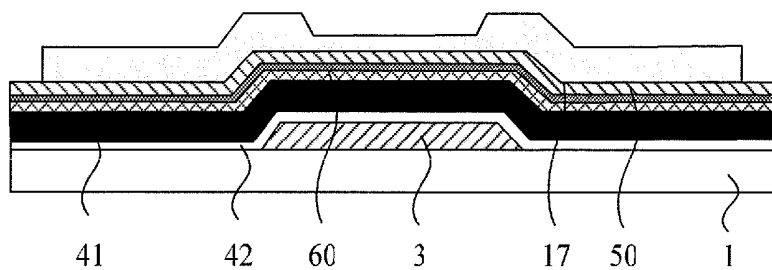


FIG. 5A

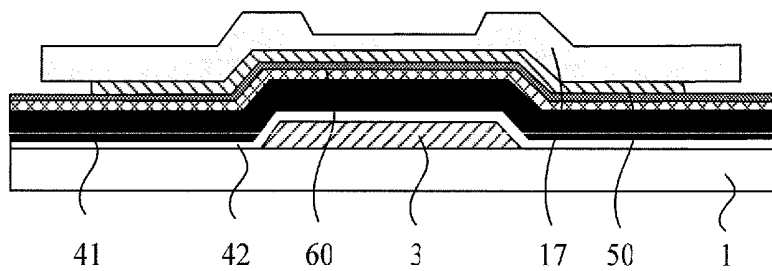


FIG. 5B

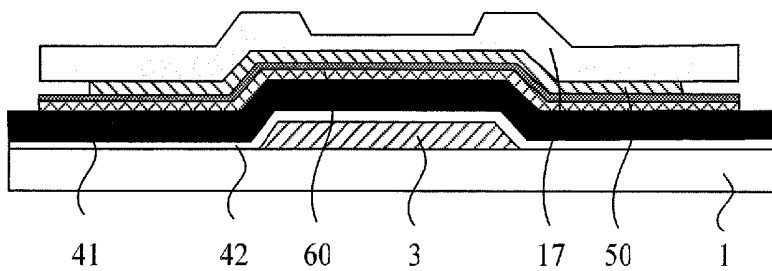


FIG. 5C

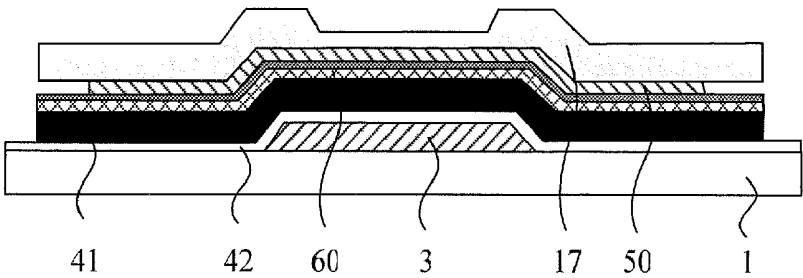


FIG. 5D

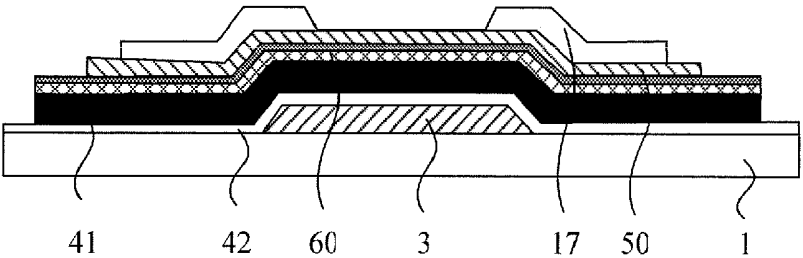


FIG. 5E

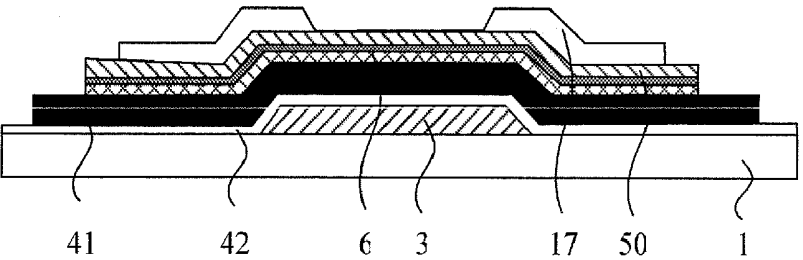


FIG. 5F

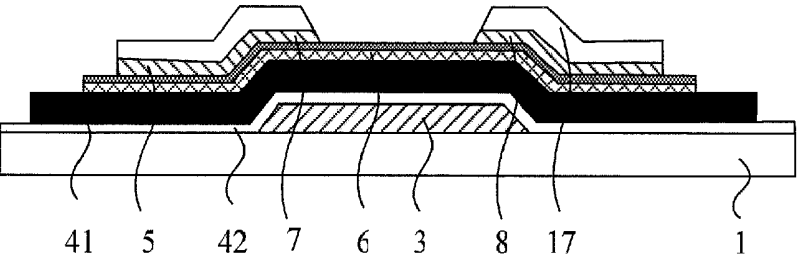


FIG. 5G

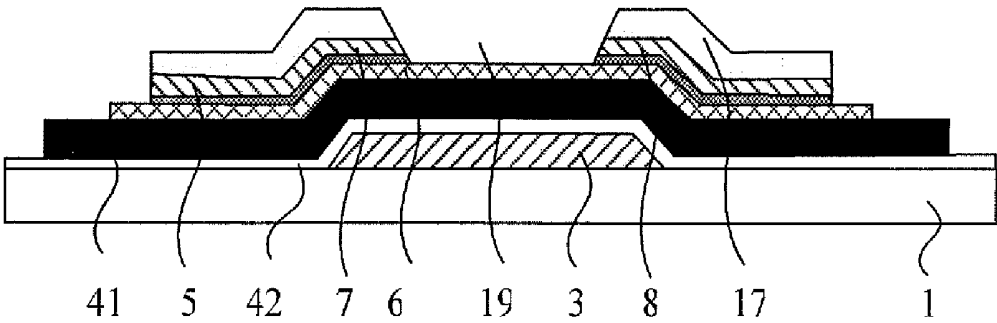


FIG.5H

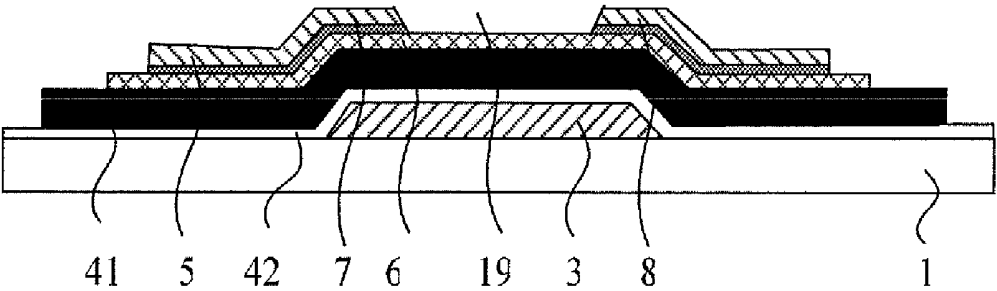


FIG.5I

ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY

BACKGROUND

[0001] Embodiments of the disclosed technology provide an array substrate and a liquid crystal display.

[0002] Liquid crystal displays are the commonly used flat panel displays at present, and thin film transistor liquid crystal displays (TFT-LCDs) are the main kind of liquid crystal displays. A TFT-LCD typically comprises an array substrate with an array structure.

[0003] FIG. 1A shows a partial top view of a typical array substrate, and FIG. 1B shows a cross sectional view taken along line A-A in FIG. 1A.

[0004] As shown in FIG. 1A and FIG. 1B, the array substrate manufactured with a conventional four-mask process generally comprises a base substrate 1 and data lines 5 and gate lines 2 that are crossed each other on the base substrate 1. The data lines 5 and the gate lines 2 collectively define a plurality of pixel units arranged in a matrix form, and each pixel unit comprises a thin film transistor (TFT) switch and a pixel electrode 11, and the TFT switch comprises a gate electrode 3, a source electrode 7, a drain electrode 8 and an active layer 6. For the pixel unit, the gate electrode 3 of the TFT is connected with one gate line 2, the source electrode 7 is connected with one data line 5, the drain electrode 8 is connected with the pixel electrode 11 of the pixel unit through a passivation hole 10, and the active layer 6 is formed between the source and the drain electrodes 7 and 8 and the gate electrode 3. A gate insulation layer 4 is formed between the gate electrode 3 and the active layer 6, a passivation layer 9 is formed between the pixel electrode 11 and the drain electrode 8, and the pixel electrode 11 is connected with the drain electrode 8 through the passivation layer via hole 10. The gate lines 2, the data lines 5, the gate electrodes 3, the source electrodes 7, the drain electrodes 8, the pixel electrodes 11 and the like can be collectively referred to as conductive patterns, while the gate insulation layer 4, the passivation layer 9 and the like can be collectively referred to as insulation layers.

[0005] A TFT-LCD needs an external light source, such as a backlight, for display; however, if the active layers of the TFTs on array substrate are illuminated by the backlight, the TFTs tend to give rise to leakage currents (I_{off}), which degrades display quality of the TFT-LCD, thus it is necessary to form a black matrix on the opposite substrate (e.g., a color filter substrate) to the array substrate, decreasing the aperture ratio of the TFT-LCD.

SUMMARY

[0006] An embodiment of the disclosed technology provides an array substrate, comprising: a base substrate, and data lines and gate lines that crossed with one another to define pixel units on the base substrate, wherein each pixel unit comprises a pixel electrode and a thin film transistor (TFT) switch, and the TFT switch comprises a gate electrode, a source electrode, a drain electrode and an active layer, and wherein a gate insulation layer is provided between the gate electrode and the active layer, and the gate insulation layer comprises a nontransparent insulation layer.

[0007] Another embodiment of the disclosed technology provides a liquid crystal display, comprising: a liquid crystal panel, which comprises the above-described array substrate

and an opposite substrate, which are assembled together with a liquid crystal layer interposed therebetween.

[0008] Further scope of applicability of the disclosed technology will become apparent from the detailed description given hereinafter. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The disclosed technology will become more fully understood from the detailed description given hereinafter and the accompanying drawings which are given by way of illustration only, and thus are not limitative of the disclosed technology and wherein:

[0010] FIG. 1A shows a partial top view of a typical array substrate, and FIG. 1B shows a cross sectional view taken along line A-A in FIG. 1A.

[0011] FIG. 2 shows a partial cross-sectional view of an array substrate according to a first embodiment of the disclosed technology embodiment.

[0012] FIG. 3 shows a partial cross-sectional view of an array substrate according to a second embodiment of the disclosed technology embodiment.

[0013] FIG. 4A shows a partial cross-sectional view of the gate lines and gate electrodes in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0014] FIG. 4B shows a partial cross-sectional view of the transparent insulation layer in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0015] FIG. 4C shows a partial cross-sectional view of the nontransparent insulation layer in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0016] FIG. 4D shows a partial cross-sectional view of the active layer thin film and the data line metal thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0017] FIG. 5A shows a partial cross-sectional view of the exposed and developed photoresist coated on the data line metal thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0018] FIG. 5B shows a partial cross-sectional view of the etched data line metal thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0019] FIG. 5C shows a partial cross-sectional view of the etched active layer thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0020] FIG. 5D shows a partial cross-sectional view of the etched nontransparent insulation layer in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0021] FIG. 5F shows a partial cross-sectional view of the further etched active layer thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0022] FIG. 5G shows a partial cross-sectional view of the formed source electrode and drain electrode in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0023] FIG. 5H shows a partial cross-sectional view of the formed channel region in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0024] FIG. 5I shows a partial cross-sectional view after removing the remaining photoresist in manufacturing the array substrate according to the second embodiment of the disclosed technology.

DETAILED DESCRIPTION

[0025] Embodiments of the disclosed technology will be described clearly and completely in combination with the drawings of the embodiments of the disclosed technology, so as to make objects, technical solutions and advantages of the embodiments of the disclosed technology to be clearer. Obviously, the described embodiments are portion of the embodiments of the disclosed technology, not all the embodiments. Based on the embodiments of the disclosed technology, the other embodiments obtained by those skilled in the related art without giving inventive work belong to the scope of the disclosed technology.

First Embodiment

[0026] FIG. 2 shows a partial cross-sectional view of an array substrate according to the first embodiment of the disclosed technology embodiment. As shown in FIG. 2, the array substrate comprises a base substrate 1, and on the base substrate 1 there are formed data lines 5 and gate lines (not shown), which are crossed with each other to define a plurality of pixel units; each pixel unit comprises a pixel electrode 11 and a thin film transistor (TFT) switch. Furthermore, each TFT switch comprises a gate electrode 3, a source electrode 7, a drain electrode 8, and an active layer 6; the gate electrode 3 is formed on the base substrate 1, the active layer 6 is formed on the gate electrode 3, and the source and drain electrodes 7 and 8 are formed on the active layer 6. Between the gate electrode 3 and the active layer 6, there is provided a gate insulation layer, and the gate insulation layer comprises a nontransparent insulation layer 41.

[0027] The gate insulation layer of the array substrate of the embodiment comprises a nontransparent insulation layer and therefore can prevent the backlight under or behind the array substrate from illuminating the active layers of the TFTs formed on the array substrate, alleviating the leakage currents of the TFTs. Therefore, the characteristics of the TFTs can be improved, and also light leakage from the backlight can be avoided, thus the area of the black matrix on the opposite substrate (e.g., color filter substrate) to the array substrate can be reduced, and the aperture ratio of the TFT-LCD can be increased.

Second Embodiment

[0028] FIG. 3 shows a partial cross-sectional view of an array substrate according to the second embodiment of the disclosed technology embodiment. As shown in FIG. 3, the array substrate comprises a base substrate 1, and on the base substrate 1 there are formed data lines 5 and gate lines (not shown), which are crossed with each other to define a plurality of pixel units; each pixel unit comprises a pixel electrode

11 and a thin film transistor (TFT) switch. Furthermore each TFT switch comprises a gate electrode 3, a source electrode 7, a drain electrode 8 and an active layer 6; the gate electrode 3 is formed on the base substrate 1, the active layer 6 is formed on the gate electrode 3, and the source and drain electrodes 7 and 8 are formed on the active layer 6. Between the gate electrode 3 and the active layer 6, there is provided a gate insulation layer, and the gate insulation layer comprises a nontransparent insulation layer 41. In addition, the gate insulation layer may further comprise a transparent insulation layer 42, and the transparent insulation layer 42 is formed under the nontransparent insulation layer 41.

[0029] Here, the gate electrode 3 is connected with one gate line, the source electrode 7 is connected with one data line 5, and the nontransparent insulation layer 41 corresponds to the data line 5, the source electrode 7, and the drain electrode 8 of the corresponding pixel unit, and accordingly the nontransparent insulation layer 41 and the transparent insulation layer 42 may also be provided under the data line 5.

[0030] In an example, the area of the nontransparent insulation layer is larger than that of the upper data line or the upper active layer. The nontransparent insulation layer 41 may comprise a black resin insulation layer. For example, the nontransparent insulation layer 41 may employ the same black resin material as that to form the black matrix on the opposite substrate (e.g., color filter substrate). The thickness of the nontransparent insulation layer made of a black resin insulation layer may be in the range of about 10000~20000 Å. Further, the thickness of the transparent insulation layer 42 may be in the range of 500~5000 Å.

[0031] The manufacturing method of the above-described array substrate of the embodiment may comprise the following steps.

[0032] Step 101, a gate metal thin film is formed on a base substrate 1 with a deposition process such as a magnetron sputtering method and patterned to form gate lines (not shown) and gate electrodes 3, as shown in FIG. 4A. FIG. 4A shows a partial cross-sectional view of the gate lines and gate electrodes in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0033] Step 102, on the base substrate 1 with the above patterns, a transparent insulation layer 42 is deposited with a plasma enhanced chemical vapor deposition (PECVD) method, and the material for the transparent insulation layer may be a transparent insulation layer, such as SiNx, and this transparent insulation layer 42 is a part of a gate insulation layer, as shown in FIG. 4B. FIG. 4B shows a partial cross-sectional view of the transparent insulation layer in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0034] Step 103, on the base substrate 1 with the above patterns, a nontransparent insulation layer 41 is coated, and the material of the nontransparent insulation layer 41 may be a photo-sensitive or not, e.g., a black resin material, and then the coated nontransparent insulation layer 41 is solidified, and also the nontransparent insulation layer 41 is a part of the gate insulation layer, as shown in FIG. 4C. FIG. 4C shows a partial cross-sectional view of the nontransparent insulation layer in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0035] Step 104, an active layer thin film 60 is formed by a PECVD method on the base substrate 1, and the active layer thin film 60 may comprise an amorphous semiconductor (a-si) thin film and a doped semiconductor (n⁺a-si) thin film

on the amorphous semiconductor thin film, and then a data line metal thin film **50** is formed by a magnetron sputtering method on the doped semiconductor thin film, as shown in FIG. 4D. FIG. 4D shows a partial cross-sectional view of the active layer thin film and the data line metal thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0036] Step 105, a layer of photoresist is applied and then exposed with a double tone mask plate, such as a half tone or gray tone mask plate, and after development of the exposed photoresist, the stacked layers are patterned with wet and dry etching processes to obtain the active layer, the data line, the source electrode and the drain electrode of a TFT on the base substrate. The detailed process may comprise the following sub-steps.

[0037] Step 201, with a double tone mask plate, the layer of photoresist **17** coated on the data line metal thin film **50** is exposed and the exposed photoresist is developed to form a photoresist completely-retained region at the positions to form the source electrode, the drain electrode and the data line, a photoresist partially-retained region at the positions to form the channel region of the TFT and the gate line, and a photoresist completely-removed region in the remaining positions, as shown in FIG. 5A. FIG. 5A shows a partial cross-sectional view of the exposed and developed photoresist coated on the data line metal thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0038] Step 202, with a wet etching process, the data line metal thin film **50** corresponding to the photoresist completely-removed region is removed, as shown in FIG. 5B. FIG. 5B shows a partial cross-sectional view of the etched data line metal thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology. After the data line metal thin film **50** corresponding to the photoresist completely-removed region is removed by etching, the data line portion of the metal thin film under the photoresist is partially overetched to obtain an undercut portion, forming the data line and the source electrode and the drain electrode of the TFT switch.

[0039] Step 203, with a dry etching process, the active layer thin film corresponding to the photoresist completely-removed region is removed, as shown in FIG. 5C. FIG. 5C shows a partial cross-sectional view of the etched active layer thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology. The nontransparent insulation layer **41** and the transparent insulation layer **42** are under the remaining active layer thin film **60**.

[0040] Step 204, the portion of the nontransparent insulation layer **41** corresponding to the photoresist completely-removed region is removed, as shown in FIG. 5D. FIG. 5D shows a partial cross-sectional view of the etched nontransparent insulation layer in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0041] Step 205, with an ashing process, the photoresist in the photoresist partially-retained region is removed but the photoresist in the photoresist completely-retained region is retained with a reduced thickness, as shown FIG. 5E. FIG. 5E shows a partial cross-sectional view after ashing the photoresist layer in manufacturing the array substrate according to the second embodiment of the disclosed technology. In particular, the photoresist **17** in the channel region of the TFT and corresponding to the photoresist partially-retained region is

removed by ashing, but the photoresist **17** at the positions of the data line, the source electrode and the drain electrode and corresponding to the photoresist completely-retained region is left with a reduced thickness.

[0042] Step 206, after the photoresist is horizontally etched in the ashing process, the portion of the active layer thin film exposed from the edges of the data line metal thin film **50** is removed, as shown in FIG. 5F. FIG. 5F shows a partial cross-sectional view of the further etched active layer thin film in manufacturing the array substrate according to the second embodiment of the disclosed technology. After the exposed portion of the active layer thin film **60** is removed by etching, the pattern of the active layer **6** is formed, and the nontransparent insulation layer **41** is still left under the active layer **6**, and the area of the nontransparent insulation layer **41** may be larger than that of the active layer **6**, which can prevent the light from the backlight from illuminating the amorphous semiconductor thin film of the active layer.

[0043] Step 207, with a metal dry etching process, for the data line metal thin film made of Mo for example, the data line metal thin film corresponding to the channel region of the TFT is removed, forming the data line **5**, the source electrode **7** and the drain electrode **8**, as shown in FIG. 5G. FIG. 5G shows a partial cross-sectional view of the formed source electrode and drain electrode in manufacturing the array substrate according to the second embodiment of the disclosed technology. Under the data line **5**, there are left the active layer thin film and also the nontransparent insulation layer **41** and transparent insulation layer **42** of the gate insulation layer, and the positions of the nontransparent insulation layer **41** and the transparent insulation layer **42** correspond to the data line, the source electrode, and the drain electrode.

[0044] Step 208, the active layer corresponding to the channel region of the TFT is partially etched to form the TFT channel **19**, as shown in FIG. 5H. FIG. 5H shows a partial cross-sectional view of the formed channel region in manufacturing the array substrate according to the second embodiment of the disclosed technology. In the channel region, the doped semiconductor layer **50** of the active layer **6** corresponding to the channel is removed, but the amorphous semiconductor **60** is partially etched in the thickness direction. Thus, the manufacturing of the TFT switch is completed here.

[0045] Step 209, the remaining photoresist is removed, as shown in FIG. 5I. FIG. 5I shows a partial cross-sectional view after removing the remaining photoresist in manufacturing the array substrate according to the second embodiment of the disclosed technology.

[0046] After the active layer **6**, the TFT channel **19**, the source electrode **7**, the drain electrode **8**, and data line **5** are formed through above-described Step 201 to Step 209, a pixel electrode is formed, as described in the below Step 106.

[0047] Step 106, a passivation layer **9** is formed by a deposition method and patterned to form a passivation layer via hole **10** therein, and then a pixel electrode conductive film is formed and patterned to form a pixel electrode **11**, as shown in FIG. 3. This pixel electrode **11** is connected with the drain electrode **8** through the passivation layer via hole **10**.

[0048] Each of the TFT on the array substrate of the embodiment employs a gate insulation layer comprises a nontransparent insulation layer (e.g., black resin insulation layer) as a part; further, the gate insulation layer may be of a two-layer configuration, the first layer of which is a transparent insulation layer (e.g., an inorganic material layer, such as SiNx) and the second layer is the nontransparent insulation

layer. After a transparent insulation layer with a thickness of about 1000 Å is formed on the base substrate, a nontransparent insulation layer, such as a black resin insulation layer, is applied on the transparent insulation layer; then, the black resin insulation layer in the pixel region is patterned, and the black resin insulation layer (nontransparent insulation layer) is left under the active layer and therefore can prevent light from a backlight from illuminating the active layer of the TFT, capable of effectively reducing light leakage currents of the TFT and improving the characteristics of the TFT. Furthermore, the array substrate of the embodiment can prevent light leakage from the backlight, reduce the area of the black matrix on the opposite substrate, improve aperture ratio of the TFT-LCD. Moreover, with an area of the nontransparent insulation layer larger than the upper drain and source electrodes and the upper data line, the nontransparent insulation layer of the array substrate can be used to replace the black matrix on the opposite substrate, which can further improve the aperture ratio of the TFT-LCD.

Third Embodiment

[0049] The third embodiment of the disclosed technology embodiment provides a liquid crystal display, which comprises a liquid crystal panel, and the liquid crystal panel comprises an array substrate according to anyone of the above-described embodiment, an opposite substrate, and a liquid crystal layer interposed between the substrates. The opposite substrate may be a color filter substrate, on which RGB (Red: Green: Blue) filter units are arranged for example; on the other hand, if the array substrate comprises color filter units, the opposite substrate can comprise no color filter units.

[0050] In the array substrate of the liquid crystal display of the embodiment, a gate insulation layer comprises a nontransparent insulation layer, which can prevent light from a backlight from illuminating on the upper active layers of TFTs and reduces light leakage current of the TFTs. Therefore, the characteristics of the TFTs can be improved, light leakage from the backlight can be avoided, the area of the black matrix on the opposite substrate can be reduced, and the aperture ratio of the liquid crystal display can be increased. In addition, the area of the nontransparent insulation layer of the gate insulation layer is larger than that of the upper data line and other elements of TFTs, thus light leakage from the backlight can be avoided further, and thus the nontransparent insulation layer can be used to replace the black matrix on the opposite substrate, increasing the aperture ration of the liquid crystal display.

[0051] The embodiment of the disclosed technology being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the spirit and scope of the disclosed technol-

ogy, and all such modifications as would be obvious to those skilled in the art are intended to be included within the scope of the following claims.

What is claimed is:

1. An array substrate, comprising:
a base substrate, and
data lines and gate lines that crossed with one another to define pixel units on the base substrate,
wherein each pixel unit comprises a pixel electrode and a thin film transistor (TFT) switch, and the TFT switch comprises a gate electrode, a source electrode, a drain electrode and an active layer, and
wherein a gate insulation layer is provided between the gate electrode and the active layer, and the gate insulation layer comprises a nontransparent insulation layer.
2. The array substrate according to claim 1, wherein the gate insulation layer further comprises a transparent insulation layer, and the transparent insulation layer is provided under the nontransparent insulation layer.
3. The array substrate according to claim 2, wherein the nontransparent insulation layer corresponds to the data line, the source electrode, and the drain electrode of the TFT switch.
4. The array substrate according to claim 2, wherein an area of the nontransparent insulation layer is larger than that of the upper data line or the upper active layer.
5. The array substrate according to claim 3, wherein an area of the nontransparent insulation layer is larger than that of the upper data line or the upper active layer.
6. The array substrate according to claim 1, wherein the nontransparent insulation layer is a black resin insulation layer.
7. The array substrate according to claim 2, wherein the nontransparent insulation layer is a black resin insulation layer.
8. The array substrate according to claim 3, wherein the nontransparent insulation layer is a black resin insulation layer.
9. The array substrate according to claim 1, wherein a thickness of the nontransparent insulation layer is in the range of about 10000~20000 Å.
10. The array substrate according to claim 2, wherein a thickness of the transparent insulation layer is in the range of about 500~5000 Å.
11. A liquid crystal display, comprising:
a liquid crystal panel, which comprises the array substrate according to 1 and an opposite substrate, which are assembled together with a liquid crystal layer interposed therebetween.
12. The liquid crystal display according to claim 11, wherein the opposite substrate is a color filter substrate.

* * * * *

专利名称(译)	阵列基板和液晶显示器		
公开(公告)号	US20120113366A1	公开(公告)日	2012-05-10
申请号	US13/291253	申请日	2011-11-08
[标]申请(专利权)人(译)	XIE ZHENYU		
申请(专利权)人(译)	谢，振宇		
当前申请(专利权)人(译)	北京京东方光电科技有限公司.		
[标]发明人	XIE ZHENYU		
发明人	XIE, ZHENYU		
IPC分类号	G02F1/1335 G02F1/1343 H01L29/786		
CPC分类号	H01L27/1214 G02F1/1368 G02F1/136209 H01L29/4908 H01L27/124		
优先权	201020601738.0 2010-11-09 CN		
其他公开文献	US8860898		
外部链接	Espacenet USPTO		

摘要(译)

提供阵列基板，其包括基础基板和彼此交叉的数据线和栅极线，以在基础基板上限定像素单元。每个像素单元包括像素电极和薄膜晶体管（TFT）开关，TFT开关包括栅电极，源电极，漏电极和有源层。栅极绝缘层设置在栅极电极和有源层之间，栅极绝缘层包括不透明的绝缘层。

