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(54) **LIQUID CRYSTAL DISPLAY PANEL AND LIQUID CRYSTAL DISPLAY DEVICE INCLUDING THE SAME**

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(57) **ABSTRACT**

Provided is a liquid crystal display device. The liquid crystal display device includes a display panel including a liquid crystal layer, wherein a first pixel region, a second pixel region, and a third pixel region are defined in the display panel and a backlight unit configured to provide light to the display panel. A first color light emitted from the first pixel region has a red color, a second color light emitted from the second pixel region has a green color, and a third color light emitted from the third pixel region has a blue color. A first ratio at which the light passes through the first pixel region and a second ratio at which the light passes through the second pixel region is greater than a third ratio at which the light passes through the third pixel region.

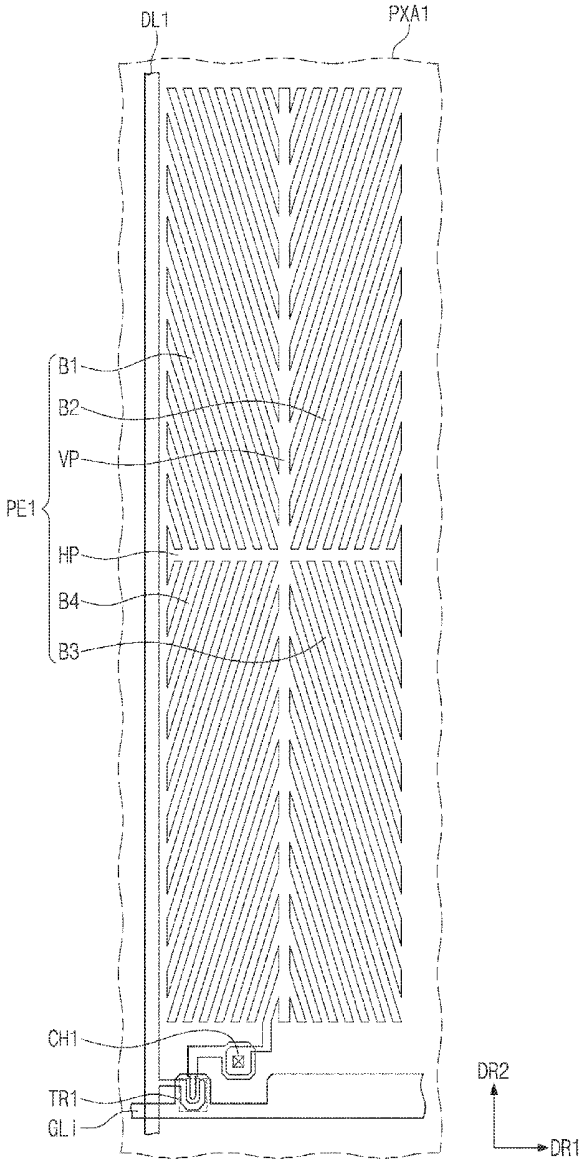


FIG. 1

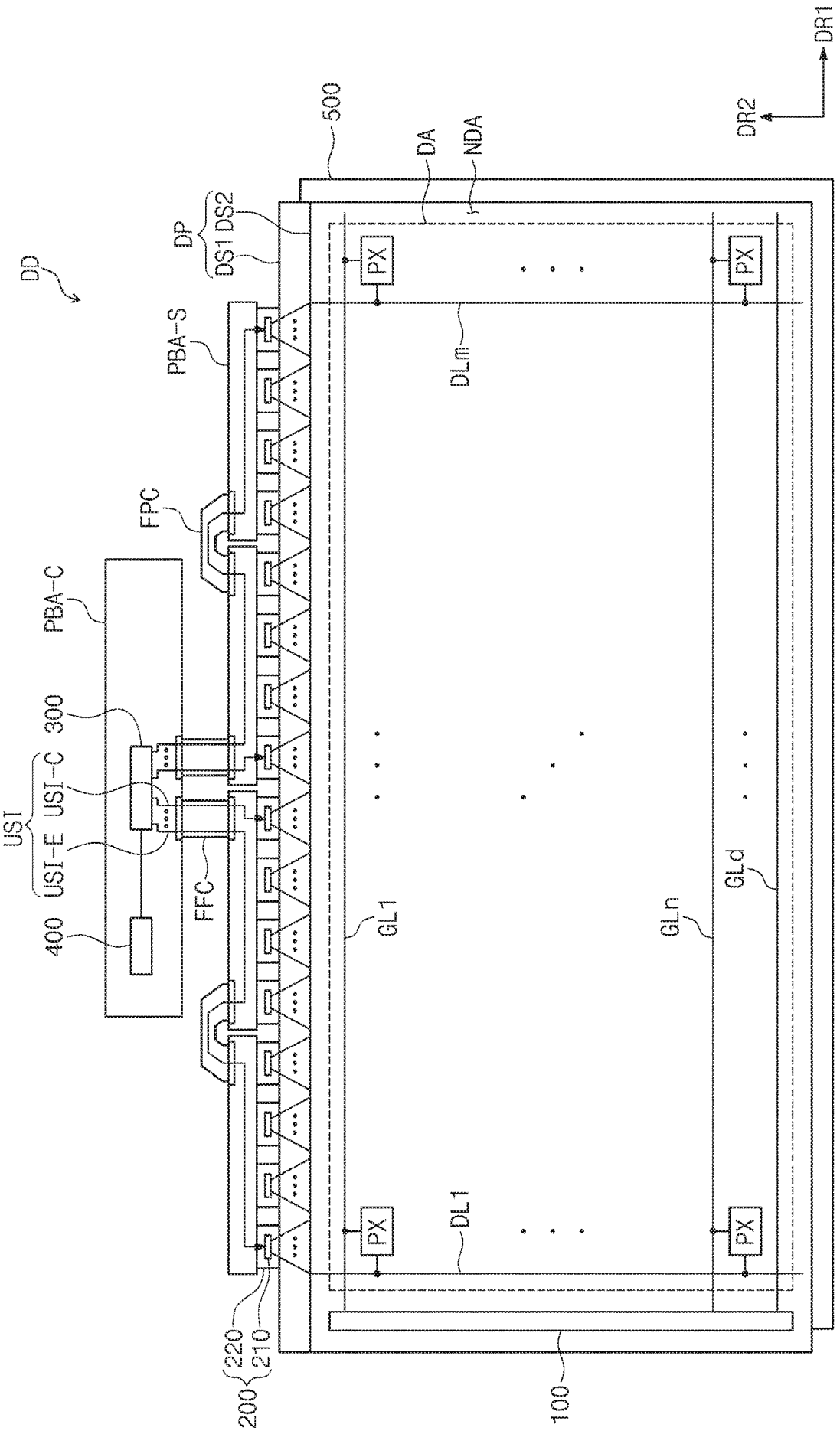

DR1
DR2
500
DA
NDA
DP
DS1
DS2
DD
PBA-S
FPC
PBA-C
300
USI
USI-C
USI-E
400
FFC
PX
DLm
DL1
GL1
GLn
GLd
220
210
200
100

FIG. 2

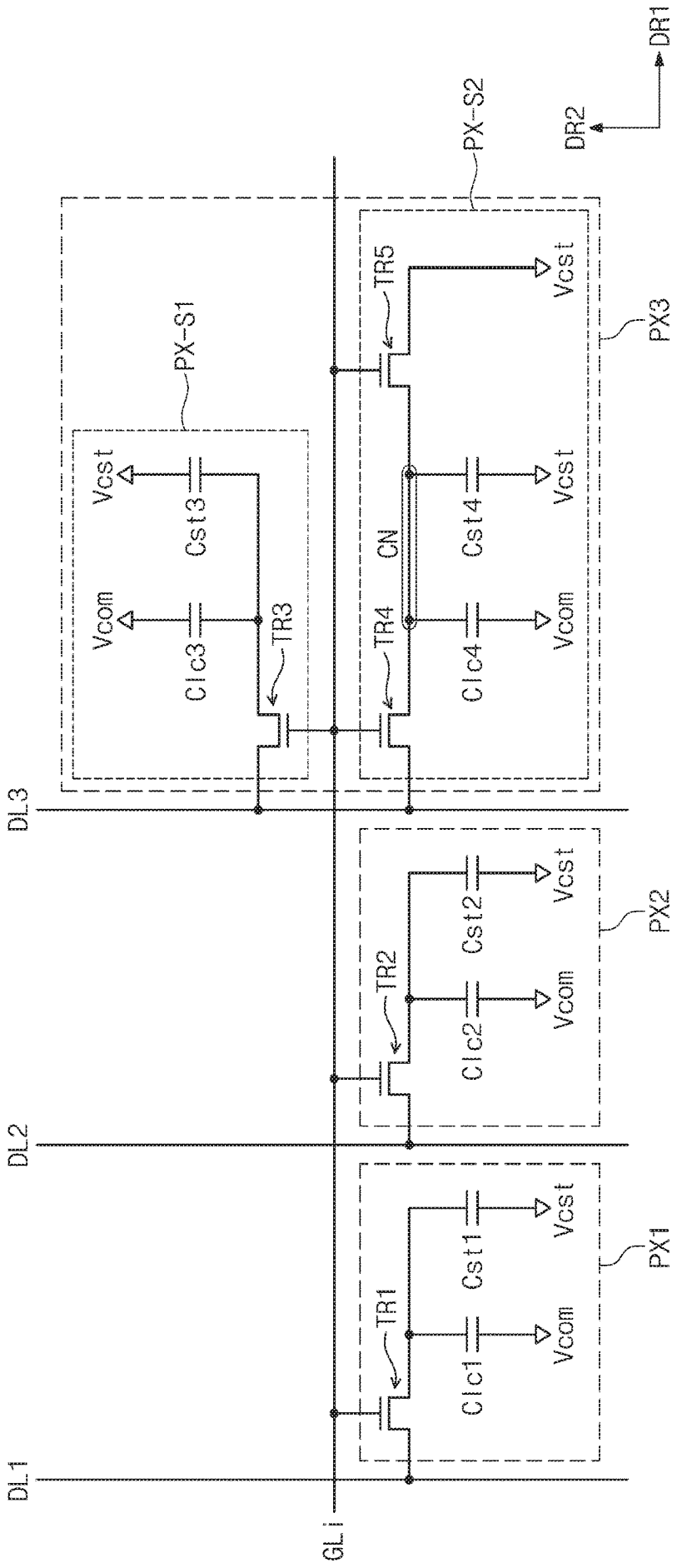

DR1
DR2
PX-S2
PX-S1
PX3
PX2
PX1
TR5
TR4
TR3
TR2
TR1
CN
Vcst
Vcom
Cst3
Clc3
Cst4
Clc4
Cst2
Clc2
Cst1
Clc1
DL3
DL2
DL1
GL1

FIG. 3A

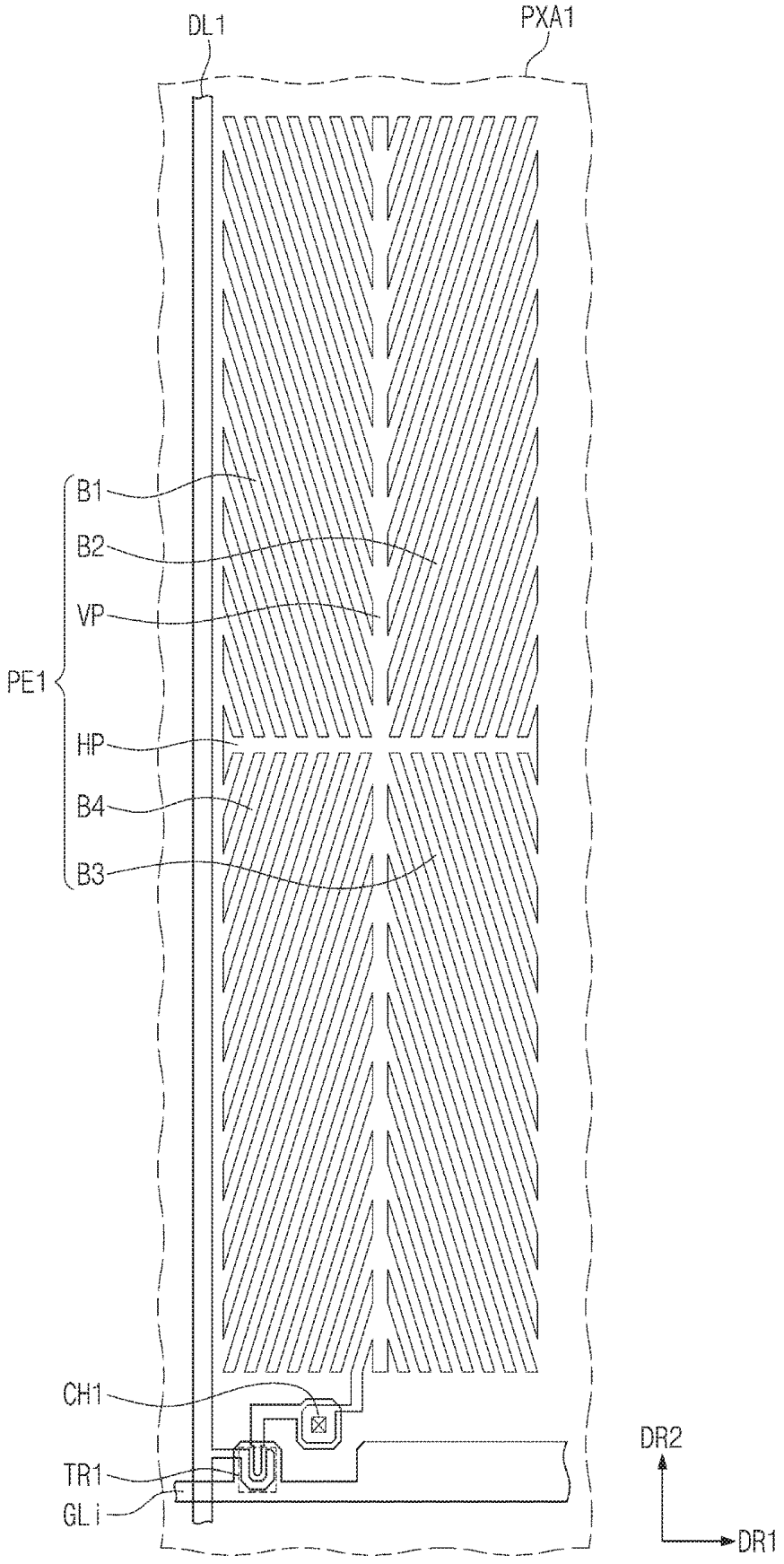


FIG. 3B

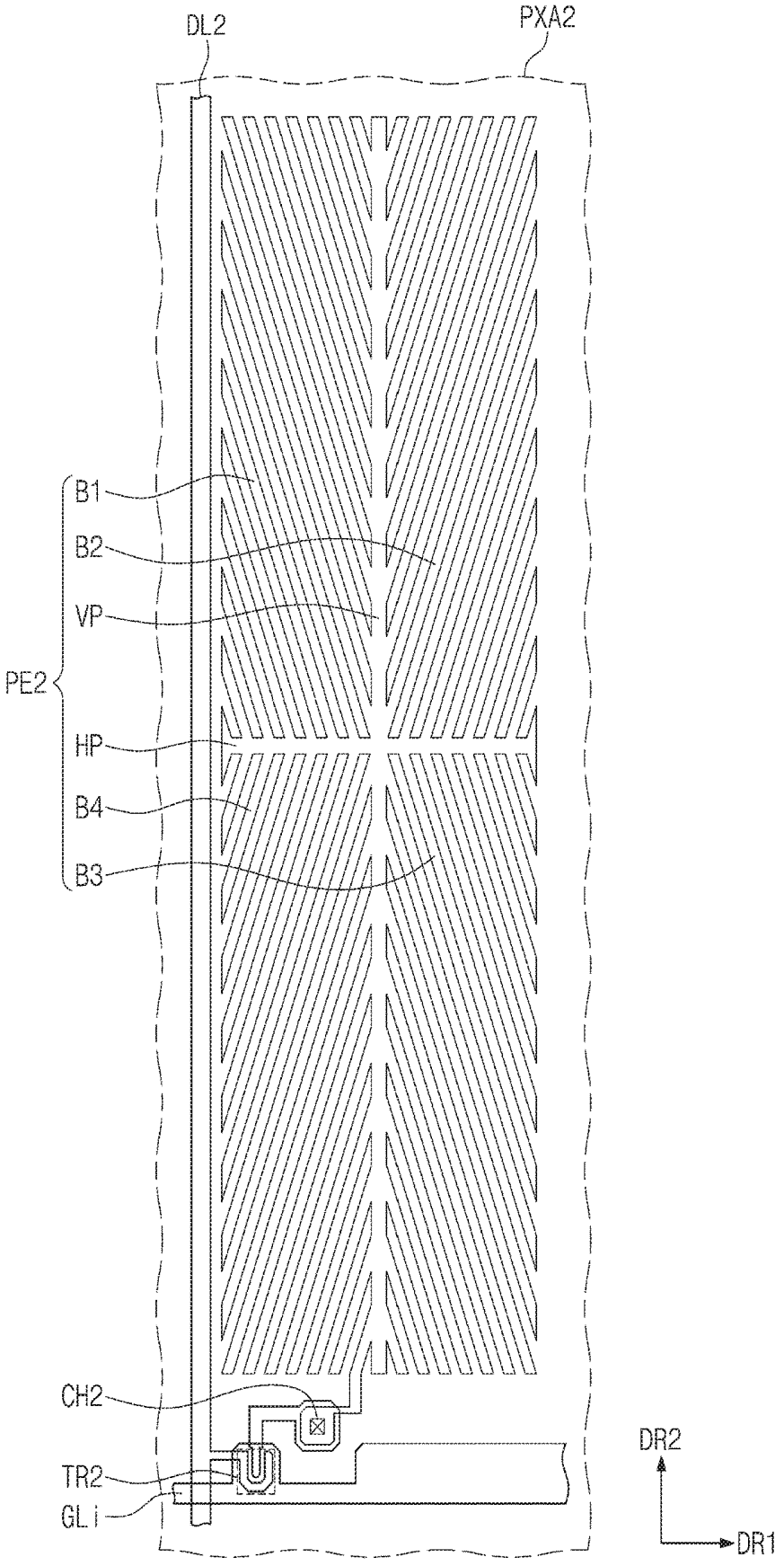


FIG. 3C

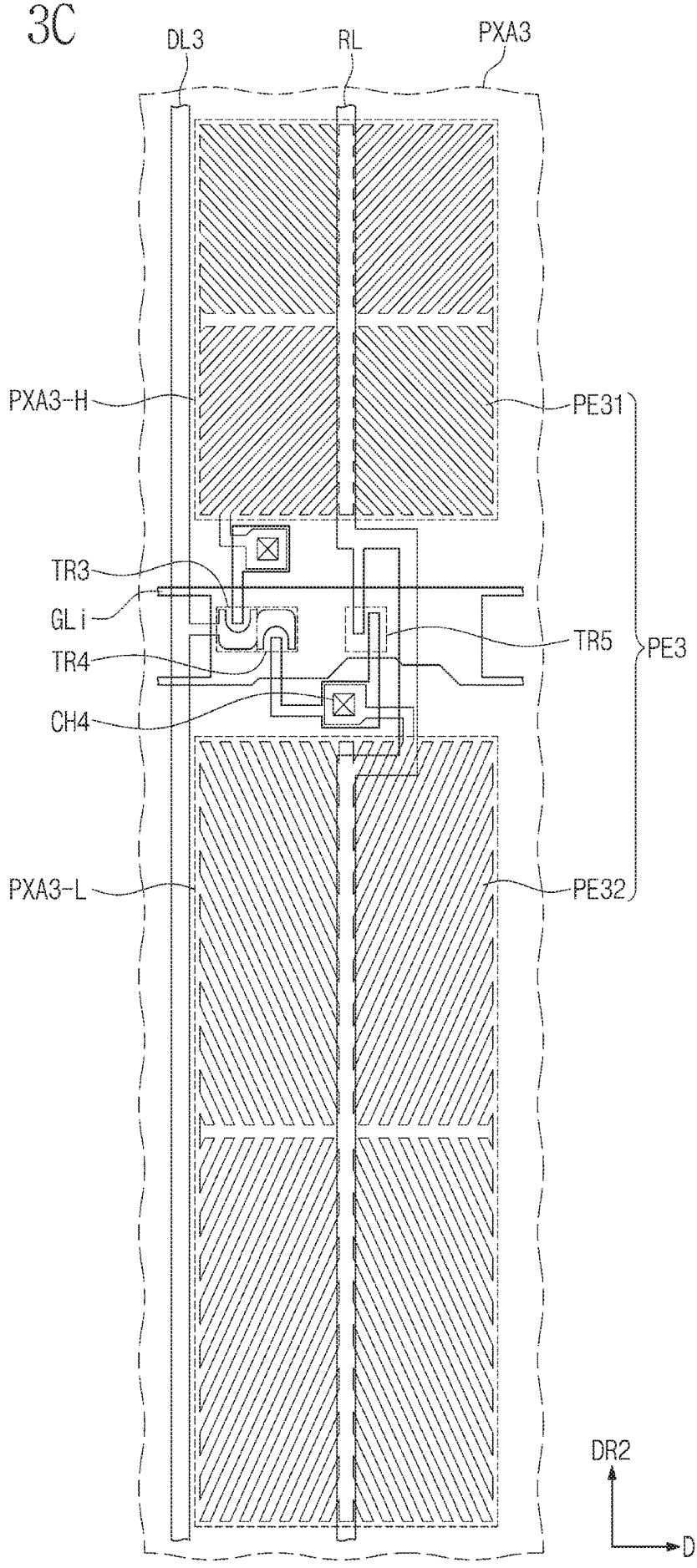

DL3
RL
PXA3
PXA3-H
PE31
TR3
GLi
TR4
CH4
TR5
PE3
PXA3-L
PE32
DR2
DR1

FIG. 4

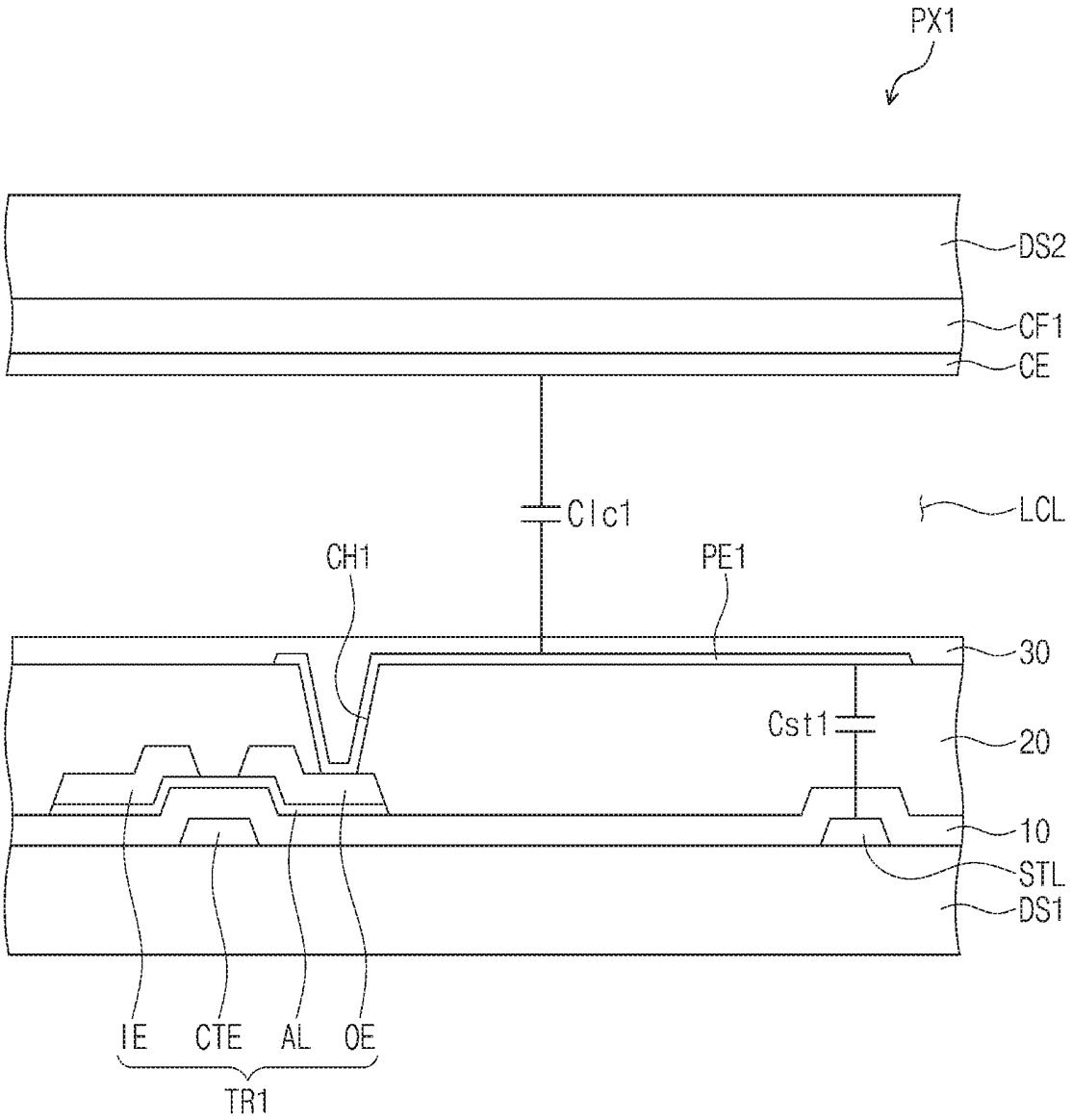

PX1
DS2
CF1
CE
Clc1
LCL
CH1
PE1
30
Cst1
20
10
STL
DS1
IE
CTE
AL
OE
TR1

FIG. 5

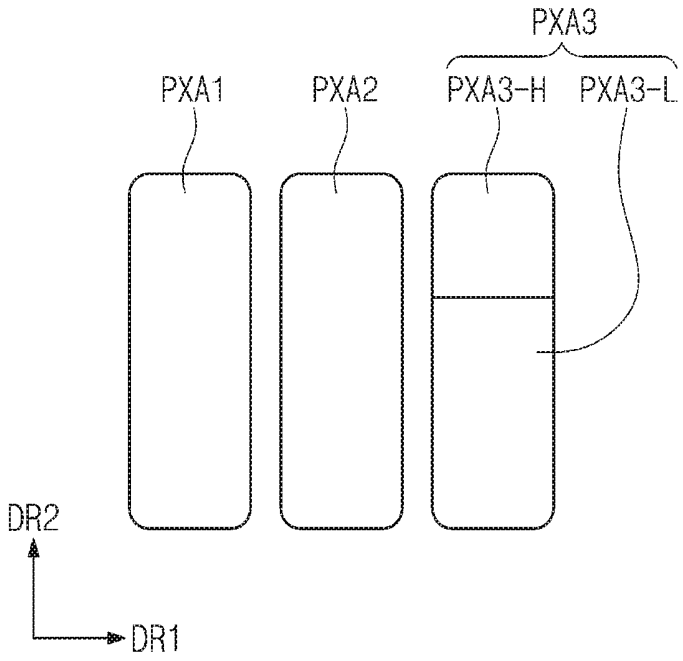

PXA3
PXA1
PXA2
PXA3-H
PXA3-L
DR2
DR1

FIG. 6

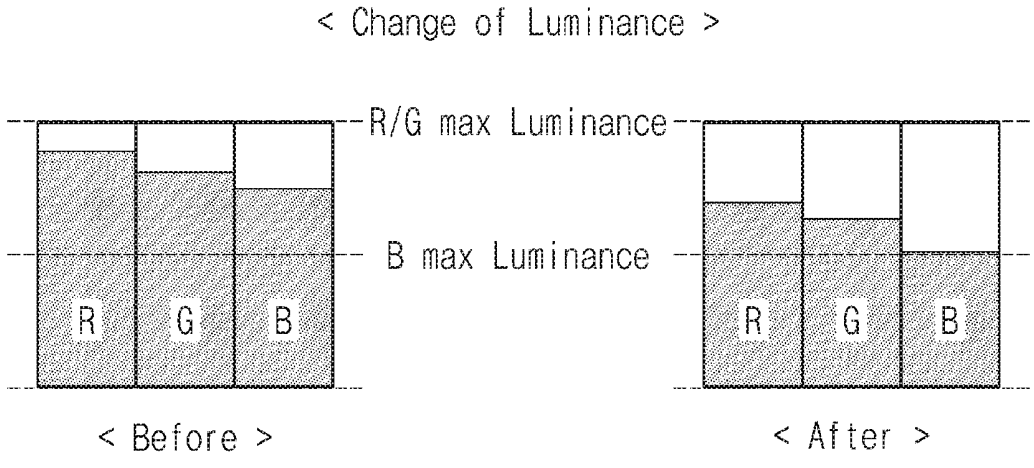

< Change of Luminance >
R/G max Luminance
B max Luminance
R
G
B
R
G
B
< Before >
< After >

FIG. 7

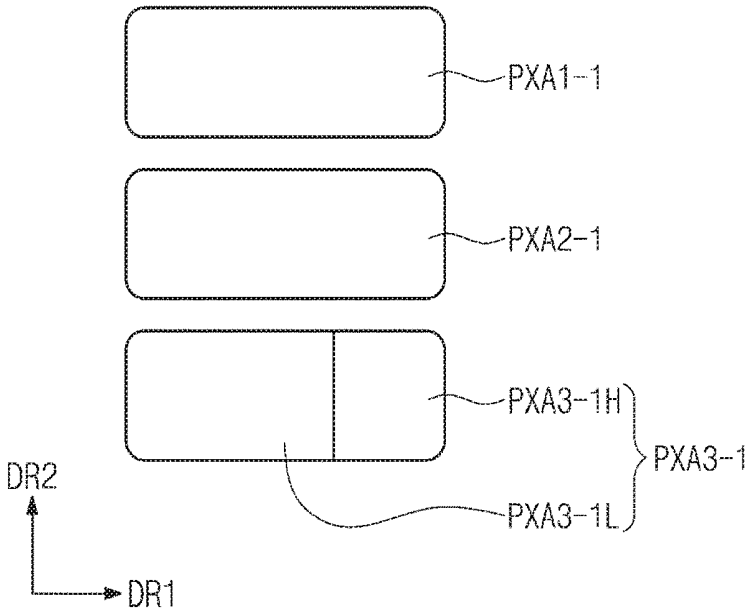
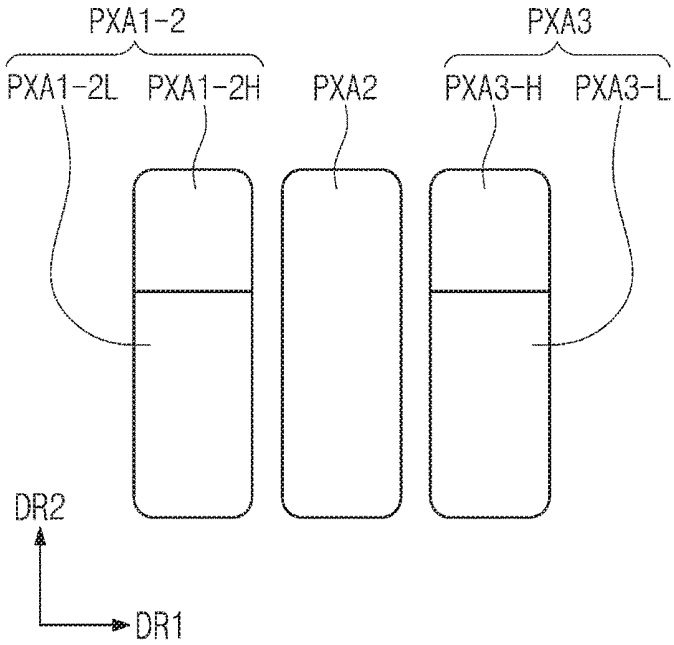

PXA1-1
PXA2-1
PXA3-1H
PXA3-1
PXA3-1L
DR2
DR1

FIG. 8


PXA1-2
PXA3
PXA1-2L
PXA1-2H
PXA2
PXA3-H
PXA3-L
DR2
DR1

LIQUID CRYSTAL DISPLAY PANEL AND LIQUID CRYSTAL DISPLAY DEVICE INCLUDING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims priority to Korean Patent Application No. 10-2018-0109052, filed on Sep. 12, 2018, and all the benefits accruing therefrom under 35 U.S.C. § 119, the content of which in its entirety is herein incorporated by reference.

BACKGROUND

[0002] The present disclosure herein relates to a liquid crystal display panel having excellent viewing angle characteristics and light transmittance, and a display device including the same.

[0003] A liquid crystal display device includes a liquid crystal display panel with two substrates facing each other, and a liquid crystal layer disposed between the substrates. The liquid crystal display device applies a voltage to the electric field generating electrode to apply an electric field to the liquid crystal layer. Accordingly, the alignment direction of the liquid crystal molecules in the liquid crystal layer is determined, and the image is displayed by controlling the polarization of the incident light.

[0004] Among liquid crystal display devices, there is a vertically aligned mode liquid crystal display device in which the long axis of the liquid crystal molecules is arranged perpendicular to the two substrates in the absence of an electric field, such that a contrast ratio is large and a wide reference viewing angle is easily implemented.

[0005] In order to improve the viewing angle characteristics of the liquid crystal display, techniques for dividing the pixel region into a plurality of domains and controlling them have been developed. Examples of such techniques include a Charge Share (CS) method and a Resistivity Division (RD) method.

[0006] In order to improve the viewing angle characteristics using a plurality of domains as described above, a large number of transistors and a large number of capacitors are required, such that the transmittance of the liquid crystal display panel is reduced.

SUMMARY

[0007] The present disclosure is to provide a liquid crystal display panel having excellent visibility and viewing angle characteristics and a high light transmittance, and a liquid crystal display device including the same.

[0008] An embodiment of the inventive concept provides a liquid crystal display device including: a display panel including a liquid crystal layer, wherein a first pixel region, a second pixel region, and a third pixel region are defined in the display panel; and a backlight unit configured to provide light to the display panel, wherein each of a wavelength of a first color light generated by transmitting the light through the first pixel region and a wavelength of a second color light generated by transmitting the light through the second pixel region is longer than a wavelength of a third color light generated by transmitting the light through the third pixel region, wherein a first ratio at which the light passes through the first pixel region and a second ratio at which the light passes through the second pixel region is greater than a third ratio at which the light passes through the third pixel region.

[0009] In an embodiment, the first color light may have a red color, the second color light may have a green color, and the third color light may have a blue color.

[0010] In an embodiment, the third pixel region may include a high gradation region and a low gradation region, wherein a gradation of light emitted from the high gradation region of the third color light may be higher than a gradation of light emitted from the low gradation region of the third color light.

[0011] In an embodiment, the display panel may include a plurality of transistors, wherein the number of transistors disposed in the first pixel region among the plurality of transistors may be equal to the number of transistors disposed in the second pixel region among the plurality of transistors, wherein the number of transistors disposed in the third pixel region among the plurality of transistors may be greater than the number of transistors disposed in the first pixel region among the plurality of transistors.

[0012] In an embodiment, the number of the transistors disposed in the first pixel region may be one, and the number of the transistors disposed in the third pixel region may be three.

[0013] In an embodiment, the display panel may further include: a first color filter overlapping the first pixel region and configured to transmit light having a wavelength of between 640 nm and 730 nm in the light; a second color filter overlapping the second pixel region and configured to transmit light having a wavelength of between 492 nm and 580 nm in the light; and a third color filter overlapping the third pixel region and configured to transmit light having a wavelength of between 420 nm and 490 nm in the light.

[0014] In an embodiment, the display panel may further include: a plurality of pixel electrodes; and a common electrode overlapping the plurality of pixel electrodes, wherein the liquid crystal layer may be disposed between the plurality of pixel electrodes and the common electrode.

[0015] In an embodiment, the number of pixel electrodes disposed in the first pixel region among the plurality of pixel electrodes may be equal to the number of pixel electrodes disposed in the second pixel region among the plurality of pixel electrodes, wherein the number of pixel electrodes disposed in the third pixel region among the plurality of pixel electrodes may be greater than the number of pixel electrodes disposed in the first pixel region.

[0016] In an embodiment, the number of the pixel electrodes disposed in the first pixel region may be one and the number of the pixel electrodes disposed in the third pixel region may be two.

[0017] In an embodiment of the inventive concept, a liquid crystal display panel includes: a first substrate where a first pixel region, a second pixel region, and a third pixel region are defined; a second substrate disposed opposite the first substrate; and a liquid crystal layer disposed between the first substrate and the second substrate, wherein a first color light emitted from the first pixel region has a red color, a second color light emitted from the second pixel region has a green color, and a third color light emitted from the third pixel region has a blue color, wherein a light transmittance of the third pixel region is less than a light transmittance of the first pixel region and a light transmittance of the second pixel region.

[0018] In an embodiment, the third pixel region may include a high gradation region and a low gradation region, wherein a gradation of light emitted from the high gradation region in the third color light may be higher than a gradation of light emitted from the low gradation region in the third color light.

[0019] In an embodiment, the liquid crystal display panel may further include a plurality of transistors disposed on the first substrate, wherein the number of transistors disposed in the first pixel region among the plurality of transistors may be equal to the number of transistors disposed in the second pixel region among the plurality of transistors, wherein the number of transistors disposed in the third pixel region among the plurality of transistors may be greater than the number of transistors disposed in the first pixel region among the plurality of transistors.

[0020] In an embodiment, the number of the transistors disposed in the first pixel region may be one, and the number of the transistors disposed in the third pixel region may be three.

[0021] In an embodiment, the liquid crystal display panel may further include a plurality of pixel electrodes, each of which is electrically connected to the plurality of transistors; and a common electrode overlapping the plurality of pixel electrodes, wherein the liquid crystal layer may be disposed between the plurality of pixel electrodes and the common electrode.

[0022] In an embodiment, the number of pixel electrodes disposed in the first pixel region among the plurality of pixel electrodes may be equal to the number of pixel electrodes disposed in the second pixel region among the plurality of pixel electrodes, wherein the number of pixel electrodes disposed in the third pixel region among the plurality of pixel electrodes may be greater than the number of pixel electrodes disposed in the first pixel region.

[0023] In an embodiment, the number of the pixel electrodes disposed in the first pixel region may be one and the number of the pixel electrodes disposed in the third pixel region may be two.

[0024] In an embodiment of the inventive concept, a liquid crystal display device includes: a display panel including a liquid crystal layer, wherein a first pixel region, a second pixel region, and a third pixel region are defined in the display panel; and a backlight unit configured to provide light to the display panel, wherein each of the first pixel region and the second pixel region includes only one transistor, and the third pixel region includes three transistors, wherein each of a wavelength of a first color light generated by transmitting the light through the first pixel region and a wavelength of a second color light generated by transmitting the light through the second pixel region is longer than a wavelength of a third color light generated by transmitting the light through the third pixel region.

[0025] In an embodiment, the first color light may have a red color, the second color light may have a green color, and the third color light may have a blue color.

[0026] In an embodiment, the third pixel region may include a high gradation region and a low gradation region, wherein a gradation of light emitted from the high gradation region of the third color light may be higher than a gradation of light emitted from the low gradation region of the third color light.

[0027] In an embodiment, a first ratio at which the light passes through the first pixel region and a second ratio at which the light passes through the second pixel region may be greater than a third ratio at which the light passes through the third pixel region.

BRIEF DESCRIPTION OF THE FIGURES

[0028] The accompanying drawings are included to provide a further understanding of the inventive concept, and are incorporated in and constitute a part of this specification. The drawings illustrate exemplary embodiments of the inventive concept and, together with the description, serve to explain principles of the inventive concept. In the drawings:

[0029] FIG. **1** is a plan view of a display device according to an embodiment of the inventive concept;

[0030] FIG. **2** is an equivalent circuit diagram of pixels according to an embodiment of the inventive concept;

[0031] FIG. **3**A shows an exemplary layout of a first pixel region corresponding to a first pixel shown in FIG. **2**;

[0032] FIG. **3**B shows an exemplary layout of a second pixel region corresponding to a second pixel shown in FIG. **2**;

[0033] FIG. **3**C shows an exemplary layout of a third pixel region corresponding to a third pixel shown in FIG. **2**;

[0034] FIG. **4** exemplarily shows a cross-sectional view corresponding to a part of the components of a first pixel shown in FIG. **2**;

[0035] FIG. **5** shows an example in which a first pixel region, a second pixel region, and a third pixel region are disposed;

[0036] FIG. **6** exemplarily shows a luminance control method for driving a display panel including pixel regions as shown in FIG. **5**; and

[0037] FIGS. **7** and **8** show examples in which a first pixel region, a second pixel region, and a third pixel region are disposed.

DETAILED DESCRIPTION

[0038] Hereinafter, another embodiment of the inventive concept will be described with reference to the drawings.

[0039] Additionally, in the drawings, the thicknesses, proportions, and dimensions of components are exaggerated for effective description. "And/or" includes all of one or more combinations defined by related components.

[0040] In various embodiments of the inventive concept, the term "include," "comprise," "including," or "comprising," specifies a property, a region, a fixed number, a step, a process, an element and/or a component but does not exclude other properties, regions, fixed numbers, steps, processes, elements and/or components.

[0041] FIG. **1** is a plan view of a display device DD according to an embodiment of the inventive concept. FIG. **2** is an equivalent circuit diagram of pixels PX**1** to PX**3** according to an embodiment of the inventive concept. FIG. **3**A shows an example layout of a first pixel region PXA**1** corresponding to a first pixel PX**1** shown in FIG. **2**. FIG. **3**B shows an example layout of a second pixel region PXA**2** corresponding to a second pixel PX**2** shown in FIG. **2**. FIG. **3**C shows an example layout of a third pixel region PXA**3** corresponding to a third pixel PX**3** shown in FIG. **2**. FIG. **4** shows a cross-sectional view corresponding to a part of the components of a first pixel PX**1** shown in FIG. **2**.

[0042] As shown in FIG. **1**, a display device according to an embodiment of the inventive concept includes a display panel DP, a gate driving circuit **100**, a data driving circuit

200, a signal control unit 300, a power management circuit 400, and a backlight unit 500.

[0043] In this embodiment, the display panel DP is described as a liquid crystal display panel. On the other hand, a liquid crystal display device including a liquid crystal display panel may further include a polarizer (not shown).

[0044] The display panel DP includes a first substrate DS1, a second substrate DS2 spaced apart from the first substrate DS1, and a liquid crystal layer LCL disposed between the first substrate DS1 and the second substrate DS2. The second substrate DS2 faces the first substrate DS1. On the plane defined by the first direction DR1 and the second direction DR2, the display panel DP includes a display area DA in which a plurality of pixels PX are arranged and a non-display area NDA surrounding the display area DA.

[0045] The display panel DP includes a plurality of gate lines GL1 to GLn disposed on the first substrate DS1 and a plurality of data lines DL1 to DLm intersecting the plurality of gate lines GL1 to GLn. The plurality of gate lines GL1 to GLn are connected to the gate driving circuit 100. The plurality of data lines DL1 to DLm are connected to the data driving circuit 200. Only some of the plurality of gate lines GL1 to GLn and only some of the plurality of data lines DL1 to DLm are illustrated in FIG. 1. Additionally, the display panel DP may further include a dummy gate line GLd disposed in the non display area NDA of the first substrate DS1.

[0046] Only some of the plurality of pixels PX are illustrated in FIG. 1. The plurality of pixels PX are respectively connected to corresponding gate lines among the plurality of gate lines GL1 to GLn and corresponding data lines among the plurality of data lines DL1 to DLm. However, the dummy gate line GLd is not connected to the plurality of pixels PX.

[0047] The plurality of pixels PX may be divided into a plurality of groups according to a color displayed. The plurality of pixels PX may display one of a plurality of primary colors. The primary colors may include red, green, blue, and white. However, the embodiment of the inventive concept is not limited thereto and the primary colors may further include various colors such as yellow, cyan, magenta, and so on.

[0048] The gate driving circuit 100 and the data driving circuit 200 receive a control signal from a signal control unit 300 (for example, a timing controller). The signal control unit 300 may be mounted on the first circuit board PBA-C and may receive power from the power management circuit 400. The first circuit board PBA-C may be a printed board assembly (PBA). The power management circuit 400 may be a Power Management IC (PMIC).

[0049] The signal control unit 300 receives image data and control signals from an external graphic control unit (not shown). The control signals may include vertical sync signals that are signals for distinguishing frame sections, horizontal sync signals that are signals for distinguishing horizontal sections, that is, row distinction signals, and data enable signals that are in high level only during a section where data is outputted to display a data incoming area, and clock signals.

[0050] The gate driving circuit 100 generates gate signals based on a control signal (hereinafter referred to as a gate control signal) received from the signal control unit 300 and outputs the generated gate signals to the gate lines GL1 to GLn.

[0051] FIG. 1 shows one gate driving circuit 100 connected to the left ends of the plurality of gate lines GL1 to GLn. In an embodiment of the inventive concept, the display device may include two gate driving circuits. One of the two gate driving circuits may be connected to the left ends of the plurality of gate lines GL1 to GLn and the other one may be connected to the right ends of the plurality of gate lines GL1 to GLn. Additionally, one of the two gate driving circuits may be connected to odd gate lines and the other one may be connected to even gate lines.

[0052] The data driving circuit 200 generates gradation voltages according to image data provided from the signal control unit 300 on the basis of a control signal (hereinafter referred to as a data control signal) received from the signal control unit 300. The data driving circuit 200 outputs the gradation voltages to the plurality of data lines DL1 to DLm as data voltages.

[0053] In this specification, signals transmitted from an external graphic control unit and transmitted to the signal control unit 300, the data driving circuit 200, and the pixel PX may be collectively referred to as a data signal. The form of the data signal from the external graphic control unit to the pixel (PX) may be changed or processed, and the data signal is a signal including data for displaying an image in the display area DA.

[0054] The data driving circuit 200 includes a driving chip 210 and a flexible circuit board 220 mounting the driving chip 210. Each of the driving chip 210 and the flexible circuit board 220 may be provided in plurality. The flexible circuit board 220 may electrically connect the second circuit board PBA-S and the first substrate DS1.

[0055] The two adjacent second circuit boards PBA-S may be connected to each other by another flexible circuit board FPC.

[0056] The second circuit board PBA-S may be connected to the first circuit board PBA-C by a flexible flat cable FFC.

[0057] The plurality of driving chips 210 provide data signals corresponding to corresponding data lines among the plurality of data lines DL1 to DLm.

[0058] The signal control unit 300 and the driving chips 210 may be connected by interfaces USI. The interfaces USI include a center interface USI-C for connecting the signal control unit 300 to a near driving chip 210 and a side interface USI-S for connecting the signal control unit 300 to a far driving chip 210.

[0059] FIG. 1 shows a Tape Carrier Package (TCP) type data driving circuit 200 as an example. According to an embodiment of the inventive concept, the data driving circuit 210 may be disposed in the non-display area NDA of the first substrate DS1 through a Chip on Glass (COG) method.

[0060] On a plane, a backlight unit 500 may be disposed below the display panel DP. The backlight unit 500 may include a plurality of light sources (not shown). The backlight unit 500 may provide light to the display panel DP and the light emitted from the backlight unit 500 may pass through the display panel DP and be visible to the users of the display device DD.

[0061] FIG. 2 shows an equivalent circuit diagram corresponding to the pixels PX1, PX2, and PX3 connected to the

first to third data lines DL1 to DL3 and the i-th gate line GLi among the pixels PX in FIG. 1.

[0062] Referring to FIG. 2, the first pixel PX1 includes a first transistor TR1, a first liquid crystal capacitor Clc1, and a first storage capacitor Cst1. In this specification, a transistor refers to a thin film transistor. According to an embodiment of the inventive concept, the first storage capacitor Cst1 may be omitted.

[0063] The first transistor TR1 is electrically connected to the i-th gate line GLi and the first data line DL1. The first transistor TR1 outputs a pixel voltage corresponding to a data signal received from the first data line DL1 in response to a gate signal received from the i-th gate line GLi.

[0064] The first liquid crystal capacitor Clc1 is charged with a pixel voltage outputted from the first transistor TR1. An arrangement of liquid crystal directors included in a liquid crystal layer LCL (see FIG. 4) is changed according to a charge amount charged in the first liquid crystal capacitor Clc1. The light incident to a liquid crystal layer may be transmitted or blocked according to an arrangement of liquid crystal directors.

[0065] Light emitted in a region corresponding to the first pixel PX1 may have a red color. In an embodiment of the inventive concept, when light emitted from the backlight unit 500 passes through a region corresponding to the first pixel PX1, light having a red color may be generated. In an embodiment of the inventive concept, when light emitted from the backlight unit 500 passes through a region corresponding to the first pixel PX1, only light having a wavelength of 640 nm or more and 730 nm or less may be transmitted.

[0066] The first storage capacitor Cst1 is connected in parallel to the first liquid crystal capacitor Clc1. The first storage capacitor Cst1 maintains the arrangement of liquid crystal directors during a predetermined section.

[0067] The second pixel PX2 includes a second transistor TR2, a second liquid crystal capacitor Clc2, and a second storage capacitor Cst2. According to an embodiment of the inventive concept, the second storage capacitor Cst2 may be omitted.

[0068] The second transistor TR2 is electrically connected to the i-th gate line GLi and the second data line DL2. The second transistor TR2 outputs a pixel voltage corresponding to a data signal received from the second data line DL2 in response to a gate signal received from the i-th gate line GLi.

[0069] The second liquid crystal capacitor Clc2 is charged with a pixel voltage outputted from the second transistor TR2. An arrangement of liquid crystal directors included in a liquid crystal layer LCL (see FIG. 4) is changed according to a charge amount charged in the second liquid crystal capacitor Clc2. The light incident to a liquid crystal layer may be transmitted or blocked according to an arrangement of liquid crystal directors.

[0070] Light emitted in a region corresponding to the second pixel PX2 may have a green color. In an embodiment of the inventive concept, when light emitted from the backlight unit 500 passes through a region corresponding to the second pixel PX2, light having a green color may be generated. In an embodiment of the inventive concept, when light emitted from the backlight unit 500 passes through a region corresponding to the second pixel PX2, only light having a wavelength of 492 nm or more and 580 nm or less may be transmitted.

[0071] The second storage capacitor Cst2 is connected in parallel to the second liquid crystal capacitor Clc2. The second storage capacitor Cst2 maintains the arrangement of liquid crystal directors during a predetermined section.

[0072] The third pixel PX3 may include a first sub-pixel PX-S 1 and a second sub-pixel PX-S2.

[0073] The first sub-pixel PX-S1 may include a third transistor TR3, a third liquid crystal capacitor Clc3, and a third storage capacitor Cst3. The second sub-pixel PX-S2 may include a fourth transistor TR4, a fifth transistor TR5, a fourth liquid crystal capacitor Clc4, and a fourth storage capacitor Cst4.

[0074] The control electrode of the third transistor TR3 is connected to the i-th gate line GLi, the input electrode of the third transistor TR3 is connected to the third data line DL3, and the output electrode of the third transistor TR3 is connected to the third liquid crystal capacitor Clc3 and the third storage capacitor Cst3.

[0075] The first electrode of the third liquid crystal capacitor Clc3 is connected to the output electrode of the third transistor TR3 and the second electrode of the third liquid crystal capacitor Clc3 receives the common voltage Vcom. The first electrode of the third storage capacitor Cst3 is connected to the output electrode of the third transistor TR3 and the second electrode of the third storage capacitor Cst3 receives the storage voltage Vcst.

[0076] The control electrode of the fourth transistor TR4 is connected to the i-th gate line GLi, the input electrode of the fourth transistor TR4 is connected to the third data line DL3, and the output electrode of the fourth transistor TR4 is connected to the fourth liquid crystal capacitor Clc4 and the fourth storage capacitor Cst4.

[0077] The control electrode of the fifth transistor TR5 is connected to the i-th gate line GLi, the input electrode of the fifth transistor TR5 receives the storage voltage Vcst, and the output electrode of the fifth transistor TR5 is connected to the output electrode of the fourth transistor TR4.

[0078] The first electrode of the fourth liquid crystal capacitor Clc4 is connected to the output electrode of the fourth transistor TR4 and the second electrode of the fourth liquid crystal capacitor Clc4 receives the common voltage Vcom. The first electrode of the fourth storage capacitor Cst4 is connected to the output electrode of the fourth transistor TR4 and the second electrode of the fourth storage capacitor Cst4 receives the storage voltage Vcst.

[0079] The common voltage Vcom and the storage voltage Vcst may have substantially the same voltage.

[0080] The third to fifth transistors TR3, TR4, and TR5 are turned on by the gate signal provided through the gate line GLi.

[0081] The data voltage of the third data line DL3 is supplied to the first sub-pixel PX-S1 through the turned-on third transistor TR3. The third liquid crystal capacitor Clc3 is charged with the pixel voltage (hereinafter referred to as the first pixel voltage) corresponding to the level difference between the provided data voltage and the common voltage Vcom. The arrangement of the liquid crystal director included in the liquid crystal layer LCL is changed according to the amount of charge charged in the third liquid crystal capacitor Clc3. The light incident to a liquid crystal layer may be transmitted or blocked according to an arrangement of liquid crystal directors. The third storage capacitor Cst3 is connected in parallel to the third liquid crystal capacitor

Clc3 to maintain the arrangement of the liquid crystal director for a predetermined period.

[0082] The data voltage of the third data line DL3 is supplied to the second sub-pixel PX-S2 through the turned-on fourth transistor TR4. In addition, the storage voltage Vcst is supplied to the second sub-pixel PX-S2 through the turned-on fifth transistor TR5.

[0083] The voltage (hereinafter referred to as a distribution voltage) at the contact node CN to which the fourth transistor TR4 and the fifth transistor TR5 are connected has a value that is distributed according to the ratio of the resistance value when each of the fourth and fifth transistors TR4 and TR5 is turned-on. That is, the distribution voltage has a value between the data voltage supplied through the turned-on fourth transistor TR4 and the storage voltage Vcst provided through the turned-on fifth transistor TR5.

[0084] Thus, the fourth liquid crystal capacitor Clc4 is charged with the pixel voltage (hereinafter referred to as the second pixel voltage) corresponding to the level difference between the distribution voltage and the common voltage Vcom. The arrangement of the liquid crystal director included in the liquid crystal layer LCL is changed according to the amount of charge charged in the second liquid crystal capacitor Clc2. The light incident to a liquid crystal layer may be transmitted or blocked according to an arrangement of liquid crystal directors. The fourth storage capacitor Cst4 is connected in parallel to the fourth liquid crystal capacitor Clc4 to maintain the arrangement of the liquid crystal director for a predetermined period.

[0085] Since the first pixel voltage charged in the third liquid crystal capacitor Clc3 and the second pixel voltage charged in the fourth liquid crystal capacitor Clc4 are different from each other, the gradation displayed in the first sub-pixel PX-S1 is different from the gradation displayed in the second sub-pixel PX-S2. Thus, visibility of the third pixel PX3 may be improved by displaying images of different gradations in the first and second sub-pixels PX-S 1 and PX-S2.

[0086] Light emitted in a region corresponding to the third pixel PX3 may have a blue color. In an embodiment of the inventive concept, when light emitted from the backlight unit **500** passes through a region corresponding to the third pixel PX3, light having a blue color may be generated. In an embodiment of the inventive concept, when light emitted from the backlight unit **500** passes through a region corresponding to the third pixel PX3, only light having a wavelength of 420 nm or more and 490 nm or less may be transmitted.

[0087] The equivalent circuit diagram of the third pixel PX3 shown in FIG. **2** is illustratively shown, but not limited thereto. In other embodiments of the inventive concept, the third and fourth storage capacitors Cst3 and Cst4 may be omitted.

[0088] Referring to FIGS. **3**A to **3**C, the display area DA may include a first pixel region PXA1, a second pixel region PXA2, and a third pixel region PXA3.

[0089] Referring to FIG. **3**A, a first pixel region PE1, a first transistor TR1, a portion of a first data line DL1, and a portion of a gate line GLi may be disposed in a first pixel region PXA1.

[0090] The first pixel electrode PE1 includes a vertical electrode VP, a horizontal electrode HP, first branch electrodes B1, second branch electrodes B2, third branch electrodes B3, and fourth branch electrodes B4. The vertical electrode VP, the horizontal electrode HP, the first branch electrodes B1, the second branch electrodes B2, the third branch electrodes B3, and the fourth branch electrodes B4 are connected so that one first pixel electrode PE1 is formed.

[0091] The vertical electrode VP extends along the second direction DR2 and the horizontal electrode HP extends along the first direction DR1. Each of the first branch electrodes B 1, the second branch electrodes B2, the third branch electrodes B3, and the fourth branch electrodes B4 extends from the vertical electrode VP or the horizontal electrode HP. The configuration and shape of the first pixel electrode PE1 shown in FIG. **3**A are examples and the configuration and shape of the first pixel electrode PE1 may be changed.

[0092] Referring to FIG. **3**B, the second pixel electrode PE2, the second transistor TR2, a portion of the second data line DL2, and a portion of the gate line GLi may be disposed in the second pixel region PXA2.

[0093] The description of the second pixel region PXA2 is substantially the same as that of the first pixel region PXA1, and thus is omitted.

[0094] Referring to FIG. **3**C, the third pixel electrode PE3, the third transistor TR3, the fourth transistor TR4, the fifth transistor TR5, a portion of the third data line DL3, and a portion of the gate line GLi may be disposed in the third pixel region PXA3.

[0095] The third pixel electrode PE3 may include a first sub-pixel electrode PE31 and a second sub-pixel electrode PE32. In an embodiment of the inventive concept, the area of the second sub-pixel electrode PE32 may be larger than the area of the first sub-pixel electrode PE31.

[0096] The structure and shape of each of the first sub-pixel electrode PE31 and the second sub-pixel electrode PE32 may be substantially similar to the structure and shape of the first pixel electrode PE1 described with reference to FIG. **3**A.

[0097] The third pixel region PXA3 may include a high gradation region PXA3-H and a low gradation region PXA3-L. The high gradation region PXA3-H is defined as the region where the first sub-pixel electrode PE31 is disposed and the low gradation region PXA3-L is defined as the region where the second sub-pixel electrode PE32 is disposed. The high gradation region PXA3-H corresponds to the first sub-pixel PX-S1 in FIG. **2** and the low gradation region PXA3-L corresponds to the second sub-pixel PX-S2 in FIG. **2**.

[0098] In this specification, the first sub-pixel electrode PE31 and the second sub-pixel electrode PE32 may be understood as different sub-pixel electrodes. In this case, it may be understood that one pixel electrode is disposed in each of the first pixel region PXA1 and the second pixel region PXA2, and two pixel electrodes are disposed in the third pixel region PXA3.

[0099] The gradation of the light emitted from the high gradation region PXA3-H may be higher than the gradation of the light emitted from the low gradation region PXA3-L.

[0100] In FIG. **4**, a part of the cross section of the first pixel PX1 is shown. Since the cross section of the second pixel PX2 and the third pixel PX3 is substantially the same as the cross section of the first pixel PX1, in the present specification, the lamination structure of the description display panel DP will be described with reference to the cross section of the first pixel PX1.

[0101] As shown in FIGS. **3**A and **4**, the first transistor TR1 includes a control electrode CTE connected to the i-th

gate line GLi, an activation layer AL overlapping the control electrode CTE, an input electrode IE connected to the first data line DL**1**, and an output electrode OE disposed apart from the input electrode IE.

[0102] The first liquid crystal capacitor Clc**1** may be formed by the first pixel electrode PE**1** and the common electrode CE. The first storage capacitor Cst**1** may be formed by the first pixel electrode PE**1** and the storage line STL overlapping the first pixel electrode PE**1**.

[0103] The i-th gate line GLi and the storage line STL are disposed on one surface of the first substrate DS**1**. The control electrode CTE is branched from the i-th gate line GLi. The i-th gate line GLi and the storage line STL may include a metal (for example, Al, Ag, Cu, Mo, Cr, Ta, Ti, and so on) or an alloy thereof. The i-th gate line GLi and the storage line STL may have a multi layer structure, and for example, may include a Ti layer and a Cu layer.

[0104] A first insulating layer **10** covering the control electrode CTE and the storage line STL is disposed on one surface of the first substrate DS**1**. The first insulating layer **10** may include at least one of an inorganic material and an organic material. The first insulating layer **10** may be an organic layer or an inorganic layer. The first insulating layer **10** may have a multi layer structure and for example, may include a silicon nitride layer and a silicon oxide layer.

[0105] The activation layer AL overlapping the control electrode CTE is disposed on the first insulating layer **10**. The activation layer AL may include a semiconductor layer (not shown) and an ohmic contact layer (not shown).

[0106] The activation layer AL may include amorphous silicon, polysilicon, or a metal oxide semiconductor.

[0107] An output electrode OE and an input electrode IE are disposed on the activation layer AL.

[0108] Although the first transistor TR**1** having a staggered structure is shown in FIG. **4** as an example, a structure of the first transistor TR**1** is not limited thereto. The first transistor TR**1** may have a planar structure.

[0109] A second insulating layer **20** covering the activation layer AL, the output electrode OE, and the input electrode IE is disposed on the first insulating layer **10**. The second insulating layer **20** provides a flat surface. The second insulating layer **20** may include an organic material.

[0110] The first pixel electrode PE**1** is displayed on the second insulating layer **20**. The first pixel electrode PE**1** is connected to the output electrode OE through a second insulating layer **20** and a first contact hole CH**1** penetrating the second insulating layer **20**. The second contact hole CH**2** shown in FIG. **3**B and the third and fourth contact holes CH**3** and CH**4** shown in FIG. **3**C may also function as the first contact hole CH**1**.

[0111] An alignment film **30** covering the first pixel electrode PE**1** may be disposed on the second insulating layer **20**.

[0112] A first color filter CF**1** is disposed on one surface of the second substrate DS**2**. The first color filter CF**1** is disposed overlapping the first pixel electrode PE**1**. A common voltage is applied to the common electrode CE. A common voltage and a pixel voltage have different values. An alignment film (not shown) covering the common electrode CE may be disposed on the common electrode CE. Another insulating layer may be disposed between the first color filter layer CF**1** and the common electrode CE.

[0113] The first color filter CF**1** may transmit light having a wavelength of 640 nm or more and 730 nm or less among the incident light. In an embodiment of the inventive concept, the first color filter CF**1** may transmit only light of a specific wavelength band among the incident light, thereby generating light having a red color.

[0114] Although not shown in the drawing, the display panel DP may further include a second color filter (not shown) disposed in the second pixel region PXA**2** and overlapping the second pixel electrode PE**2**. The second color filter may transmit light having a wavelength of 492 nm or more and 580 nm or less among the incident light. In an embodiment of the inventive concept, the second color filter may transmit only light of a specific wavelength band among the incident light, thereby generating light having a green color.

[0115] Although not shown in the drawing, the display panel DP may further include a third color filter (not shown) disposed in the third pixel region PXA**3** and overlapping the third pixel electrode PE**3**. The third color filter may transmit light having a wavelength of 420 nm or more and 490 nm or less among the incident light. In an embodiment of the inventive concept, the third color filter may transmit only light of a specific wavelength band among the incident light, thereby generating light having a blue color.

[0116] On the other hand, a section of the pixel PX shown in FIG. **4** is just one example. In another example embodiment, at least one of the first color filter layer CF**1** and the common electrode CE may be disposed on the first substrate DS**1**. That is, a liquid crystal display panel according to this embodiment of the inventive concept may include a pixel in a Vertical Alignment (VA) mode, a Patterned Vertical Alignment (PVA) mode, an in-plane switching (IPS) mode, a fringe-field switching (FFS) mode, or a Plane to Line Switching (PLS) mode.

[0117] In the case of having the layout structure of the third pixel region PXA**3** shown in FIG. **3**C, the visibility or the viewing angle characteristics are improved as compared with the layout structure of the first and second pixel regions PXA**1** and PXA**2** shown in FIGS. **3**A and **3**B. On the other hand, in the case of having the layout structure of the third pixel region PXA**3** shown in FIG. **3**C, more transistors are arranged than in the case of having the layout structure of the first and second pixel regions PXA**1** and PXA**2** shown in FIGS. **3**A and **3**B, and accordingly, the light transmittance of the third pixel region PXA**3** becomes lower than the light transmittance of the first and second pixel regions PXA**1** and PXA**2**.

[0118] That is, the ratio (hereinafter referred to as a first ratio) of the light emitted from the backlight unit **500** to the first pixel region PXA**1** may be substantially the same as the ratio (hereinafter referred to as a second ratio) at which light emitted from the backlight unit **500** passes through the second pixel region PXA**2**. However, the ratio (hereinafter referred to as the third ratio) of the light emitted from the backlight unit **500** to the third pixel region PXA**3** may be smaller than the first ratio or the second ratio.

[0119] Thus, the visibility and viewing angle characteristics and the light transmittance characteristics are in a trade off relationship with each other.

[0120] When assuming that red light, green light, and blue light having the same area are emitted, the ratio of the red light to the total luminance is about 15% and the ratio of the green light to the total luminance is about 80%, and the ratio of the blue light to the total luminance is about 5%. Therefore, when the amount of green light in red light, green

light, and blue light is reduced, it greatly affects the overall luminance, but when the amount of blue light is reduced, it does not significantly affect the overall luminance.

[0121] Therefore, as shown in FIG. **2**, a structure for improving the visibility and the viewing angle characteristic may be applied only to the third pixel PX**3** from which blue light is emitted, and a structure for securing a high light transmittance may be applied to the first pixel PX**1** and the second pixel PX**2**. By the combination of the first to third pixels PX**1** to PX**3**, the viewing angle and visibility characteristics are improved and the display panel DP having high light transmittance may be provided.

[0122] FIG. **5** shows an example in which a first pixel region PXA**1**, a second pixel region PXA**2**, and a third pixel region PXA**3** are disposed. FIG. **6** exemplarily shows a luminance control method for driving a display panel DP including pixel regions PXA**1** to PXA**3** as shown in FIG. **5**.

[0123] Referring to **5**, the horizontal length measured on the first direction DR**1** of the first pixel region PXA**1**, the second pixel region PXA**2**, and the third pixel region PXA**3** may be shorter than a particular vertical length on the second direction DR**2**.

[0124] The first pixel region PXA**1**, the second pixel region PXA**2**, and the third pixel region PXA**3** may be sequentially arranged in the first direction DR**1**.

[0125] Referring to FIG. **6**, since the third pixel region PXA**3** emitting blue light has a lower light transmittance than the first pixel region PXA**1** emitting red light and the second pixel region PXA**2** emitting green light, the maximum luminance B max luminance that the blue light may have is lower than the maximum luminance RIG max luminance that the red light and the green light may have. Therefore, if the luminance of the light emitted from each of the first to third pixel regions PXA**1** to PXA**3** is not adjusted, red light, green light, and blue light are not combined at an originally expected ratio, resulting in a problem that desired colors are not emitted.

[0126] Therefore, when the luminance of the red light and the green light is reduced in correspondence to the maximum luminance B max luminance that the blue light may have, a desired color may be realized through a combination of these.

[0127] FIG. **7** shows an example in which a first pixel region PXA**1-1**, a second pixel region PXA**2-1**, and a third pixel region PXA**3-1** are disposed. The third pixel region PXA**3-1** includes a high gradation region PXA**3-1**H and a low gradation region PXA**3-1**L.

[0128] The horizontal length measured on the first direction DR**1** of the first pixel region PXA**1-1**, the second pixel region PXA**2-1**, and the third pixel region PXA**3-1** may be longer than a particular vertical length on the second direction DR**2**.

[0129] The first pixel region PXA**1-1**, the second pixel region PXA**2-1**, and the third pixel region PXA**3-1** may be sequentially arranged in the second direction DR**2**.

[0130] In addition, the description of each of the first pixel region PXA**1-1**, the second pixel region PXA**2-1**, and the third pixel region PXA**3-1** is substantially the same as the description of each of the first pixel region PXA**1**, the second pixel region PXA**2**, and the third pixel region PXA**3** described above, such that its description will be omitted.

[0131] FIG. **8** shows an example in which a first pixel region PXA**1-2**, a second pixel region PXA**2**, and a third pixel region PXA**3** are disposed. FIG. **8** is a view of the first pixel region PXA**1-1** of FIG. **7** changed to the first pixel region PXA**1-2**.

[0132] The first pixel region PXA**1-2** may include a high gradation region PXA**1-2**H and a low gradation region PXA-**2**L.

[0133] Although the first pixel region PXA**1-2** is a region that emits light having a red color, it may have a structure for improving the visibility and viewing angle characteristics as shown in FIG. **3**C. As described above, since the ratio of the red light to the total luminance is about 15% and it is smaller than the ratio of the green light to the total luminance, by the arrangement of the pixel regions PXA**1-2**, PXA**2**, and PXA**3** shown in FIG. **8**, it is possible to provide a display panel DP having good visibility and viewing angle characteristics and excellent light transmittance.

[0134] According to an embodiment of the inventive concept, a liquid crystal display panel having excellent visibility and viewing angle characteristics and a liquid crystal display device including the liquid crystal display panel may be provided.

[0135] Also, according to an embodiment of the inventive concept, it is possible to provide a liquid crystal display panel having excellent light transmittance at a high resolution and a liquid crystal display device including the liquid crystal display panel.

[0136] Although the exemplary embodiments of the inventive concept have been described, it is understood that the inventive concept should not be limited to these exemplary embodiments but various changes and modifications may be made by one ordinary skilled in the art within the spirit and scope of the inventive concept as hereinafter claimed.

What is claimed is:

1. A liquid crystal display device comprising:

a display panel including a liquid crystal layer, wherein a first pixel region, a second pixel region, and a third pixel region are defined in the display panel; and

a backlight unit configured to provide light to the display panel,

wherein each of a wavelength of a first color light generated by transmitting the light through the first pixel region and a wavelength of a second color light generated by transmitting the light through the second pixel region is longer than a wavelength of a third color light generated by transmitting the light through the third pixel region,

wherein a first ratio at which the light passes through the first pixel region and a second ratio at which the light passes through the second pixel region is greater than a third ratio at which the light passes through the third pixel region.

2. The liquid crystal display device of claim **1**, wherein the first color light has a red color, the second color light has a green color, and the third color light has a blue color.

3. The liquid crystal display device of claim **2**, wherein the third pixel region comprises a high gradation region and a low gradation region,

wherein a gradation of light emitted from the high gradation region of the third color light is higher than a gradation of light emitted from the low gradation region of the third color light.

4. The liquid crystal display device of claim **1**, wherein the display panel comprises a plurality of transistors,

wherein the number of transistors disposed in the first pixel region among the plurality of transistors is equal to the number of transistors disposed in the second pixel region among the plurality of transistors,

wherein the number of transistors disposed in the third pixel region among the plurality of transistors is greater than the number of transistors disposed in the first pixel region among the plurality of transistors.

5. The liquid crystal display device of claim **4**, wherein the number of the transistors disposed in the first pixel region is one, and the number of the transistors disposed in the third pixel region is three.

6. The liquid crystal display device of claim **1**, wherein the display panel further comprises:

a first color filter overlapping the first pixel region and configured to transmit light having a wavelength of between 640 nm and 730 nm in the light;

a second color filter overlapping the second pixel region and configured to transmit light having a wavelength of between 492 nm and 580 nm in the light; and

a third color filter overlapping the third pixel region and configured to transmit light having a wavelength of between 420 nm and 490 nm in the light.

7. The liquid crystal display device of claim **1**, wherein the display panel further comprises:

a plurality of pixel electrodes; and

a common electrode overlapping the plurality of pixel electrodes,

wherein the liquid crystal layer is disposed between the plurality of pixel electrodes and the common electrode.

8. The liquid crystal display device of claim **7**, wherein the number of pixel electrodes disposed in the first pixel region among the plurality of pixel electrodes is equal to the number of pixel electrodes disposed in the second pixel region among the plurality of pixel electrodes,

wherein the number of pixel electrodes disposed in the third pixel region among the plurality of pixel electrodes is greater than the number of pixel electrodes disposed in the first pixel region.

9. The liquid crystal display device of claim **8**, wherein the number of the pixel electrodes disposed in the first pixel region is one and the number of the pixel electrodes disposed in the third pixel region is two.

10. A liquid crystal display panel comprising:

a first substrate where a first pixel region, a second pixel region, and a third pixel region are defined;

a second substrate facing the first substrate; and

a liquid crystal layer disposed between the first substrate and the second substrate,

wherein a first color light emitted from the first pixel region has a red color, a second color light emitted from the second pixel region has a green color, and a third color light emitted from the third pixel region has a blue color,

wherein a light transmittance of the third pixel region is less than a light transmittance of the first pixel region and a light transmittance of the second pixel region.

11. The liquid crystal display panel of claim **10**, wherein the third pixel region comprises a high gradation region and a low gradation region,

wherein a gradation of light emitted from the high gradation region in the third color light is higher than a gradation of light emitted from the low gradation region in the third color light.

12. The liquid crystal display panel of claim **11**, further comprising a plurality of transistors disposed on the first substrate,

wherein the number of transistors disposed in the first pixel region among the plurality of transistors is equal to the number of transistors disposed in the second pixel region among the plurality of transistors,

wherein the number of transistors disposed in the third pixel region among the plurality of transistors is greater than the number of transistors disposed in the first pixel region among the plurality of transistors.

13. The liquid crystal display panel of claim **12**, wherein the number of the transistors disposed in the first pixel region is one, and the number of the transistors disposed in the third pixel region is three.

14. The liquid crystal display panel of claim **12**, further comprising a plurality of pixel electrodes, each of which is electrically connected to the plurality of transistors; and

a common electrode overlapping the plurality of pixel electrodes,

wherein the liquid crystal layer is disposed between the plurality of pixel electrodes and the common electrode.

15. The liquid crystal display panel of claim **14**, wherein the number of pixel electrodes disposed in the first pixel region among the plurality of pixel electrodes is equal to the number of pixel electrodes disposed in the second pixel region among the plurality of pixel electrodes,

wherein the number of pixel electrodes disposed in the third pixel region among the plurality of pixel electrodes is greater than the number of pixel electrodes disposed in the first pixel region.

16. The liquid crystal display panel of claim **15**, wherein the number of the pixel electrodes disposed in the first pixel region is one and the number of the pixel electrodes disposed in the third pixel region is two.

17. A liquid crystal display device comprising:

a display panel including a liquid crystal layer, wherein a first pixel region, a second pixel region, and a third pixel region are defined in the display panel; and

a backlight unit configured to provide light to the display panel,

wherein each of the first pixel region and the second pixel region comprises only one transistor, and the third pixel region comprises three transistors,

wherein each of a wavelength of a first color light generated by transmitting the light through the first pixel region and a wavelength of a second color light generated by transmitting the light through the second pixel region is longer than a wavelength of a third color light generated by transmitting the light through the third pixel region.

18. The liquid crystal display device of claim **17**, wherein the first color light has a red color, the second color light has a green color, and the third color light has a blue color.

19. The liquid crystal display device of claim **18**, wherein the third pixel region comprises a high gradation region and a low gradation region,

wherein a gradation of light emitted from the high gradation region of the third color light is higher than a gradation of light emitted from the low gradation region of the third color light.

20. The liquid crystal display device of claim **17**, wherein a first ratio at which the light passes through the first pixel region and a second ratio at which the light passes through the second pixel region is greater than a third ratio at which the light passes through the third pixel region.

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专利名称(译)	液晶显示面板和包括该液晶显示面板的液晶显示装置		
公开(公告)号	US20200081282A1	公开(公告)日	2020-03-12
申请号	US16/512330	申请日	2019-07-15
[标]申请(专利权)人(译)	三星显示有限公司		
申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	TAE HEUNG SIK		
发明人	TAE, HEUNG-SIK SHIM, YOONSEOP		
IPC分类号	G02F1/1368 G02F1/1335		
CPC分类号	G02F1/133514 G02F2201/52 G02F1/1368 G02F1/136213 G02F1/134309 G02F1/1362 G02F2001/136222 G02F1/13624 G02F1/136286 G02F2001/134345 G02F2001/134354		
优先权	1020180109052 2018-09-12 KR		
外部链接	Espacenet USPTO		

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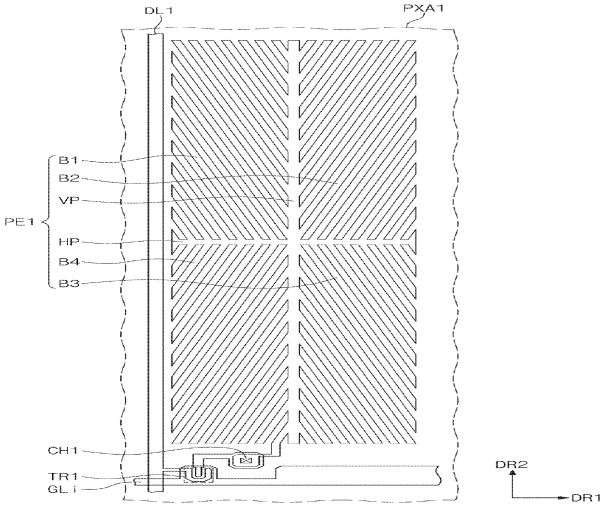
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