



US 20180164634A1

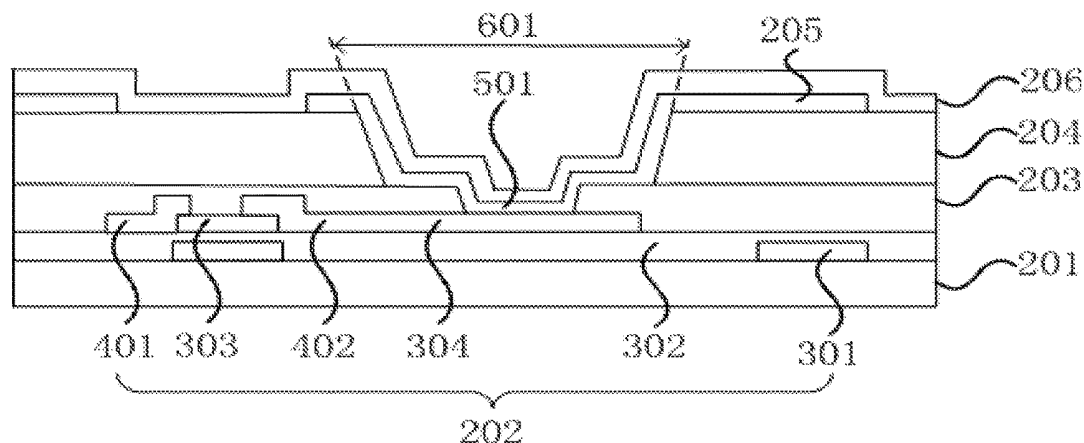
(19) **United States**(12) **Patent Application Publication**
DENG(10) **Pub. No.: US 2018/0164634 A1**(43) **Pub. Date: Jun. 14, 2018**(54) **ARRAY SUBSTRATE AND LIQUID CRYSTAL
DISPLAY PANEL****Publication Classification**(71) Applicant: **SHENZHEN CHINA STAR
OPTOELECTRONICS
TECHNOLOGY CO., LTD.**, Shenzhen
(CN)(51) **Int. Cl.**
G02F 1/1335 (2006.01)
G02F 1/1343 (2006.01)
G02F 1/1362 (2006.01)(72) Inventor: **Zhuming DENG**, Shenzhen (CN)(52) **U.S. Cl.**
CPC **G02F 1/133514** (2013.01); **G02F**
2001/1635 (2013.01); **G02F 1/136286**
(2013.01); **G02F 1/1343** (2013.01)(73) Assignee: **SHENZHEN CHINA STAR
OPTOELECTRONICS
TECHNOLOGY CO., LTD.**, Shenzhen
(CN)(57) **ABSTRACT**(21) Appl. No.: **15/305,187**(22) PCT Filed: **Jun. 3, 2016**(86) PCT No.: **PCT/CN2016/084765**

§ 371 (c)(1),

(2) Date: **Oct. 19, 2016**(30) **Foreign Application Priority Data**

Apr. 12, 2016 (CN) 201610224791.5

An array substrate and a liquid crystal display (LCD) panel thereof are described. The array substrate includes a bottom substrate; a thin film transistor disposed on the bottom substrate; a first passivation layer disposed on the thin film transistor and comprising a first opening which exposes the drain electrode region of the thin film transistor; a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer comprises a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor; a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and a second passivation layer disposed on the pixel electrode layer.



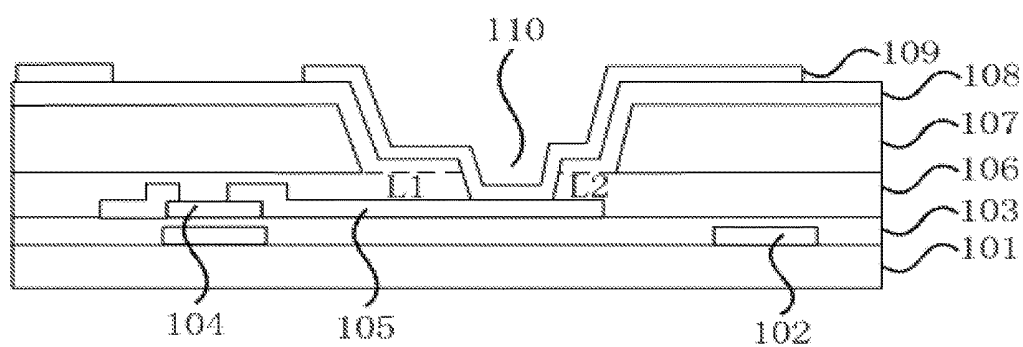


FIG. 1 (Prior Art)

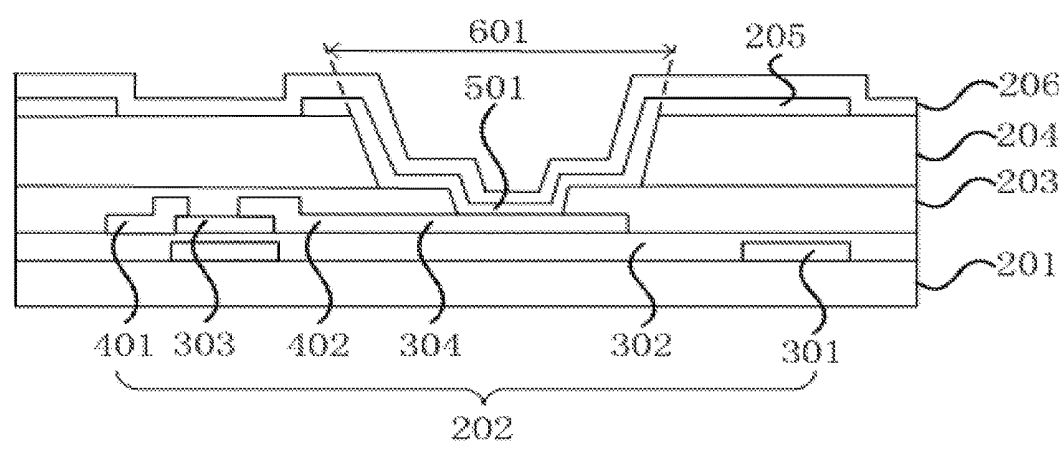


FIG. 2

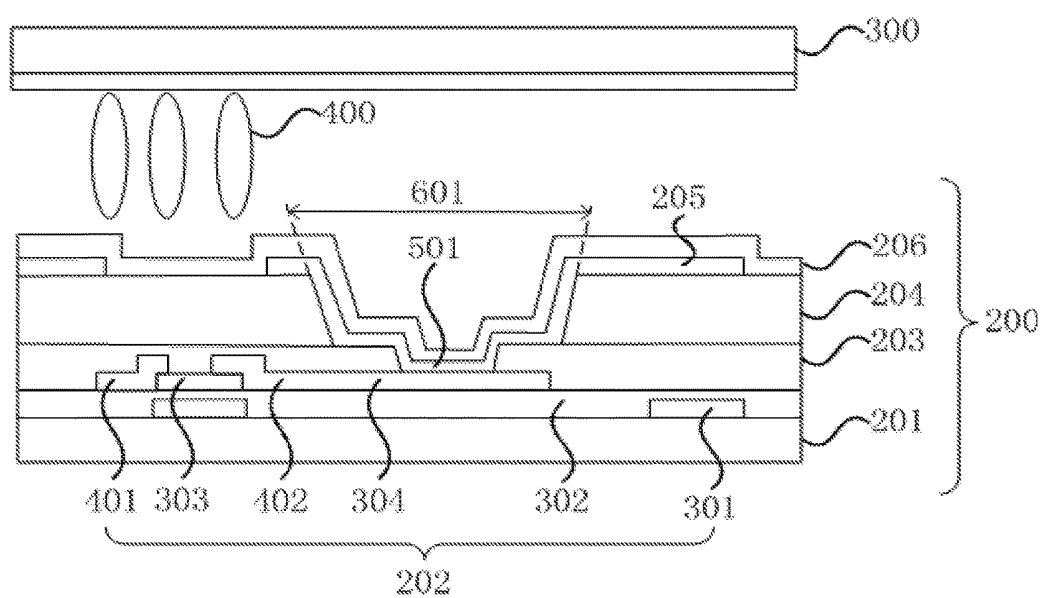


FIG. 3

ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY PANEL

BACKGROUND OF THE INVENTION

Field of Invention

[0001] The present invention relates to a technical field of liquid crystal display (LCD), and more particularly to an array substrate and an LCD panel.

Description of Prior Art

[0002] With the rapid development of technology, more and more LCD devices are widely used. To achieve the requirement of better color display in the LCD devices, a color film is formed on an array substrate of conventional LCD device to provide RGB primary colors on the array substrate, thereby avoiding the alignment between the array substrate and color filter substrate for better full color display of the LCD device. The above-described technique is termed as Color Filter on Array (COA).

[0003] FIG. 1 is a schematic structural view of a conventional COA array substrate. The COA array substrate includes a bottom substrate **101**, a first metal layer **102** disposed on the bottom substrate **101** and configured to form scan lines and a gate region of a thin film field-effect transistor, a gate insulation layer **103** disposed on the first metal layer **102**, a semiconductor layer **104** disposed on the gate insulation layer **103** and configured to form the channel of the thin film field-effect transistor, a second metal layer **105** disposed on the semiconductor layer **104** and configured to form a source region and a drain region of the thin film field-effect transistor and data lines, a first passivation layer **106** disposed on the second metal layer **105** and gate insulation layer **103**, a color resist layer **107** disposed on the first passivation layer **106** and configured to form a color filter film, a second passivation layer **108** disposed on the color resist layer **107**, and a pixel electrode layer **109** disposed on the second passivation layer **108**.

[0004] To electrically connect the pixel electrode layer **109** with second metal layer **105**, a plurality of openings are formed in the first passivation layer **106**, color resist layer **107** and second passivation layer **108**. Generally, after the opening of first passivation layer **106** is formed, the color resist layer **107** is formed, and after the opening of color resist layer **107** is formed, the second passivation layer **108** is formed. Afterwards, since the opening **110** of second passivation layer **108** are formed due to the alignment error of manufacturing procedure, the openings of first passivation layer **106** and second passivation layer **108** cannot be aligned to the opening of the color resist layer **107** completely, thereby downgrading an overlapping status between the first passivation layer **106** and second passivation layer **108**. As shown in FIG. 1, the lengths **L1** and **L2** are depicted as dashed lines where **L1** and **L2** are the overlapping widths of first passivation layer **106** and second passivation layer **108** respectively. The openings of first passivation layer **106** and second passivation layer **108** shift to the right side with respect to the color resist layer **107** so that the length **L2** is less than length **L1** and thus, the overlapping widths of first passivation layer **106** near the length **L2** are decreased. If the shifting widths of two openings are too large, the protection of the color resist layer is poor in the increased overlapping widths of first passivation layer **106** and second passivation

layer **108** so that the bubble in the color resist layer exudes near the opening of color filter film, thereby downgrading the display quality of the products.

SUMMARY OF THE INVENTION

[0005] One objective of the present invention is to provide an array substrate and a liquid crystal display (LCD) panel to prevent the bubble in the color resist layer from exuding near the opening of color filter film.

[0006] Based on the above objective, one embodiment of the present invention sets forth an array substrate. The array substrate includes a bottom substrate; a thin film transistor disposed on the bottom substrate, the thin film transistor including a first metal layer disposed on the bottom substrate and configured to form a plurality of scan lines and a gate electrode region of a thin film field-effect transistor; a first insulation layer disposed on the first metal layer; a semiconductor layer disposed on the first insulation layer and configured to form a channel region of the thin film field-effect transistor; and a second metal layer disposed on the semiconductor layer and configured to form a source electrode region and a drain electrode region of the thin film field-effect transistor and form a plurality of data lines; a first passivation layer disposed on the thin film transistor and including a first opening which exposes the drain electrode region of the thin film transistor; a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer includes a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor, a hole diameter of the second opening is greater than a hole diameter of the first opening, and the color resist layer includes a plurality of color resists wherein two adjacent color resists therebetween form the second opening; a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and a second passivation layer disposed on the pixel electrode layer.

[0007] In one embodiment, the array substrate includes a bottom substrate; a thin film transistor disposed on the bottom substrate; a first passivation layer disposed on the thin film transistor and including a first opening which exposes the drain electrode region of the thin film transistor; a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer includes a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor; a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and a second passivation layer disposed on the pixel electrode layer.

[0008] In one embodiment, the thin film transistor includes a first metal layer disposed on the bottom substrate and configured to form a plurality of scan lines and a gate electrode region of a thin film field-effect transistor; a first insulation layer disposed on the first metal layer; a semiconductor layer disposed on the first insulation layer and configured to form a channel region of the thin film field-effect transistor; and a second metal layer disposed on the semiconductor layer and configured to form a source electrode region and a drain electrode region of the thin film field-effect transistor and form a plurality of data lines.

[0009] In one embodiment, a hole diameter of the second opening is greater than a hole diameter of the first opening.

[0010] In one embodiment, the color resist layer includes a plurality of color resists and two adjacent color resists therebetween form the second opening.

[0011] In one embodiment, the color resists includes a color R resist, a color G resist and a color B resist.

[0012] In one embodiment, a liquid crystal display panel includes an array substrate and a glass substrate opposite the array substrate wherein a liquid crystal is filled into the array substrate and glass substrate therebetween, the array substrate including a bottom substrate; a thin film transistor disposed on the bottom substrate; a first passivation layer disposed on the thin film transistor and including a first opening which exposes the drain electrode region of the thin film transistor; a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer includes a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor; a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and a second passivation layer disposed on the pixel electrode layer.

[0013] In one embodiment, the thin film transistor includes a first metal layer disposed on the bottom substrate and configured to form a plurality of scan lines and a gate electrode region of a thin film field-effect transistor; a first insulation layer disposed on the first metal layer; a semiconductor layer disposed on the first insulation layer and configured to form a channel region of the thin film field-effect transistor; and a second metal layer disposed on the semiconductor layer and configured to form a source electrode region and a drain electrode region of the thin film field-effect transistor and form a plurality of data lines.

[0014] In one embodiment, a hole diameter of the second opening is greater than a hole diameter of the first opening.

[0015] In one embodiment, the color resist layer includes a plurality of color resists and two adjacent color resists therebetween form the second opening.

[0016] In one embodiment, the color resists includes a color R resist, a color G resist and a color B resist.

[0017] The advantage of the present invention is that the pixel electrode layer is formed under the second passivation layer. In other word, after the pixel electrode layer is formed, the second passivation layer is then formed so that it is not required to pass through the second passivation layer while electrically connecting the pixel electrode layer to the drain electrode region of the thin film transistor. Therefore, in the display region, there is no need to form openings in the second passivation layer to maintain the integrity of the second passivation layer. The integrity of the second passivation layer is capable of protecting the color resist layer to avoid the bubble in the second opening.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 is a schematic structural view of a conventional COA array substrate;

[0019] FIG. 2 is a schematic structural view of an array substrate according to one embodiment of the present invention; and

[0020] FIG. 3 is a schematic structural view of an LCD panel according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0021] The following embodiments refer to the accompanying drawings for exemplifying specific implementable embodiments of an array substrate and an LCD panel of the present invention. Furthermore, directional terms described by the present invention, such as upper, lower, front, back, left, right, inner, outer, side, etc., are only directions by referring to the accompanying drawings, and thus the used directional terms are used to describe and understand the present invention, but the present invention is not limited thereto. In the drawings, the same reference symbol represents the same or a similar component.

[0022] FIG. 2 is a schematic structural view of an array substrate according to one embodiment of the present invention. The array substrate includes a bottom substrate **201**, a thin film transistor **202**, a first passivation layer **203**, a color resist layer **204**, a pixel electrode layer **205** and a second passivation layer **206**.

[0023] In one embodiment, the material of bottom substrate **201** is made of glass, which is configured to be a substrate of the thin film transistor **202** disposed on the bottom substrate **201**.

[0024] The thin film transistor **202** includes a first metal layer **301**, a first insulation layer **302**, a semiconductor layer **303** and a second metal layer **304**.

[0025] The first metal layer **301** disposed on the bottom substrate **201** is configured to form scan lines (not shown) and a gate electrode region of thin film transistor **202** where the material of first metal layer **301** is selected from chromium, molybdenum, aluminum and copper. The first insulation layer **302** disposed on the first metal layer **301** is configured to be a gate insulation layer where the first insulation layer **302** is composed of silicon nitride layer. The semiconductor layer **303** disposed on the first insulation layer **302** is configured to form a channel region of thin film transistor **202** where the semiconductor layer **303** is composed of amorphous silicon layer. The second metal layer **304** disposed on the semiconductor layer **303** is configured to form a source electrode region **401** and drain electrode region **402** of thin film transistor, and data lines (not shown), where the material of second metal layer **304** is selected from chromium, molybdenum, aluminum and copper.

[0026] The first passivation layer **203** disposed on the thin film transistor and includes a first opening **501** which exposes the drain electrode region **402** of thin film transistor **202**.

[0027] The color resist layer **204** disposed on the first passivation layer **203** is configured to form a color filter. For example, the color filter may be RGB color resist and black matrix. The color resist layer **204** includes a second opening **601** which corresponds to the first opening **501** to expose the drain electrode region **402** of thin film transistor **202**. Preferably, a hole diameter of the second opening **601** is greater than a hole diameter of the first opening **501** so that the drain electrode region **402** exposed from the first opening **501** can be completely exposed from the second opening **601**. Meanwhile, the alignment between the second opening **601** and first opening **501** during the manufacturing procedures is able to prevent the offset between the second opening **601** and first opening **501**.

[0028] Furthermore, the color resist layer **204** includes a plurality of color resists where two adjacent color resists therebetween form the second opening **601**. In one embodi-

ment, the color resists includes a color R resist, a color G resist, a color B resist and a color W resist. For example, the second opening 601 is disposed between the color R resist and color G resist.

[0029] The pixel electrode layer 205 is disposed on the color resist layer 204 and formed by electrically connecting the first opening 501 and second opening 601 to the drain electrode region 402 of thin film transistor 202 where the pixel electrode layer 205 is composed of indium-tin oxide. The pixel electrode layer 205 covers the color resist layer 204 and covers the first passivation layer 203, which is exposed from the second opening 601, and the drain electrode region 402, which is exposed from the first opening 501.

[0030] The second passivation layer 206 is disposed on the pixel electrode layer 205 and covers the pixel electrode layer 205 in the second opening 601. Therefore, if the second passivation layer 206 is disposed on the pixel electrode layer 205 for electrically connecting the pixel electrode layer 205 to the drain electrode region 402, there is no need to form openings in the second passivation layer 206 to maintain the integrity of the second passivation layer 206. The integrity of the second passivation layer 206 is capable of protecting the color resist layer to avoid the bubble in the second opening 601.

[0031] FIG. 3 is a schematic structural view of an LCD panel according to one embodiment of the present invention. The LCD panel includes an array substrate 200 and a glass substrate 300 opposite the array substrate 200 where a liquid crystal 400 is filled into the array substrate 200 and glass substrate 300 therebetween. In FIG. 2, the array substrate 200 includes a bottom substrate 201, a thin film transistor 202, a first passivation layer 203, a color resist layer 204, a pixel electrode layer 205 and a second passivation layer 206 where the array substrate 200 is similar to or the same as the array substrate in the above-mentioned descriptions.

[0032] As is understood by a person skilled in the art, the foregoing preferred embodiments of the present invention are illustrative rather than limiting of the present invention. It is intended that they cover various modifications and similar arrangements be included within the spirit and scope of the present invention, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure.

What is claimed is:

1. An array substrate, comprising:

a bottom substrate;

a thin film transistor disposed on the bottom substrate, the thin film transistor comprising:

a first metal layer disposed on the bottom substrate and configured to form a plurality of scan lines and a gate electrode region of a thin film field-effect transistor;

a first insulation layer disposed on the first metal layer;

a semiconductor layer disposed on the first insulation layer and configured to form a channel region of the thin film field-effect transistor; and

a second metal layer disposed on the semiconductor layer and configured to form a source electrode region and a drain electrode region of the thin film field-effect transistor and form a plurality of data lines;

a first passivation layer disposed on the thin film transistor and comprising a first opening which exposes the drain electrode region of the thin film transistor;

a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer comprises a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor, a hole diameter of the second opening is greater than a hole diameter of the first opening, and the color resist layer comprises a plurality of color resists wherein two adjacent color resists therebetween form the second opening;

a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and

a second passivation layer disposed on the pixel electrode layer.

2. The array substrate of claim 1, wherein the color resists comprises a color R resist, a color G resist and a color B resist.

3. An array substrate, comprising:

a bottom substrate;

a thin film transistor disposed on the bottom substrate;

a first passivation layer disposed on the thin film transistor and comprising a first opening which exposes the drain electrode region of the thin film transistor;

a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer comprises a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor;

a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and

a second passivation layer disposed on the pixel electrode layer.

4. The array substrate of claim 3, wherein the thin film transistor comprises:

a first metal layer disposed on the bottom substrate and configured to form a plurality of scan lines and a gate electrode region of a thin film field-effect transistor;

a first insulation layer disposed on the first metal layer;

a semiconductor layer disposed on the first insulation layer and configured to form a channel region of the thin film field-effect transistor; and

a second metal layer disposed on the semiconductor layer and configured to form a source electrode region and a drain electrode region of the thin film field-effect transistor and form a plurality of data lines.

5. The array substrate of claim 3, wherein a hole diameter of the second opening is greater than a hole diameter of the first opening.

6. The array substrate of claim 3, wherein the color resist layer comprises a plurality of color resists and two adjacent color resists therebetween form the second opening.

7. The array substrate of claim 3, wherein the color resists comprises a color R resist, a color G resist and a color B resist.

8. A liquid crystal display panel comprising an array substrate and a glass substrate opposite the array substrate wherein a liquid crystal is filled into the array substrate and glass substrate therebetween, the array substrate comprising:

a bottom substrate;

a thin film transistor disposed on the bottom substrate;

a first passivation layer disposed on the thin film transistor and comprising a first opening which exposes the drain electrode region of the thin film transistor;

a color resist layer disposed on the first passivation layer and configured to form a color filter, wherein the color resist layer comprises a second opening corresponding to the first opening to expose the drain electrode region of the thin film transistor;

a pixel electrode layer disposed on the color resist layer and formed by electrically connecting the first opening and the second opening to the drain electrode region of the thin film transistor; and

a second passivation layer disposed on the pixel electrode layer.

9. The liquid crystal display panel of claim **8**, wherein the thin film transistor comprises:

a first metal layer disposed on the bottom substrate and configured to form a plurality of scan lines and a gate electrode region of a thin film field-effect transistor;

a first insulation layer disposed on the first metal layer; a semiconductor layer disposed on the first insulation layer and configured to form a channel region of the thin film field-effect transistor; and

a second metal layer disposed on the semiconductor layer and configured to form a source electrode region and a drain electrode region of the thin film field-effect transistor and form a plurality of data lines.

10. The liquid crystal display panel of claim **8**, wherein a hole diameter of the second opening is greater than a hole diameter of the first opening.

11. The liquid crystal display panel of claim **8**, wherein the color resist layer comprises a plurality of color resists and two adjacent color resists therebetween form the second opening.

12. The liquid crystal display panel of claim **8**, wherein the color resists comprises a color R resist, a color G resist and a color B resist.

* * * * *

专利名称(译)	阵列基板和液晶显示板		
公开(公告)号	US20180164634A1	公开(公告)日	2018-06-14
申请号	US15/305187	申请日	2016-06-03
[标]申请(专利权)人(译)	深圳市华星光电技术有限公司		
申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
当前申请(专利权)人(译)	深圳市中国星光电科技有限公司.		
[标]发明人	DENG ZHUMING		
发明人	DENG, ZHUMING		
IPC分类号	G02F1/1335 G02F1/1343 G02F1/1362		
CPC分类号	G02F1/133514 G02F1/1343 G02F1/136286 G02F2001/1635 G02F1/1362 G02F1/136227 G02F2001/136222		
优先权	201610224791.5 2016-04-12 CN		
外部链接	Espacenet USPTO		

摘要(译)

描述阵列基板及其液晶显示器 (LCD) 面板。阵列基板包括底部基板;设置在底部基板上的薄膜晶体管;第一钝化层, 所述第一钝化层设置在所述薄膜晶体管上并且包括暴露所述薄膜晶体管的所述漏电极区域的第一开口;设置在所述第一钝化层上并配置为形成滤色器的彩色抗蚀剂层, 其中所述彩色抗蚀剂层包括与所述第一开口相对应的第二开口以暴露所述薄膜晶体管的漏极区域;像素电极层, 设置在所述色阻层上, 并通过将所述第一开口和所述第二开口电连接到所述薄膜晶体管的所述漏电极区域而形成;以及设置在像素电极层上的第二钝化层。

