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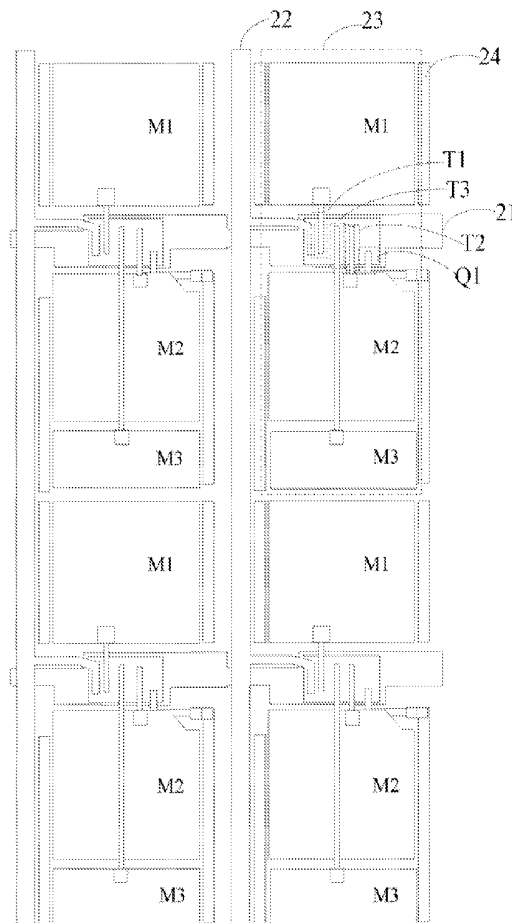
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(57)

ABSTRACT

An array substrate and a liquid crystal panel are disclosed. Each of the pixel cells of the array substrate includes at least two pixel electrodes and at least two switch circuits. The first pixel electrode connects to the corresponding scanning line and corresponding data line of the pixel cell via the first switch circuit. The second pixel electrode connects to the corresponding scanning line of the pixel cell via the second switch circuit. The second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode is connected to the corresponding data line of the pixel cell. In this way, the color distortion in wide viewing angle and the display performance are enhanced.



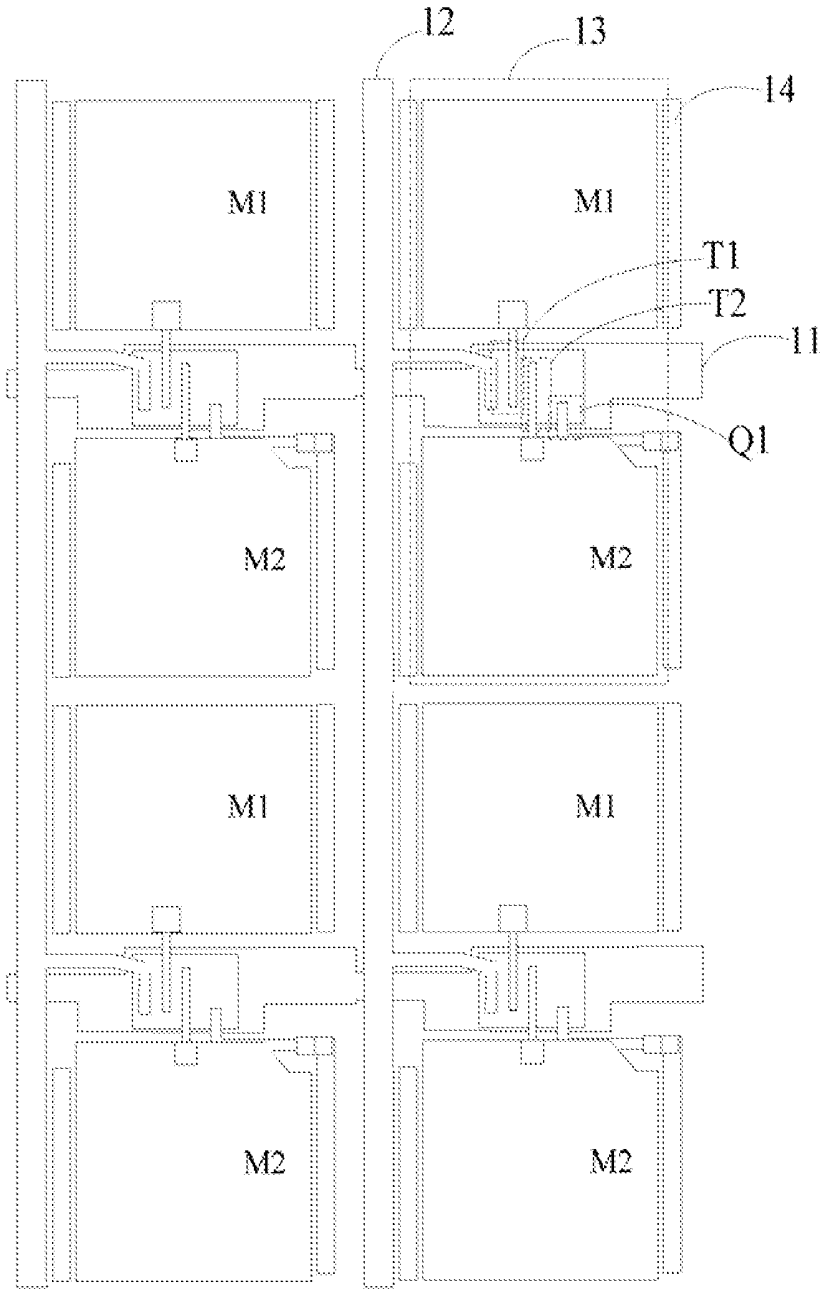


FIG. 1

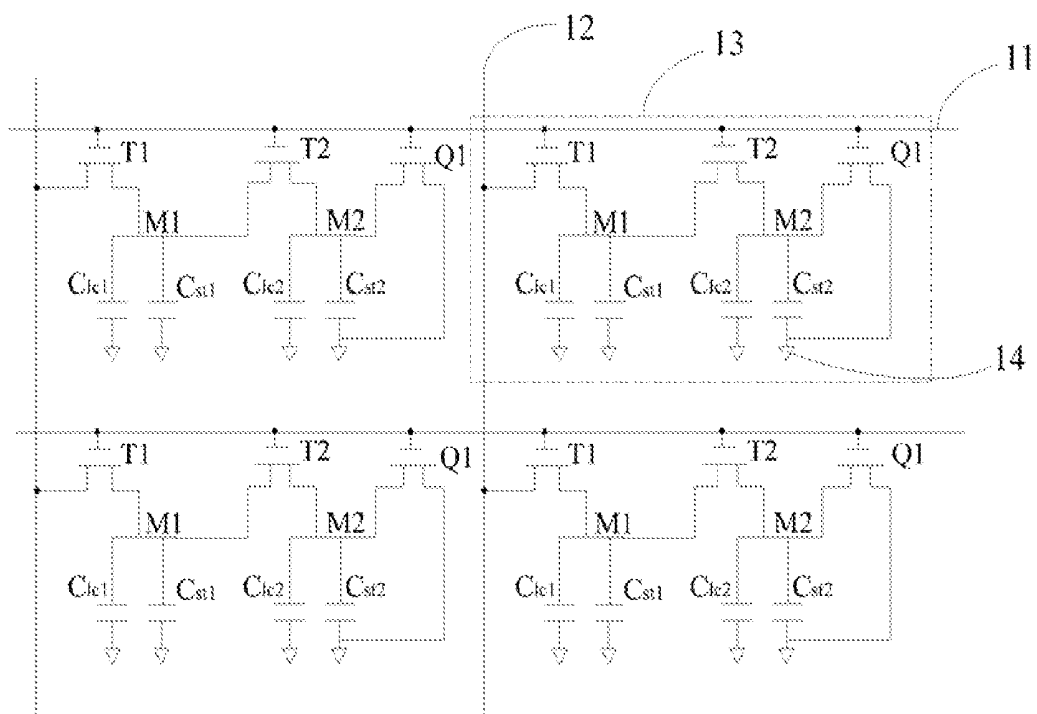


FIG. 2

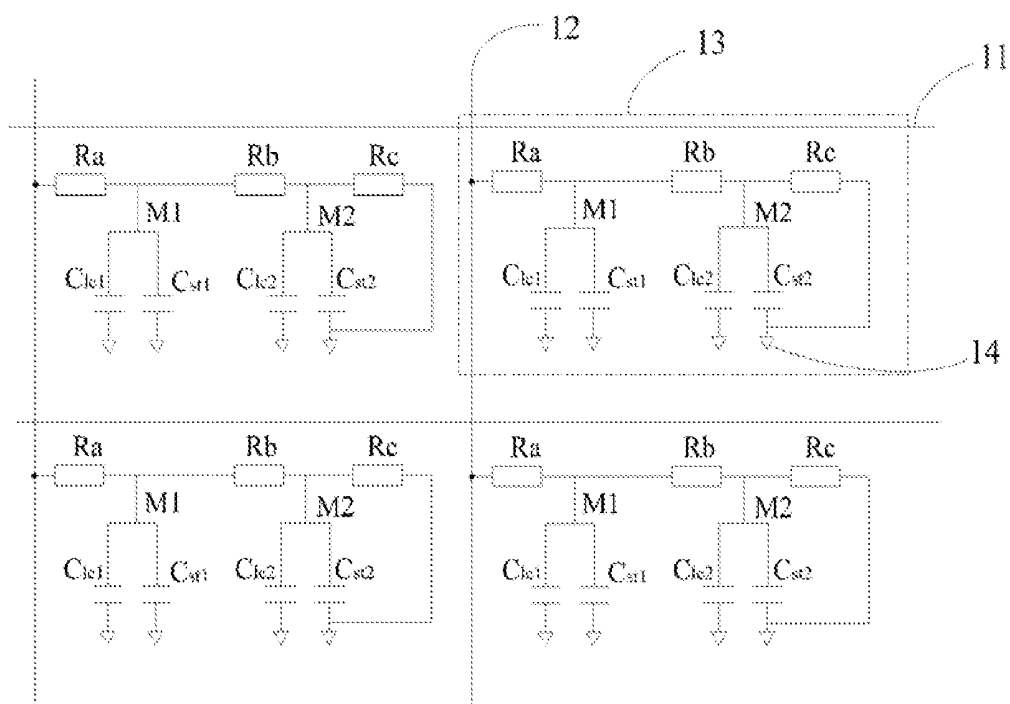


FIG. 3

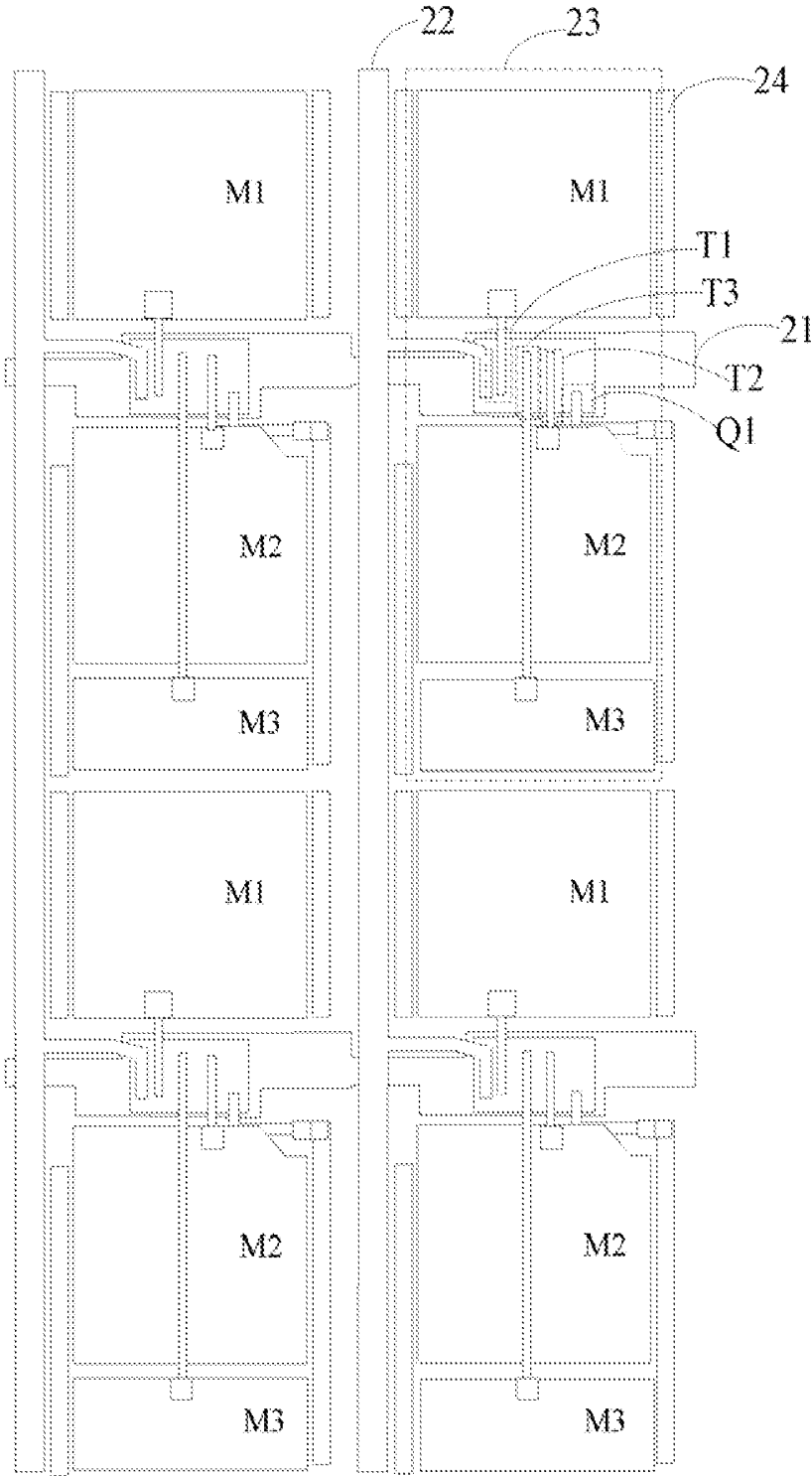


FIG. 4

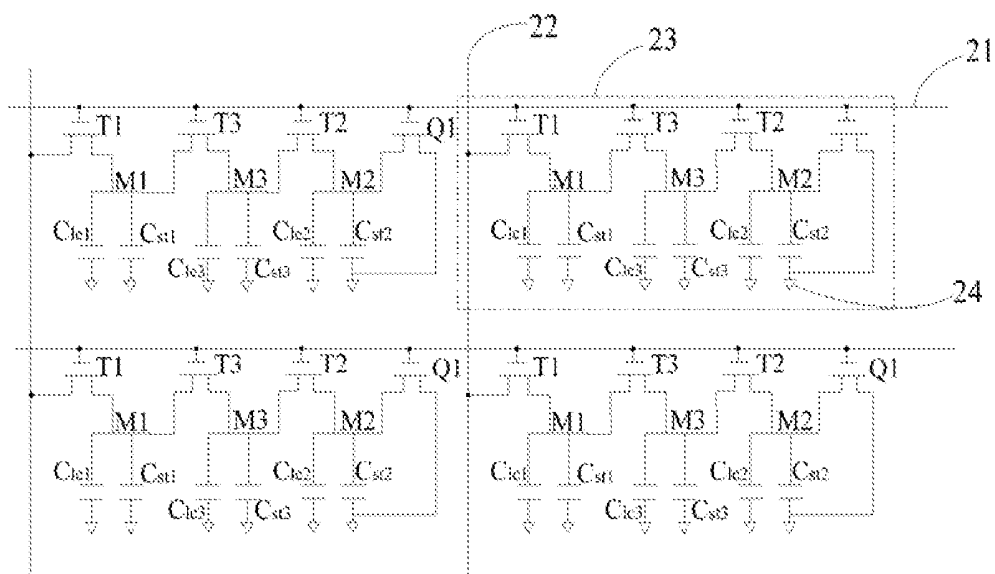


FIG. 5

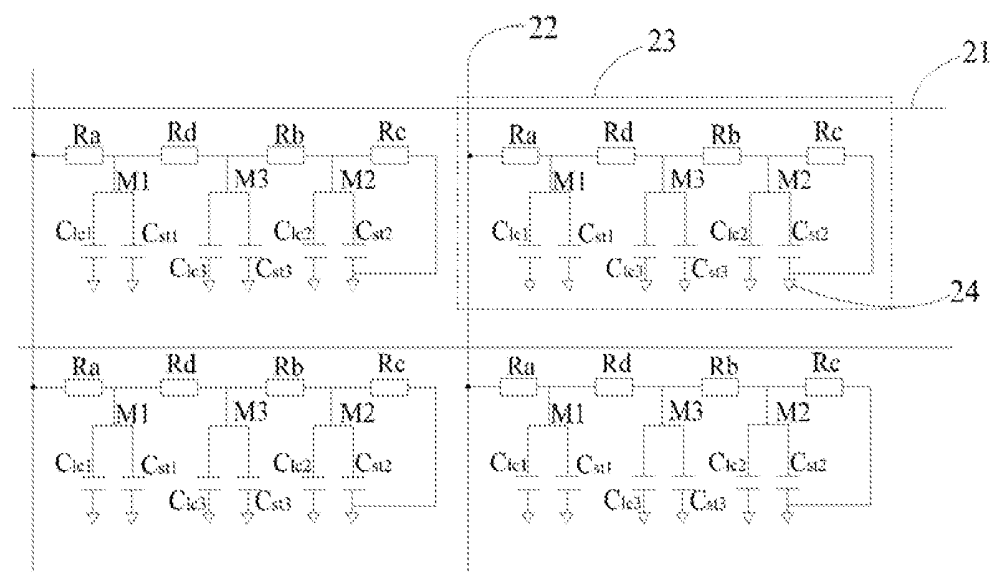


FIG. 6

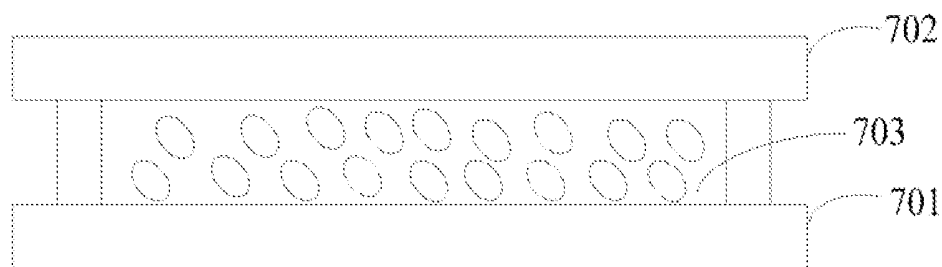


FIG. 7

ARRAY SUBSTRATE AND THE LIQUID CRYSTAL PANEL

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present disclosure relates to display technology, and more particularly to an array substrate and a liquid crystal panel.

[0003] 2. Discussion of the Related Art

[0004] Vertical Alignment (VA) LCDs are characterized by attributes including quick response time and high contrast, and thus have become a current trend of LCD.

[0005] However, the alignments of liquid crystal are different and thus the reflective rates of the liquid crystal are not the same, which results in intensity change of the incident light beams. In other words, the transmission capability is decreased when the angle of the squint is large. The color observed at the right viewing angle is different from that observed at the squinted viewing angle such that the color distortion occurs in wide viewing angle.

SUMMARY

[0006] The object of the invention is to provide an array substrate and a liquid crystal panel to reduce the color difference in wide viewing angle so as to enhance the display performance.

[0007] in one aspect, an array substrate includes: a plurality of scanning lines, a plurality of data lines, a plurality of pixel cells, and a common electrode for inputting a common voltage, and each of the pixel cells corresponds to one scanning line and one data line; each of the pixel cells includes two pixel electrodes and two switch circuits, the two pixel electrodes include a first pixel electrode and a second pixel electrode, the two switch circuits include a first switch circuit operating on the first pixel electrode and a second switch circuit operating on the second pixel electrode, each of the pixel cells further includes a controlled transistor having a control end, a first end, and a second end, the first pixel electrode connects to the corresponding scanning line and data line of the pixel cell via the first switch circuit, the second pixel electrode connects to the corresponding data line of the pixel cell via the second switch circuit, and the second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode connects to the corresponding data line of the pixel cell, the control end of the controlled transistor connects to the corresponding scanning line of the pixel cell, the first end of the controlled transistor connects to the second pixel electrode, and the second end of the controlled transistor connects to the common electrode; and wherein when the corresponding scanning line of the pixel cell inputs the scanning signals to turn on the first switch circuit, the second switch circuit and the controlled transistor, the first pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit, the second pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit and the second switch circuit in turn, the voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit, and a current amount of the first switch circuit is different from that of the second switch circuit when the switch circuits are turn on so as to obtain different voltage

difference between the first pixel electrode and the second pixel electrode, the controlled transistor is a discharging thin film transistor (TFT), a control end of the controlled transistor corresponds to a gate of the discharging TFT, a first end of the controlled transistor corresponds to a source of the discharging TFT, and a second end of the controlled transistor corresponds to a drain of the discharging TFT, the discharging TFT changes the voltage of the second pixel electrode when the discharging TFT is turn on, a width/length ratio of the discharging TFT is smaller than a predetermined value such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero when the discharging TFT is turn on.

[0008] Wherein the first switch circuit is a first TFT, the second switch circuit is a second TFT, the width/length ratio of the first TFT is different from that of the second TET such that the current amount of the first TFT is different from that of the second TFT when the TFTs are turn on.

[0009] Wherein each of the pixel cells further includes a third pixel electrode and a third switch circuit, the third pixel electrode connects to the corresponding scanning line of the pixel cell via the third switch circuit, and the third pixel electrode connects to the first switch circuit via the third switch circuit such that the third pixel electrode connects to the corresponding data line of the pixel cell.

[0010] in another aspect, an array substrate includes: a plurality of scanning lines, a plurality of data lines, a plurality of pixel cells, and a common electrode for inputting a common voltage, and each of the pixel cells corresponds to one scanning line and one data line; each of the pixel cells includes two pixel electrodes and two switch circuits, the two pixel electrodes include a first pixel electrode and a second pixel electrode, the two switch circuits include a first switch circuit operating on the first pixel electrode and a second switch circuit operating on the second pixel electrode, each of the pixel cells further includes a controlled transistor having a control end, a first end, and a second end, the first pixel electrode connects to the corresponding scanning line and data line of the pixel cell via the first switch circuit, the second pixel electrode connects to the corresponding data line of the pixel cell via the second switch circuit, and the second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode connects to the corresponding data line of the pixel cell, the control end of the controlled transistor connects to the corresponding scanning line of the pixel cell, the first end of the controlled transistor connects to the second pixel electrode, and the second end of the controlled transistor connects to the common electrode; and wherein when the corresponding scanning line of the pixel cell inputs the scanning signals to turn on the first switch circuit, the second switch circuit and the controlled transistor, the first pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit, the second pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit and the second switch circuit in turn, the voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit, and the controlled transistor changes the voltage of the second pixel electrode when the controlled transistor is turn on such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero.

[0011] Wherein the current amount of the first switch circuit is different from that of the second switch circuit when the switch circuits are turn on so as to obtain different voltage difference between the first pixel electrode and the second pixel electrode.

[0012] Wherein the first switch circuit is a first TFT, the second switch circuit is a second TFT, the width/length ratio of the first TFT is different from that of the second TFT such that the current amount of the first TFT is different from that of the second TFT when the TFTs are turn on.

[0013] Wherein each of the pixel cells further includes a third pixel electrode and a third switch circuit, the third pixel electrode connects to the corresponding scanning line of the pixel cell via the third switch circuit, and the third pixel electrode connects to the first switch circuit via the third switch circuit such that the third pixel electrode connects to the corresponding data line of the pixel cell; and the second pixel electrode connects to the first switch circuit via the second switch circuit and the third switch circuit in turn such that the second pixel electrode connects to the corresponding data line of the pixel cell.

[0014] Wherein the controlled transistor is a discharging TFT, a control end of the controlled transistor corresponds to a gate of the discharging TFT, a first end of the controlled transistor corresponds to a source of the discharging TFT, and a second end of the controlled transistor corresponds to a drain of the discharging TFT, and a width/length ratio of the discharging TFT is smaller than a predetermined value such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero when the discharging TFT is turn on.

[0015] in another aspect, a display panel includes: an array substrate, a color filtering substrate and a liquid crystal layer between the array substrate and the color filtering substrate; and the array substrate includes: a plurality of scanning lines, a plurality of data lines, a plurality of pixel cells, and a common electrode for inputting a common voltage, and each of the pixel cells corresponds to one scanning line and one data line; each of the pixel cells includes two pixel electrodes and two switch circuits, the two pixel electrode include a first pixel electrode and a second pixel electrode, the two switch circuits include a first switch circuit operating on the first pixel electrode and a second switch circuit operating on the second pixel electrode, each of the pixel cells further includes a controlled transistor having a control end, a first end, and a second end, the first pixel electrode connects to the corresponding scanning line and data line of the pixel cell is the first switch circuit, the second pixel electrode connects to the corresponding data line of the pixel cell via the second switch circuit, and the second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode connects to the corresponding data line of the pixel cell, the control end of the controlled transistor connects to the corresponding scanning line of the pixel cell, the first end of the controlled transistor connects to the second pixel electrode, and the second end of the controlled transistor connects to the common electrode; and wherein when the corresponding scanning line of the pixel cell inputs the scanning signals to turn on the first switch circuit, the second switch circuit and the controlled transistor, the first pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit, the second pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch

circuit and the second switch circuit in turn, the voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit, and the controlled transistor changes the voltage of the second pixel electrode when the controlled transistor is turn on such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero.

[0016] Wherein the current amount of the first switch circuit is different from that of the second switch circuit when the switch circuits are turn on so as to obtain different voltage difference between the first pixel electrode and the second pixel electrode.

[0017] Wherein the first switch circuit is a first TFT, the second switch circuit is a second TFT the width/length ratio of the first TFT is different from that of the second TFT such that the current amount of the first TFT is different from that of the second TFT when the TFTs are turn on.

[0018] Wherein each of the pixel cells further includes a third pixel electrode and a third switch circuit, the third pixel electrode connects to the corresponding scanning line of the pixel cell via the third switch circuit, and the third pixel electrode connects to the first switch circuit via the third switch circuit such that the third pixel electrode connects to the corresponding data line of the pixel cell; and the second pixel electrode connects to the first switch circuit via the second switch circuit and the third switch circuit in turn such that the second pixel electrode connects to the corresponding data line of the pixel cell.

[0019] Wherein the controlled transistor is a discharging TFT, a control end of the controlled transistor corresponds to a gate of the discharging TFT, a first end of the controlled transistor corresponds to a source of the discharging TFT, and a second end of the controlled transistor corresponds to a drain of the discharging TFT, and a width/length ratio of the discharging TFT is smaller than a predetermined value such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero when the discharging TFT is turn on.

[0020] In view of the above, each of the pixel cells of the array substrate includes at least two pixel electrodes and at least two switch circuits. The first pixel electrode connects to the corresponding scanning line and corresponding data line of the pixel cell via the first switch circuit. The second pixel electrode connects to the corresponding scanning line of the pixel cell via the second switch circuit. The second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode is connected to the corresponding data line of the pixel cell. The voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit. In this way, the color distortion in wide viewing angle and the display performance are enhanced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] FIG. 1 is a schematic view of the array substrate in accordance with one embodiment.

[0022] FIG. 2 is an equivalent-circuit diagram of the pixel cell of FIG. 1.

[0023] FIG. 3 is an equivalent-circuit diagram of the pixel cell of FIG. 2 when the switch circuit and the controlled transistor are turn on.

[0024] FIG. 4 is a schematic view of the array substrate in accordance with another embodiment.

[0025] FIG. 5 is an equivalent-circuit diagram of the pixel cell in accordance with another embodiment.

[0026] FIG. 6 is an equivalent-circuit diagram of the pixel cell of FIG. 5 when the switch circuit and the controlled transistor are turn on.

[0027] FIG. 7 is a schematic view of the liquid crystal panel in accordance with one embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0028] Embodiments of the invention will now be described, more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown.

[0029] in order to reduce the color distortion in wide viewing angle, one pixel is divided into a plurality of pixel areas. By applying different voltage to the pixel areas, the alignment of the liquid crystal in two areas are different, which reduces the color distortion in wide viewing angle. Thus, the low color shift (LCS) effect is achieved.

[0030] Referring to FIGS. 1 and 2, the array substrate includes a plurality of scanning lines 11 a plurality of data lines 12, a plurality of pixel cells 13, and a common electrode 14 for inputting a common voltage.

[0031] Each of the pixel cells 13 includes two pixel electrode and two switch circuits. The two pixel electrode are the first pixel electrode M1 and the second pixel electrode M2. The two switch circuits are implemented by thin film transistors (TFTs) including a first TFT T1 operating on the first pixel electrode M1 and a second TFT T2 operating on the second pixel electrode M2. Each of the first TFT T1 and the second TFT T2 include a control end, an input end, and an output end. The gate of the first TFT T1 and the second TFT T2 electrically connect to the corresponding scanning line 11 of the pixel cell 13. The source of the first TFT T1 electrically connects to the corresponding data line 12 of the pixel cell 13. The drain of the first TFT T1 electrically connects to the first pixel electrode M1. The source of the second TFT T2 electrically connects to the drain of the first TFT T1. The drain of the second TFT T2 electrically connects to the second pixel electrode M2 such that the second pixel electrode M2 connects to the first TFT T1 via the second TFT T2. Thus, the second pixel electrode M2 connects to the corresponding data line 12 of the pixel cell 13.

[0032] The pixel cell 13 further includes a controlled transistor Q1. The controlled transistor Q1 includes a control end, a first end, and a second end. The control end of the controlled transistor Q1 electrically connects to the corresponding scanning line 11 of the pixel cell 13. The first end of the controlled transistor Q1 electrically connects to the second pixel electrode M2. The second end of the controlled transistor Q1 electrically connects to the common electrode 14. The controlled transistor Q1 is a discharging TFT. The control end of the controlled transistor Q1 corresponds to the gate of the discharging TFT. The first end of the controlled transistor Q1 corresponds to the source of the discharging TFT. The second end of the controlled transistor Q1 corresponds to the drain of the discharging TFT.

[0033] In other embodiments, the first switch circuit, the second switch circuit, the controlled transistor may be, but not limited to triode or Darlington transistor.

[0034] When the pixel cell 13 is driven, the common electrode 14 inputs the common voltage. The scanning line 11 inputs scanning signals to turn on the first TFT T1, the second TFT T2 and the controlled transistor Q1. The data line 12 inputs data signals. The data signals are input to the first pixel electrode M1 via the first TFT T1, and then input to the second pixel electrode M2 via the first TFT T1 and the second TFT T2 in turn. As such, the first pixel electrode M1 receives the data signals from the data line 12 via the first TFT T1, and the second pixel electrode M2 receives the data signals from the data line 12 via the first TFT T1 and the second TFT T2 in turn. The voltage of the first pixel electrode M1 is different from that of the second pixel electrode M2 due to the operations of the first TFT T1 and the second TFT T2. Referring to FIG. 3, when the TFT is turn on, the TFT is equivalent to a resistor having a certain resistance. The value of the resistance is positively dependent from a width/length ratio of the TFT. When the width/length ratio is greater, the value of the equivalent resistance is smaller when the TFT is turn on, and vice versa. The first TFT T1 is equivalent to the resistor Ra when being turned on. The second TFT T2 is equivalent to the resistor Rb when being turn on. The controlled transistor Q1 is equivalent to the resistor Rc when being turn on. When the scanning line 11 inputs the scanning signals, the resistor Ra, the resistor Rb, and the resistor Rc are serially connected. The data signals from the data line 12 are input to the first pixel electrode M1 via the resistor Ra, and are input to the second pixel electrode M2 via the resistor Ra and the resistor Rb in turn. The voltage Vs represents the voltage input from the data line 12. Basing on the voltage-division principle, the voltage of the first pixel electrode M1 is calculated by the equation of:

$$V1 = Vs * (Rb + Rc) / (Ra + Rb + Rc) \quad (1)$$

[0035] The voltage of the second pixel electrode M2 is calculated by the equation of:

$$V2 = Vs * Rc / (Ra + Rb + Rc) \quad (2)$$

[0036] it can be understood that the voltage of the second pixel electrode M2 is smaller than the voltage of the first pixel electrode M1 such that the voltage difference between the first pixel electrode M1 and the second pixel electrode M2 equals to a certain value. The voltage difference is not equal to zero and thus the color distortion in wide viewing angle can be enhanced.

[0037] In the embodiment, the first TFT T1 is similar to the second TFT T2, that is, the width/length ratio of the first TFT T1 and the second TFT T2 are the same. As such, the resistance of the resistor Ra and the resistor Rb is equivalent when the first TFT T1 and the second TFT T2 are turn on. In this way, the current amount of the first TFT T1 and the second TFT T2 when being turn on are also the same. Basing on the voltage-division principle, the voltage of the first pixel electrode M1 can be different from that of the second pixel electrode M2 under the circumstance that the values of the equivalent resistors are the same. Thus, the color distortion in side viewing angle is enhanced.

[0038] in addition, the voltage of the second pixel electrode M2 is changed when the controlled transistor Q1 is turn on such that the voltage difference between the second pixel electrode M2 and the common electrode 14 is decreased and is not equal to zero. Specifically, when the positive polarity is inverse (the data signals is larger than the common voltage), the scanning line 11 inputs the scanning signals to turn on the controlled transistor Q1. A portion. of the charges of the second pixel electrode M2 is transferred to the common elec-

trode **14** such that the voltage of the second pixel electrode **M2** is decreased. Thus, the voltage of the second pixel electrode **M2** is different from that of the first pixel electrode **M1**. In addition, the voltage difference between the second pixel electrode **M2** and the common electrode **14** is decreased so as to reduce the color distortion in wide viewing angle. When the negative polarity is inverse (the data signals is smaller than the common voltage), the second pixel electrode **M2** is charged by the common electrode **14** so as to increase the voltage of the second pixel electrode **M2**. The increased amount of the voltage of the second pixel electrode **M2** is not equal to the voltage difference between the second pixel electrode **M2** and the first pixel electrode **M1** due to the operations of the controlled transistor **Q1**. As such, the voltage difference between the first pixel electrode **M1** and the second pixel electrode **M2** equals to a certain value. In addition, when the voltage of the second pixel electrode **M2** is increased, the voltage difference between the second pixel electrode **M2** and the common electrode **14** is decreased, which further reduces the color distortion in wide viewing angle. Furthermore, the voltage difference between the second pixel electrode **M2** and the common electrode **14** is not equal to zero when the controlled transistor **Q1** is turn on so as to ensure that the second pixel electrode **M2** can be in a normally displaying state. Thus, regardless of the positive polarity or the negative polarity is inverse, the voltage of the second pixel electrode **M2** is changed when the controlled transistor **Q1** is turn on such that the voltage difference between the second pixel electrode **M2** and the common electrode **14** is decreased and is not equal to zero. In the embodiment, the controlled transistor **Q1** is the TFT and the width/length ratio of the controlled transistor **Q1** is smaller than a predetermined value, which results in a smaller current amount when the controlled transistor **Q1** is turn on. Further, the charge transferring speed between the second pixel electrode **M2** and the common electrode **14** is slower so as to keep the second pixel electrode **M2** and the common electrode **14** from transiting to a charges balance state when the controlled transistor **Q1** is turn on. The voltage difference between the second pixel electrode **M2** and the common electrode **14** equals to the certain value. BY controlling the charge transferring speed between the second pixel electrode **M2** and the common electrode **14**, the voltage of the first pixel electrode **M1** is different from that of the second pixel electrode **M2** when the negative polarity is inverse.

[0039] In other embodiments, the width/length ratio of the first TFT **T1** and the second TFT **T2** are different such that the current amount of the first TFT **T1** and the second TFT **T2** are different. As such, the voltage difference between the first pixel electrode and the second pixel electrode are different. For example, when the width/length ratio of the first TFT **T1** is larger than that of the second TFT **T2**, the voltage difference between the first pixel electrode and the second pixel electrode is enlarged, which provides a better display performance. In another example, the width/length ratio of the first TFT **T1** is smaller than that of the second TFT **T2**.

[0040] By configuring the width/length ratio of the first TFT **T1** and the second TFT **T2**, the values of the equivalent resistance are changed when the first TFT **T1** and the second TFT **T2** are turn on. Thus, the voltage difference between the first pixel electrode and the second pixel electrode is obtained to achieve different LCS effects.

[0041] In other embodiments, the voltage difference between the first pixel electrode and the second pixel electrode is changed without configuring the width/length ratio of

the TFTs. The first switch circuit is implemented by only the first TFT and the second switch circuit is implemented by the second TFT and a divider resistor such that the current amount of the first switch circuit and the second circuit are not the same when being turn on. As such, different voltage difference between the first pixel electrode and the second pixel electrode can be obtained. Specifically, the first pixel electrode connects to the corresponding data line of the pixel cell via the first TFT. The second pixel electrode connects to the first TFT via the second TFT and the divider resistor in turn such that the second pixel electrode connects to the corresponding data line of the pixel cell. The width/length ratio of the first TFT and the second TFT are the same. By configuring the resistance of the divider resistor, the current amount of the second switch circuit is adjusted such that the current amount of the first switch circuit and the second switch circuit are different when the first switch circuit and the second switch circuit are turn on. In this way, the voltage difference between the first pixel electrode and the second pixel electrode are different so as to achieve different LCS effect. In other embodiments, different voltage are applied to the first pixel electrode and the second pixel electrode. The first switch circuit include one or a plurality of divider resistors. The second switch circuit may include a plurality of divider resistors such that the voltage of the first pixel electrode is different from that of the second pixel electrode.

[0042] FIGS. 4 and 5 show the array substrate in accordance with another embodiment. The pixel cell **23** further includes a third pixel electrode **M3** and a third switch circuit. The third switch circuit is a third TFT **T3**. The third pixel electrode **M3** connects to the corresponding scanning line **21** of the pixel cell **23** via the third TFT **T3**. The third pixel electrode **M3** connects to the first TFT **T1** via the third TFT **T3** such that the third pixel electrode **M3** connects to the corresponding data line **22** of the pixel cell. The second pixel electrode **M2** connects to the first TFT **T1** via the first TFT **T1** and the second TFT **T2** in turn such that the second pixel electrode **M2** connects to the corresponding data line **22** of the pixel cell **23**. Specifically, the gate of the first TFT **T1**, the second TFT **T2**, and the third TFT **T3** connect to the corresponding scanning line **21** of the pixel cell **23**. The source of the first TFT **T1** connects to the corresponding data line **22** of the pixel cell **23**. The drain of the first TFT **T1** connects to the first pixel electrode **M1**. The source of the third TFT **T3** connects to the drain of the first TFT **T1**. The drain of the third TFT **T3** connects to the third pixel electrode **M3**. The source of the second TFT **T2** connects to the drain of the third TFT **T3**. The drain of the second TFT **T2** connects to second pixel electrode **M2**.

[0043] When the scanning line **21** inputs the scanning signals to turn on the first TFT **T1**, the second TFT **T2**, the third TFT **T3** and the controlled transistor **Q1**, the data line **22** inputs the data signals. The first pixel electrode **M1** receives the data signals via the first TFT **T1**. The third pixel electrode **M3** receives the data signals via the first TFT **T1** and the third TFT **T3** in turn. The second pixel electrode **M2** receives the data signals via the first TFT **T1**, the second TFT **T2**, and the third TFT **T3** in turn. Referring to FIG. 6, the first TFT **T1**, the second TFT **T2**, the third TFT **T3**, and the controlled transistor **Q1** are respectively equivalent to the resistor R_a , R_b , R_d , and R_c . The voltage V_s represents the voltage input from the data line **23**. The voltage of the first pixel electrode **M1** is calculated by the equation of:

$$V_1 = V_s * (R_d + R_b + R_c) / (R_a + R_b + R_d + R_c) \quad (3)$$

[0044] The voltage of the third pixel electrode M3 is calculated by the equation of:

$$V3 = V_s * (Rb + Rc) / (Ra + Rb + Rd + Rc) \quad (4)$$

[0045] The voltage of the second pixel electrode M2 is calculated by the equation of:

$$V2 = V_s * Rc / (Ra + Rb + Rc) \quad (5)$$

[0046] It can be understood that the voltage of the third pixel electrode M3 is smaller than that of the first pixel electrode M1. The voltage of the second pixel electrode M2 is smaller than that of the third pixel electrode M3. As such, the voltage difference between the first pixel electrode M1, the second pixel electrode M2, and the third pixel electrode M3 equals to one certain value and thus the color distortion in wide viewing angle is enhanced. By configuring the width/length ratio of the first TFT T1, the second TFT T2 and the third TFT T3, the resistance is adjusted when the first TFT T1, the second TFT T2, and the third TFT T3 are turn on. In this way, the voltage of the first pixel electrode M1, the second pixel electrode M2, and the third pixel electrode M3 are adjusted so as to obtain different voltage difference and to achieve different LCS effect.

[0047] In other embodiments, each of the pixel cells includes four or five pixel electrodes, which can be implemented by the above method.

[0048] FIG. 7 is a schematic view of the liquid crystal display in accordance with one embodiment. The liquid crystal panel includes the array substrate 701, a color filtering substrate 702, and a liquid crystal layer 703. The array substrate 701 may be the array substrate in the above embodiments.

[0049] It is believed that the present embodiments and their advantages will be understood from the foregoing description, and it will be apparent that various changes may be made thereto without departing from the spirit and scope of the invention or sacrificing all of its material advantages, the examples hereinbefore described merely being preferred or exemplary embodiments of the invention.

What is claimed is:

1. An array substrate, comprising:

a plurality of scanning lines, a plurality of data lines, a plurality of pixel cells, and a common electrode for inputting a common voltage, and each of the pixel cells corresponds to one scanning line and one data line;

each of the pixel cells includes two pixel electrodes and two switch circuits, the two pixel electrode include a first pixel electrode and a second pixel electrode, the two switch circuits include a first switch circuit operating on the first pixel electrode and a second switch circuit operating on the second pixel electrode, each of the pixel cells further includes a controlled transistor having a control end, a first end, and a second end, the first pixel electrode connects to the corresponding scanning line and data line of the pixel cell via the first switch circuit, the second pixel electrode connects to the corresponding data line of the pixel cell via the second switch circuit, and the second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode connects to the corresponding data line of the pixel cell, the control end of the controlled transistor connects to the corresponding scanning line of the pixel cell, the first end of the controlled

transistor connects to the second pixel electrode, and the second end of the controlled transistor connects to the common electrode; and

wherein when the corresponding scanning line of the pixel cell inputs the scanning signals to turn on the first switch circuit, the second switch circuit and the controlled transistor, the first pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit, the second pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit and the second switch circuit in turn, the voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit, and a current amount of the first switch circuit is different from that of the second switch circuit when the switch circuits are turn on so as to obtain different voltage difference between the first pixel electrode and the second pixel electrode, the controlled transistor is a discharging thin film transistor (TFT), a control end of the controlled transistor corresponds to a gate of the discharging TFT, a first end of the controlled transistor corresponds to a source of the discharging TFT and a second end of the controlled transistor corresponds to a drain of the discharging TFT, the discharging TFT changes the voltage of the second pixel electrode when the discharging TFT is turn on, a width/length ratio of the discharging TFT is smaller than a predetermined value such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero when the discharging TFT is turn on.

2. The array substrate as claimed in claim 1, wherein the first switch circuit is a first TFT, the second switch circuit is a second TFT, the width/length ratio of the first TFT is different from that of the second TFT such that the current amount of the first TFT is different from that of the second TFT when the TFTs are turn on.

3. The array substrate as claimed in claim 1, wherein each of the pixel cells further includes a third pixel electrode and a third switch circuit, the third pixel electrode connects to the corresponding scanning line of the pixel cell via the third switch circuit, and the third pixel electrode connects to the first switch circuit via the third switch circuit such that the third pixel electrode connects to the corresponding data line of the pixel cell.

4. An array substrate, comprising:

a plurality of scanning lines, a plurality of data lines, a plurality of pixel cells, and a common electrode for inputting a common voltage, and each of the pixel cells corresponds to one scanning line and one data line;

each of the pixel cells includes two pixel electrodes and two switch circuits, the two pixel electrode include a first pixel electrode and a second pixel electrode, the two switch circuits include a first switch circuit operating on the first pixel electrode and a second switch circuit operating on the second pixel electrode, each of the pixel cells further includes a controlled transistor having a control end, a first end, and a second end, the first pixel electrode connects to the corresponding scanning line and data line of the pixel cell via the first switch circuit, the second pixel electrode connects to the corresponding data line of the pixel cell via the second switch circuit, and the second pixel electrode connects to the first

switch circuit at least via the second switch circuit such that the second pixel electrode connects to the corresponding data line of the pixel cell, the control end of the controlled transistor connects to the corresponding scanning line of the pixel cell, the first end of the controlled transistor connects to the second pixel electrode, and the second end of the controlled transistor connects to the common electrode; and

wherein when the corresponding scanning line of the pixel cell inputs the scanning signals to turn on the first switch circuit, the second switch circuit and the controlled transistor, the first pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit, the second pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit and the second switch circuit in turn, the voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit, and the controlled transistor changes the voltage of the second pixel electrode when the controlled transistor is turn on such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero.

5. The array substrate as claimed in claim 4, wherein the current amount of the first switch circuit is different from that of the second switch circuit when the switch circuits are turn on so as to obtain different voltage difference between the first pixel electrode and the second pixel electrode.

6. The array substrate as claimed in claim 5, wherein the first switch circuit is a first TFT, the second switch circuit is a second TFT the width/length ratio of the first TFT is different from that of the second TFT such that the current amount of the first TFT is different from that of the second TFT when the TFTs are turn on.

7. The array substrate as claimed in claim 4, wherein each of the pixel cells further includes a third pixel electrode and a third switch circuit, the third pixel electrode connects to the corresponding scanning line of the pixel cell via the third switch circuit, and the third pixel electrode connects to the first switch circuit via the third switch circuit such that the third pixel electrode connects to the corresponding data line of the pixel cell; and

the second pixel electrode connects to the first switch circuit via the second switch circuit and the third switch circuit in turn such that the second pixel electrode connects to the corresponding data line of the pixel cell.

8. The array substrate as claimed in claim 4, wherein the controlled transistor is a discharging TFT, a control end of the controlled transistor corresponds to a gate of the discharging TFT, a first end of the controlled transistor corresponds to a source of the discharging TFT, and a second end of the controlled transistor corresponds to a drain of the discharging TFT, and a width/length ratio of the discharging TFT is smaller than a predetermined value such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero when the discharging TFT is turn on.

9. A display panel, comprising:

an array substrate, a color filtering substrate and a liquid, crystal layer between the array substrate and the color filtering substrate; and

the array substrate includes:

a plurality of scanning lines, a plurality of data lines, a plurality of pixel cells, and a common electrode for inputting a common voltage, and each of the pixel cells corresponds to one scanning line and one data line;

each of the pixel cells includes two pixel electrodes and two switch circuits, the two pixel electrode include a first pixel electrode and a second pixel electrode, the two switch circuits include a first switch circuit operating on the first pixel electrode and a second switch circuit operating on the second pixel electrode, each of the pixel cells further includes a controlled transistor having a control end, a first end, and a second end, the first pixel electrode connects to the corresponding scanning line and data line of the pixel cell via the first switch circuit the second pixel electrode connects to the corresponding data line of the pixel cell via the second switch circuit, and the second pixel electrode connects to the first switch circuit at least via the second switch circuit such that the second pixel electrode connects to the corresponding data line of the pixel cell, the control end of the controlled transistor connects to the corresponding scanning line of the pixel cell, the first end of the controlled transistor connects to the second pixel electrode, and the second end of the controlled transistor connects to the common electrode; and

wherein when the corresponding scanning line of the pixel cell inputs the scanning signals to turn on the first switch circuit, the second switch circuit and the controlled transistor, the first pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit, the second pixel electrode receives the data signals from the corresponding data lines of the pixel cell via the first switch circuit and the second switch circuit in turn, the voltage difference between the first pixel electrode and the second pixel electrode is not equal to zero during operations of the first switch circuit and the second switch circuit, and the controlled transistor changes the voltage of the second pixel electrode when the controlled transistor is turn on such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero.

10. The liquid crystal panel as claimed in claim 9, wherein the current amount of the first switch circuit is different from that of the second switch circuit when the switch circuits are turn on so as to obtain different voltage difference between the first pixel electrode and the second pixel electrode.

11. The liquid crystal panel as claimed in claim 10, wherein the first switch circuit is a first TFT, the second switch circuit is a second TFT, the width/length ratio of the first TFT is different from that of the second TFT such that the current amount of the first TFT is different from that of the second TFT when the TFTs are turn on.

12. The liquid crystal panel as claimed in claim 9, wherein each of the pixel cells further includes a third pixel electrode and a third switch circuit, the third pixel electrode connects to the corresponding scanning line of the pixel cell via the third switch circuit, and the third pixel electrode connects to the first switch circuit via the third switch circuit such that the third pixel electrode connects to the corresponding data line of the pixel cell; and

the second pixel electrode connects to the first switch circuit via the second switch circuit and the third switch

circuit in turn such that the second pixel electrode connects to the corresponding data line of the pixel cell.

13. The liquid crystal panel as claimed in claim 9, wherein the controlled transistor is a discharging TFT, a control end of the controlled transistor corresponds to a gate of the discharging TFT, a first end of the controlled transistor corresponds to a source of the discharging TFT, and a second end of the controlled transistor corresponds to a drain of the discharging TFT, and a width/length ratio of the discharging TFT is smaller than a predetermined value such that the voltage difference between the second pixel electrode and the common electrode is decreased and is not equal to zero when the discharging TFT is turn on.

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专利名称(译)	阵列基板和液晶面板		
公开(公告)号	US20160210924A1	公开(公告)日	2016-07-21
申请号	US14/232271	申请日	2013-07-25
[标]申请(专利权)人(译)	深圳嘉星光电科技有限公司		
申请(专利权)人(译)	深圳市嘉星光电科技有限公司，INC.		
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[标]发明人	YAO XIAOHUI CHEN CHENG HUNG		
发明人	YAO, XIAOHUI CHEN, CHENG-HUNG		
IPC分类号	G09G3/36 G02F1/1368 G02F1/1362		
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外部链接	Espacenet USPTO		

摘要(译)

公开了一种阵列基板和液晶面板。阵列基板的每个像素单元包括至少两个像素电极和至少两个开关电路。第一像素电极通过第一开关电路连接到对应的扫描线和像素单元的对应数据线。第二像素电极通过第二开关电路连接到像素单元的相应扫描线。第二像素电极至少经由第二开关电路连接到第一开关电路，使得第二像素电极连接到像素单元的对应数据线。这样，宽视角的颜色失真和显示性能是增强。

