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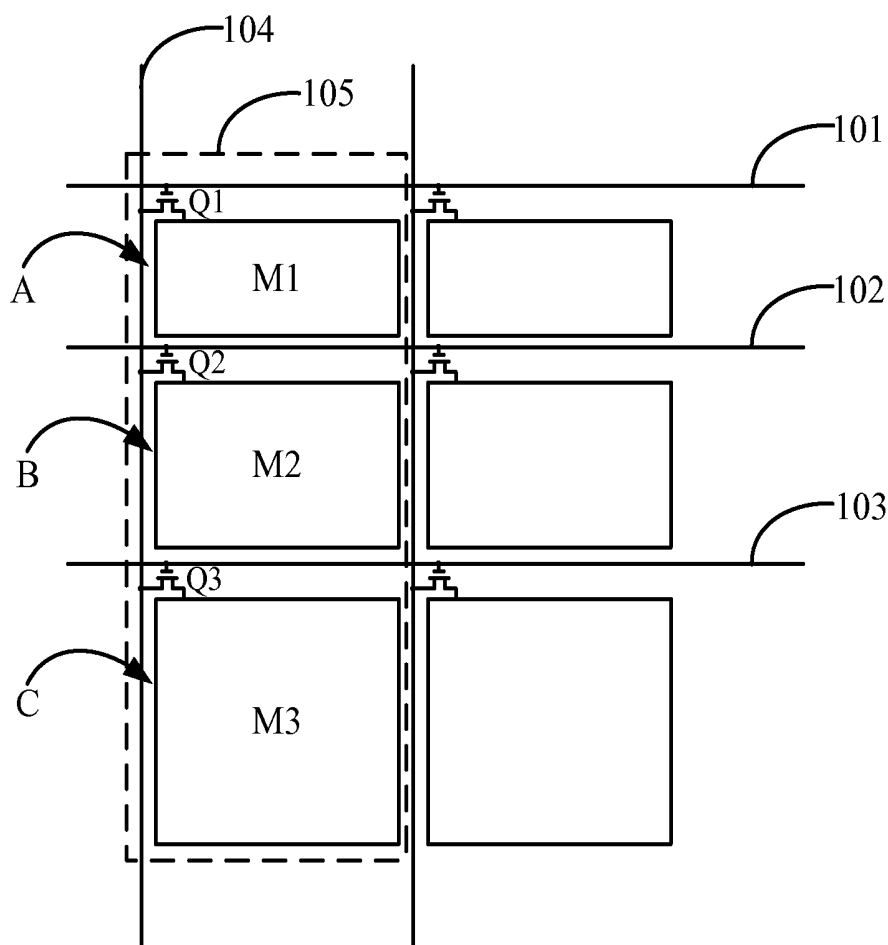
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(57) **ABSTRACT**

The present invention discloses an array substrate and a liquid crystal display panel. In the array substrate, each pixel unit has a first pixel area, a second pixel area, and a third pixel area. The voltage applied at the first pixel area is V_a . The voltage applied at the second pixel area is V_b , and the voltage applied at the third pixel area is V_c , and the relationship among the voltages is $V_a > V_b > V_c$. Ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%. Therefore, it can reduce the color difference at the large viewing angle to obtain a better low color shift effect and improve the display quality.



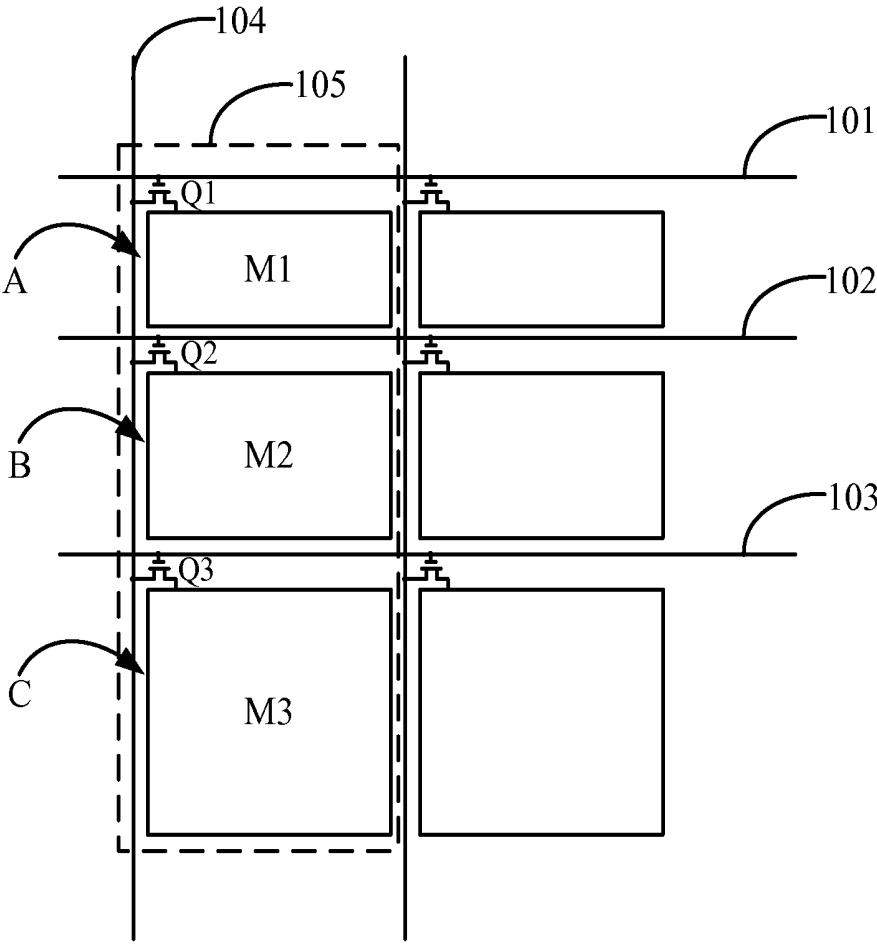


FIG. 1

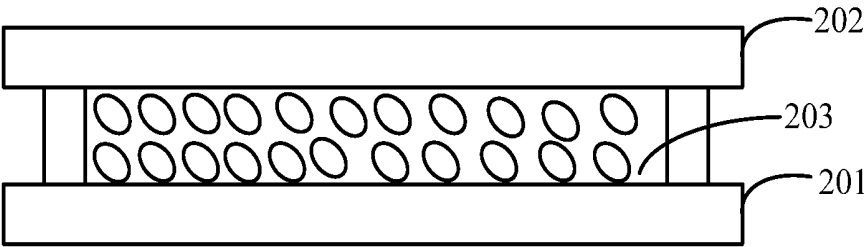


FIG. 2

ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY PANEL

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to the field of liquid crystal display technology, and more particularly to an array substrate and a liquid crystal display panel.

[0003] 2. Description of Related Art

[0004] Compared to the traditional CRT monitor, liquid crystal display (LCD) device has advantages of slim, compact, low power consumption, lifelike images, no flicker such that it gradually becomes the main development direction of the display market. The LCD device mainly utilizes the electro-optical effect of the liquid crystal by applying a voltage to control the tilt angle of the liquid crystal molecules. Therefore, the light emitted from the backlight source can pass through or not pass through the liquid crystal layer to achieve a selective light or dark effect so as to generate different colors and pictures to achieve the purpose of the display image.

[0005] However, the LCD device exist the color shift problem. Because the LCD device utilizes the liquid crystal to achieve the display, under different viewing angles, the effective refractive index of the liquid crystal molecules are not the same so as to cause the change of the light intensity of the transmitted light. Specific phenomenon is a reduced ability to transmit the light under oblique viewing angles. The display colors at the positive viewing angle and at oblique viewing angle are inconsistent, that is, the image which is observed normally at the positive viewing angle become abnormal at the oblique angle and it exist the color shift.

SUMMARY OF THE INVENTION

[0006] The main object of the present invention is to provide an array substrate and a liquid crystal display panel in order to effectively reduce the color difference at large viewing angle and improve display quality.

[0007] In order to solve the above technical problems, a technical solution provided by the present invention is an array substrate comprising: multiple first scan lines; multiple second scan lines; multiple third scan lines; multiple data lines; and multiple pixels units, each pixel unit corresponding to one of the first scan lines, one of the second scan lines, one of the third scan lines, and one of the data lines; each pixel unit including a first pixel area, a second pixel area, and a third pixel area; each pixel unit is a R pixel unit, a G pixel unit or a B pixel unit; wherein

[0008] voltages applied at the first pixel area, the second pixel area, and the third pixel area are respectively V_a , V_b , and V_c ; the first pixel area includes a first switch and a first pixel electrode, the second pixel area includes a second switch and a second pixel electrode, and the third pixel area includes a third switch and a third pixel electrode; the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first switch, the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second switch, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third switch;

[0009] when the first scan line inputs a scan signal to control the first switch to turn on, the data line inputs the voltage V_a to the first pixel electrode through the first switch, when

the second scan line inputs a scan signal to control the second switch to turn on, the data line inputs the voltage V_b to the second pixel electrode through the second switch, and when the third scan line inputs a scan signal to control the third switch to turn on, the data line inputs the voltage V_c to the third pixel electrode through the third switch;

[0010] the voltage V_a , V_b , and V_c have the following relationship: $V_a > V_b > V_c$, wherein, ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%.

[0011] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 7%-15%, a range of the area ratio of the second pixel area to the pixel unit is 23%-30%, and a range of the area ratio of the third pixel area to the pixel unit is 60%-70%.

[0012] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 17%-22%, a range of the area ratio of the second pixel area to the pixel unit is 33%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 40%-50%.

[0013] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 10%-20%, a range of the area ratio of the second pixel area to the pixel unit is 25%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 45%-65%.

[0014] Wherein, the multiple first scan lines, the multiple second scan lines, and the multiple third scan lines are arranged in rows, and the multiple data lines are arranged in columns; the first pixel electrode, the second pixel electrode, and the third pixel electrode are arranged in a column direction.

[0015] Wherein, the first switch is a first thin film transistor, and the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first thin film transistor; the second switch is a second thin film transistor, and the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second thin film transistor; the third switch is a third thin film transistor, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third thin film transistor.

[0016] In order to solve the above technical problems, another technical solution provided by the present invention is: an array substrate comprising: multiple pixels units, each pixel unit including a first pixel area, a second pixel area, and a third pixel area; wherein

[0017] voltages applied at the first pixel area, the second pixel area, and the third pixel area are respectively V_a , V_b , and V_c ; the voltage V_a , V_b , and V_c have the following relationship: $V_a > V_b > V_c$, wherein, ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%.

[0018] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 7%-15%, a range of the area ratio of the second pixel area to the pixel unit is 23%-30%, and a range of the area ratio of the third pixel area to the pixel unit is 60%-70%.

[0019] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 17%-22%, a range of the area ratio of the second pixel area to the pixel unit is 33%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 40%-50%.

[0020] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 10%-20%, a range of the area ratio of the second pixel area to the pixel unit is 25%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 45%-65%.

[0021] Wherein, each pixel unit is an R pixel unit a G pixel unit or a B pixel unit.

[0022] Wherein, the array substrate further comprises multiple first scan lines, multiple second scan lines, multiple third scan lines, and multiple data lines; each pixel unit corresponds to one of the first scan lines, one of second scan lines, one of the third scan lines, and one of the data lines; the first pixel area includes a first switch and a first pixel electrode, the second pixel area includes a second switch and a second pixel electrode, and the third pixel area includes a third switch and a third pixel electrode; the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first switch, the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second switch, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third switch; when the first scan line inputs a scan signal to control the first switch to turn on, the data line inputs the voltage V_a to the first pixel electrode through the first switch, when the second scan line inputs a scan signal to control the second switch to turn on, the data line inputs the voltage V_b to the second pixel electrode through the second switch, and when the third scan line inputs a scan signal to control the third switch to turn on, the data line inputs the voltage V_c to the third pixel electrode through the third switch.

[0023] Wherein, the multiple first scan lines, the multiple second scan lines, and the multiple third scan lines are arranged in rows, and the multiple data lines are arranged in columns; the first pixel electrode, the second pixel electrode, and the third pixel electrode are arranged in a column direction.

[0024] Wherein, the first switch is a first thin film transistor, and the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first thin film transistor; the second switch is a second thin film transistor, and the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second thin film transistor; the third switch is a third thin film transistor, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third thin film transistor.

[0025] In order to solve the above technical problems, another technical solution provided by the present invention is a liquid crystal display panel comprising: an array substrate; a color filter substrate; and a liquid crystal layer located between the array substrate and the color filter substrate; wherein, the array substrate comprises multiple pixels units, each pixel unit including a first pixel area, a second pixel area, and a third pixel area; wherein voltages applied at the first pixel area, the second pixel area, and the third pixel area are respectively V_a , V_b , and V_c ; the voltage V_a , V_b , and V_c have the following relationship: $V_a > V_b > V_c$, wherein, ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%

[0026] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 7%-15%, a range of the area ratio of the

second pixel area to the pixel unit is 23%-30%, and a range of the area ratio of the third pixel area to the pixel unit is 60%-70%.

[0027] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 17%-22%, a range of the area ratio of the second pixel area to the pixel unit is 33%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 40%-50%.

[0028] Wherein, a range of the area ratio of the first pixel area to the pixel unit is 10%-20%, a range of the area ratio of the second pixel area to the pixel unit is 25%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 45%-65%.

[0029] The beneficial effects of the present invention are: comparing with the prior art, in an array substrate of the present invention, each pixel unit has a first pixel area a second pixel area and a third pixel area. The voltage applied at the first pixel area is V_a . The voltage applied at the second pixel area is V_b , and the voltage applied, at the third pixel area is V_c such that $V_a > V_b > V_c$. Ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%. Therefore, it can reduce the color difference at the large viewing angle to obtain a better low color shift effect and improve the display quality.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] FIG. 1 is a schematic structure diagram of an array substrate according to an embodiment of the present invention; and

[0031] FIG. 2 is a schematic structure diagram of a liquid crystal display panel according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0032] The following content combines with the drawings and the embodiment for describing the present invention in detail.

[0033] With, reference to FIG. 1, in an embodiment of an array substrate of the present invention, the array substrate comprises multiple first scan lines 101, multiple second scan lines 102, multiple third scan lines 103, multiple data lines 104 and multiple pixels units 105. Each pixel unit 105 corresponds to one of the first scan lines 101, one of the second scan lines 102, one of the third scan lines 103, and one of the data lines 104. Each pixel unit 105 is corresponding to an R pixel unit, a G pixel unit or a B pixel unit.

[0034] Each pixel unit 105 comprises a first pixel area A, a second pixel area B and a third pixel area C. Wherein, the first pixel area A includes a first switch Q1 and a first pixel electrode M1 the second pixel area B includes a second switch Q2 and a second pixel electrode M2, the third pixel area C includes, a third switch Q3 and a third pixel electrode M3. Each of the first switch Q1, the second switch Q2 and the third switch Q3 includes a control terminal, an input terminal and an output terminal. The control terminal of the first switch Q1 electrically connects to the first scan line 101 of the corresponding pixel unit 105. The input terminal of the first switch Q1 electrically connects to the data line 104 of the corresponding pixel unit 105. The output terminal of the first switch Q1 electrically connects to the first pixel electrode M1 of the corresponding pixel unit 105.

[0035] The control terminal of the second switch Q2 electrically connects to the second scan line 1102 of the corresponding pixel unit 105. The input terminal of the second switch Q2 electrically connects to the data line 104 of the corresponding pixel unit 105. The output terminal of the second switch Q2 electrically connects to the second pixel electrode M2 of the corresponding pixel unit 105.

[0036] The control terminal of the third switch Q3 electrically connects to the third scan line 1103 of the corresponding pixel unit 105. The input terminal of the third switch Q3 electrically connects to the data line 104 of the corresponding pixel unit 105. The output terminal of the third switch Q3 electrically connects to the third pixel electrode M3 of the corresponding pixel unit 105.

[0037] In the present embodiment, the first switch Q1, the second switch Q2 and the third switch Q3 are all thin film transistors, respectively, the first thin film transistor, the second thin film transistor and the third thin film transistor, wherein the control terminals of the switches correspond to the gates of the thin film transistor, the input terminals of the switches correspond to the sources of the thin film transistors, the output terminals of the switches correspond to the drains of the thin film transistor. In other embodiments, the three switches may be bipolar transistors, darlington transistors, etc., and it is not limited, here.

[0038] The first scan line 101, the second scan line 102, and the third scan line 103 are arranged in rows, and the data lines 104 are arranged in columns. The first pixel area A, the second pixel area B, and the third pixel area C are sequentially arranged in a column direction, that is, the three pixel electrodes M1, M2 and M3 are sequentially arranged in the column direction. In other embodiments, the first scan line, the second scan line and the third scan line can also be arranged in columns, and the data line can also be arranged in rows, which is not limited here. Of course, the three pixel area can be arbitrarily arranged in the column direction, such as the first pixel area locating between the second pixel area and the third pixel area, or the third pixel area locating between the first pixel area and the second pixel area, which is not specifically limited.

[0039] For the first scan line 101, the second scan line 102, and the third scan line 103, it sequentially inputs a scan signal. When it inputs a scan signal for the first scan line 101 to control the first switch Q1 to turn on, the data line 104 inputs a voltage Va to the first pixel electrode M1 through the first switch Q1 so that the voltage of the first pixel area A is Va; When it inputs a scan signal for the second scan line 102 to control the second switch Q2 to turn on, the data line 104 inputs a voltage Vb to the second pixel electrode M2 through the second switch Q2 so that the voltage of the second pixel area B is Vb. When it inputs a scan signal for the third scan line 103 to control the third switch Q3 to turn on, the data line 104 inputs a voltage Vc to the third pixel electrode M3 through the third switch Q3 so that the voltage of the third pixel area C is Vc.

[0040] Wherein the voltages inputted at the first pixel electrode M1, the second pixel electrode M2 and the third pixel electrode M3 are different. The voltages Va, Vb and Vc have the following relationship: $V_a > V_b > V_c$, that is, the voltages of the three pixel areas A, B and C have the relationship: $V_a > V_b > V_c$. According to the voltage relationship among the first pixel area A, the second pixel area B, and the third pixel area C, it controls an area ratio of the area occupied by the first pixel area A, the second pixel area B, or the third pixel area C

to the pixel unit 105 in order to obtain a better color shift effect. Wherein, after a large number of experiments and simulations, it can summarize that: a range of the area ratio of the first pixel area A to the pixel unit 105 is from 5% to 25%. A range of the area ratio of the second pixel area B to the pixel unit 105 is from 20% to 45%, and a range of the area ratio of the third pixel area C to the pixel unit 105 is from 35% to 75%. The total area occupied by the three pixel areas A, B and C is the area of the pixel unit 105.

[0041] Furthermore, a range of the area ratio of the first pixel area A to the pixel unit 105 is from 7% to 15%, a range of the area ratio of the second pixel area B to the pixel unit 105 is from 23% to 30%, and a range of the area ratio of the third pixel area C to the pixel unit 105 is from 60% to 70%. The total area occupied by the three pixel areas A, B and C is the area of the pixel unit 105.

[0042] For example, in this embodiment, an area ratio of the first pixel area A to the pixel unit 105 is 9%, an area ratio of the second pixel area B to the pixel unit 105 is 26%, and an area ratio of the third pixel area C to the pixel unit 105 is 65%. Of course, in other embodiments, area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit can be 12%, 28%, 60%, or be 15%, 23%, 62%, etc. As long as they can satisfy the above conditions, it is not limited herein.

[0043] In the present embodiment, it divides the pixel unit 105 into three pixel area A, B and C, and respectively applies the different voltages to the three pixel areas A, B and C. The voltage applied at the first pixel area A is Va, The voltage applied at the second pixel area B is Vb, and the voltage applied at the third pixel area C is Vc such that $V_a > V_b > V_c$. According to this basis, after a large number of experiments and simulations, it can summarize that: the ranges of the area ratios of the first pixel area A, the second pixel area B and the third pixel area C to the pixel unit 105 are respectively 5%-25%, 20%-45% and 35%-75%. Therefore, it can reduce the color difference at the large viewing angle to obtain a better low color shift effect and improve the display quality.

[0044] In an alternative embodiment, under satisfying the condition of the ranges of the area ratios of the first pixel area A, the second pixel area B and the third pixel area C to the pixel unit 105 are respectively 5%-25%, 20%-45% and 35%-75% according to the present invention. Furthermore, a range of the area ratio of the first pixel area A to the pixel unit 105 can be 17%-22%, a range of the area ratio of the second pixel area B to the pixel unit 105 can be 33%-40%, and a range of the area ratio of the third pixel area C to the pixel unit 105 can be 40%-50%.

[0045] Of course in another embodiment, ranges of the area ratios of the first pixel area, the second pixel area, and the third pixel area C to the pixel unit 105 can respectively be 9%-16%, 28%-38%, and 48%-55%. It can also respectively be 10%-20%, 25%-40%, and 45%-65%.

[0046] In addition, the array substrate may use three data lines to apply corresponding voltages to three pixel areas. For example, each pixel unit corresponds to a first data line, a second data line, a third data line and a scan line. The first pixel electrode of the first pixel area connects to the first data line and the scan line through the first switch; the second pixel electrode of the second pixel area connects to the second data line and the scan line through the second switch; the third pixel electrode of the third pixel area connects to the third data line and the scan line through the third switch. When the scan line inputs a scan signal, the first data line inputs a voltage Va

to the first pixel electrode, the second data line inputs a voltage V_b to the second pixel electrode, the third data line inputs a voltage V_c to the third pixel electrode, wherein the voltage V_b and V_c have the following relationship: $V_a > V_b > V_c$. In this way, it can respectively apply different voltages to the three pixel areas. Wherein the ranges of the area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75% in order to effectively reduce the color difference at large viewing angle and improve display quality.

[0047] With reference to FIG. 2, in the liquid crystal display (LCD) panel according to an embodiment of the present invention, the LCD panel includes an array substrate **201**, a color filter substrate **202** and a liquid crystal layer **203** located between the substrate **201** and the color filter substrate **202**. Wherein, the array substrate **201** is one of the array substrates in the above embodiments.

[0048] The above embodiments of the present invention are not used to limit the claims of this invention. Any use of the content in the specification or in the drawings of the present invention which produces equivalent structures or equivalent processes, or directly or indirectly used in other related technical fields is still covered by the claims in the present invention.

What is claimed is:

1. An array substrate comprising:

multiple first scan lines;

multiple second scan lines;

multiple third scan lines;

multiple data lines; and

multiple pixels units, each pixel unit corresponding to one of the first scan lines, one of the second scan lines, one of the third scan lines, and one of the data lines; each pixel unit including a first pixel area, a second pixel area, and a third pixel area; each pixel unit is a R pixel unit, a G pixel unit or a B pixel unit; wherein

voltages applied at the first pixel area, the second pixel area, and the third pixel area are respectively V_a , V_b , and V_c ; the first pixel area includes a first switch and a first pixel electrode, the second pixel area includes a second switch and a second pixel electrode, and the third pixel area includes a third switch and a third pixel electrode; the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first switch, the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second switch, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third switch;

when the first scan line inputs a scan signal to control the first switch to turn on, the data line inputs the voltage V_a to the first pixel electrode through the first switch, when the second scan line inputs a scan signal to control the second switch to turn on the data line inputs the voltage V_b to the second pixel electrode through the second switch, and when the third scan line inputs a scan signal to control the third switch to turn on, the data line inputs the voltage V_c to the third pixel electrode through the third switch;

the voltage V_a , V_b , and V_c have the following relationship: $V_a > V_b > V_c$, wherein, ranges of area ratios of the first

pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%.

2. The array substrate according to claim 1, wherein, a range of the area ratio of the first pixel area to the pixel unit is 7%-15%, a range of the area ratio of the second pixel area to the pixel unit is 23%-30%, and a range of the area ratio of the third pixel area to the pixel unit is 60%-70%.

3. The array substrate according to claim 1, wherein, a range of the area ratio of the first pixel area to the pixel unit is 17%-22%, a range of the area ratio of the second pixel area to the pixel unit is 33%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 40%-50%.

4. The array substrate according to claim 1, wherein, a range of the area ratio of the first pixel area to the pixel unit is 10%-20%, a range of the area ratio of the second pixel area to the pixel unit is 25%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 45%-65%.

5. The array substrate according to claim 1, wherein, the multiple first scan lines, the multiple second scan lines, and the multiple third scan lines are arranged in rows, and the multiple data lines are arranged in columns; the first pixel electrode, the second pixel electrode, and the third pixel electrode are arranged in a column direction.

6. The array substrate according to claim 1, wherein,

the first switch is a first thin film transistor, and the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first thin film transistor; the second switch is a second thin film transistor, and the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second thin film transistor; the third switch is a third thin film transistor, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third thin film transistor.

7. An array substrate comprising:

multiple pixels units, each pixel unit including a first pixel area a second pixel area, and a third pixel area; wherein

voltages applied at the first pixel area, the second pixel area, and the third pixel area are respectively V_a , V_b , and V_c ; the voltage V_a , V_b , and V_c have the following relationship: $V_a > V_b > V_c$, wherein, ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%.

8. The array substrate according to claim 7, wherein, a range of the area ratio of the first pixel area to the pixel unit is 7%-15%, a range of the area ratio of the second pixel area to the pixel unit is 23%-30%, and a range of the area ratio of the third pixel area to the pixel unit is 60%-70%.

9. The array substrate according to claim 7, wherein, a range of the area ratio of the first pixel area to the pixel unit is 17%-22%, a range of the area ratio of the second pixel area to the pixel unit is 33%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 40%-50%.

10. The array substrate according to claim 7, wherein, a range of the area ratio of the first pixel area to the pixel unit is 10%-20%, a range of the area ratio of the second pixel area to the pixel unit is 25%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 45%-65%.

11. The array substrate according to claim 7, wherein, each pixel unit is an R pixel unit, a G pixel unit or a B pixel unit.

12. The array substrate according to claim 7, wherein, the array substrate further comprises multiple first scan lines, multiple second scan lines, multiple third scan lines, and multiple data lines;

each pixel unit corresponds to one of the first scan lines, one of the second scan lines, one of the third scan lines, and one of the data lines;

the first pixel area includes a first switch and a first pixel electrode, the second pixel area includes a second switch and a second pixel electrode, and the third pixel area includes a third switch and a third pixel electrode; the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first switch, the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second switch, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third switch;

when the first scan line inputs a scan signal to control the first switch to turn on, the data line inputs the voltage Va to the first pixel electrode through the first switch, when the second scan line inputs a scan signal to control the second switch to turn on, the data line inputs the voltage Vb to the second pixel electrode through the second switch, and when the third scan line inputs a scan signal to control the third switch to turn on, the data line inputs the voltage Vc to the third pixel electrode through the third switch.

13. The array substrate according to claim 12, wherein, the multiple first scan lines, the multiple second scan lines, and the multiple third scan lines are arranged in rows, and the multiple data lines are arranged in columns; the first pixel electrode, the second pixel electrode, and the third pixel electrode are arranged in a column direction.

14. The array substrate according to claim 12, wherein, the first switch is a first thin film transistor, and the first pixel electrode connects to the first scan line and the data line of the corresponding pixel unit through the first thin film transistor;

the second switch is a second thin film transistor, and the second pixel electrode connects to the second scan line and the data line of the corresponding pixel unit through the second thin film transistor; the third switch is a third thin film transistor, and the third pixel electrode connects to the third scan line and the data line of the corresponding pixel unit through the third thin film transistor.

15. A liquid crystal display panel comprising:

an array substrate;

a color filter substrate; and

a liquid crystal layer located between the array substrate and the color filter substrate; wherein,

the array substrate comprises multiple pixels units, each pixel unit including a first pixel area, a second pixel area, and a third pixel area; wherein voltages applied at the first pixel area, the second pixel area, and the third pixel area are respectively Va, Vb, and Vc; the voltage Va, Vb, and Vc have the following relationship: $V_a > V_b > V_c$, wherein, ranges of area ratios of the first pixel area, the second pixel area and the third pixel area to the pixel unit are respectively 5%-25%, 20%-45% and 35%-75%.

16. The liquid crystal display panel according to claim 15, wherein, a range of the area ratio of the first pixel area to the pixel unit is 7%-15%, a range of the area ratio of the second pixel area to the pixel unit is 23%-30% and a range of the area ratio of the third pixel area to the pixel unit is 60%-70%.

17. The liquid crystal display panel according to claim 15, wherein, a range of the area ratio of the first pixel area to the pixel unit is 17%-22%, a range of the area ratio of the second pixel area to the pixel unit is 33%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 40%-50%.

18. The liquid crystal display panel according to claim 15, wherein, a range of the area ratio of the first pixel area to the pixel unit is 10%-20%, a range of the area ratio of the second pixel area to the pixel unit is 25%-40%, and a range of the area ratio of the third pixel area to the pixel unit is 45%-65%.

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专利名称(译)	阵列基板和液晶显示板		
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摘要(译)

本发明公开了一种阵列基板和液晶显示面板。在阵列基板中，每个像素单元具有第一像素区域，第二像素区域和第三像素区域。在第一像素区域施加的电压是 V_a 。在第二像素区域施加的电压是 V_b ，在第三像素区域施加的电压是 V_c ，并且电压之间的关系是 $V_a > V_b > V_c$ 。第一像素区域，第二像素区域和第三像素区域与像素单元的面积比的范围分别为5%-25%，20%-45%和35%-75%。因此，它可以减小大视角处的色差，以获得更好的低色移效果并提高显示质量。

