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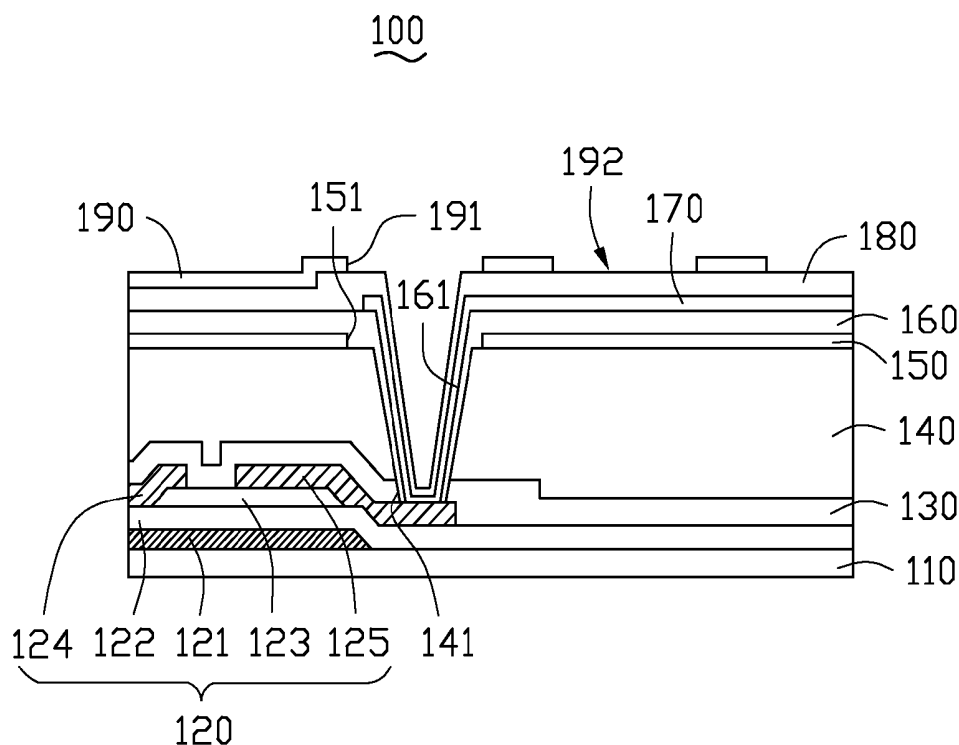
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(57) **ABSTRACT**

An array substrate for a liquid crystal display device includes a first storage capacitor and a second storage capacitor for increased capacitance. The first storage capacitor is formed by a first common electrode and a pixel electrode. The second storage capacitor is formed by a second common electrode and the pixel electrode.

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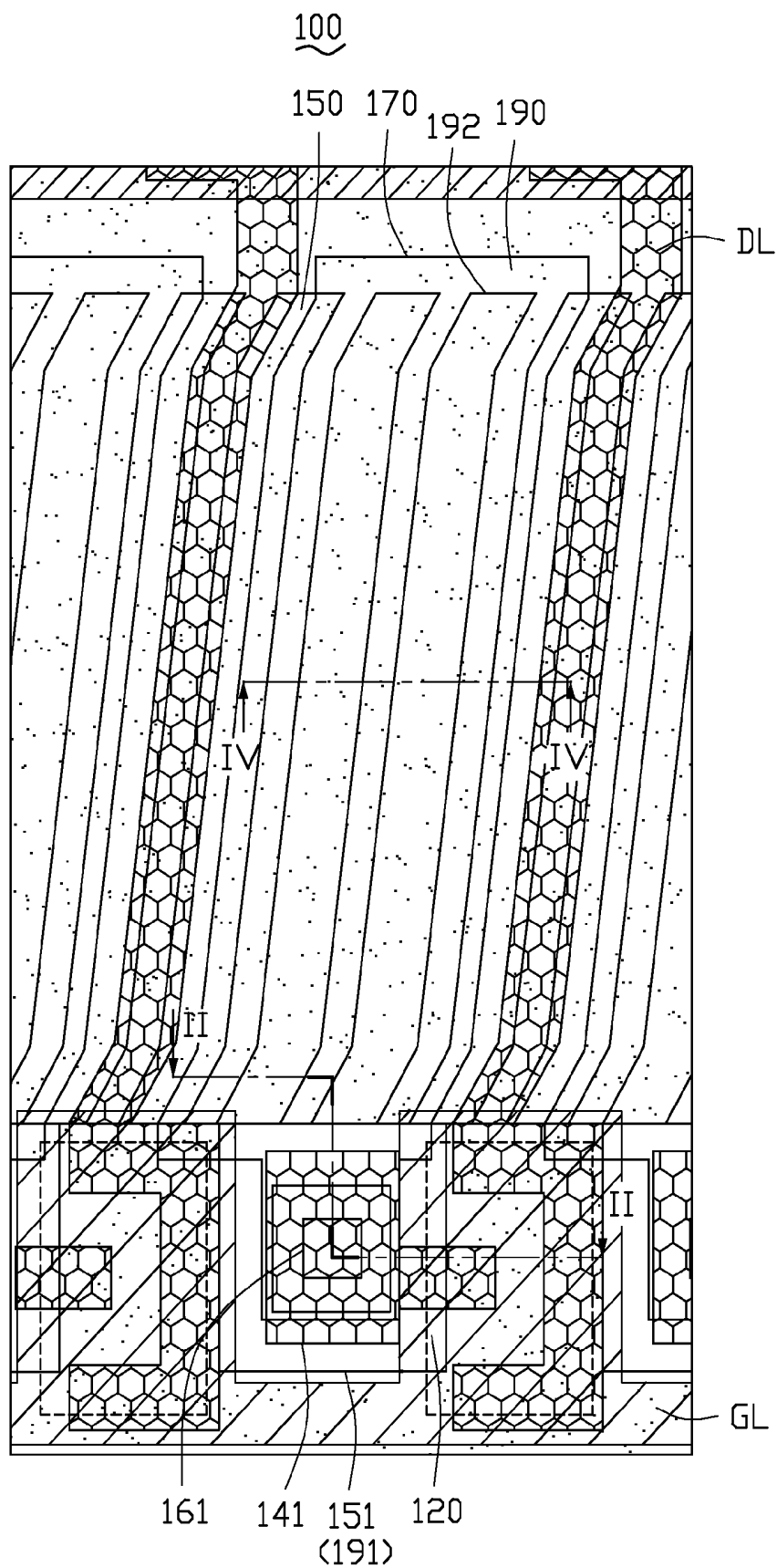


FIG. 1

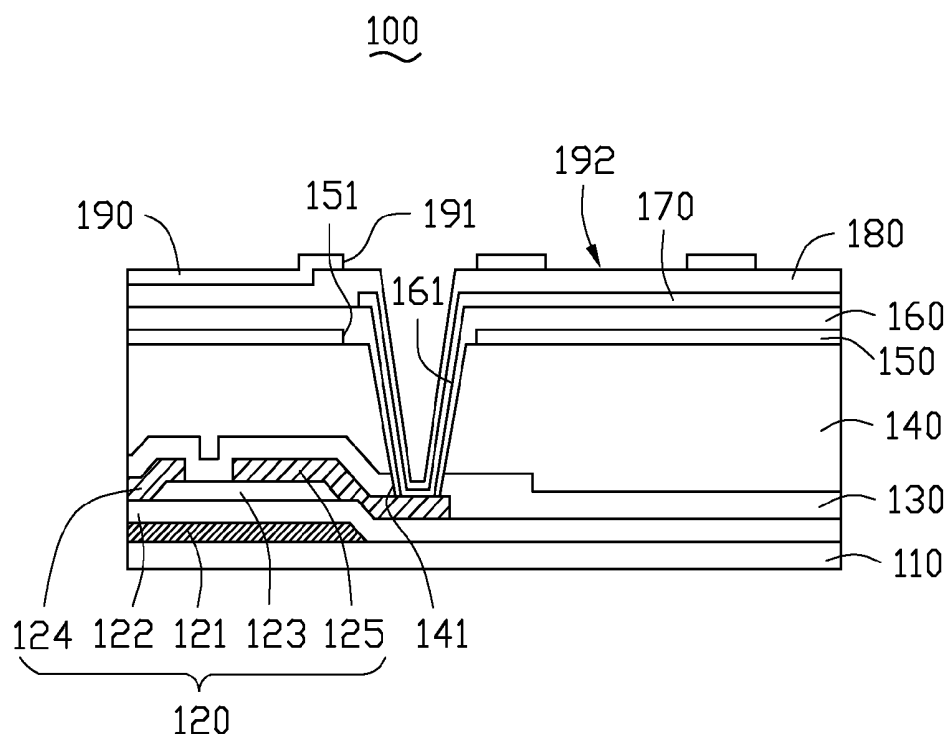


FIG. 2

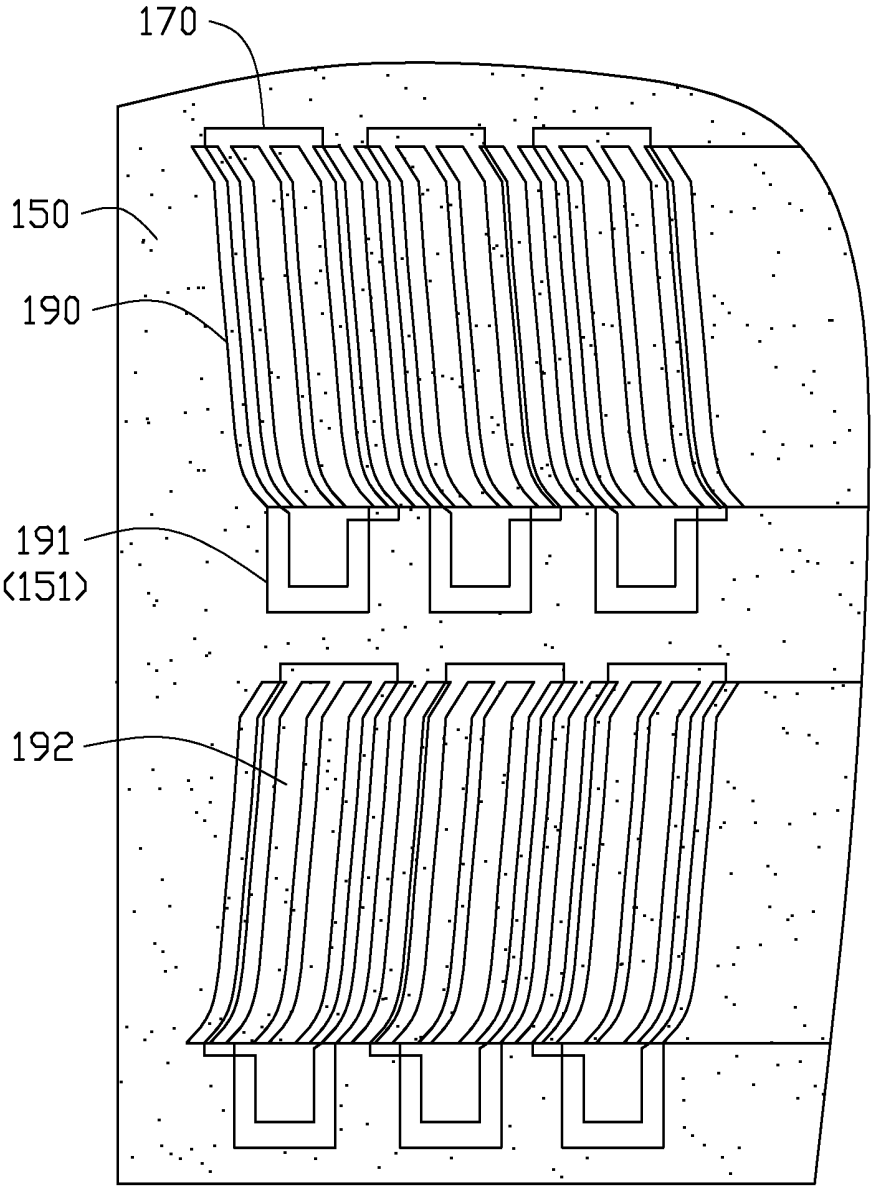


FIG. 3

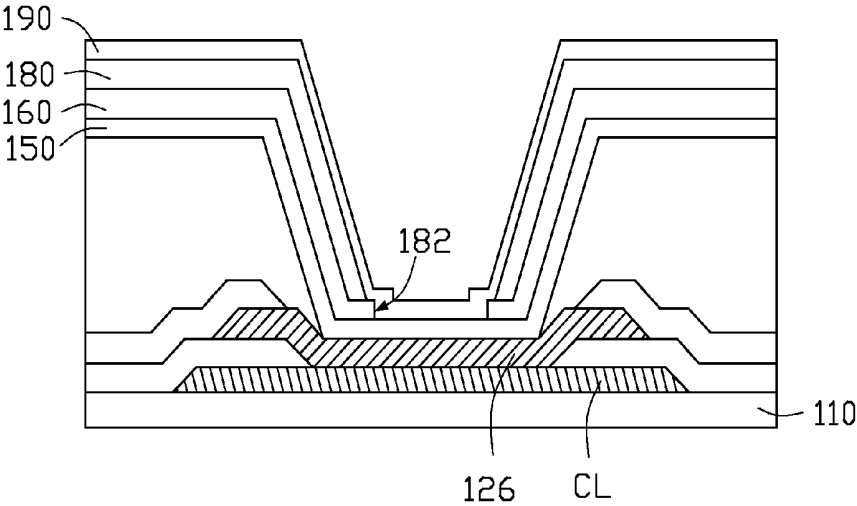


FIG. 4

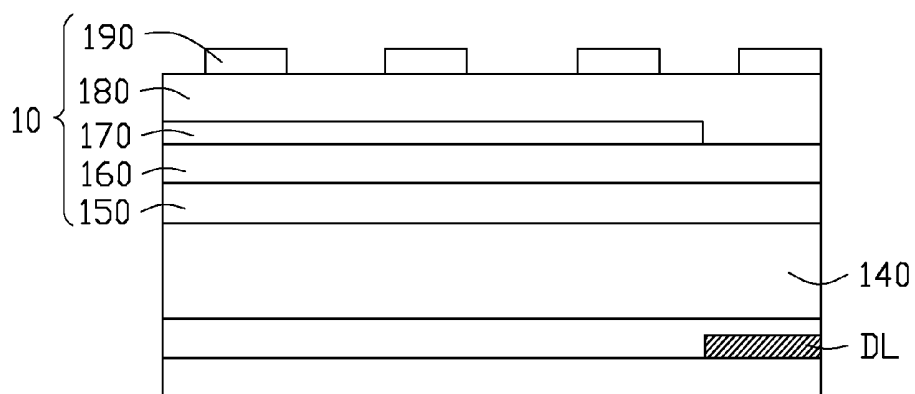


FIG. 5

FIG. 6

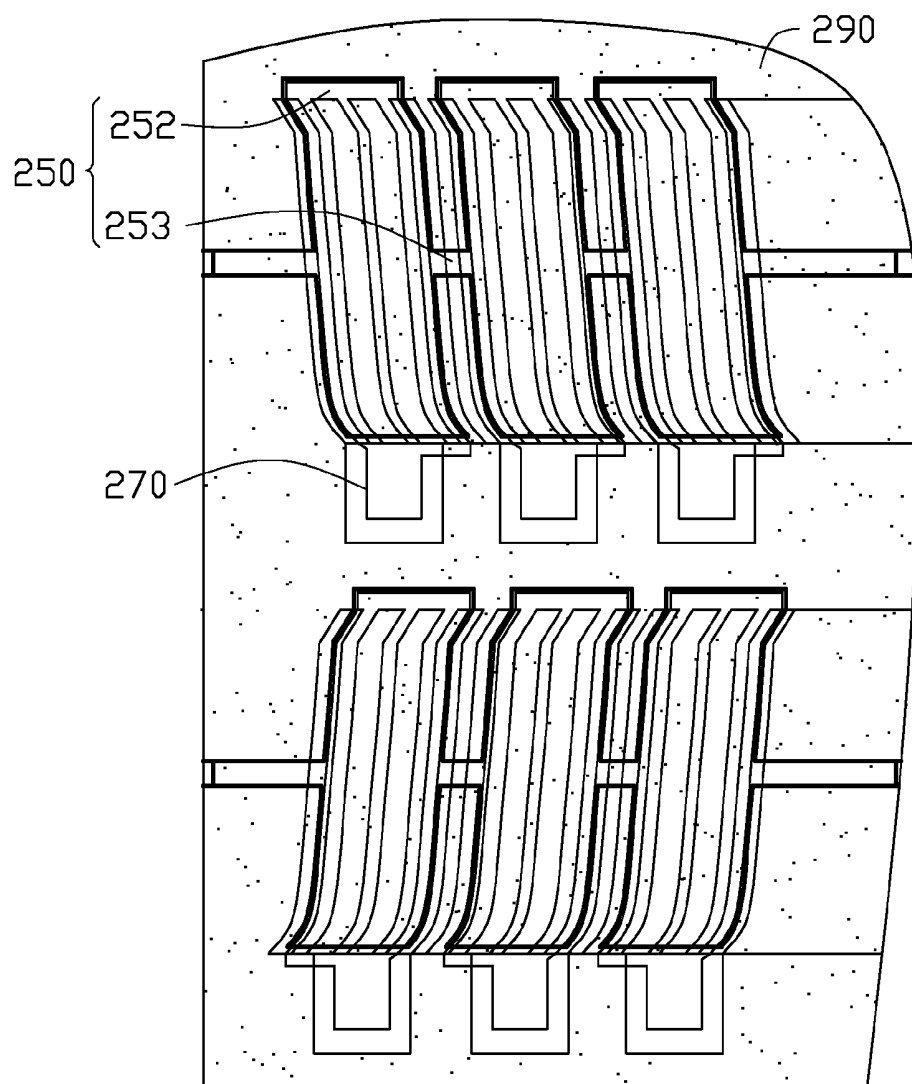


FIG. 7

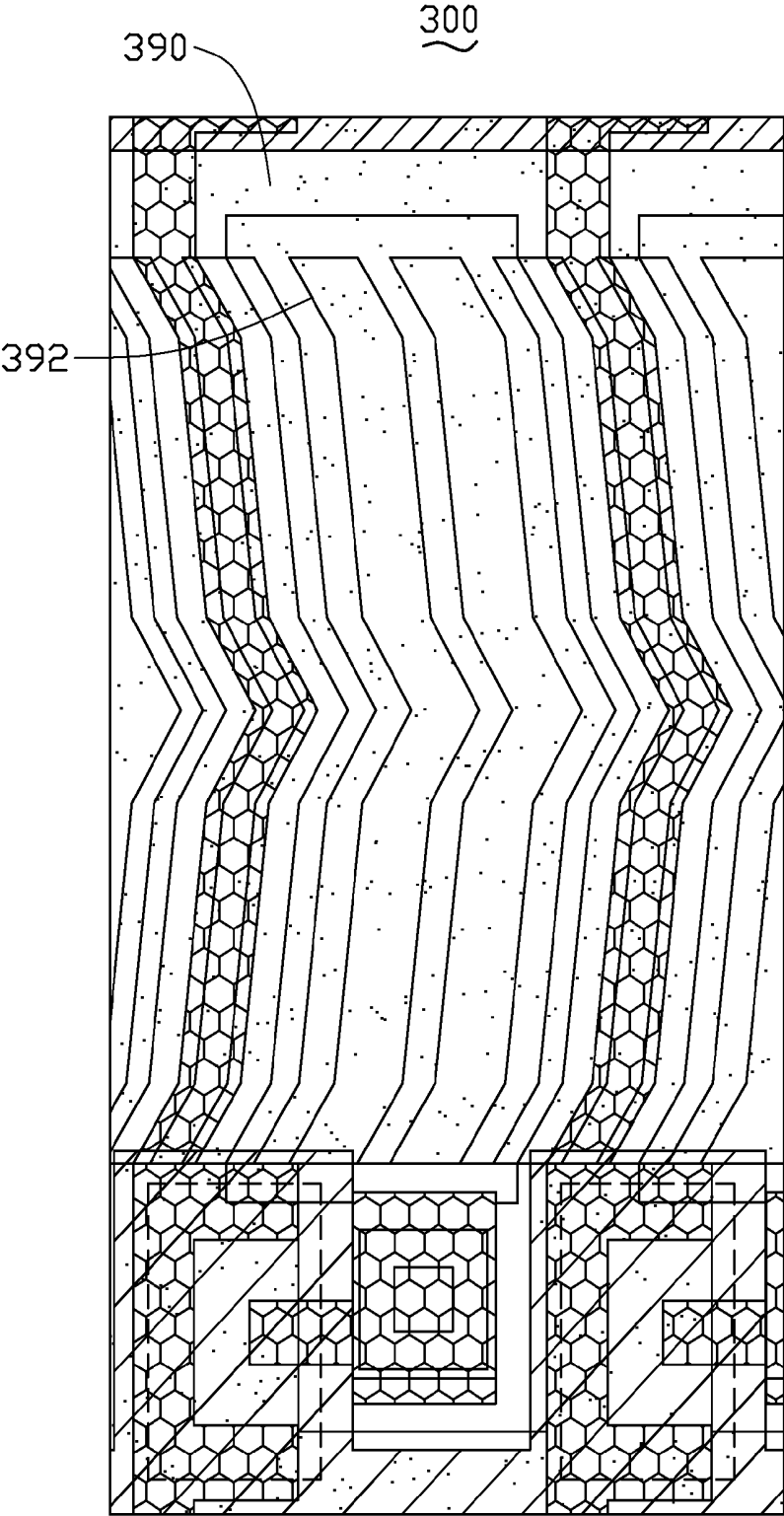


FIG. 8

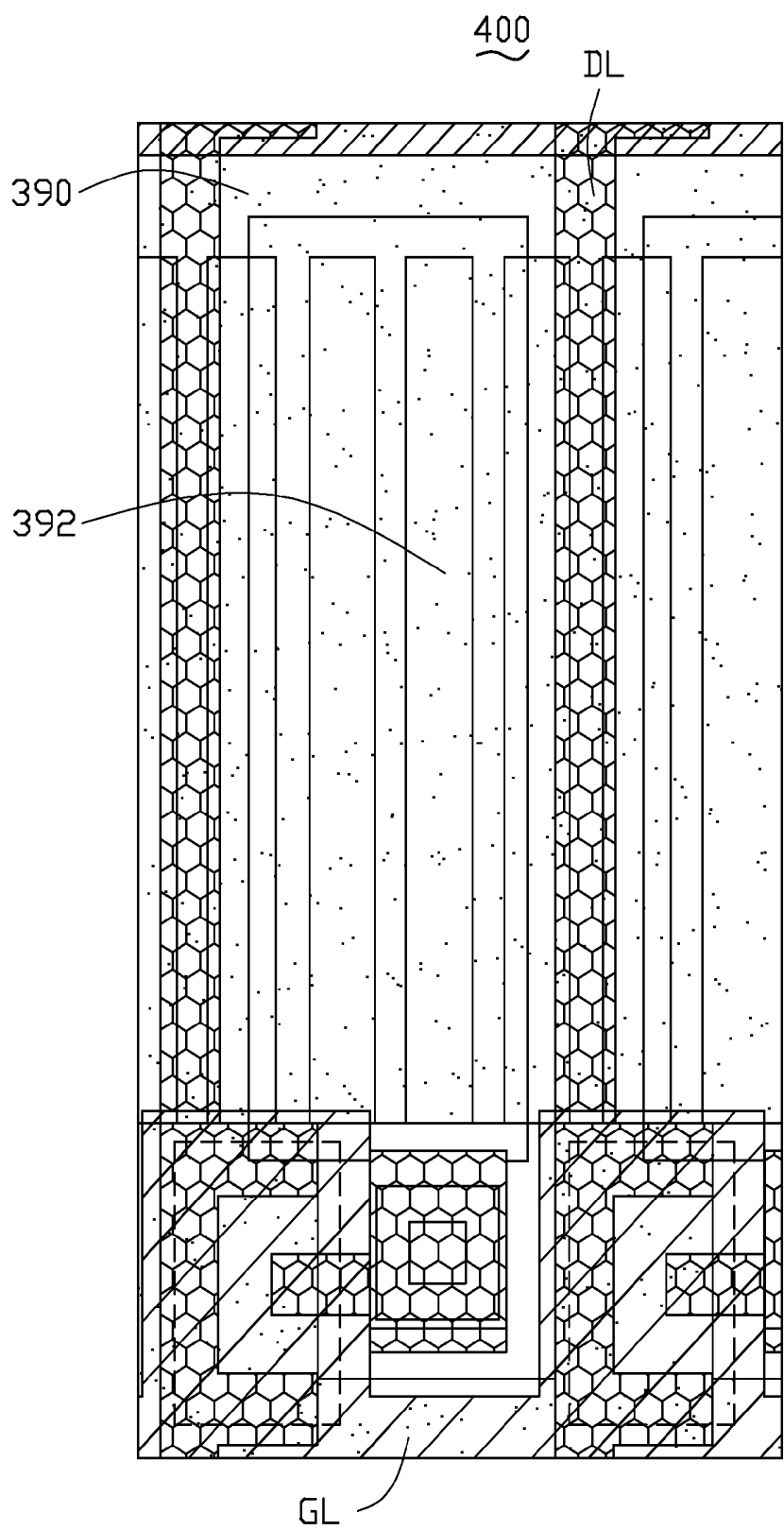


FIG. 9

ARRAY SUBSTRATE AND LIQUID CRYSTAL DISPLAY DEVICE USING SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority to Taiwanese Patent Application No. 102131190 filed on Aug. 30, 2013 in the Taiwan Intellectual Property Office, the contents of which are incorporated by reference herein.

FIELD

[0002] The disclosure generally relates to a liquid crystal display device including an array substrate.

BACKGROUND

[0003] A fringe field switching liquid crystal display (FFS-LCD) device has one or more common electrodes and a plurality of pixel electrodes formed on an array substrate. The common electrode and the pixel electrodes drive a plurality of liquid crystal molecules by means of a fringe field. Generally, an FFS-LCD has a high aperture ratio and a wide viewing angle. To improve a resolution of the FFS-LCD, a density of the pixel electrodes may be increased while a capacitance of a storage capacitor is decreased.

[0004] The storage capacitor is formed by the common electrode and the pixel electrodes, with an insulation layer sandwiched between the common electrode and the pixel electrodes. The capacitance of the storage capacitor is calculated by a formula: $C_{ST} = \epsilon A/d$, wherein C_{ST} denotes the capacitance of the storage capacitor, ϵ denotes a dielectric constant of the insulation layer, A denotes an active area of the common electrode and the pixel electrode, and d denotes a thickness of the insulation layer. Thus, the capacitance of the storage capacitor is directly proportional to the active area A and is inversely proportional to the thickness d .

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] Implementations of the present technology will now be described, by way of example only, with reference to the attached figures.

[0006] FIG. 1 is a cross-sectional plan view of an array substrate of a liquid crystal display device according to a first embodiment.

[0007] FIG. 2 is a sectional view of the array substrate along line II-II of FIG. 1.

[0008] FIG. 3 is a partial sectional view of an electrode structure of the array substrate of FIG. 1.

[0009] FIG. 4 is a sectional view of a pad of a common electrode of the array substrate of the array substrate of the FIG. 1.

[0010] FIG. 5 is a sectional view of the array substrate along line IV-IV of FIG. 1.

[0011] FIG. 6 is a cross-sectional plan view of an array substrate of a liquid crystal display device according to a second embodiment.

[0012] FIG. 7 is a partial sectional view of an electrode structure of the array substrate of FIG. 6.

[0013] FIG. 8 is a cross-sectional plan view of an array substrate of a liquid crystal display device according to a third embodiment.

[0014] FIG. 9 is a cross-sectional plan view of an array substrate of a liquid crystal display device according to a fourth embodiment.

DETAILED DESCRIPTION

[0015] It will be appreciated that for simplicity and clarity of illustration, where appropriate, reference numerals have been repeated among the different figures to indicate corresponding or analogous elements. In addition, numerous specific details are set forth in order to provide a thorough understanding of the embodiments described herein. However, it will be understood by those of ordinary skill in the art that the embodiments described herein can be practiced without these specific details. In other instances, methods, procedures, and components have not been described in detail so as not to obscure the related relevant feature being described. The drawings are not necessarily to scale and the proportions of certain parts may be exaggerated to better illustrate details and features. The description is not to be considered as limiting the scope of the embodiments described herein.

[0016] FIG. 1 shows a cross-sectional plan view of an array substrate 100 of a liquid crystal display device according to a first embodiment. In the embodiment, the liquid crystal display device can be a fringe field switching liquid crystal display (FFS-LCD) device. The array substrate 100 can include a plurality of scanning lines GL and a plurality of data lines DL. The scanning lines GL are parallel to each other. The data lines DL are parallel to each other, and independently intersect with the scanning lines GL. The scanning lines GL and the data lines DL define multiple sub-pixels where the scanning lines GL cross the data lines DL. Each sub-pixel can include a thin film transistor (TFT) 120 and a pixel electrode 170. In the embodiment, the pixel electrode 170 can be a plate-like structure in the sub-pixel, to couple to the TFT 120.

[0017] The array substrate 100 further includes a first common electrode 150 and a second common electrode 190. In the embodiment, the array substrate 100 includes a three-layer electrode structure. The first common electrode 150 overlaps with the second common electrode 190. The first common electrode 150 covers the multiple sub-pixels and the second common electrode 190 covers the first common electrode. In the embodiment, the first common electrode 150 can be a plate-like structure. The second common electrode 190 can include a plurality of parallel slits 192. A fringe field is formed between the second common electrode 190 and the pixel electrode 170 to drive a plurality of liquid crystal molecules (not shown). In FIG. 1, the slits 192 can be strip-shaped. In another embodiment, the slits 192 can be <-shaped or other angled shape.

[0018] FIG. 2 shows a sectional view of the array substrate 100 along line II-II of FIG. 1. The array substrate 100 further includes a substrate 110, a passivation layer 130, a planar layer 140, and a first protection layer 160. The TFT 120 is arranged on the substrate 110. Each TFT 120 can include a gate 121, a gate insulator 122, a channel layer 123, a source 124, and a drain 125. The gate 121 is located on the substrate 110 and is covered by the gate insulator 122. The channel layer 123 is arranged on the gate insulator 122 to correspond to the gate 121. The source 124 and the drain 125 are located on opposite sides of the channel layer 123.

[0019] The passivation layer 130 covers the TFT 120 and the substrate 110, while the passivation layer 130 itself is covered by the planar layer 140. In the embodiment, the planar layer 140 is made of organic materials and a thickness of the planar layer 140 is greater than a thickness of the passivation layer 130. A first opening hole 141 is defined to

pass through the passivation layer 130 and the planar layer 140 to expose one part of the drain 125.

[0020] A second opening hole 151 is defined in the first common electrode 150 and communicates with the first opening hole 141. A diameter of the second opening hole 151 is greater than a diameter of the first opening hole 141. The first opening hole 141 in cooperation with the second opening hole 151 defines a connecting hole. Internal walls of both the first and second opening holes 141 and 151 are covered by the first protection layer 160. A third opening hole 161 is defined in the first protection layer 160 to expose one part of the drain 125 via the connecting hole defined by the first and second opening holes 141 and 151. The pixel electrode 170 is arranged on the first protection layer 160 to connect to the drain 125 via the third opening hole 161.

[0021] The second protection layer 180 is arranged on and covers the pixel electrode 170 of the substrate 110, such that the pixel electrode 170 at the third opening hole 161 is protected by the second protection layer 180. A fourth opening hole 191 is defined in the second common electrode 190 and communicates with the third opening hole 161 which is covered by the second protection layer 180. The second common electrode 190 is arranged on the second protection layer 180. The fourth opening hole 191 and the second opening hole 151 have the same diameter. In the embodiment, the fourth opening hole 191 and the second opening hole 151 are coaxial with the first opening hole 141. The fourth opening hole 191 is defined in the second common electrode 190 to avoid any short circuit between the second common electrode 190 and the pixel electrode 170.

[0022] FIG. 3 shows a partial sectional view of an electrode structure of the array substrate 100. The first common electrode 150 covers the plurality of sub-pixels in an unbroken fashion, and the second opening hole 151 is defined in the first common electrode to correspond to each sub-pixel. The pixel electrodes 170 are plate-shaped structures, and each pixel electrode 170 is arranged in one sub-pixel. The second common electrode 190 unbrokenly covers the first common electrode 150. The fourth opening hole 191 is defined in the second common electrode 190 to correspond to each sub-pixel. A plurality of slits 192 is defined in the second common electrode 190. The slits 192 are symmetrical between two adjacent sub-pixels.

[0023] FIG. 4 shows a sectional view of a pad of a common electrode of the array substrate 100. The array substrate 100 can further include a common line CL arranged on the substrate 110. The first protection layer 160 and the second protection layer 180 are sandwiched between the first common electrode 150 and the second common electrode 190. A through hole 182 is defined to pass through the first protection layer 160 and the second protection layer 180. One part of the first common electrode 150 is coupled to the second common electrode 190 via the through hole 182. The first common electrode 150 is electrically coupled to the common line CL to receive a common signal. The first common electrode 150 can be coupled to the common line CL via a metal layer 126 arranged on the common line CL. The metal layer 126 can be made of the same material as that of the data line DL, the source 124, and the drain 125.

[0024] FIG. 5 shows a sectional view of the array substrate 100 along line IV-IV of FIG. 1. The storage capacitor 10 is located in the planar layer 140. The storage capacitor 10 is formed by the first common electrode 150, the first protection layer 160, the pixel electrode 170, the second protection layer

180, and the second common electrode 190. The pixel electrode 170, the first common electrode 150, and the second common electrode 190 are made of a transparent conductive material such as indium-tin-oxide (ITO) or indium-zinc-oxide (IZO). The first protection layer 160 and the second protection layer 180 are made of an insulated material such as silicon oxide (SiO_x) or silicon nitride (SiN_x).

[0025] The first common electrode 150 overlaps a portion of the pixel electrode 170 to form a first storage capacitor. The second common electrode 190 overlaps the other portion of the pixel electrode 170 to form a second storage capacitor. The first storage capacitor is coupled with the second storage capacitor in parallel. The array substrate 100 includes the second common electrode 190 to increase a storage capacitance per unit area of the array substrate 100.

[0026] FIG. 6 shows a cross-sectional plan view of an array substrate 200. FIG. 7 shows a partial sectional view of an electrode structure of the array substrate 200. The array substrate 200 can include a first common electrode 250, a pixel electrode 270, and a second common electrode 290. The array substrate 200 is similar to the array substrate 100 except that the first common electrode 250 covers one part of the data line DL. As an overlapping area between the first common electrode 250 and the data line DL is decreased, a parasitic capacitance between the first common electrode 250 and the data line DL is also decreased. The first common electrode 250 can include a plurality of strip-shaped common electrodes 252 and a plurality of connection portions of the first common electrode 253. Each strip-shaped common electrode 252 is located in one sub-pixel and each connection portion of the first common electrode 253 is located between two adjacent sub-pixels in one row. The plurality of strip-shaped common electrodes 252 extends along the scanning line GL. No strip-shaped common electrode 252 overlaps with the data line DL. The connection portion of the first common electrode 253 does overlap one part of data line DL.

[0027] FIG. 8 shows a cross-sectional plan view of an array substrate 300. The array substrate 300 is similar to the array substrate 100 except that the slits 392 of the second common electrode 390 are <-shaped.

[0028] FIG. 9 shows a cross-sectional plan view of an array substrate 400. The array substrate 400 is similar to the array substrate 100 except that the data line DL and the slits 492 are perpendicular to the scanning line GL. Each of the slits 492 is strip-shaped.

[0029] In summary, the array substrate includes a first common electrode and a second common electrode to increase a storage capacitance per unit area. Therefore, design flexibility is increased, particularly in high-resolution LCDs. Increased storage capacitance for high-resolution LCDs and pixel density avoids flicker and crosstalk.

[0030] It is to be understood that even though numerous characteristics and advantages of the present embodiments have been set forth in the foregoing description, with details of the structures and functions of the embodiments, the disclosure is illustrative only and changes may be in detail, especially in the matter of arrangement of parts within the principles of the embodiments, to the full extent indicated by the broad general meaning of the terms in which the appended claims are expressed.

What is claimed is:

1. An array substrate comprising:
 - a storage capacitor including:
 - a first common electrode;
 - a first protection layer on the first common electrode;

a pixel electrode on the first protection layer;
a second protection layer on the pixel electrode; and
a second common electrode arranged on the second protection layer and electrically coupled to the first common electrode, the second common electrode having a plurality of slits.

2. The array substrate of claim 1, further comprising a substrate, a thin film transistor (TFT) arranged on the substrate, a passivation layer covering the TFT, and a planar layer covering the passivation layer, wherein the storage capacitor is located in the planar layer.

3. The array substrate of claim 1, further comprising a substrate, a thin film transistor (TFT) arranged on the substrate, a passivation layer covering the TFT, and a planar layer covering the passivation layer, wherein a first opening hole is defined passing through the passivation layer to expose one portion of the TFT; a second opening hole is defined in the first common electrode and communicates with the first opening hole, a diameter of the second opening hole is greater than a diameter of the first opening hole; and a third opening hole is defined in the first protection layer to expose the one part of a drain the TFT.

4. The array substrate of claim 3, wherein the pixel electrode is electrically coupled to the TFT via the third opening hole.

5. The array substrate of claim 3, wherein a fourth opening hole is defined in the second common electrode, and a diameter of the fourth opening hole is equal to a diameter of the second opening hole.

6. The array substrate of claim 1, wherein a first storage capacitor is formed by the first common electrode and the pixel electrode; and a second storage capacitor is formed by the second common electrode and the pixel electrode.

7. The array substrate of claim 1, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the pixel electrode is plate-shaped electrode in each sub-pixel.

8. The array substrate of claim 1, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the first common electrode continuously covers the plurality of sub-pixels.

9. The array substrate of claim 1, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the second common electrode overlaps with the first common electrode to continuously cover the plurality of sub-pixels.

10. The array substrate of claim 1, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the first common electrode comprises a plurality of strip-shaped common electrodes and a plurality of connection portions and each connection portion of the first common electrode overlaps one part of one data line.

11. A liquid crystal display device, comprising:
an array substrate comprising:
a storage capacitor comprising:
a first common electrode;
a first protection layer arranged on the first common electrode;

a pixel electrode arranged on the first protection layer;
a second protection layer arranged on the pixel electrode;

a second common electrode arranged on the second protection layer; and the second common electrode electrically coupled to the first common electrode, and the second common electrode having a plurality of slits.

12. The liquid crystal display device of claim 11, further comprising a substrate, a thin film transistor (TFT) arranged on the substrate, a passivation layer covering the TFT, and a planar layer covering the passivation layer, wherein the storage capacitor is located in the planar layer.

13. The liquid crystal display device of claim 11, further comprising a substrate, a thin film transistor (TFT) arranged on the substrate, a passivation layer covering the TFT, and a planar layer covering the passivation layer, wherein a first opening hole is defined passing through the passivation layer to expose one portion of the TFT; a second opening hole is defined in the first common electrode and communicates with the first opening hole, a diameter of the second opening hole is greater than a diameter of the first opening hole; and a third opening hole is defined in the first protection layer to expose the one part of a drain the TFT.

14. The liquid crystal display device of claim 13, wherein the pixel electrode is electrically coupled to the TFT via the third opening hole.

15. The liquid crystal display device of claim 13, wherein a fourth opening hole is defined in the second common electrode, and a diameter of the fourth opening hole is equal to a diameter of the second opening hole.

16. The liquid crystal display device of claim 11, wherein a first storage capacitor is formed by the first common electrode and the pixel electrode; and a second storage capacitor is formed by the second common electrode and the pixel electrode.

17. The liquid crystal display device of claim 11, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the pixel electrode is plate-shaped electrode in each sub-pixel.

18. The liquid crystal display device of claim 11, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the first common electrode continuously covers the plurality of sub-pixels.

19. The liquid crystal display device of claim 11, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the second common electrode overlaps with the first common electrode to continuously cover the plurality of sub-pixels.

20. The liquid crystal display device of claim 11, further comprising a plurality of scanning lines and a plurality of data lines, the scanning lines and the data lines define multiple sub-pixels where the scanning lines cross the data lines, wherein the first common electrode comprises a plurality of strip-shaped common electrodes and a plurality of connection portions and each connection portion of the first common electrode overlaps one part of one data line.

* * * * *

专利名称(译)	阵列基板和使用其的液晶显示装置		
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申请号	US14/474553	申请日	2014-09-02
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申请(专利权)人(译)	叶欣科技咨询有限公司.		
当前申请(专利权)人(译)	叶欣科技咨询有限公司.		
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其他公开文献	US9823528		
外部链接	Espacenet USPTO		

摘要(译)

一种用于液晶显示装置的阵列基板，包括第一存储电容器和用于增加电容的第二存储电容器。第一存储电容器由第一公共电极和像素电极形成。第二存储电容器由第二公共电极和像素电极形成。

