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(54) **DATA DRIVER AND LIQUID CRYSTAL DISPLAY USING THE SAME**

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(57) **ABSTRACT**

A data driver includes a gamma voltage generator that generates red, green, and blue gamma voltages according to red, green, and blue adjustment signals, and a digital to analog converter that converts data signals received from a latch to positive or negative analog video signals using the red, green, and blue gamma voltages received from the gamma voltage generator.

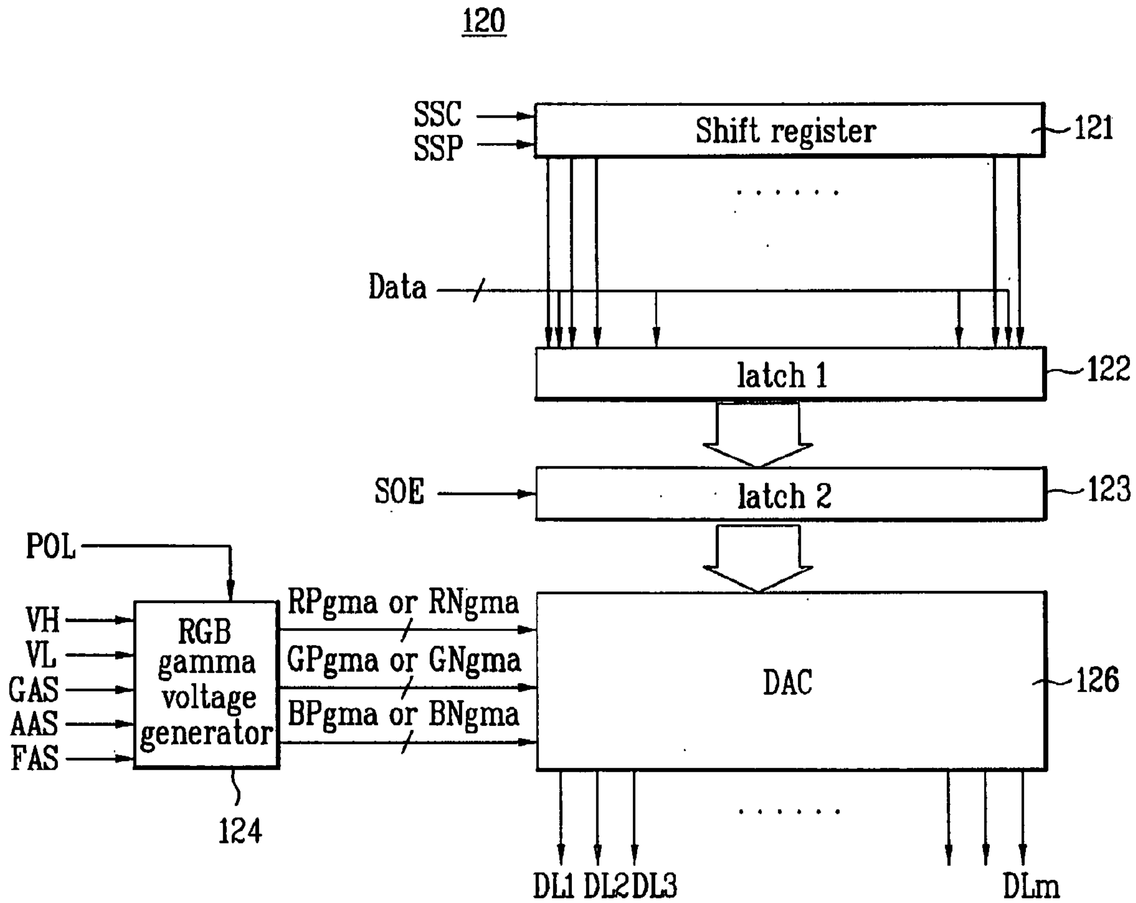


FIG. 1
Related Art

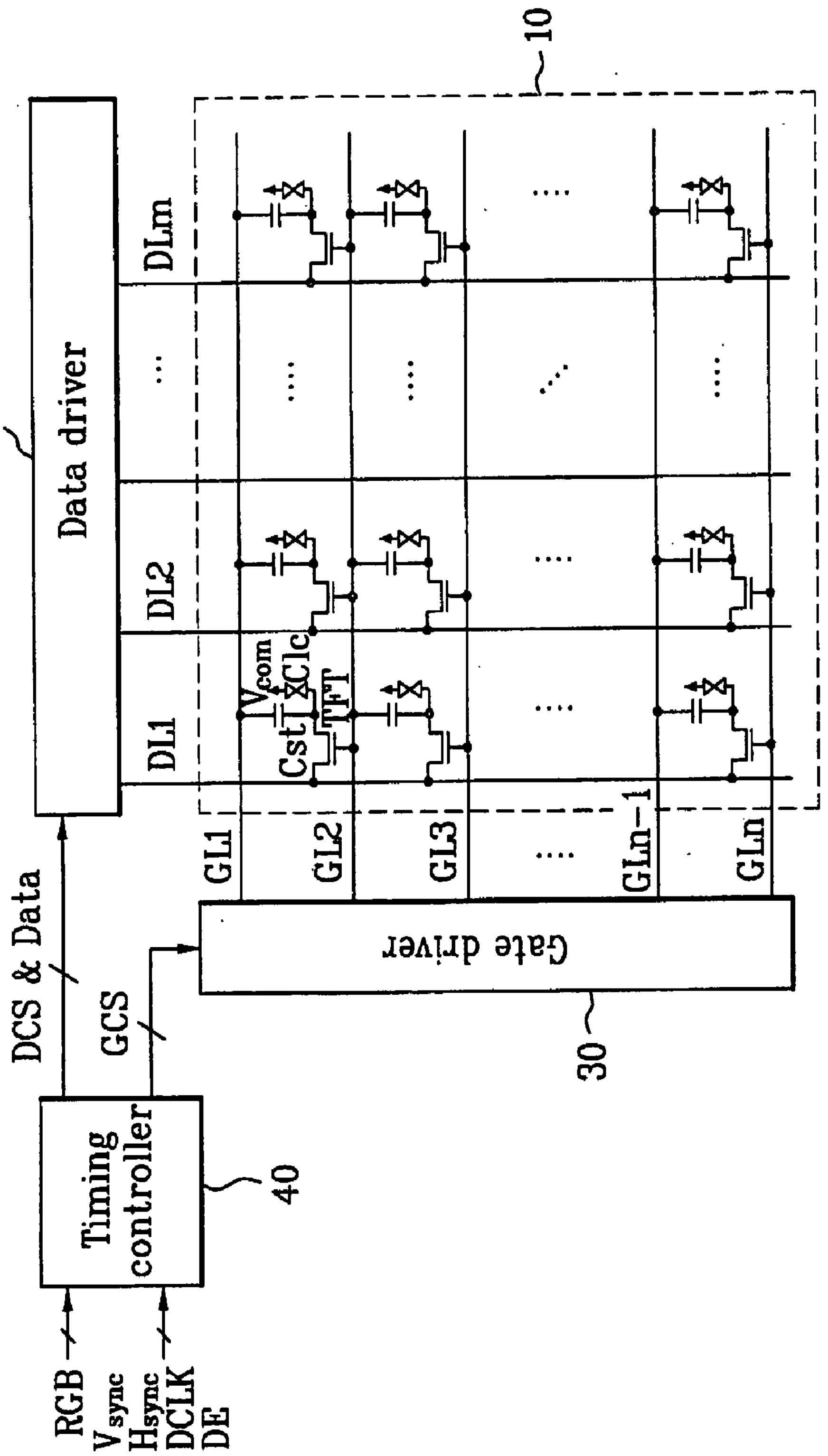


FIG. 2
Related Art

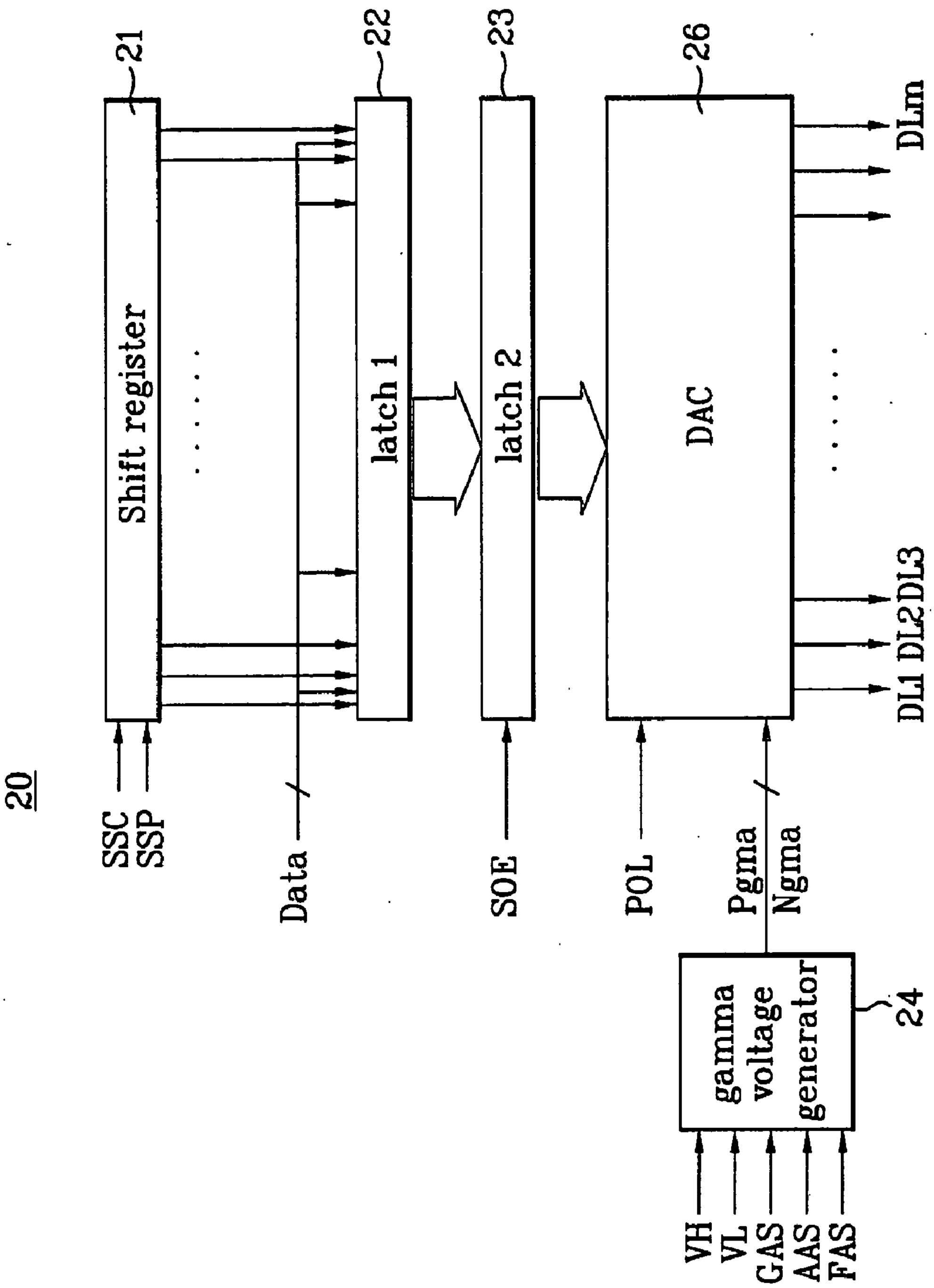


FIG. 3A
Related Art

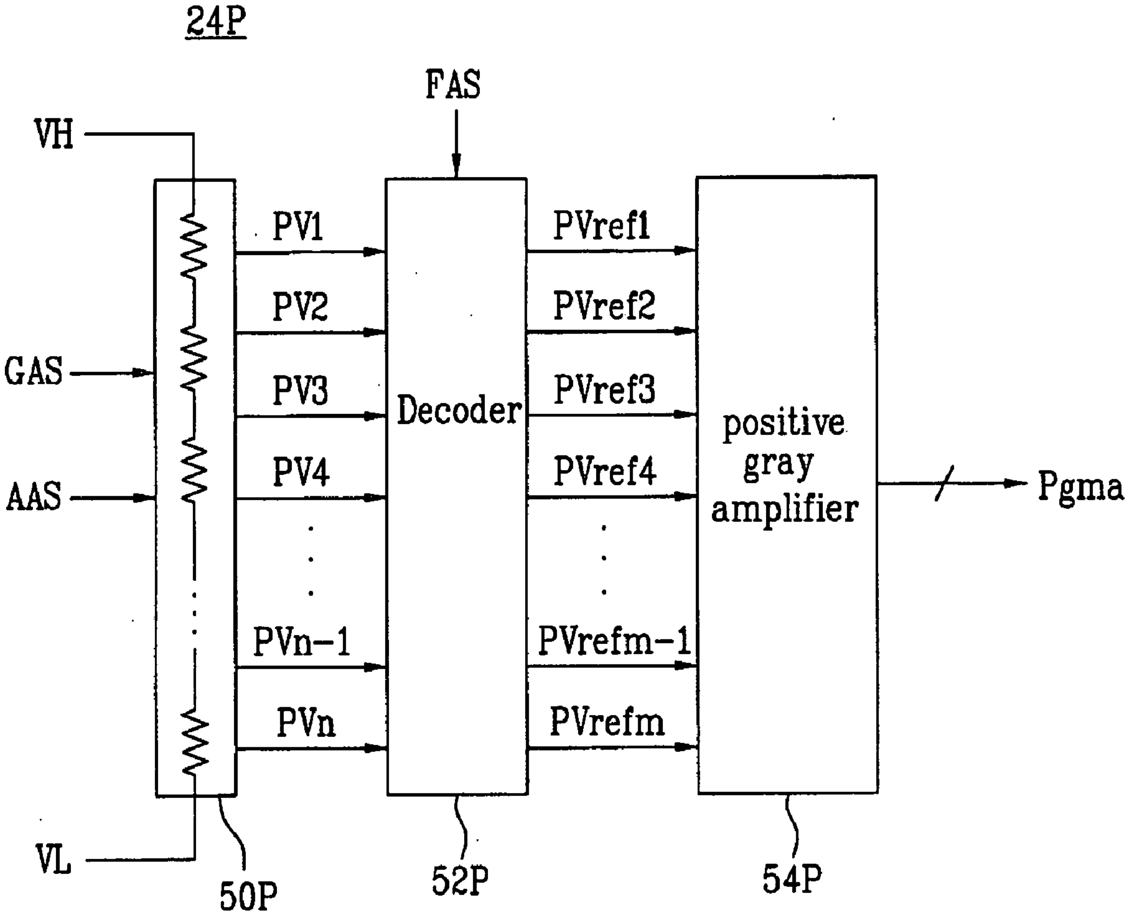


FIG. 3B

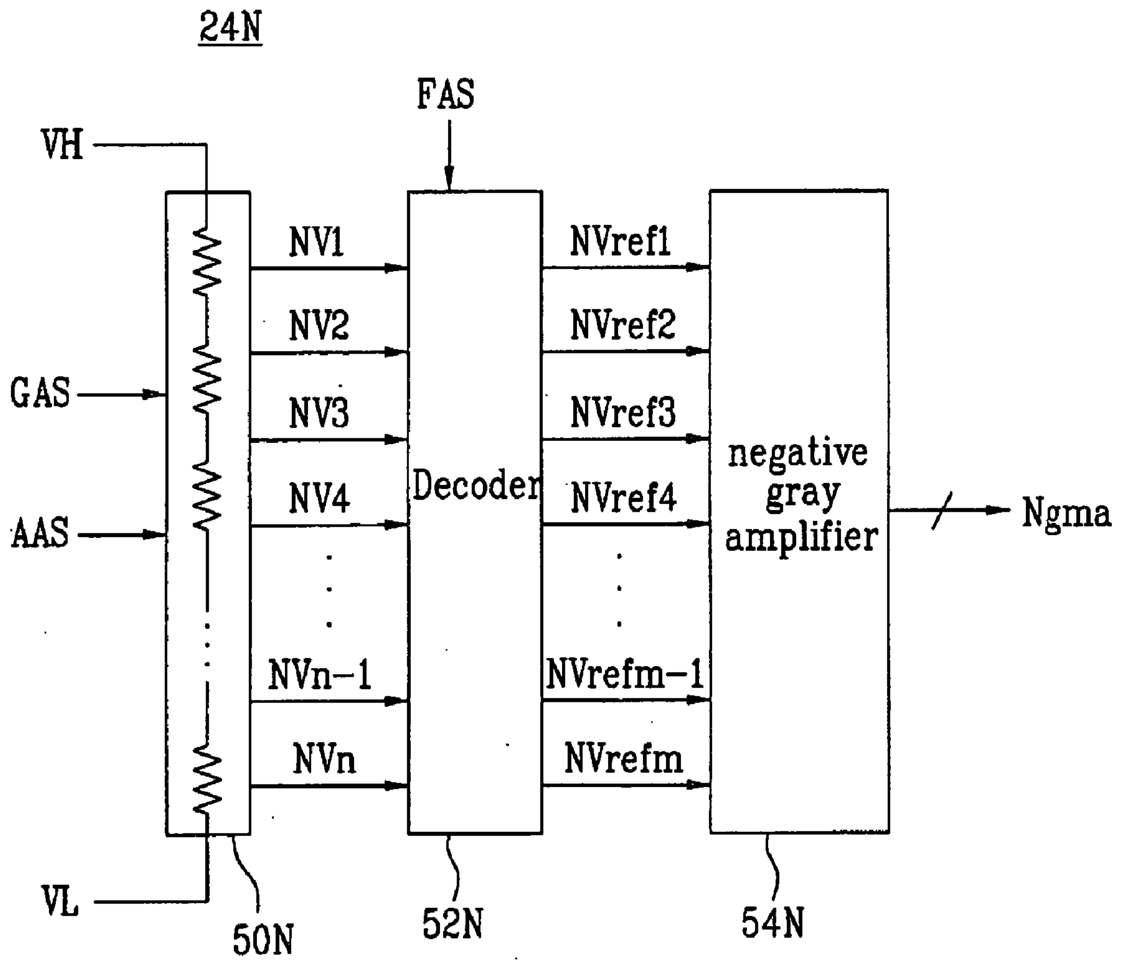

24N
FAS
VH
NV1
NV2
NV3
NV4
NVn-1
NVn
GAS
AAS
VL
Decoder
NVref1
NVref2
NVref3
NVref4
NVrefm-1
NVrefm
negative gray amplifier
Ngma
50N
52N
54N

FIG. 4

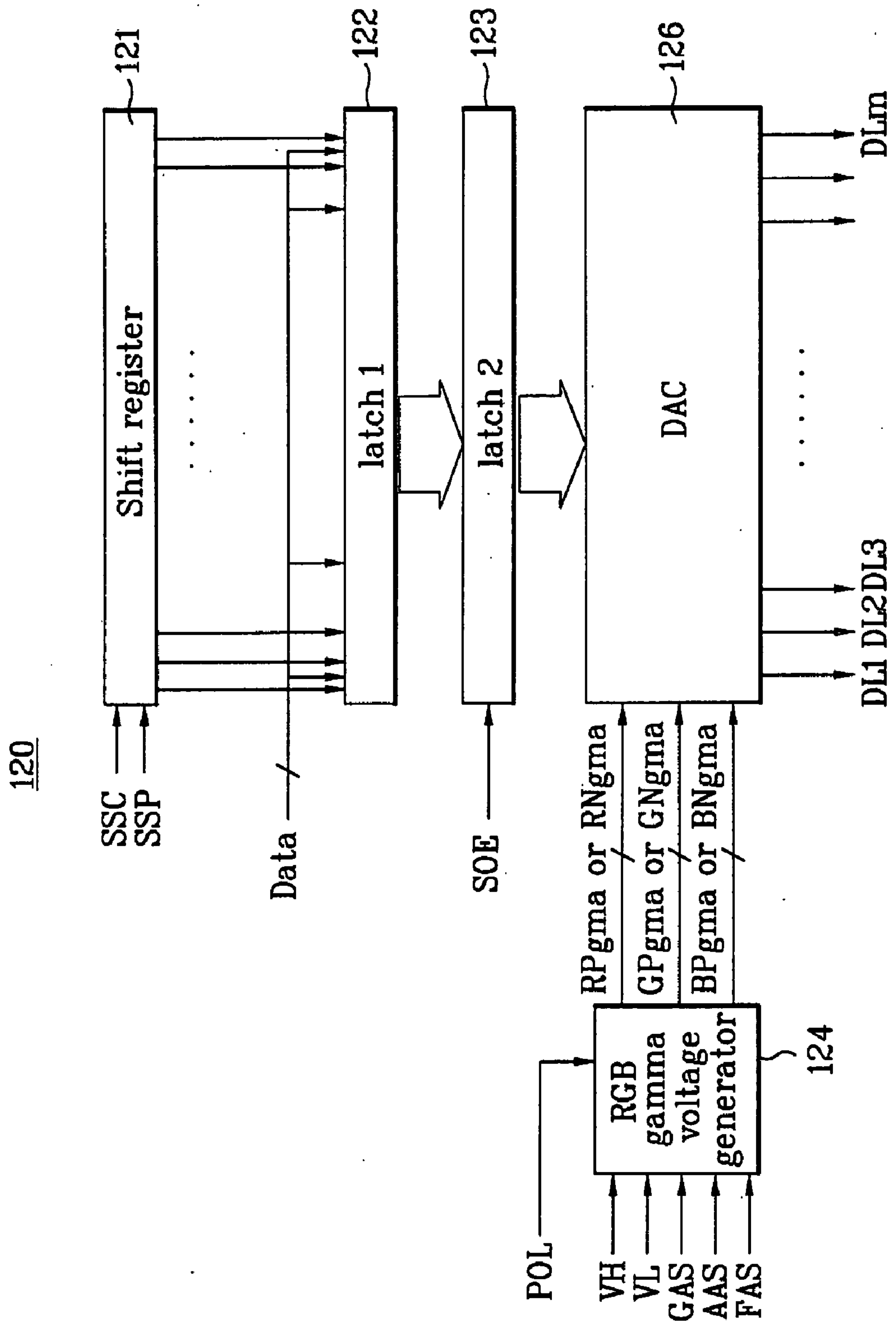
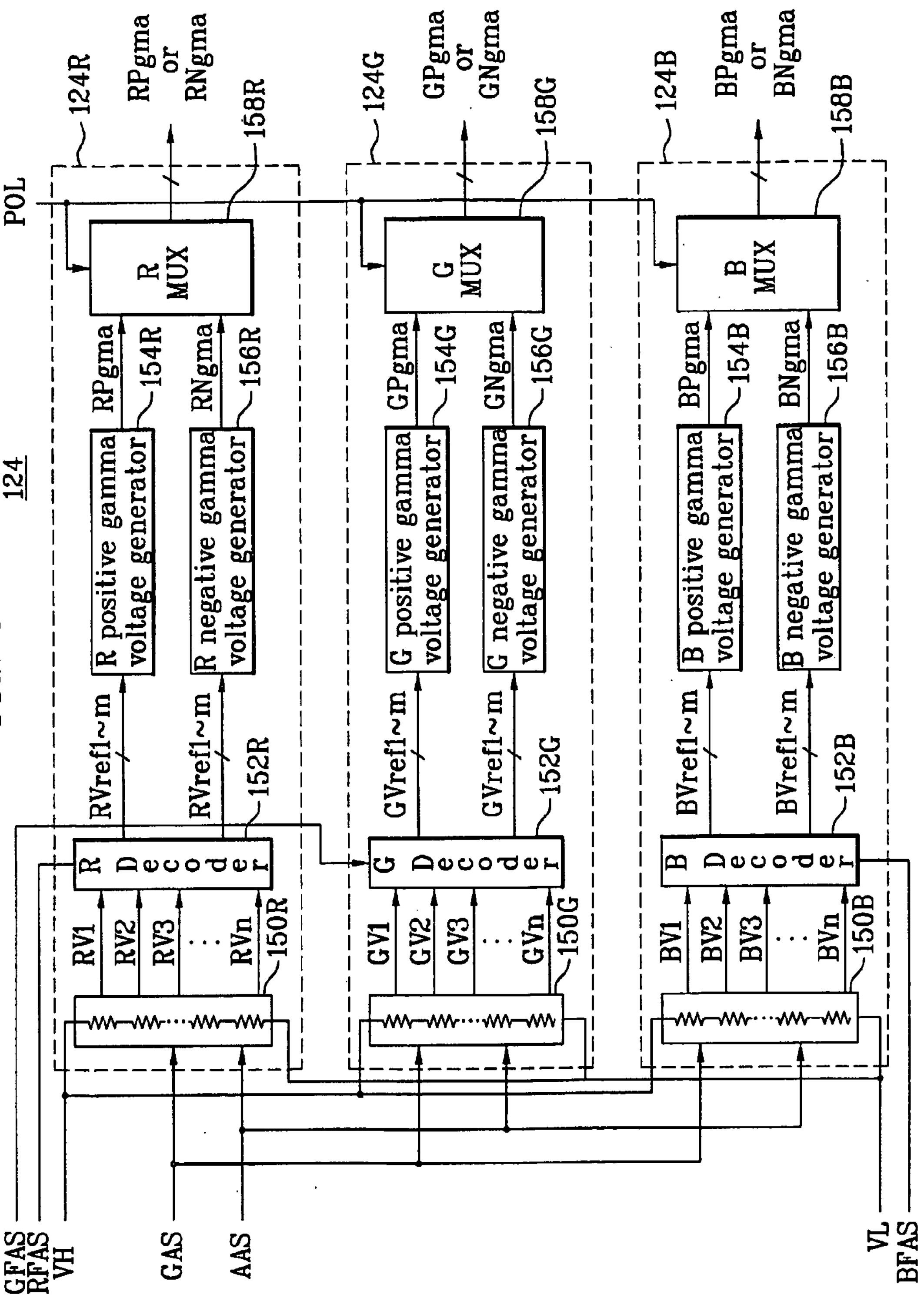

120
121
Shift register
SSC
SSP
122
latch 1
Data
123
latch 2
SOE
126
DAC
DLm
DL1 DL2 DL3
RPgma or RNgma
GPgma or GNgma
BPgma or BNgma
RGB gamma voltage generator
124
POL
VH
VL
GAS
AAS
FAS

FIG. 5


124
124R
124G
124B
POL
RPgma or RNgma
GPgma or GNgma
BPgma or BNgma
158R
158G
158B
R MUX
G MUX
B MUX
RPgma
RNgma
GPgma
GNgma
BPgma
BNgma
154R
156R
154G
156G
154B
156B
R positive gamma voltage generator
R negative gamma voltage generator
G positive gamma voltage generator
G negative gamma voltage generator
B positive gamma voltage generator
B negative gamma voltage generator
RVref1~m
GVref1~m
BVref1~m
152R
152G
152B
R Decoder
G Decoder
B Decoder
RV1
RV2
RV3
RVn
GV1
GV2
GV3
GVn
BV1
BV2
BV3
BVn
150R
150G
150B
GFAS
RFAS
VH
GAS
AAS
VL
BFAS

DATA DRIVER AND LIQUID CRYSTAL DISPLAY USING THE SAME

[0001] This application claims the benefit of the Korean Patent Application No. 2005-039729, filed on May 12, 2005, which is hereby incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a liquid crystal display, and more particularly, to a data driver and a liquid crystal display using the same which can improve the image quality. Although the present invention is suitable for a wide scope of applications, it is particularly suitable for adjusting chromaticity in a liquid crystal display.

[0004] 2. Discussion of the Related Art

[0005] In general, a liquid crystal display (LCD) generates images by controlling light transmittance of liquid crystal cells according to video signals. An active matrix liquid crystal display, which includes switching elements formed respectively in liquid crystal cells, is suitable to display moving images. Thin film transistors (TFT) are typically used as the switching elements in the active matrix liquid crystal display.

[0006] **FIG. 1** shows a schematic diagram of an apparatus for driving an LCD according to the related art. As shown in **FIG. 1**, the related art apparatus for driving an LCD includes an image display unit **10**, a data driver **20**, a gate driver **30**, and a timing controller **40**. The image display unit **10** includes liquid crystal cells formed in areas defined by gate lines GL**1** to GLn crossing data lines DL**1** to DLm. The data driver **20** supplies analog video signals to the data lines DL**1** to DLm. The gate driver **30** supplies scan pulses to the gate lines GL**1** to GLn. The timing controller **40** aligns externally provided source data RGB to supply aligned data to the data driver **20**, generates data control signals DCS to control the data driver **20**, and generates gate control signals GCS to control the gate driver **30**.

[0007] The image display unit **10** includes a transistor array substrate (not shown) and a color filter array substrate (not shown) that are affixed together. Spacers (not shown) maintain a cell gap between the two array substrates, and a liquid crystal (not shown) is filled into the gap provided by the spacers. Liquid crystal cells are formed respectively in areas defined by the n-th gate lines GL**1** to GLn crossing the m-th data lines DL**1** to DLm. Thin film transistors (TFTs) are connected the n-th gate lines GL**1** to GLn and the m-th data lines DL**1** to DLm in each of the liquid crystal cells. In response to scan pulses from the gate lines GL**1** to GLn, the TFTs provide data signals from the data lines DL**1** to DLm to the liquid crystal cells. Each of the liquid crystal cells includes a pixel electrode connected to a corresponding TFT and a common electrode, which face each other with a liquid crystal therebetween. Thus, each liquid crystal cell can be equivalently expressed as a liquid crystal capacitor Clc. Each liquid crystal cell also includes a storage capacitor Cst that is connected to a previous gate line to maintain a data signal with which the liquid crystal capacitor Clc is charged until the liquid crystal capacitor Clc is charged with a next data signal.

[0008] The timing controller **40** arranges source data RGB input from the outside so as to be suitable to drive the image display unit **10** and provides such arranged source data RGB to the data driver **20**. Using a main clock MCLK, a data enable signal DE, and horizontal and vertical synchronization signals Hsync and Vsync, the timing controller **40** generates a data control signal DCS and a gate control signal GCS to control the drive timings of the data driver **20** and the gate driver **30**.

[0009] The gate driver **30** includes a shift register that sequentially generates scan pulses (i.e., high gate pulses) in response to a gate start pulse GSP and a gate shift clock GSC included in the gate control signal GCS from the timing controller **40**. The gate driver **30** sequentially provides the high gate pulses to gate lines GL**1** to GLn in the image display unit **10** to turn on TFTs connected to the gate lines GL**1** to GLn.

[0010] The data driver **20** converts the arranged data signals Data from the timing controller **40** to analog video signals corresponding to the data control signal DCS received from the timing controller **40**. The data driver **20** provides the analog video signals, corresponding to a single horizontal line, to the data lines DL**1** to DLm every horizontal period during which a single scan pulse is provided. In response to a polarity control signal POL, the data driver **20** reverses the polarity of the analog video signals provided to the data line DL**1** to DLm on a line by line basis.

[0011] **FIG. 2** is a block diagram of the data driver shown in **FIG. 1**. As shown in **FIG. 2**, the data driver **20** includes a shift register **21**, a first latch **22**, a second latch **23**, a gamma voltage generator **24**, and a digital to analog converter (DAC) **26**. The shift register **21** generates sampling signals using a source shift clock SSC and a source start pulse SSP included in the data control signal DCS from the timing controller **40**. Specifically, the shift register **21** generates sampling signals by shifting the source start pulse SSP in response to the source shift clock SSC and sequentially provides the sampling signals to the first latch **22**. The first latch **22** sequentially samples the arranged data signals Data received from the timing controller **40** in response to the sampling signals from the shift register **21** and provides the sampled data signals to the second latch **23**. The second latch **23** stores the sampled data signals received from the first latch **22** on a line by line basis and simultaneously outputs the stored data signals, corresponding to a single line, to the DAC **26** in synchronization with a source output enable signal SOE included in the data control signal DCS.

[0012] **FIGS. 3A and 3B** illustrate the gamma voltage generator shown in **FIG. 2**. The gamma voltage generator **24** generates a plurality of positive gamma voltages Pgma and a plurality of negative (−) gamma voltages Ngma at voltage divider nodes between a plurality of resistors connected in series between first and second voltages VH and VL and provides the positive and negative gamma voltages Pgma and Ngma to the DAC **26**. To generate these voltages, the gamma voltage generator **24** includes a positive gamma voltage generator **24**P as shown in **FIG. 3A**, which generates a plurality of positive gamma voltages Pgma, and a negative gamma voltage generator **24**N as shown in **FIG. 3B**, which generates a plurality of negative (−) gamma voltages Ngma.

[0013] As shown in **FIG. 3A**, the positive gamma voltage generator **24**P includes a positive resistor set **50**P, a positive decoder **52**P, and a positive gray amplifier **54**P. The positive resistor set **50**P includes a plurality of resistors connected in series between the first and second voltages VH and VL and outputs n positive divided voltages PV1 to PVn using the resistors connected in series. The positive decoder **52**P decodes the n divided voltages PV1 to PVn received from the positive resistor set **50**P and outputs m positive reference gamma voltages PVref1 to PVrefm. The positive gray amplifier **54**P generates a plurality of positive gamma voltage Pgma using the m positive reference gamma voltages PVref1 to PVrefm output from the positive decoder **52**P.

[0014] The positive resistor set **50**P includes a plurality of resistors connected in series between a first voltage VH and a second voltage VL lower than the first voltage VH. The positive resistor set **50**P provides a plurality of different positive divided voltages PV1 to PVn, generated at the voltage divider nodes between the resistors through voltage division corresponding to resistances of the resistors, to the positive decoder **52**P. The positive resistor set **50**P adjusts the resistances of the resistors in response to a curve adjustment signal GAS and an amplitude adjustment signal AAS received from the outside, thereby adjusting a gamma curve and a gamma voltage amplitude.

[0015] The positive decoder **52**P decodes a plurality of positive divided voltages PV1 to PVn received from the positive resistor set **50**P in response to a fine adjustment signal FAS received from the outside and generates m positive reference gamma voltages PVref1 to PVrefm. To accomplish this, the positive decoder **52**P includes a plurality of decoders that generates m-**2** positive reference gamma voltages PVref2 to PVrefm-**1** except the highest and lowest positive reference gamma voltages PVref1 and PVrefm.

[0016] The positive gray amplifier **54**P further divides m positive reference gamma voltages PVref1 to PVrefin received from the positive decoder **52**P and generates a plurality of positive gamma voltages Pgma corresponding to gray levels of the data signals Data to be provided to the data driver **20**. The positive gray amplifier **54**P provides the positive gamma voltages Pgma to the DAC **26**, as shown in **FIG. 2**.

[0017] As shown in **FIG. 3B**, the negative gamma voltage generator **24**N includes a negative resistor set **50**N, a negative decoder **52**N, and a negative gray amplifier **54**N. The negative resistor set **50**N includes a plurality of resistors connected in series between the first and second voltages VH and VL and outputs n negative divided voltages NV1 to NVn using the resistors connected in series. The negative decoder **52**N decodes the n divided voltages NV1 to NVn received from the negative resistor set **50**N and outputs m negative reference gamma voltages NVref1 to NVrefm. The negative gray amplifier **54**N generates a plurality of negative gamma voltage Ngma using the m negative reference gamma voltages NVref1 to NVrefm output from the negative decoder **52**N.

[0018] The negative resistor set **50**N includes a plurality of resistors connected in series between a first voltage VH and a second voltage VL lower than the first voltage VH. The negative resistor set **50**N provides a plurality of different negative divided voltages NV1 to NVn, generated at the voltage divider nodes between the resistors through voltage division corresponding to resistances of the resistors, to the negative decoder **52**N. The negative resistor set **50**N adjusts the resistances of the resistors in response to a curve adjustment signal GAS and an amplitude adjustment signal AAS received from the outside, thereby adjusting the gamma curve and the gamma voltage amplitude.

[0019] The negative decoder **52**N decodes a plurality of negative divided voltages NV1 to NVn received from the negative resistor set **50**N in response to a fine adjustment signal FAS received from the outside and generates m negative reference gamma voltages NVref1 to NVrefm. To accomplish this, the negative decoder **52**N includes a plurality of decoders that generates m-**2** negative reference gamma voltages NVref2 to NVrefm-**1** except the highest and lowest negative reference gamma voltages NVref1 and NVrefm.

[0020] The negative gray amplifier **54**N further divides m negative reference gamma voltages NVref1 to NVrefm received from the negative decoder **52**N and generates a plurality of negative gamma voltages Ngma corresponding to gray levels of the data signals Data to be provided to the data driver **20**. The negative gray amplifier **54**N provides the negative gamma voltages Ngma to the DAC **26**, as shown in **FIG. 2**.

[0021] Using a plurality of positive gamma voltages Pgma and a plurality of negative gamma voltages Ngma received from the gamma voltage generator **24**, the DAC **26** converts data signals received from the second latch **23** to positive or negative analog video signals. The DAC **26** simultaneously outputs the analog video signals, corresponding to a single line, to the data lines DL1 to DLm. The DAC **26** generates positive or negative video signals in response to a polarity control signal POL included in the data control signal DCS from the timing controller **40**.

[0022] As described above, the related art data driver **20** performs digital to analog conversion using positive and negative gamma voltages Pgma and Ngma produced by a single positive resistor set **50**P and a single negative resistor set **50**N.

[0023] In the meantime, red R, green G, and blue B color filters are manufactured corresponding to chromaticity coordinates of red, green, and blue colors for the related art liquid crystal display. However, the related art liquid crystal display uses the same gamma voltage for the red, green, and blue liquid crystal cells despite that these cells have different electro-optical characteristics. Thus, the related art liquid crystal display cannot accomplish individual gamma voltages of red, green, and blue colors and cannot adjust individual chromaticity coordinates of red, green, and blue colors. In addition, R, G, and B color characteristics may vary slightly due to small variations in the common voltage during line-inversion operation of the image display unit **10** in the related art liquid crystal display, thereby reducing the image quality. Further, both the positive and negative gamma voltages Pgma and Ngma are provided to the DAC **26** in the related art liquid crystal display, thereby complicating the structure of the DAC **26** and increasing the size thereof.

SUMMARY OF THE INVENTION

[0024] Accordingly, the present invention is directed to a data driver and a liquid crystal display using the same that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[0025] An object of the present invention is to provide a data driver and a liquid crystal display using the same with improved image quality.

[0026] Another object of the present invention is to provide a data driver and a liquid crystal display using the same which can simplify the structure of a DA converter included in the data driver and reduce the size thereof.

[0027] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0028] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, a data driver includes: a gamma voltage generator that generates red, green, and blue gamma voltages according to red, green, and blue adjustment signals; and a digital to analog converter that converts the data signals received from a latch to positive or negative analog video signals using the red, green, and blue positive gamma voltages or red, green, and blue negative gamma voltages received from the gamma voltage generator.

[0029] In another aspect, a data driver includes: a shift register that generates sampling signals using a shift clock and a start pulse; a latch that sequentially samples data signals, received from the outside, in response to the sampling signals; a gamma voltage generator that generates red, green, and blue positive gamma voltages and red, green, and blue negative gamma voltages and selectively outputs the red, green, and blue positive gamma voltages or the red, green, and blue negative gamma voltages according to a polarity control signal; and a digital to analog converter that converts the data signals received from the latch to positive or negative analog video signals using the red, green, and blue positive gamma voltages or the red, green, and blue negative gamma voltages received from the gamma voltage generator.

[0030] In another aspect, a liquid crystal display includes: an image display unit that displays images by controlling light transmittance of liquid crystal cells provided in areas defined by gate and data lines crossing each other; a gate driver supplying scan pulses to the gate lines; a data driver supplying positive or negative analog video signals to the data lines; and a timing controller supplying data signals to the data driver and controls drive timings of the data driver and the gate driver, wherein the data driver includes: a shift register that generates sampling signals using a shift clock and a start pulse; a latch that sequentially samples the data signals, received from the timing controller, according to the sampling signals; an gamma voltage generator that generates red, green, and blue positive gamma voltages and red, green, and blue negative gamma voltages and selectively outputs the red, green, and blue positive gamma voltages or red, green, and blue negative gamma voltages according to a polarity control signal; and a digital to analog converter that converts the sampled data signals received from the latch to the positive or negative analog video signals using the red, green, and blue positive gamma voltages or the red, green, and the blue negative gamma voltages received from the gamma voltage generator.

[0031] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0033] **FIG. 1** shows a schematic diagram of an apparatus for driving an LCD according to the related art;

[0034] **FIG. 2** is a block diagram of the data driver shown in **FIG. 1**;

[0035] **FIGS. 3A and 3B** illustrate the gamma voltage generator shown in **FIG. 2**;

[0036] **FIG. 4** is a block diagram of a data driver according to an embodiment of the present invention; and

[0037] **FIG. 5** is a block diagram of the RGB gamma voltage generator shown in **FIG. 4**.

DETAILED DESCRIPTION OF THE INVENTION

[0038] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0039] **FIG. 4** is a block diagram of a data driver in a liquid crystal display according to an embodiment of the present invention. Components, other than the data driver, of the liquid crystal display in the embodiment of the present invention are similar to those of the conventional liquid crystal display shown in **FIG. 1**. Thus, a description of the components, other than the data driver, of the liquid crystal display in the embodiment of the present invention is replaced with the description of those of the related art liquid crystal display shown in **FIG. 1**.

[0040] As shown in **FIG. 4**, the data driver **120** according to the embodiment of the present invention includes a shift register **121**, a first latch **122**, a second latch **123**, an RGB gamma voltage generator **124**, and a digital to analog converter (DAC) **126**. The shift register **121** generates sampling signals using a source shift clock SSC and a source start pulse SSP. The first latch **122** sequentially samples data signals Data input from the outside in response to the sampling signals. The second latch **123** simultaneously outputs the data signals sampled by the first latch **122**, which correspond to a single line, according to a source output enable signal SOE. The RGB gamma voltage generator **124** generates RGB positive gamma voltages (RPgma, GPgma, and BPgma) and RGB negative gamma voltages (RNgma, GNgma, and BNgma) and selectively outputs the RGB positive gamma voltages (RPgma, GPgma, and BPgma) or the RGB negative gamma voltages (RNgma, GNgma, and BNgma) according to a polarity control signal POL. Using the RGB positive gamma voltages (RPgma, GPgma, and BPgma) or the RGB negative gamma voltages (RNgma, GNgma, and BNgma) from the RGB gamma voltage generator **124**, the DAC **126** converts the data signals Data corresponding to a single line, received from the second latch **123**, to positive or negative analog video signals. The shift register **121** generates sampling signals using a source shift clock SSC and a source start pulse SSP from a timing controller (not shown). Specifically, the shift register **121** generates sampling signals by shifting the source start pulse SSP in response to the source shift clock SSC and sequentially provides the sampling signals to the first latch **122**. The following is a more detailed description of the data driver **120** shown in **FIG. 4**.

[0041] The first latch **122** sequentially samples arranged data signals Data, received from the timing controller through data bus lines, in response to the sampling signals from the shift register **121** and then provides the sampled data signals to the second latch **123**.

[0042] The second latch **123** stores the sampled data signals received from the first latch **122** on a line by line basis and simultaneously outputs the stored data signals Data, corresponding to a single line, to the DAC **126** in synchronization with the source output enable signal SOE.

[0043] The RGB gamma voltage generator **124** generates a plurality of RGB positive gamma voltages (RPgma, RPgma, and RPgma) and a plurality of RGB negative gamma voltages (RNgma, GNgma, and BNgma) at voltage divider nodes between a plurality of resistors connected in series between first and second voltages VH and VL and selectively provides the plurality of RGB positive gamma voltages RPgma, RPgma, and RPgma or the plurality of RGB negative gamma voltages RNgma, GNgma, and BNgma to the DA converter **124** according to the polarity control signal POL. Here, the polarity control signal POL is reversed for each single horizontal line.

[0044] **FIG. 5** is a block diagram of the RGB gamma voltage generator shown in **FIG. 4**. As shown in **FIG. 5**, the RGB gamma voltage generator **124** includes a red gamma voltage generator **124**R that generates red R positive and negative gamma voltages RPgma and RNgma, a green gamma voltage generator **124**G that generates green G positive and negative gamma voltages GPgma and GNgma, and a blue gamma voltage generator **124**B that generates blue B positive and negative gamma voltages BPgma and BNgma.

[0045] The red gamma voltage generator **124**R includes a red resistor set **150**R, a red decoder **152**R, a red positive gamma voltage generator **154**R, a red negative gamma voltage generator **156**R, and a red multiplexer **158**R.

[0046] The red resistor set **150**R includes a plurality of red resistors connected in series between the first and second voltages VH and VL and generates n red R divided voltages RV**1** to RVn using the red resistors connected in series. The red resistor set **150**R provides n different R divided voltages RV**1** to RVn, generated at voltage divider nodes between the R resistors through voltage division corresponding to resistances of the resistors, to the red decoder **152**R. The red resistor set **150**R adjusts the resistances of the red resistors according to a curve adjustment signal GAS and an amplitude adjustment signal AAS received from the outside, thereby adjusting a gamma curve and a gamma voltage amplitude.

[0047] The red decoder **152**R decodes n red divided voltages RV**1** to RVn received from the red resistor set **150**R according to a red fine adjustment signal RFAS received from the outside and generates m red reference gamma voltages RVref**1** to RVrefm. To accomplish this, the red decoder **152**R includes a plurality of decoders that generates m-**2** red reference gamma voltages RVref**2** to RVrefm-**1** except the highest and lowest red reference gamma voltages RVref**1** and RVrefm.

[0048] The red positive gamma voltage generator **154**R further divides m red reference gamma voltages RVref**1** to RVrefm received from the red decoder **152**R and generates a plurality of red positive gamma voltages RPgma corresponding to gray levels of the data signals Data. The red positive gamma voltage generator **154**R provides the red positive gamma voltages RPgma to the red multiplexer **158**R.

[0049] The red negative gamma voltage generator **156**R further divides m red reference gamma voltages RVref**1** to RVrefm received from the red decoder **152**R and generates a plurality of red negative gamma voltages RNgma corresponding to gray levels of the data signals Data. The red negative gamma voltage generator **156**R provides the red negative gamma voltages RNgma to the red multiplexer **158**R.

[0050] The red multiplexer **158**R selectively provides the plurality of red positive gamma voltages RPgma or the plurality of red negative gamma voltages RNgma to the DAC **126** according to the polarity control signal POL. To accomplish this, the red multiplexer **158**R includes a plurality of multiplexers (not shown). When the polarity control signal POL is high, the red multiplexer **158**R provides the plurality of red positive gamma voltages RPgma to the DAC **126**, as shown in **FIG. 4**. When the polarity control signal POL is low, the red multiplexer **158**R provides the plurality of red negative gamma voltages RNgma to the DAC **126**.

[0051] The green gamma voltage generator **124**G includes a green resistor set **150**G, a green decoder **152**G, a green positive gamma voltage generator **154**G, a green negative gamma voltage generator **156**G, and a green multiplexer **158**G.

[0052] The green resistor set **150**G includes a plurality of green resistors connected in series between the first and second voltages VH and VL and generates n green G divided voltages GV**1** to GVn using the green resistors connected in series. The green resistor set **150**G provides n different G divided voltages GV**1** to GVn, generated at voltage divider nodes between the G resistors through voltage division corresponding to resistances of the green resistors, to the green decoder **152**G. The green resistor set **150**G adjusts the resistances of the resistors according to the curve adjustment signal GAS and the amplitude adjustment signal AAS received from the outside, thereby adjusting the gamma curve and the gamma voltage amplitude.

[0053] The green decoder **152**G decodes n green divided voltages GV**1** to GVn received from the green resistor set **150**G according to a green fine adjustment signal GFAS received from the outside and generates m green reference gamma voltages GVref**1** to GVrefm. To accomplish this, the green decoder **152**G includes a plurality of decoders that generates m-**2** green reference gamma voltages GVref**2** to GVrefm-**1** except the highest and lowest green reference gamma voltages GVref**1** and GVrefm.

[0054] The green positive gamma voltage generator **154**G further divides m green reference gamma voltages GVref**1** to GVrefm received from the green decoder **152**G and generates a plurality of green positive gamma voltages GPgma corresponding to gray levels of the data signals Data. The green positive gamma voltage generator **154**G provides the green positive gamma voltages GPgma to the green multiplexer **158**G.

[0055] The green negative positive gamma voltage generator **156**G further divides m green reference gamma voltages GVref**1** to GVrefm received from the green decoder **152**G and generates a plurality of green negative gamma voltages GNgma corresponding to gray levels of the data signals Data. The green negative gamma voltage generator **156**G provides the green negative gamma voltages GNgma to the green multiplexer **158**G.

[0056] The green multiplexer **158**G selectively provides the plurality of green positive gamma voltages GPgma or the plurality of green negative gamma voltages GNgma to the DAC **126** according to the polarity control signal POL. To accomplish this, the green multiplexer **158**G includes a plurality of multiplexers (not shown). When the polarity control signal POL is high, the green multiplexer **158**G provides the plurality of green positive gamma voltages GPgma to the DAC **126**, as shown in **FIG. 4**. When the polarity control signal POL is low, the green multiplexer **158**G provides the plurality of green negative gamma voltages GNgma to the DAC **126**.

[0057] The blue gamma voltage generator **124**B includes a blue resistor set **150**B, a blue decoder **152**B, a blue positive gamma voltage generator **154**B, a blue negative gamma voltage generator **156**B, and a blue multiplexer **158**B.

[0058] The blue resistor set **150**B includes a plurality of blue resistors connected in series between the first and second voltages VH and VL and generates n blue B divided voltages BV**1** to BVn using the blue resistors connected in series. The blue resistor set **150**B provides n different B divided voltages BV**1** to BVn, generated at voltage divider nodes between the B resistors through voltage division corresponding to resistances of the resistors, to the blue decoder **152**B. The blue resistor set **150**B adjusts the resistances of the resistors according to the curve adjustment signal GAS and the amplitude adjustment signal AAS received from the outside, thereby adjusting the gamma curve and the gamma voltage amplitude.

[0059] The blue decoder **152**B decodes n blue divided voltages BV**1** to BVn received from the blue resistor set **150**B according to a blue fine adjustment signal BFAS received from the outside and generates m blue reference gamma voltages BVref**1** to BVrefm. To accomplish this, the blue decoder **152**B includes a plurality of decoders that generates m-**2** blue reference gamma voltages BVref**2** to BVrefm-**1** except the highest and lowest blue reference gamma voltages BVref**1** and BVrefm.

[0060] The blue positive gamma voltage generator **154**B further divides m blue reference gamma voltages BVref**1** to BVrefm received from the blue decoder **152**B and generates a plurality of blue positive gamma voltages BPgma corresponding to gray levels of the data signals Data. The blue positive gamma voltage generator **154**B provides the blue positive gamma voltages BPgma to the blue multiplexer **158**B.

[0061] The blue negative gamma voltage generator **156**B further divides m blue reference gamma voltages BVref**1** to BVrefm received from the blue decoder **152**B and generates a plurality of blue negative gamma voltages BNgma corresponding to gray levels of the data signals Data. The blue negative gamma voltage generator **156**B provides the blue negative gamma voltages BNgma to the blue multiplexer **158**B.

[0062] The blue multiplexer **158**B selectively provides the plurality of blue positive gamma voltages BPgma or the plurality of blue negative gamma voltages BNgma to the DAC **126** according to the polarity control signal POL. To accomplish this, the blue multiplexer **158**B includes a plurality of multiplexers (not shown). When the polarity control signal POL is high, the blue multiplexer **158**B provides the plurality of blue positive gamma voltages BPgma to the DAC **126**, as shown in **FIG. 4**. When the polarity control signal POL is low, the blue multiplexer **158**B provides the plurality of blue negative gamma voltages BNgma to the DAC **126**, as shown in **FIG. 4**.

[0063] The DAC **126** converts the data signals Data received from the second latch **123** to positive or negative analog video signals using the plurality of RGB positive gamma voltages (RPgma, GPgma, and BPgma) or RGB negative gamma voltages (RNgma, GNgma, and BNgma) received from the RGB gamma voltage generator **124** according to the polarity control signal POL. The DAC **126** simultaneously outputs the positive or negative analog video signals, corresponding to a single line, to the data lines DL1 to DLm.

[0064] When the DAC **126** receives the plurality of R, G, and B positive gamma voltages RPgma, GPgma, and BPgma from the RGB gamma voltage generator **124** according to the polarity control signal POL, the DAC **126** converts the data signals Data, received from the second latch **123**, to RGB positive analog video signals using the plurality of R, G, and B positive gamma voltages (RPgma, GPgma, and BPgma). When the DAC **126** receives the plurality of R, G, and B negative gamma voltages (RNgma, GNgma, and BNgma) from the RGB gamma voltage generator **124** according to the polarity control signal POL, the DAC **126** converts the data signals Data, received from the second latch **123**, to RGB negative analog video signals using the plurality of R, G, and B negative gamma voltages (RNgma, GNgma, and BNgma). Thus, the data driver **120** according to the embodiment of the present invention converts the digital data signals to analog video signals using individual gamma voltages of red, green, and blue colors. Accordingly, the data driver **120** can adjust individual chromaticity coordinates of red, green, and blue colors through individual gamma voltages of red, green, and blue colors. The data driver **120** according to the embodiment of the present invention can be used to provide analog video signals to small-size liquid crystal displays, such as mobile communication terminals or the like.

[0065] As is apparent from the above description, embodiments of the present invention provides a data driver and a liquid crystal display using the same, which converts digital data signals to analog video signals using individual gamma voltages of red, green, and blue colors so that individual chromaticity coordinates of red, green, and blue colors can be adjusted through individual gamma voltages of red, green, and blue colors, and which also minimizes a reduction in the image quality caused by small variations in the common voltage. In addition, since RGB positive or negative gamma voltages are selectively provided to a DAC according to a polarity control signal, the structure of the DAC is simplified and the size thereof is reduced.

[0066] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

What is claimed is:

1. A data driver comprising:

a gamma voltage generator that generates red, green, and blue gamma voltages according to red, green, and blue adjustment signals; and

a digital to analog converter that converts data signals received from a latch to positive or negative analog video signals using the red, green, and blue gamma voltages received from the gamma voltage generator.

2. The data driver of claim 1, wherein the gamma voltage generator generates red, green, and blue positive gamma voltages and red, green, and blue negative gamma voltages according to the red, green, and blue adjustment signals and selectively outputs the red, green, and blue positive gamma voltages or the red, green, and blue negative gamma voltages according to a polarity control signal.

3. The data driver of claim 1, further comprising:

a shift register that generates sampling signals using a shift clock and a start pulse; and

a latch that sequentially samples data signals, received from the outside, in response to the sampling signals and provides the sampled data signals to the digital to analog converter.

4. The data driver of claim 1, wherein the gamma voltage generator includes:

a red gamma voltage generator connected between first and second voltages different from each other, the red gamma voltage generator generating the red positive gamma voltage and the red negative gamma voltage according to the red adjustment signal, and selectively outputting the red positive gamma voltage or red negative gamma voltage in response to a polarity control signal;

a green gamma voltage generator connected between first and second voltages different from each other, the green gamma voltage generator generating the green positive gamma voltage and the green negative gamma voltage according to the green adjustment signal, and selectively outputting the green positive gamma voltage or green negative gamma voltage in response to the polarity control signal; and

a blue gamma voltage generator connected between first and second voltages different from each other, the blue gamma voltage generator generating the blue positive gamma voltage and the blue negative gamma voltage according to the blue adjustment signal, and selectively outputting the blue positive gamma voltage or blue negative gamma voltage in response to the polarity control signal.

5. The data driver of claim 4, wherein the red gamma voltage generator includes:

a red resistor set including a plurality of red resistors that are connected in series between the first and second voltages and are used to generate n red divided voltages;

a red decoder that decodes the n red divided voltages received from the red resistor set and generates m red reference gamma voltages according to the red adjustment signal;

a red positive gamma voltages generator that further divides the m red reference gamma voltages received from the red decoder and generates a plurality of red positive gamma voltages corresponding to gray levels of the data signals;

a red negative gamma voltages generator that further divides the m red reference gamma voltages received from the red decoder and generates a plurality of red negative gamma voltages corresponding to the gray levels of the data signals; and

a red multiplexer that selectively outputs the plurality of red positive gamma voltages or the plurality of red negative gamma voltages to the digital to analog converter in response to the polarity control signal.

6. The data driver of claim 4, wherein the green gamma voltage generator includes:

a green resistor set including a plurality of green resistors that are connected in series between the first and second voltages and are used to generate n green divided voltages;

a green decoder that decodes the n green divided voltages received from the green resistor set and generates m green reference gamma voltages according to the green adjustment signal;

a green positive gamma voltages generator that further divides the m green reference gamma voltages received from the green decoder and generates a plurality of green positive gamma voltages corresponding to gray levels of the data signals;

a green negative gamma voltages generator that further divides the m green reference gamma voltages received from the green decoder and generates a plurality of green negative gamma voltages corresponding to the gray levels of the data signals; and

a green multiplexer that selectively outputs the plurality of green positive gamma voltages or the plurality of green negative gamma voltages to the digital to analog converter in response to the polarity control signal.

7. The data driver of claim 4, wherein the blue gamma voltage generator includes:

a blue resistor set including a plurality of blue resistors that are connected in series between the first and second voltages and are used to generate n blue divided voltages;

a blue decoder that decodes the n blue divided voltages received from the blue resistor set and generates m blue reference gamma voltages according to the blue adjustment signal;

a blue positive gamma voltages generator that further divides the m blue reference gamma voltages received from the blue decoder and generates a plurality of blue positive gamma voltages corresponding to gray levels of the data signals;

a blue negative gamma voltages generator that further divides the m blue reference gamma voltages received from the blue decoder and generates a plurality of blue negative gamma voltages corresponding to the gray levels of the data signals; and

a blue multiplexer that selectively outputs the plurality of blue positive gamma voltages or the plurality of blue negative gamma voltages to the digital to analog converter according to the polarity control signal.

8. A data driver comprising:

a shift register that generates sampling signals using a shift clock and a start pulse;

a latch that sequentially samples data signals, received from the outside, in response to the sampling signals;

a gamma voltage generator that generates red, green, and blue positive gamma voltages and red, green, and blue negative gamma voltages and selectively outputs the red, green, and blue positive gamma voltages or the red, green, and blue negative gamma voltages according to a polarity control signal; and

a digital to analog converter that converts the data signals received from the latch to positive or negative analog video signals using the red, green, and blue positive gamma voltages or the red, green, and blue negative gamma voltages received from the gamma voltage generator.

9. The data driver of claim 8, wherein the gamma voltage generator includes:

a red gamma voltage generator connected between first and second voltages different from each other, the red gamma voltage generator generating the red positive gamma voltage and the red negative gamma voltage, and selectively outputting the red positive gamma voltage or red negative gamma voltage in response to the polarity control signal;

a green gamma voltage generator connected between first and second voltages different from each other, the green gamma voltage generator generating the green positive gamma voltage and the green negative gamma voltage, and selectively outputting the green positive gamma voltage or green negative gamma voltage in response to the polarity control signal; and

a blue gamma voltage generator connected between first and second voltages different from each other, the blue gamma voltage generator generating the blue positive gamma voltage and the blue negative gamma voltage, and selectively outputting the blue positive gamma voltage or blue negative gamma voltage in response to the polarity control signal.

10. The data driver of claim 9, wherein the red gamma voltage generator includes:

a red resistor set including a plurality of red resistors that are connected in series between the first and second voltages and are used to generate n red divided voltages;

a red decoder that decodes the n red divided voltages received from the red resistor set and generates m red reference gamma voltages;

a red positive gamma voltages generator that further divides the m red reference gamma voltages received from the red decoder and generates a plurality of red positive gamma voltages corresponding to gray levels of the data signals;

a red negative gamma voltages generator that further divides the m red reference gamma voltages received from the red decoder and generates a plurality of red negative gamma voltages corresponding to the gray levels of the data signals; and

a red multiplexer that selectively outputs the plurality of red positive gamma voltages or the plurality of red negative gamma voltages to the digital to analog converter in response to the polarity control signal.

11. The data driver of claim 10, wherein the red decoder generates the m red reference gamma voltages according to a red adjustment signal.

12. The data driver of claim 9, wherein the green gamma voltage generator includes:

a green resistor set including a plurality of green resistors that are connected in series between the first and second voltages and are used to generate n green divided voltages;

a green decoder that decodes the n green divided voltages received from the green resistor set and generates m green reference gamma voltages;

a green positive gamma voltages generator that further divides the m green reference gamma voltages received from the green decoder and generates a plurality of green positive gamma voltages corresponding to gray levels of the data signals;

a green negative gamma voltages generator that further divides the m green reference gamma voltages received from the green decoder and generates a plurality of green negative gamma voltages corresponding to the gray levels of the data signals; and

a green multiplexer that selectively outputs the plurality of green positive gamma voltages or the plurality of green negative gamma voltages to the digital to analog converter in response to the polarity control signal.

13. The data driver of claim 12, wherein the green decoder generates the m green reference gamma voltages according to a green adjustment signal.

14. The data driver of claim 9, wherein the blue gamma voltage generator includes:

a blue resistor set including a plurality of blue resistors that are connected in series between the first and second voltages and are used to generate n blue divided voltages;

a blue decoder that decodes the n blue divided voltages received from the blue resistor set and generates m blue reference gamma voltages;

a blue positive gamma voltages generator that further divides the m blue reference gamma voltages received from the blue decoder and generates a plurality of blue positive gamma voltages corresponding to gray levels of the data signals;

a blue negative gamma voltages generator that further divides the m blue reference gamma voltages received from the blue decoder and generates a plurality of blue negative gamma voltages corresponding to the gray levels of the data signals; and

a blue multiplexer that selectively outputs the plurality of blue positive gamma voltages or the plurality of blue negative gamma voltages to the digital to analog converter according to the polarity control signal.

15. The data driver of claim 14, wherein the blue decoder generates the m blue reference gamma voltages according to a blue adjustment signal.

16. A liquid crystal display comprising:

an image display unit that displays images by controlling light transmittance of liquid crystal cells provided in areas defined by gate and data lines crossing each other;

a gate driver supplying scan pulses to the gate lines;

a data driver supplying positive or negative analog video signals to the data lines; and

a timing controller supplying data signals to the data driver and controls drive timings of the data driver and the gate driver,

wherein the data driver includes:

a shift register that generates sampling signals using a shift clock and a start pulse;

a latch that sequentially samples the data signals, received from the timing controller, according to the sampling signals;

an gamma voltage generator that generates red, green, and blue positive gamma voltages and red, green, and blue negative gamma voltages and selectively outputs the red, green, and blue positive gamma voltages or red, green, and blue negative gamma voltages according to a polarity control signal; and

a digital to analog converter that converts the sampled data signals received from the latch to the positive or negative analog video signals using the red, green, and blue positive gamma voltages or the red, green, and the blue negative gamma voltages received from the gamma voltage generator.

17. The liquid crystal display of claim 16, wherein the gamma voltage generator includes:

a red gamma voltage generator connected between first and second voltages different from each other, the red gamma voltage generator generating the red positive gamma voltage and the red negative gamma voltage, and selectively outputting the red positive gamma voltage or the red negative gamma voltage in response to the polarity control signal;

a green gamma voltage generator connected between first and second voltages different from each other, the green gamma voltage generator generating the green positive gamma voltage and the green negative gamma voltage, and selectively outputting the green positive gamma voltage or the green negative gamma voltage in response to the polarity control signal; and

a red gamma voltage generator connected between first and second voltages different from each other, the red gamma voltage generator generating the red positive gamma voltage and the red negative gamma voltage, and selectively outputting the red positive gamma voltage or the red negative gamma voltage in response to the polarity control signal.

18. The liquid crystal display of claim 17, wherein the red gamma voltage generator includes:

a red resistor set including a plurality of red resistors that are connected in series between the first and second voltages and are used to generate n red divided voltages;

a red decoder that decodes the n red divided voltages received from the red resistor set and generates m red reference gamma voltages;

a red positive gamma voltages generator that further divides the m red reference gamma voltages received from the red decoder and generates a plurality of red positive gamma voltages corresponding to gray levels of the data signals;

a red negative gamma voltages generator that further divides the m red reference gamma voltages received from the red decoder and generates a plurality of red negative gamma voltages corresponding to the gray levels of the data signals; and

a red multiplexer that selectively outputs the plurality of red positive gamma voltages or the plurality of red negative gamma voltages to the digital to analog converter in response to the polarity control signal.

19. The liquid crystal display of claim 17, wherein the green gamma voltage generator includes:

a green resistor set including a plurality of green resistors that are connected in series between the first and second voltages and are used to generate n green divided voltages;

a green decoder that decodes the n green divided voltages received from the green resistor set and generates m green reference gamma voltages;

a green positive gamma voltages generator that further divides the m green reference gamma voltages received from the green decoder and generates a plurality of green positive gamma voltages corresponding to gray levels of the data signals;

a green negative gamma voltages generator that further divides the m green reference gamma voltages received from the green decoder and generates a plurality of green negative gamma voltages corresponding to the gray levels of the data signals; and

a green multiplexer that selectively outputs the plurality of green positive gamma voltages or the plurality of green negative gamma voltages to the digital to analog converter in response to the polarity control signal.

20. The liquid crystal display of claim 17, wherein the blue gamma voltage generator includes:

a blue resistor set including a plurality of blue resistors that are connected in series between the first and second voltages and are used to generate n blue divided voltages;

a blue decoder that decodes the n blue divided voltages received from the blue resistor set and generates m blue reference gamma voltages;

a blue positive gamma voltages generator that further divides the m blue reference gamma voltages received from the blue decoder and generates a plurality of blue positive gamma voltages corresponding to gray levels of the data signals;

a blue negative gamma voltages generator that further divides the m blue reference gamma voltages received from the blue decoder and generates a plurality of blue negative gamma voltages corresponding to the gray levels of the data signals; and

a blue multiplexer that selectively outputs the plurality of blue positive gamma voltages or the plurality of blue negative gamma voltages to the digital to analog converter in response to the polarity control signal.

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摘要(译)

数据驱动器包括：伽马电压发生器，其根据红色，绿色和蓝色调节信号产生红色，绿色和蓝色伽马电压;以及数模转换器，其将从锁存器接收的数据信号转换为正或负模拟视频信号。使用从伽马电压发生器接收的红色，绿色和蓝色伽马电压。