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(19) **United States**(12) **Patent Application Publication** (10) **Pub. No.: US 2003/0030630 A1**
(43) **Pub. Date: Feb. 13, 2003**(54) **METHOD FOR COMPENSATING A
PERTURBED CAPACITIVE CIRCUIT AND
APPLICATION TO MATRIX DISPLAY
DEVICE**(30) **Foreign Application Priority Data**

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Publication Classification(75) **Inventors: Jean-Marc Bayot, La Buisse (FR);
Hughes Lebrun, Coublevie (FR)**(51) **Int. Cl.⁷ G09G 5/00**(52) **U.S. Cl. 345/204**(57) **ABSTRACT**

Correspondence Address:

**OBLON SPIVAK MCCLELLAND MAIER &
NEUSTADT PC
FOURTH FLOOR
1755 JEFFERSON DAVIS HIGHWAY
ARLINGTON, VA 22202 (US)**

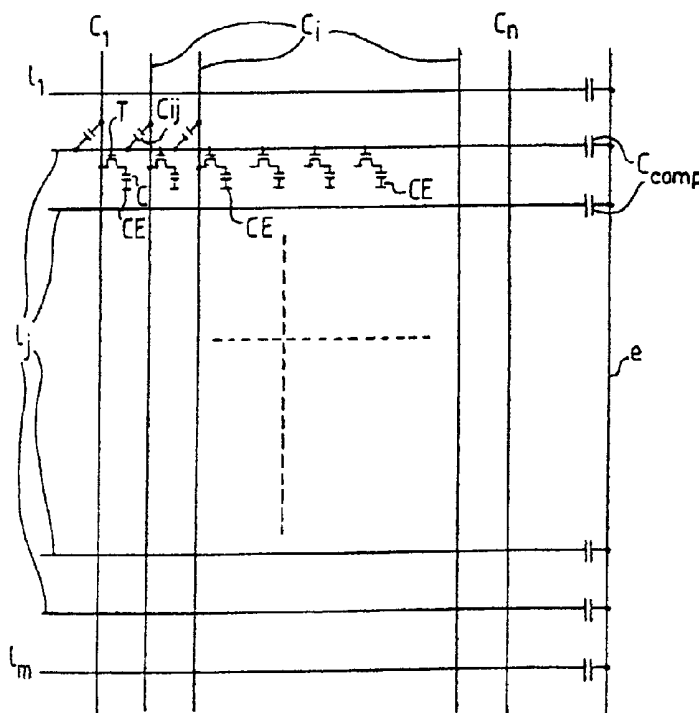
The present invention relates to a process for compensating a circuit comprising at least one first conductor (l_j) with a specified potential, at least one second conductor (c_i) generating disturbances on the first conductor by capacitive coupling, and a first bus (CE) with a reference voltage, coupled capacitively to the first conductor.

The process comprises the following steps:

measurement of the current flowing on the first bus (CE) upon the application of a voltage to the second conductor,

integration of a measured current so as to obtain a compensation voltage to be applied to the first conductor.

Applications to liquid crystal screens of the AM-LCD type.

(73) **Assignee: THALES AVIONICS LCD S.A., PARIS
(FR)**(21) **Appl. No.: 10/204,313**(22) **PCT Filed: Feb. 23, 2001**(86) **PCT No.: PCT/FR01/00539**

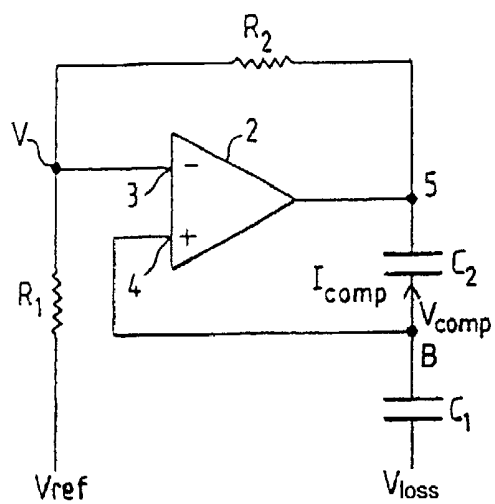


FIG. 1

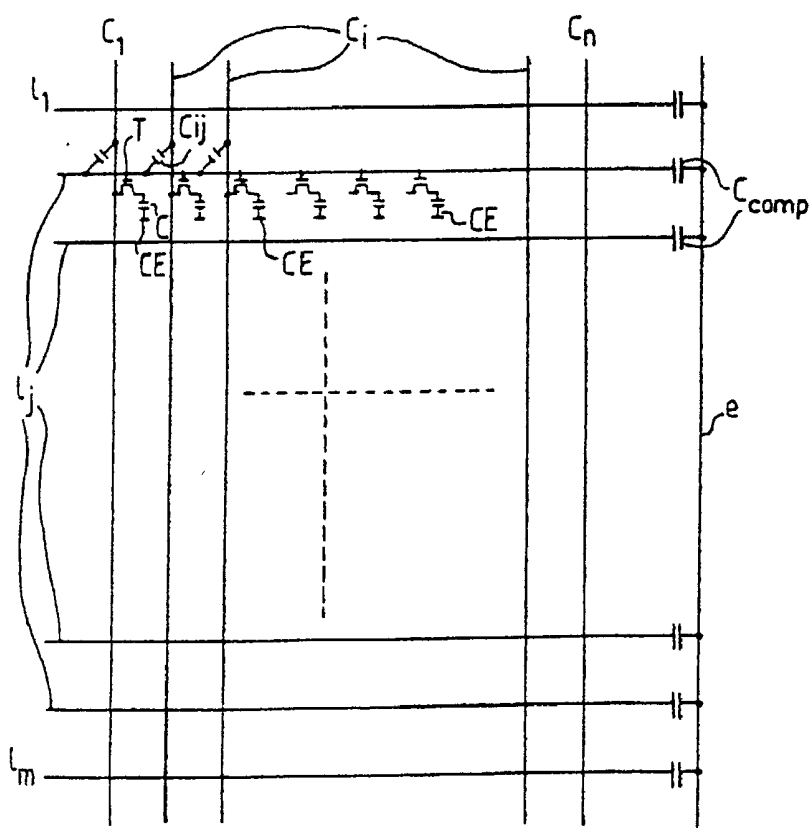


FIG. 2

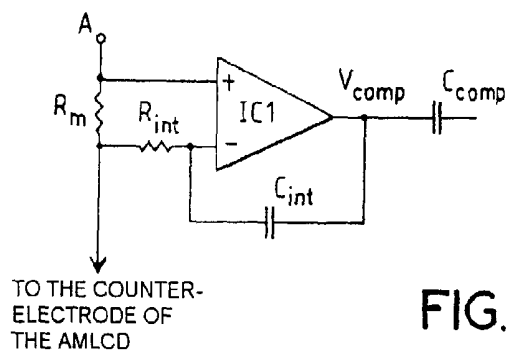


FIG.3

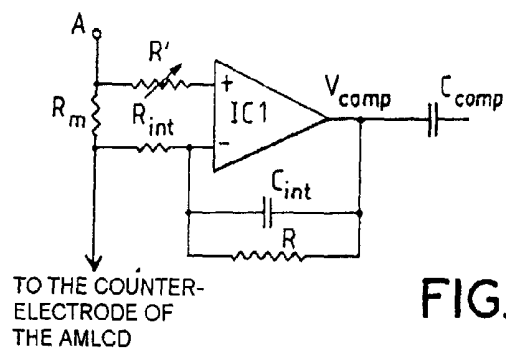


FIG.4

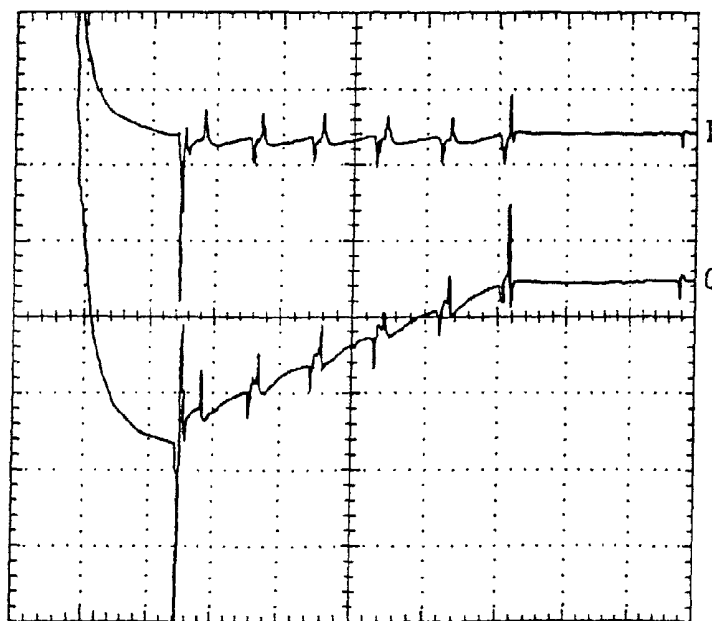


FIG.5

METHOD FOR COMPENSATING A PERTURBED CAPACITIVE CIRCUIT AND APPLICATION TO MATRIX DISPLAY DEVICE

[0001] The present invention relates to an improvement to the process for compensating a disturbed capacitive circuit. It relates more especially to a process for compensating for the capacitive disturbances in a matrix display screen.

[0002] The present invention also relates to the application of this process to matrix display screens, more especially to display screens of the active matrix type. It therefore relates to a device for compensation of potential for a display screen controlled by an array of electrodes disposed in rows and columns. It is more especially involved with active matrix liquid crystal screens, but other screens of the same type may also be used such as LCOS screens or screens operating on the same principle.

[0003] To facilitate the description, the present invention will be described while referring to a display screen of the active matrix LCD or liquid crystal screen type. However, it may also be applied to any disturbed capacitive system which requires compensation, the latter being carried out without appending any specific measurement line, but by using a conductor plane such as the counter electrode of an active matrix LCD screen, already present by design in the capacitive system.

[0004] In the case of a display screen of the active matrix liquid crystal screen type, the latter consists, in a known manner, of a set of parallel rows and of a set of parallel columns disposed perpendicularly to one another to which are linked image-elements or pixels by way of a switching means such as a TFT transistor. This type of screen can operate sequentially, the rows being activated one after another while the data are displayed on the columns or vice versa. In the case of row by row sequential operation, the control circuit for the rows imposes a first selection potential on the chosen row, the other rows being taken to a reference potential. For a part of the duration corresponding to the row control, a potential dependent on the data to be displayed is imposed on all the columns by the column control circuits. Therefore, all the column control circuits change state simultaneously. These simultaneous changes of state therefore produce a capacitive coupling between rows and columns which is greater the larger the difference between the control impedance and the load impedance in favor of the latter. Now, this coupling referred to as column-row-column or CRC coupling causes variations in contrast from one column to another of the screen, if it is not compensated.

[0005] Thus, various solutions have been proposed for compensating the capacitive couplings existing between the rows and the columns of a matrix screen using row or column control devices, more especially those exhibiting a high or medium output impedance. A compensation circuit of this type is described for example in French patent application No. 94 05987 filed on May 17, 1994 in the name of THOMSON-LCD and published under No. 2 720 185. In this case, an additional electrode coupled capacitively by capacitors to each of the rows of the screen is used to carry out the compensation, and an additional line also coupled capacitively to the columns of the screen which it crosses is used to detect the compensation level to be introduced. In this case, two additional electrodes are required to carry out the measurement of the imbalance due to the capacitive coupling and the compensation of this imbalance.

[0006] To remedy this drawback, French patent application No. 97 06940 filed on Jun. 5, 1997 and published under No. 2 764 424 in the name of THOMSON-LCD has proposed the use of just a single additional electrode or bus to carry out both the measurement of the imbalance and the compensation of this imbalance. In this case, use is made of a circuit for compensating for the imbalances due to the row/column capacitive coupling during the control phases, whose input and output are coupled to said additional bus. As represented in FIG. 1, the compensation circuit used consists of an operational amplifier 2, one input of which, namely the negative input 3, is linked by way of an impedance, namely the resistor R1 in the embodiment represented, to a reference voltage V_{ref} . This input 3 is also linked by way of a second impedance, namely the resistor R2, to the output 5 of the operational amplifier. Moreover, the second input, namely the positive input 4, is linked to the point B of connection to the additional compensation bus and it is also connected across a first capacitor C2 to the output 5 of the operational amplifier. On the other hand, the point B is connected to the compensation bus across the compensation capacitor C1 whose value is equal to the sum of the capacitors linking the additional bus or buses to each row of the matrix array. To detect the losses V_{loss} with the above arrangement, when the rows are disturbed capacitively by the columns, the output 5 of the operational amplifier 2 is modified in such a way as to bring the row voltage down to a value equal to the reference voltage therefore making it possible to compensate for the imbalance with the same bus.

[0007] The above circuit is a negative-impedance compensator. It converts any current in the compensation capacitor C1 into a reverse voltage variation in this same capacitor. This type of circuit is very sensitive to the leakage currents in the row control circuits and to the currents emanating from the capacitors of the compensation bus upon the application of other screen control signals. Therefore, the circuit described above starts oscillating when the compensation voltage becomes too large.

[0008] The aim of the present invention is to remedy the abovementioned drawbacks by proposing a novel process for compensating a capacitively disturbed circuit as well as a novel circuit for implementing the process.

[0009] Thus, the subject of the present invention is a process for compensating for the capacitive disturbances in a display screen comprising an array of electrodes disposed matrix-wise in rows lj (j varying from 1 to m) and columns ci (i varying from 1 to n), the electrodes being linked to image-elements or pixels, a coupling capacitor being associated with each row/column crossover, a conductor plane with a reference voltage forming capacitive elements together with the image-elements and having by design a nonzero capacitance with the set of columns, a row-control circuit and a column-control circuit and at least one compensation conductor bus crossing the set of rows, said process being characterized by the following steps:

[0010] measurement of the current flowing in the conductor plane upon the application of a voltage to at least one column,

[0011] integration of the measured current so as to obtain a compensation voltage to be applied to at least one row by way of the compensation conductor bus coupled capacitively to the rows.

[0012] According to a preferred embodiment, the measurement of the current is carried out by a first impedance in series with the conductor plane and the integration of the current is carried out by an integrator circuit arranged in parallel with the first impedance. Preferably, the integrator circuit is constituted by an operational amplifier and a negative feedback circuit consisting of a capacitor arranged between the output terminal and one of the input terminals of the operational amplifier. According to a variant, the negative feedback circuit can consist of a capacitor and a parallel impedance, thereby limiting the gain of the integrator at high frequencies.

[0013] According to another characteristic, a second impedance is arranged in series between said input terminal of the operational amplifier and a terminal of the first impedance, this second impedance possibly being variable. A third impedance can be connected between the other terminal of the first impedance and the second input terminal of the operational amplifier.

[0014] This third impedance can also be variable.

[0015] The present invention also relates to a display screen comprising an array of electrodes disposed matrix-wise in rows L_j (j varying from 1 to m) and columns C_i (i varying from 1 to n), the electrodes being linked to image-elements or pixels, a coupling capacitor being associated with each row/column crossover, a conductor plane with a reference voltage forming capacitive elements together with the image-elements and having by design a nonzero capacitance with the set of columns, row- and column-control circuits and at least one compensation conductor bus crossing the set of rows, the conductor plane and the conductor bus being connected to a circuit for compensating for the disturbances due to the row/column capacitive coupling implementing the above process.

[0016] Preferably, the display screen is an active matrix liquid crystal screen or LCOS screen or any display screen of similar type. Moreover, the conductor plane with a reference voltage is constituted by the counter electrode of the display screen.

[0017] Other characteristics and advantages of the present invention will become apparent on reading the description of a preferred embodiment, this description being given with reference to the appended drawings in which:

[0018] **FIG. 1** already described represents a compensation circuit according to the prior art,

[0019] **FIG. 2** diagrammatically represents a liquid crystal display screen of the active matrix type to which the present invention may be applied,

[0020] **FIG. 3** represents a compensation circuit in accordance with the present invention,

[0021] **FIG. 4** represents a variant of the compensation circuit in accordance with the present invention, and

[0022] **FIG. 5** represents measurements of voltage across the terminals of the measurement resistor and on the compensation bus which are performed on a XGA screen.

[0023] A matrix array display screen, more especially a liquid crystal screen furnished with a compensation bus making it possible to implement the present invention will be described with reference to **FIG. 2**. This display screen

consists of a matrix array of rows L_j (j varying from 1 to m) and columns C_i (i varying from 1 to n) disposed perpendicularly. At the crossover of each row and of each column is a control transistor T , in general a thin film transistor or TFT which controls a pixel symbolized by a capacitor C . In the case of a liquid crystal screen, one of the electrodes of the capacitor C consists of the pixel electrode while the other electrode consists of a counter electrode CE common to all the pixels. In a known manner, the rows are connected to row control circuits (not represented) while the columns are connected to column control circuits (not represented). As explained in the introduction, when the outputs of the row control circuits are not at low impedance, there are nonnegligible capacitive couplings represented by the capacitances C_{ij} between the rows and the columns. Hence, to remedy this drawback and as represented in **FIG. 2**, at least one additional bus or compensation bus e is provided. This compensation bus e is embodied parallel to the columns C_i and is coupled capacitively by capacitances referenced C_{comp} to each of the rows L_j of the screen.

[0024] In the circuit described above, the counter electrode which constitutes the reference electrode for the liquid crystal capacitor can be regarded as a voltage reference for the display screen. Now, each column has a nonzero capacitance with the counter electrode and the column charges or discharges this capacitor with each switching. In accordance with the present invention, the variation in the voltage of the columns can therefore be deduced from the measurement of the current in the voltage reference plane, namely in the counter electrode. Specifically, the voltage switching at the level of the columns generates inrushes of current into the counter electrode and the integral of the current measured in the counter electrode is proportional to the voltage variation of the column during switching. This value may therefore be used to compensate for the disturbances due to the row/column coupling or CRC disturbances.

[0025] A first circuit making it possible to carry out the compensation in accordance with the present invention will now be described with reference to **FIG. 3**. This circuit essentially comprises a means of measuring the current flowing around the counter electrode upon the application of a voltage to the columns of an LCD screen and a means making it possible to integrate the current measured in such a way as to obtain a compensation voltage to be applied to the rows by way of the compensation bus. The means for measuring the current consists of an impedance, namely the resistor R_m arranged in series with the counter electrode of the active matrix liquid crystal screen. This resistor R_m is connected, at the level of the terminal A, to the circuit for controlling the counter electrode signal which makes it possible to apply a reference voltage to the counter electrode. The integration circuit consists in a known manner of an operational amplifier $IC1$ whose output is connected by way of a capacitor C_{int} to one of the inputs, namely the $-$ input of the amplifier $IC1$. On the other hand, a resistor R_{int} is arranged in series with the $-$ input of the operational amplifier $IC1$. The resistor R_m for measuring the current flowing in the counter electrode is arranged between the $+$ terminal of the amplifier $IC1$ and the terminal of the resistor R_{int} which is not connected to the $-$ input of the amplifier $IC1$. The resistor R_m is therefore arranged in series between the circuit for controlling the counter electrode signal and the counter electrode of the liquid crystal screen. With the circuit described above, the potential difference across the

terminals of the resistor R_m is proportional to the current which passes through the counter electrode. This current is integrated by the operational amplifier IC1 and the capacitor C_{int} and gives as output a voltage V_{comp} which is proportional to the compensation voltage. This voltage V_{comp} is applied to the rows of the screen by way of the compensation capacitors C_{comp} . Preferably, to obtain a suitable compensation voltage, the resistor R_{int} is a variable resistor making it possible to adjust the gain of the integrator. According to a variant embodiment, the counter electrode can be replaced by a ground plane. In this case, the invention operates in an absolutely identical manner when the current is measured in said ground plane which then serves as reference for the storage capacitors of all the pixels if the columns have a nonzero capacitance with the ground plane.

[0026] Represented in FIG. 4 is a variant embodiment of the circuit. In this case, the negative feedback circuit arranged between the output and the $-$ input of the operational amplifier is constituted by a filter formed of the capacitor C_{int} and of a resistor R arranged in parallel. This structure limits the gain of the integrator at high frequencies. Moreover, a resistor R' , variable or otherwise, is arranged between the $+$ terminal of the operational amplifier and the terminal A. The other elements are identical.

[0027] The circuit described above does not oscillate as represented by the curves of FIG. 5 in which the curve I represents the voltage measurement across the terminals of the resistor R_m and the curve O represents the voltage on the compensation bus as a function of time. The measurements were made on an XGA screen exhibiting a demultiplexing factor of 5, on which at the start of each row, the column voltage is precharged to a reference voltage, this explaining the spike observed in the curves.

[0028] The present invention applies not only to display screens of the type with integrated control devices, comprising in particular high-impedance row control circuits, but it can also apply to display screens with external control circuits. In this case, the measurement of the current is performed on the voltage for turning off the rows at the input of the external control circuits. The output of the operational amplifier arranged as an integrator is linked to the compensation bus "e" of FIG. 2.

[0029] It is obvious to the person skilled in the art that the present invention may be applied to all types of active matrix display screens, of the type comprising a conductor plane similar to the counter electrode of an LCD screen. It may be applied not only to active matrix liquid crystal screens of the type described above but also to LCOS screens, whatever technology is used for embodying the transistors, namely amorphous silicon, low-temperature polycrystalline silicon, high-temperature polycrystalline silicon or crystalline silicon.

1. A process for compensating for the capacitive disturbances in a display screen comprising an array of electrodes disposed matrix-wise in rows l_j (j varying from 1 to m) and columns c_i (i varying from 1 to n), the electrodes being linked to image-elements or pixels, a coupling capacitor being associated with each row/column crossover, a conductor plane with a reference voltage forming capacitive

elements together with the image-elements and having by design a nonzero capacitance with the set of columns, a row-control circuit and a column-control circuit and at least one compensation conductor bus crossing the set of rows, characterized by the following steps:

measurement of the current flowing in the conductor plane upon the application of a voltage to at least one column ($C1$),

integration of the measured current so as to obtain a compensation voltage to be applied to at least one row by way of the compensation conductor bus (e) coupled capacitively to the rows.

2. The process as claimed in claim 1, characterized in that the measurement of the current is carried out by a first impedance (R_m) in series with the conductor plane.

3. The process as claimed in claims 1 and 2, characterized in that the integration of the current is carried out by an integrator circuit (IC1, C_{int} , R) arranged in parallel with the first impedance (R_m).

4. The process as claimed in claim 3, characterized in that the integrator circuit is constituted by an operational amplifier (IC1) and a capacitor (C_{int}) arranged between the output terminal and one of the input terminals of the operational amplifier.

5. The process as claimed in claim 3, characterized in that the integrator circuit is constituted by an operational amplifier (IC1) and a filter formed of a capacitor (C_{int}) and of a resistor (R) in parallel, and which is arranged between the output terminal and one of the input terminals of the operational amplifier (IC1).

6. The process as claimed in claims 4 and 5, characterized in that a second impedance (R_{int}) is arranged in series between said input terminal of the operational amplifier and a terminal of the first impedance.

7. The process as claimed in claims 4 to 6, characterized in that a third impedance (R') is arranged in series between the other input terminal of the operational amplifier and the other terminal of the first impedance (R_m).

8. A display screen comprising an array of electrodes disposed matrix-wise in rows l_j (j varying from 1 to m) and columns c_i (i varying from 1 to n), the electrodes being linked to image-elements or pixels, a coupling capacitor being associated with each row/column crossover, a conductor plane with a reference voltage forming capacitive elements together with the image-elements and having by design a nonzero capacitance with the set of columns, a row-control circuit and a column-control circuit and at least one compensation conductor bus crossing the set of rows, characterized in that the conductor plane and the conductor bus are connected to a circuit for compensating for the disturbances due to the row/column capacitive couplings implementing the process according to any one of claims 1 to 7.

9. The display screen as claimed in claim 7, characterized in that it consists of an active matrix liquid crystal screen or LCOS screen.

10. The display screen as claimed in claims 8 and 9, characterized in that the conductor plane with a reference voltage is constituted by the counter electrode.

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专利名称(译)	补偿扰动电容电路的方法和矩阵显示装置的应用		
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[标]申请(专利权)人(译)	THALES AVIONICS LCD		
申请(专利权)人(译)	THALES AVIONICS LCD S.A.		
当前申请(专利权)人(译)	汤姆森许可		
[标]发明人	BAYOT JEAN MARC LEBRUN HUGUES		
发明人	BAYOT, JEAN-MARC LEBRUN, HUGUES		
IPC分类号	G02F1/133 G09G3/20 G09G3/32 G09G3/3208 G09G3/36 G09G5/00		
CPC分类号	G09G3/20 G09G3/32 G09G3/3208 G09G3/3648 G09G3/3655 G09G2300/043 G09G2300/08 G09G2320/0209		
优先权	2000002410 2000-02-25 FR		
其他公开文献	US6972747		
外部链接	Espacenet USPTO		

摘要(译)

本发明涉及一种补偿电路的方法，该电路包括至少一个具有特定电位的第一导体 (l_j)，至少一个第二导体 (c_i) 通过电容耦合在第一导体上产生干扰，以及第一总线 (CE) 具有参考电压，电容耦合到第一导体。该过程包括以下步骤：在向第二导体施加电压时测量在第一总线 (CE) 上流动的电流，测量电流的积分，以便获得要施加到第一导体的补偿电压。适用于AM-LCD型液晶屏。

