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(54) **ACTIVE MATRIX SUBSTRATE AND DISPLAY DEVICE**

**Publication Classification**

(76) Inventors: **Ryuji Kurihara**, Taki-gun (JP); **Yuhko Hisada**, Matsusaka-shi (JP); **Toshihide Tsubata**, Tsu-shi (JP); **Masanori Takeuchi**, Tsu-shi (JP); **Tomokazu Ohtsubo**, Suzuka-shi (JP)

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(57) **ABSTRACT**

Correspondence Address:  
**KEATING & BENNETT, LLP**  
**10400 EATON PLACE**  
**SUITE 312**  
**FAIRFAX, VA 22030 (US)**

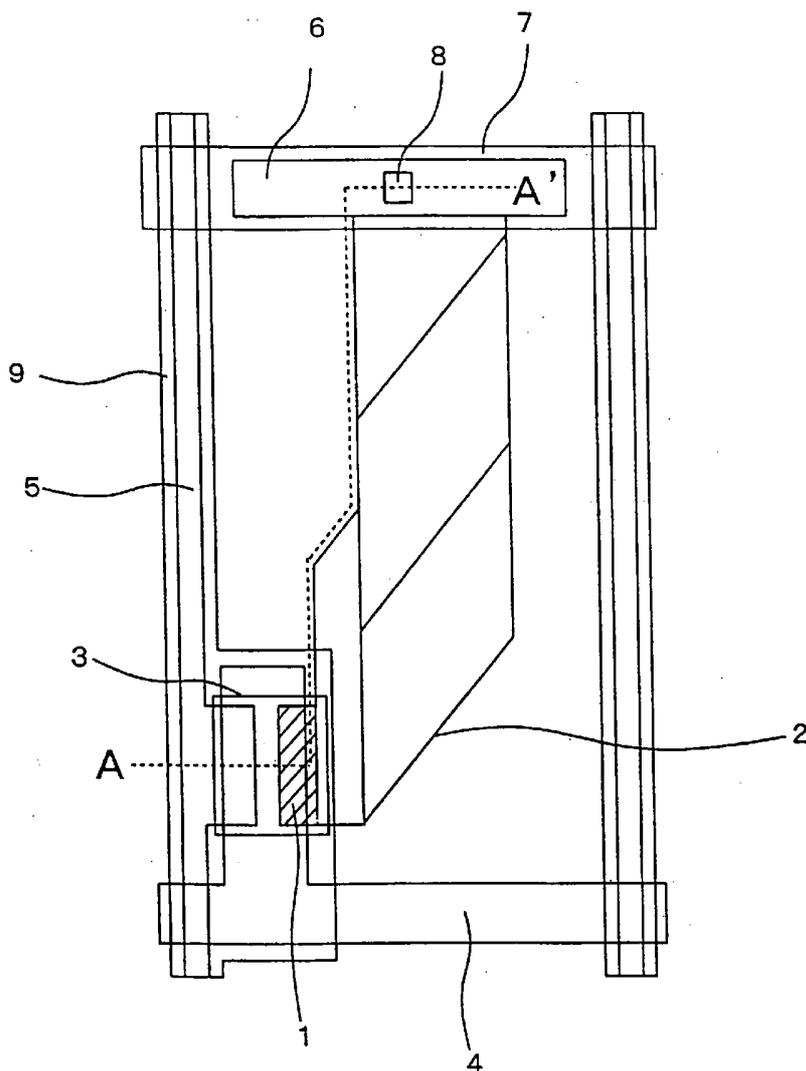
The active matrix substrate of the present invention is an active matrix substrate in which a drain extraction line can be prevented from breaking without a plurality of active elements such as TFT (thin film transistor) elements, MIM (metal-insulator-metal) elements, MOS transistor elements, diodes, and varistors being disposed, and is suited for use in large-size liquid crystal television or a like liquid crystal display device equipped with a large-size liquid crystal display panel. The active matrix substrate of the present invention is an active matrix substrate comprising an active element connected, via a drain extraction line, to a storage capacitor upper electrode, wherein the drain extraction line has at least two routes.

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Dec. 1, 2004 (JP) ..... 2004-349031



DRAWINGS

Fig.1-1

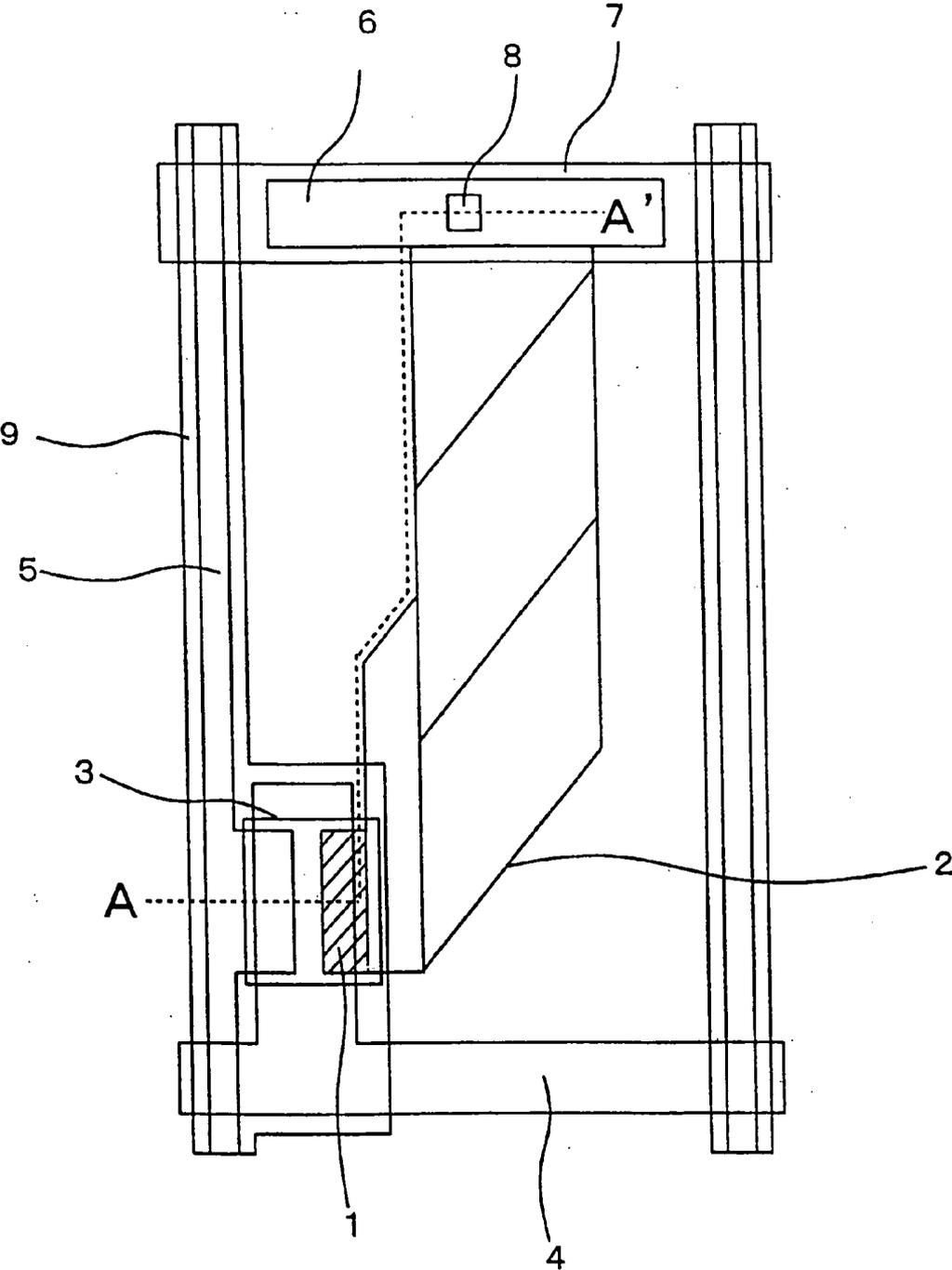


Fig.1-2

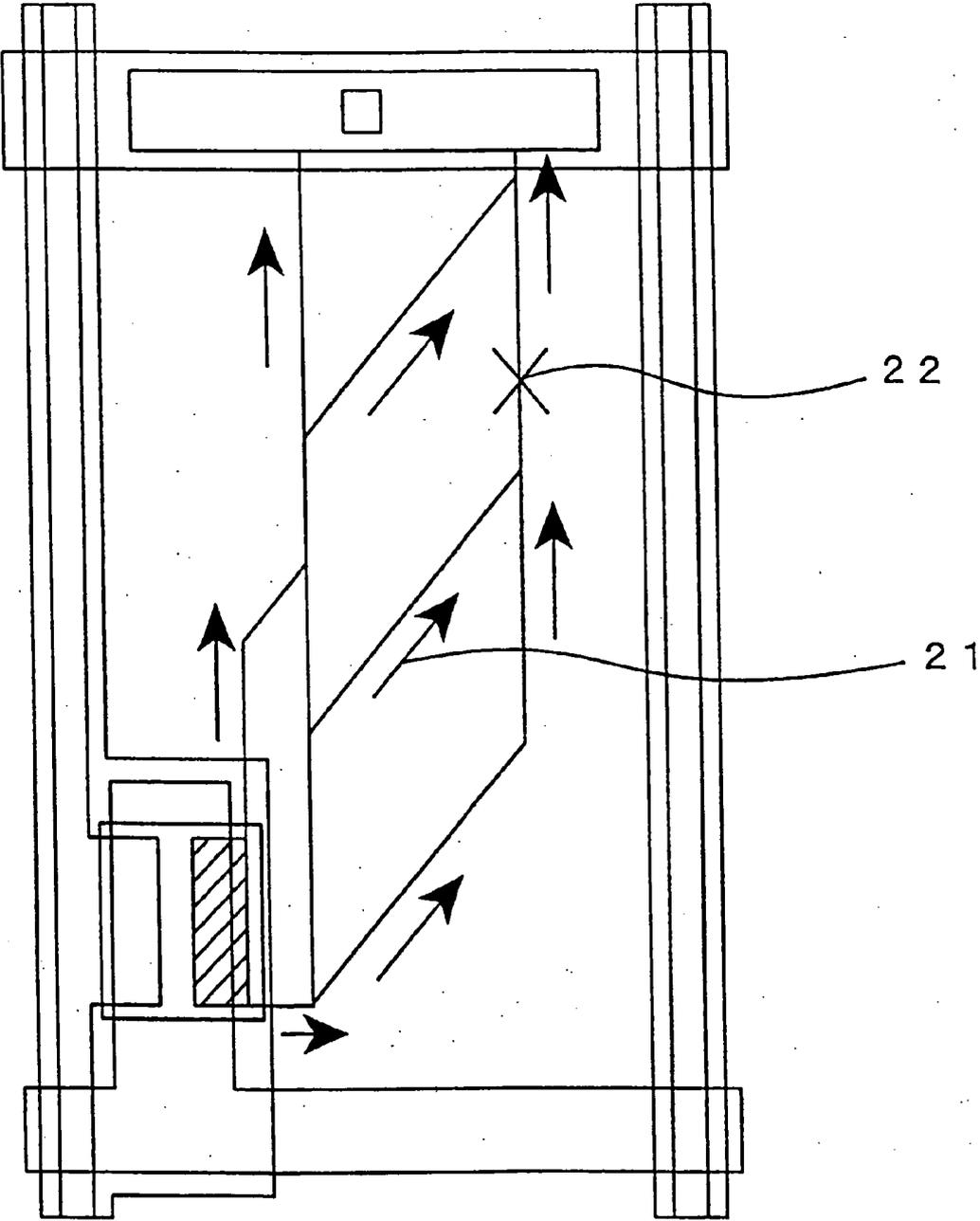


Fig.2

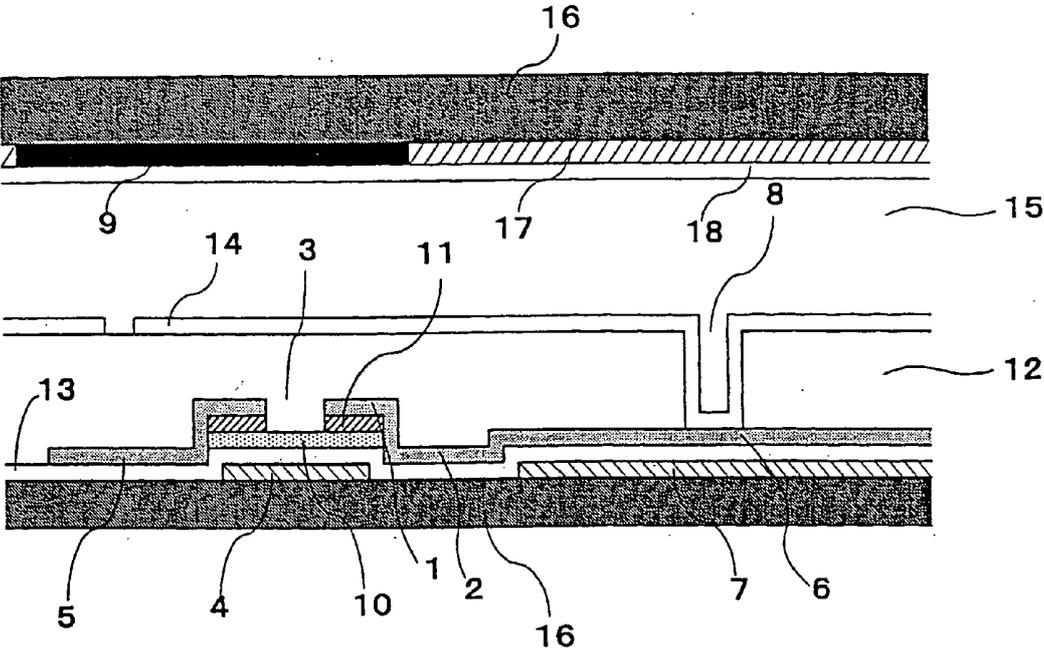


Fig.3

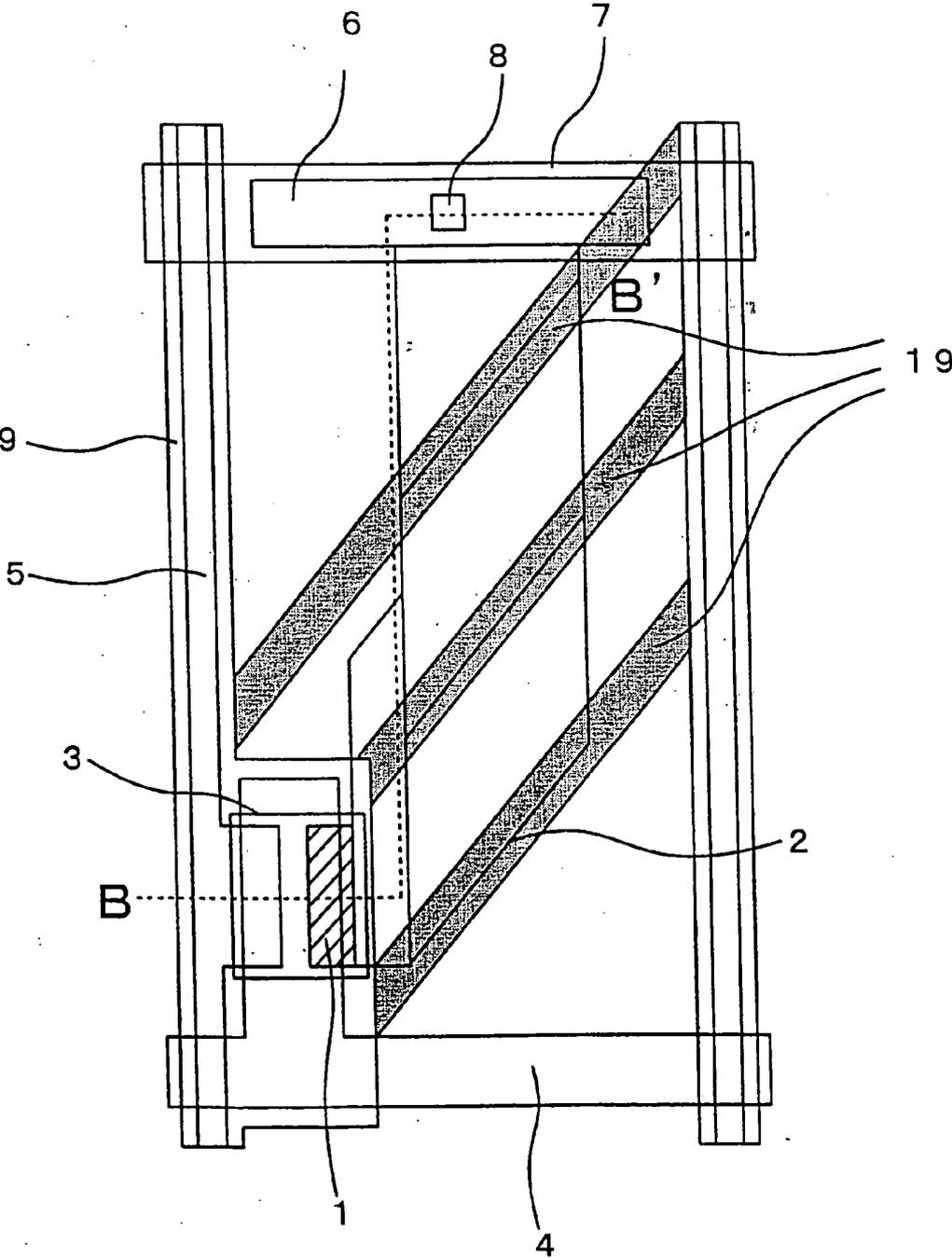


Fig.4

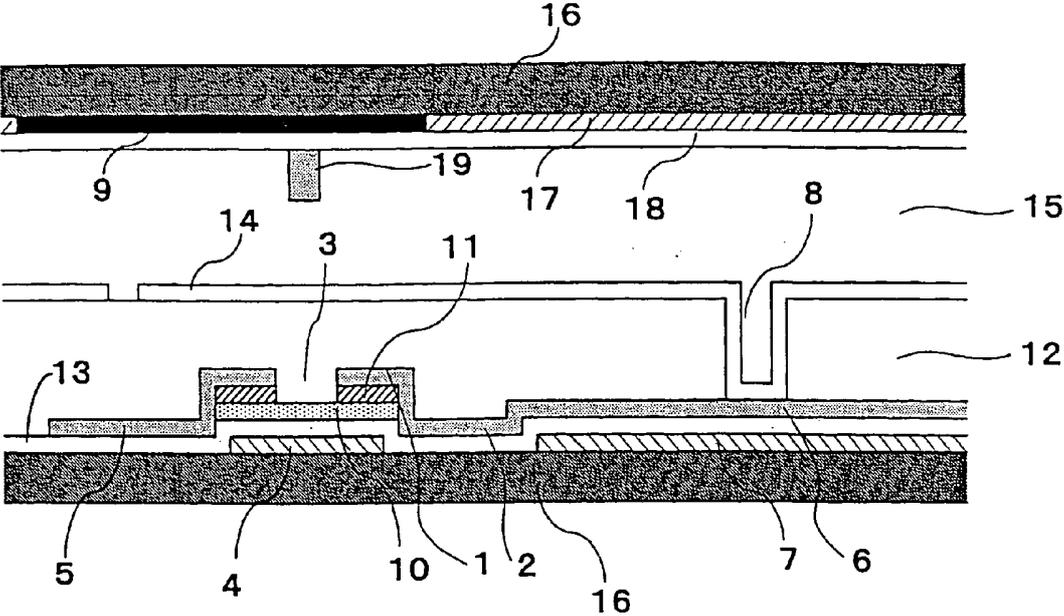


Fig.5-1

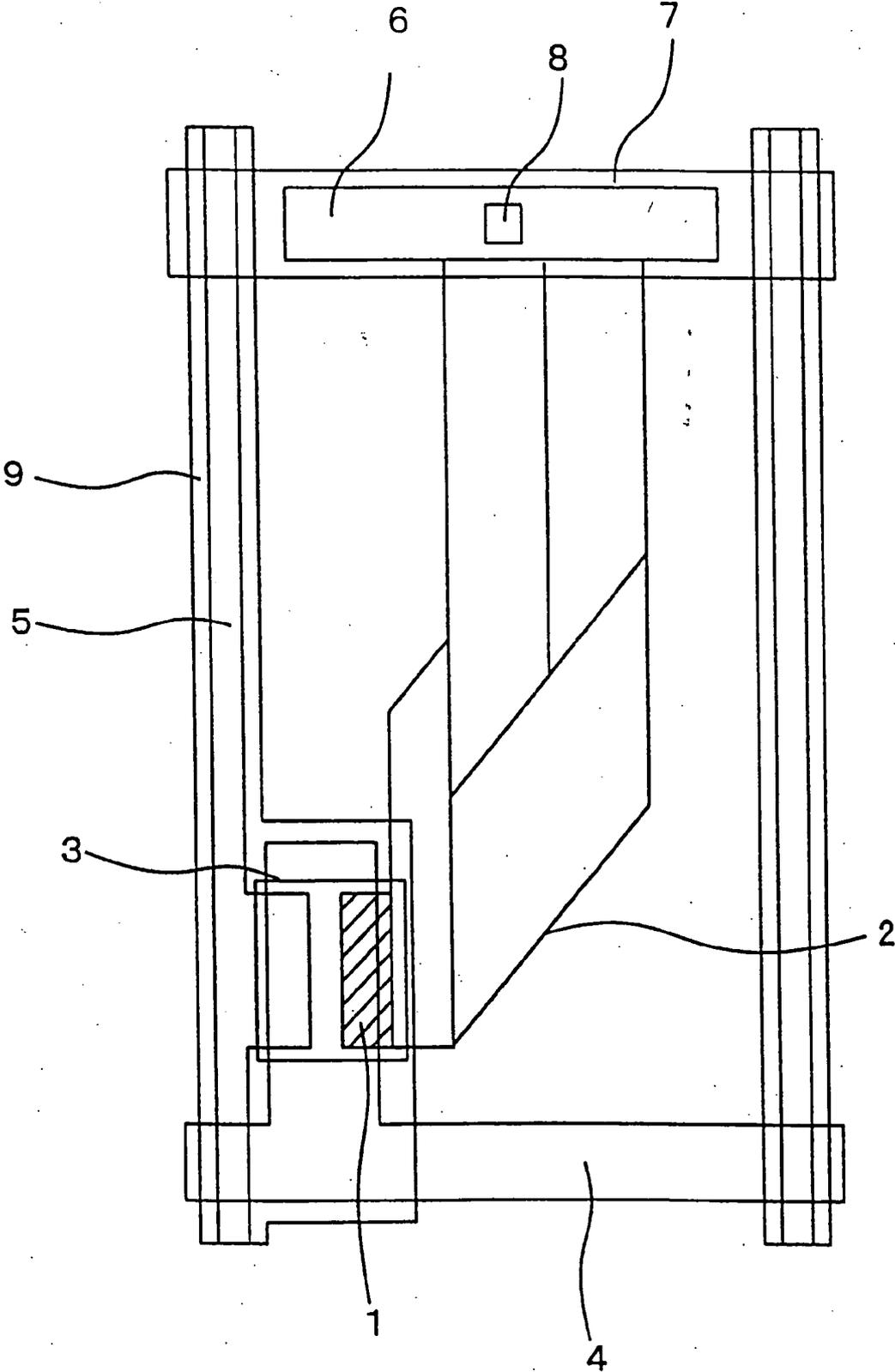


Fig.5-2

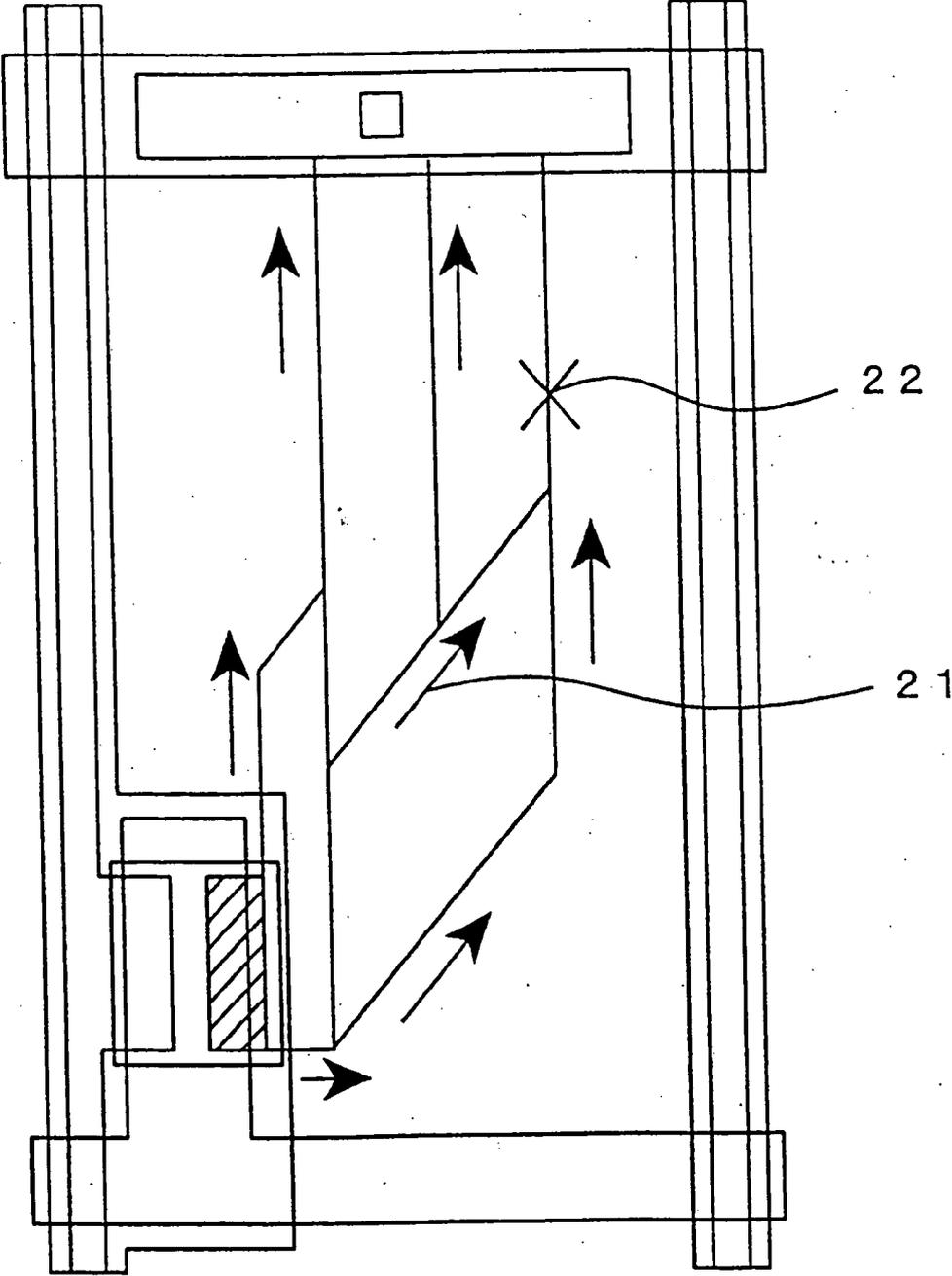


Fig.6-1

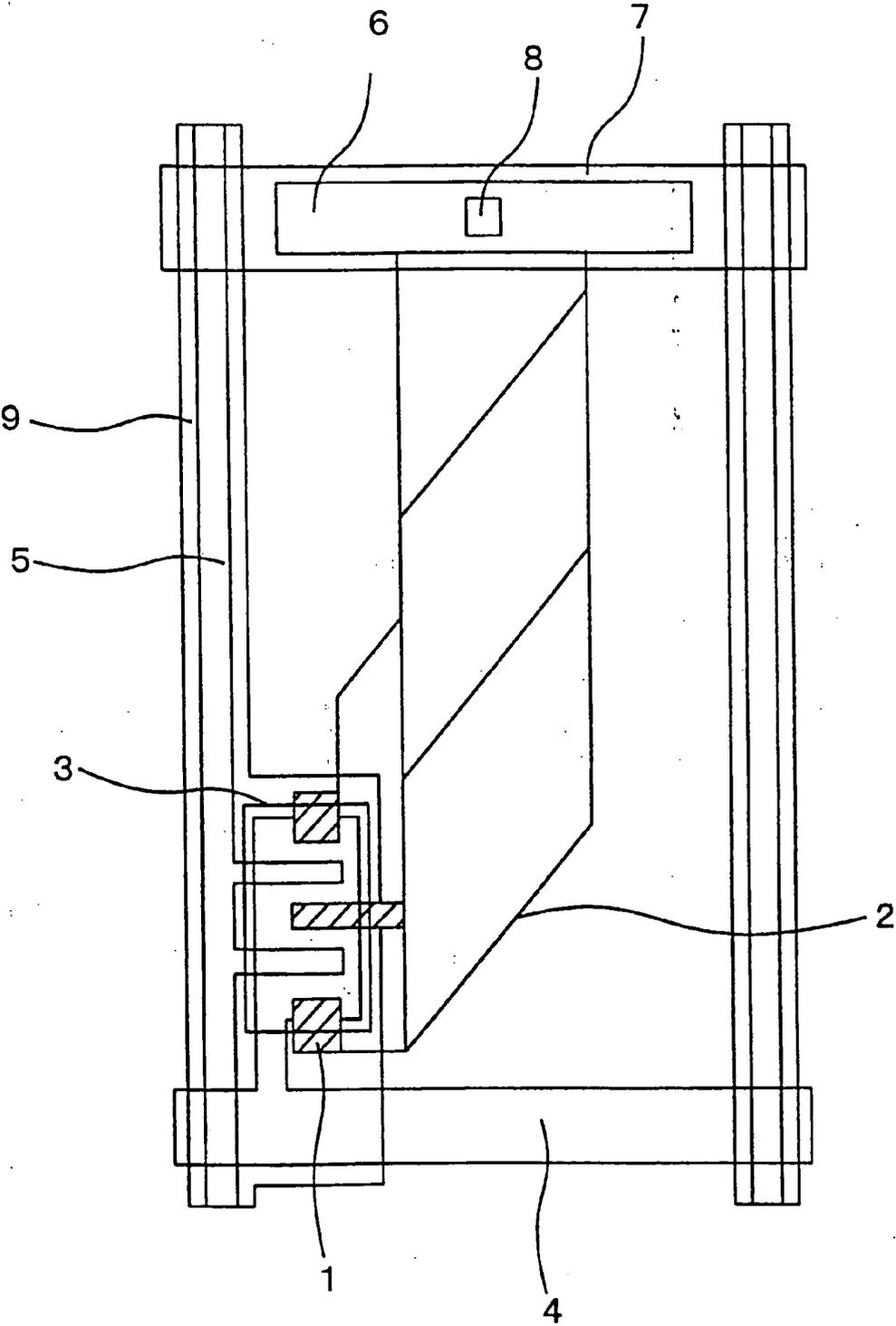


Fig.6-2

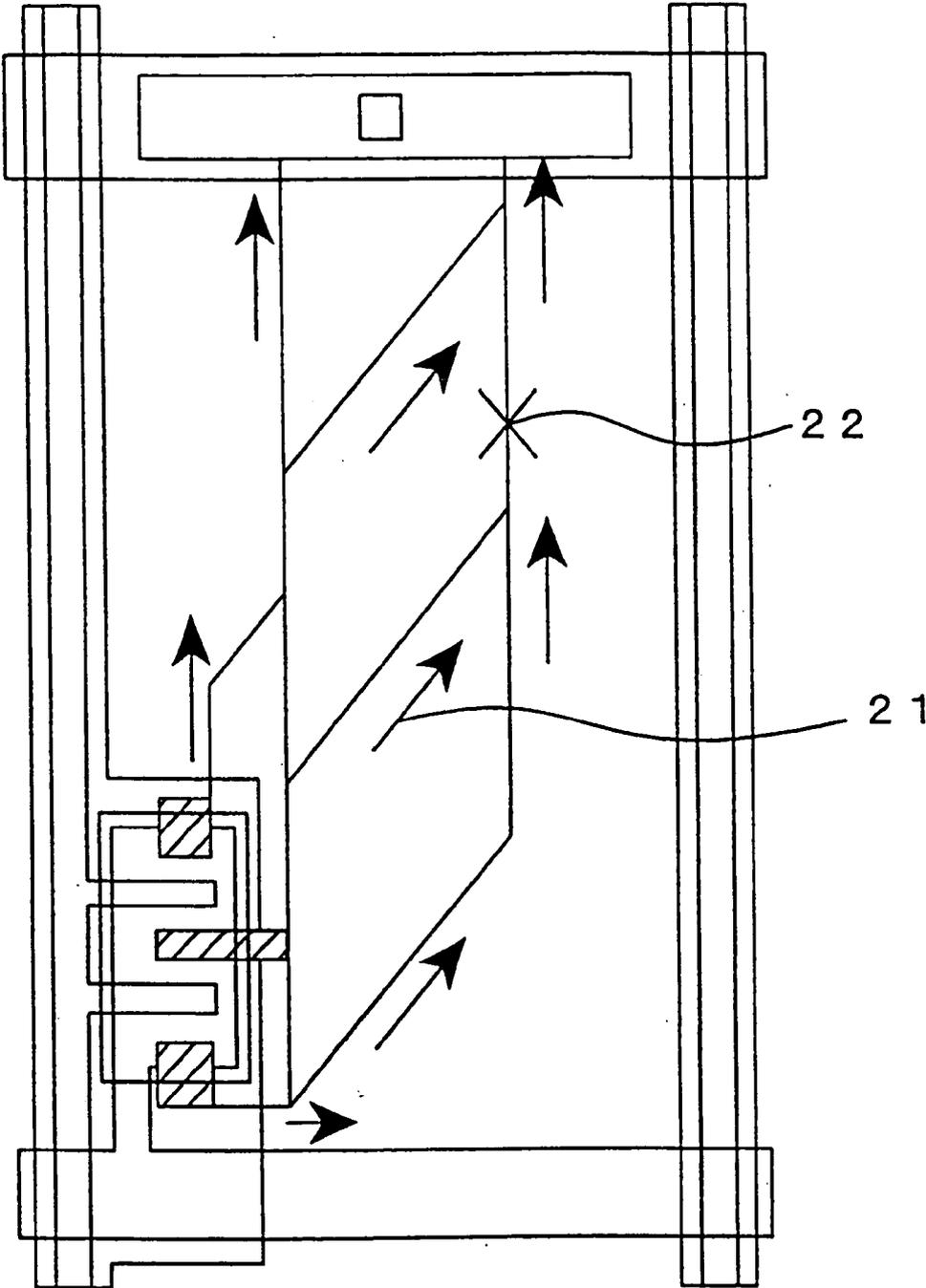


Fig.7-1

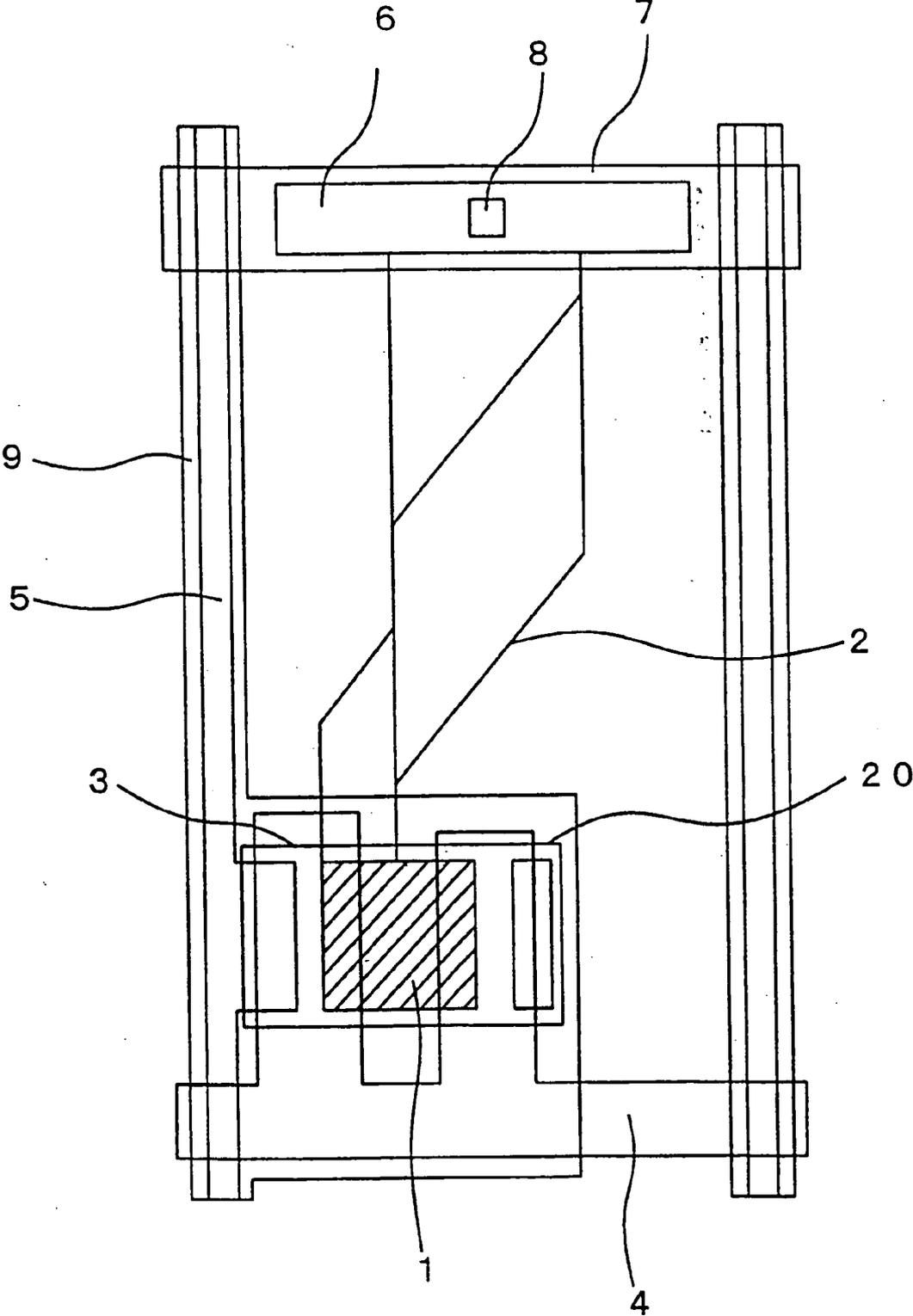


Fig.7-2

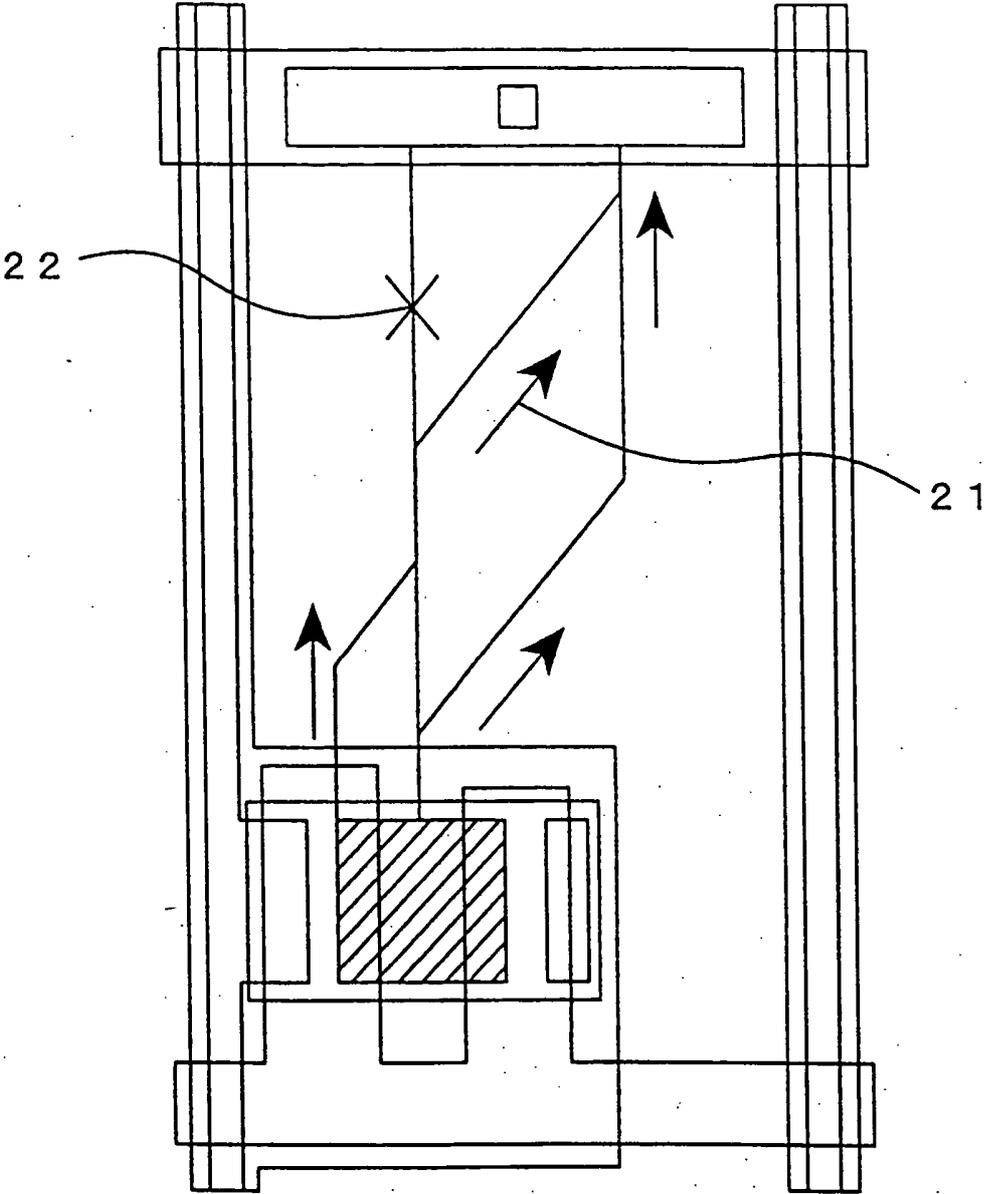


Fig. 8

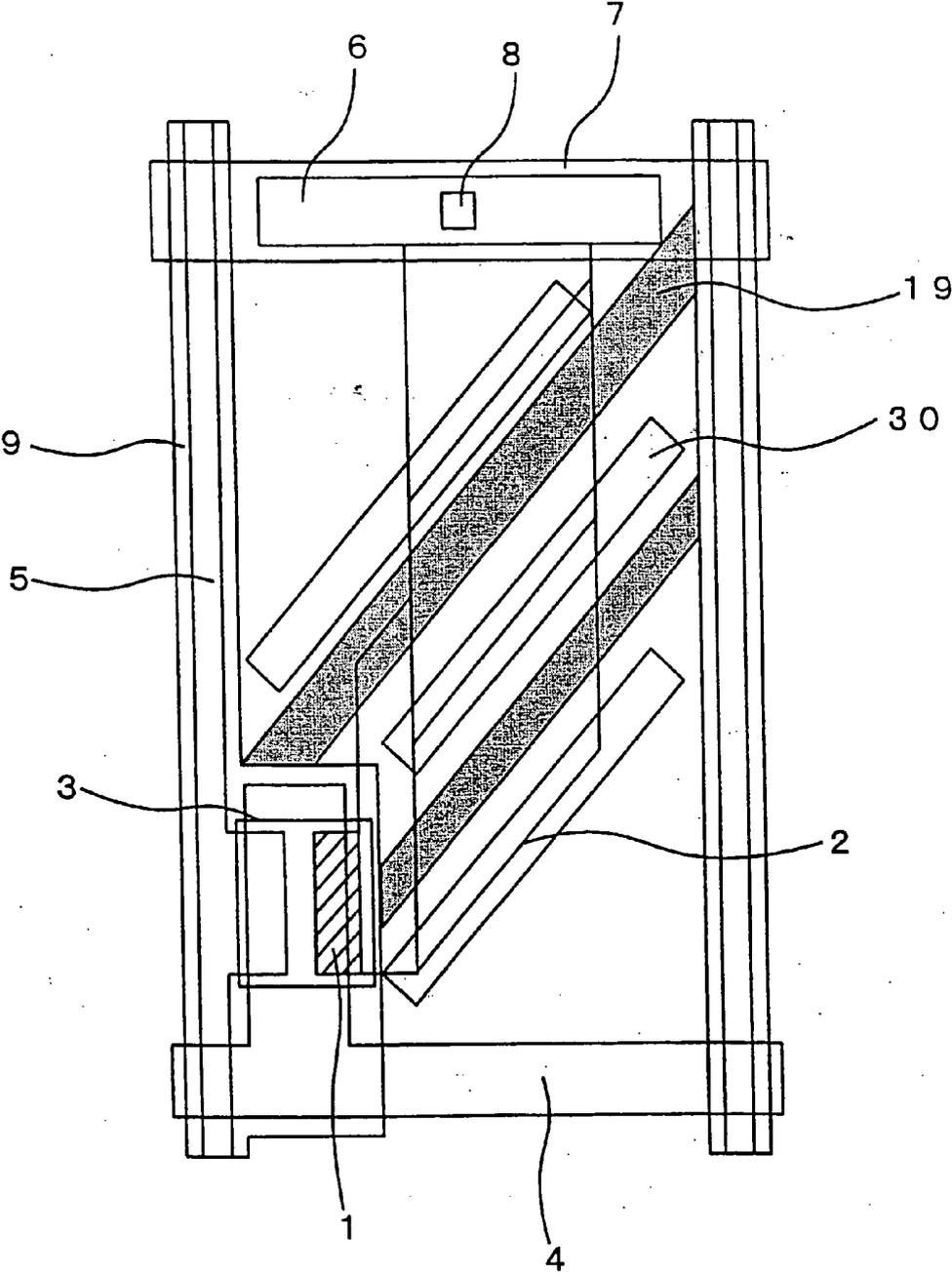


Fig.9

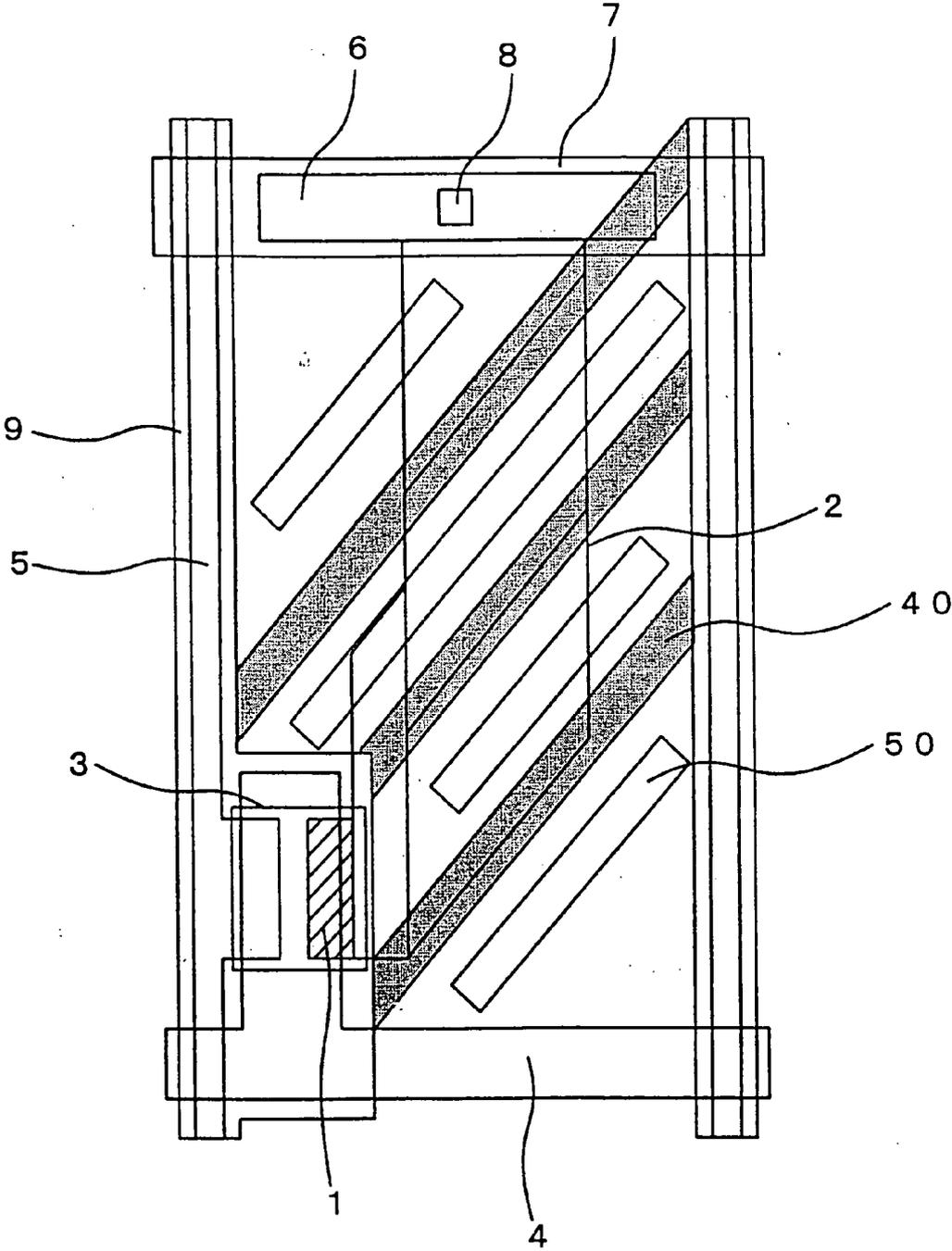


Fig.10A

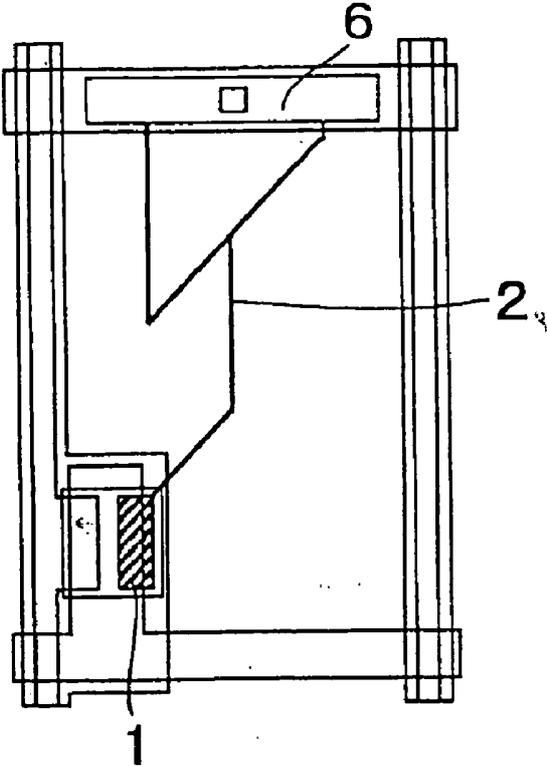


Fig.10B

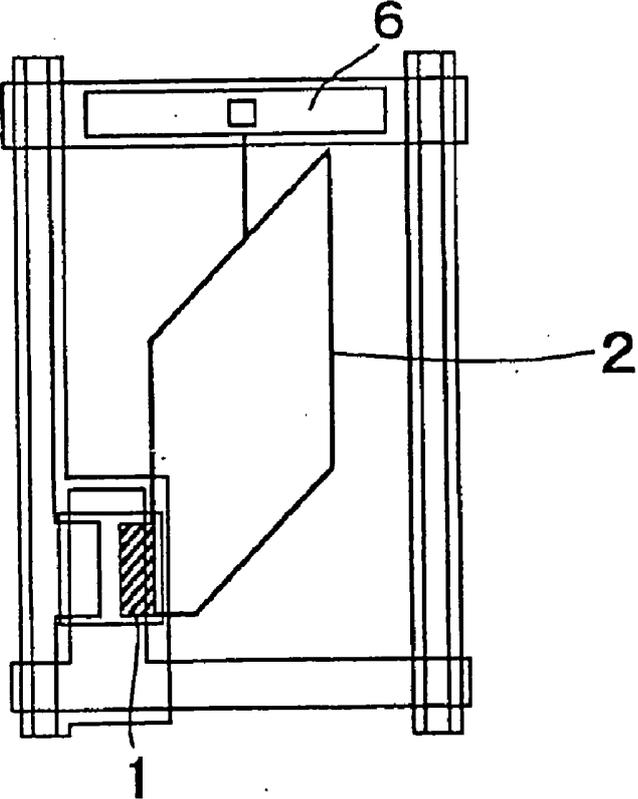


Fig. 10C

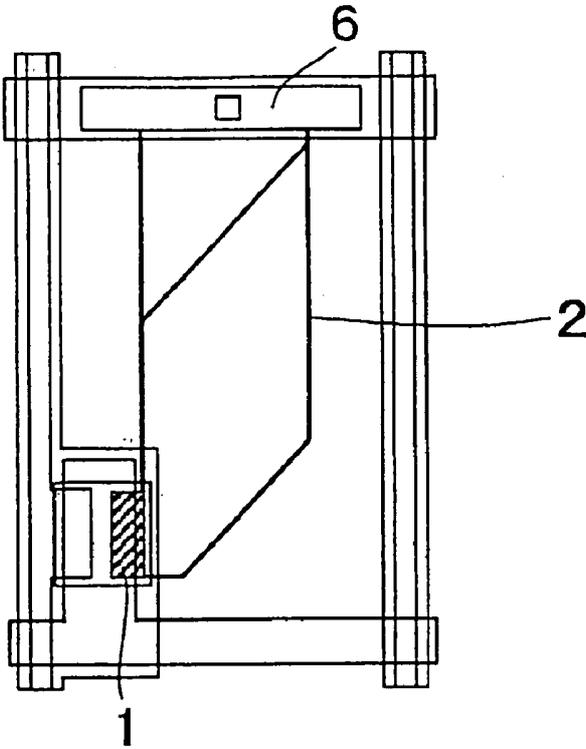


Fig. 10D

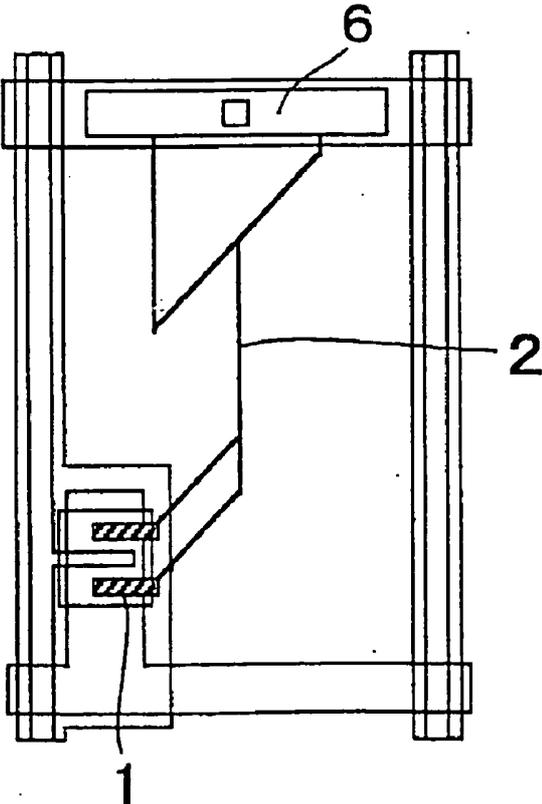


Fig.10E

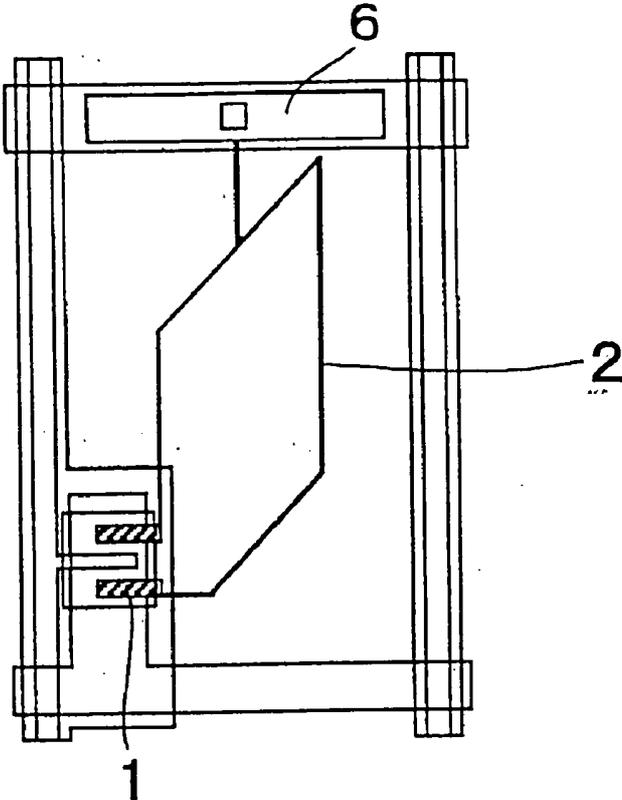


Fig.10F

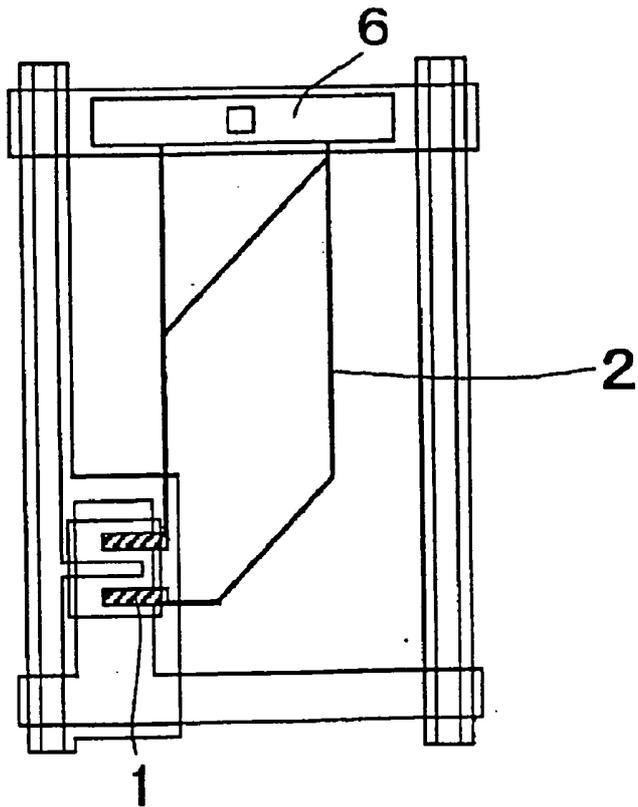


Fig.11-1

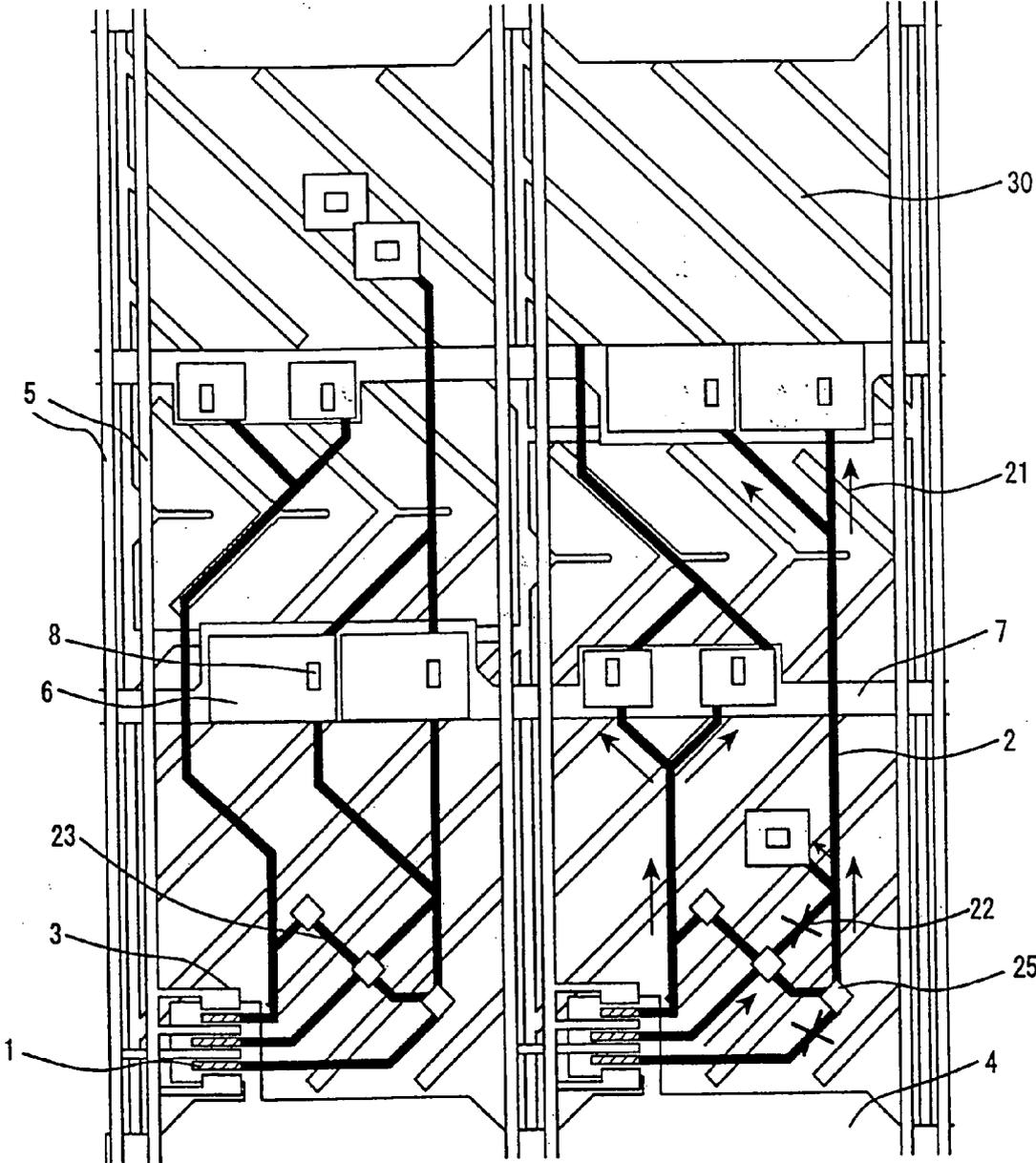


Fig.11-2A

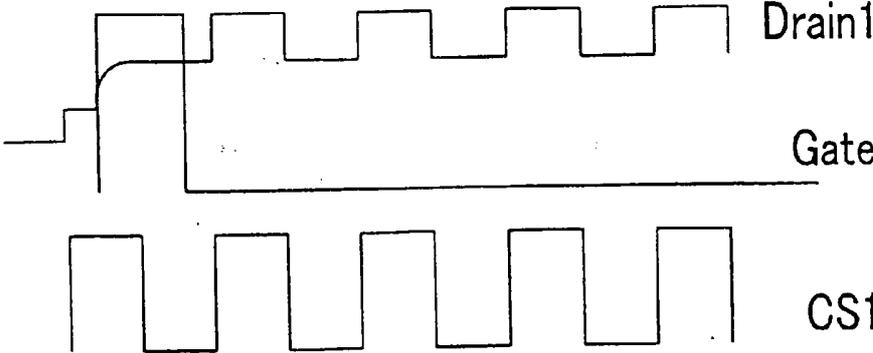


Fig.11-2B

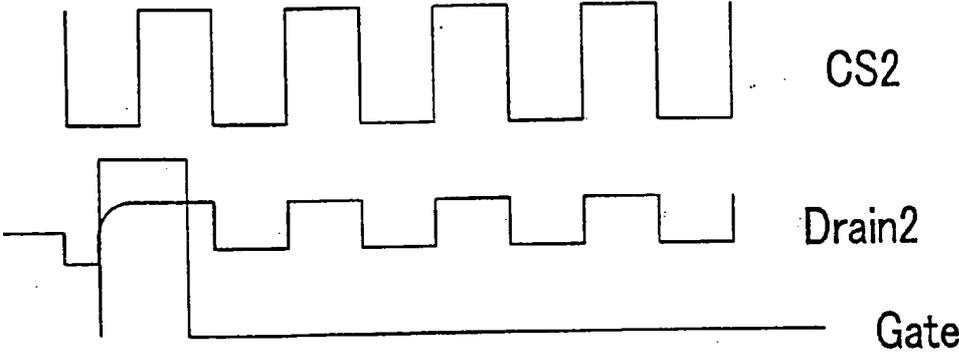


Fig.11-2C

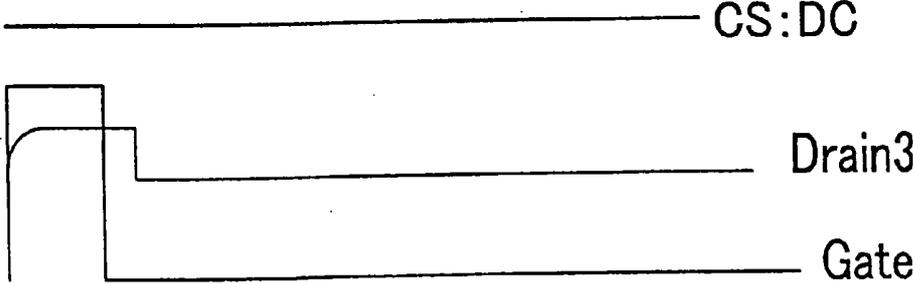


Fig.11-3

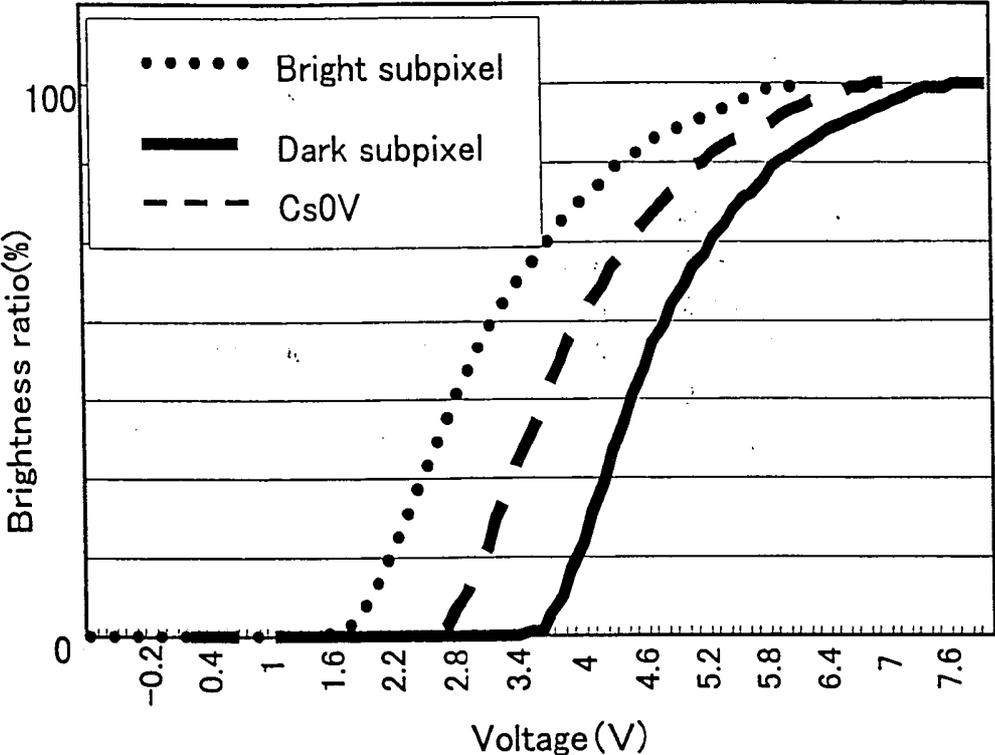


Fig.11-4A

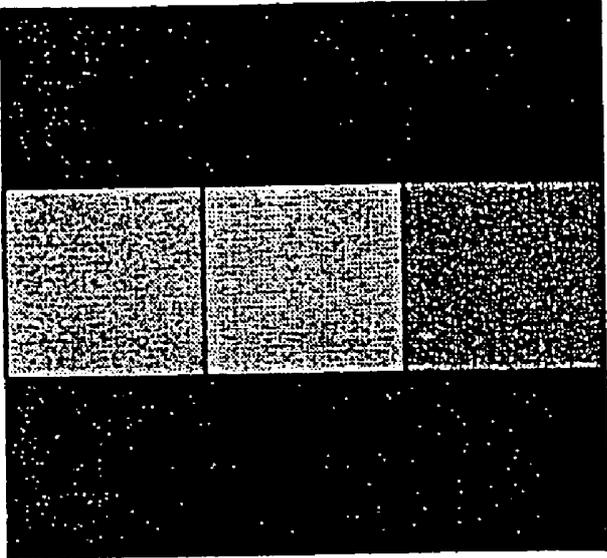


Fig.11-4B

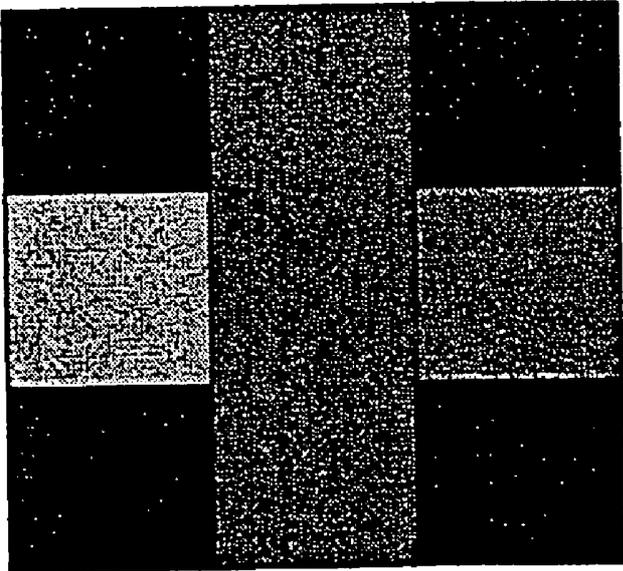


Fig.12-1

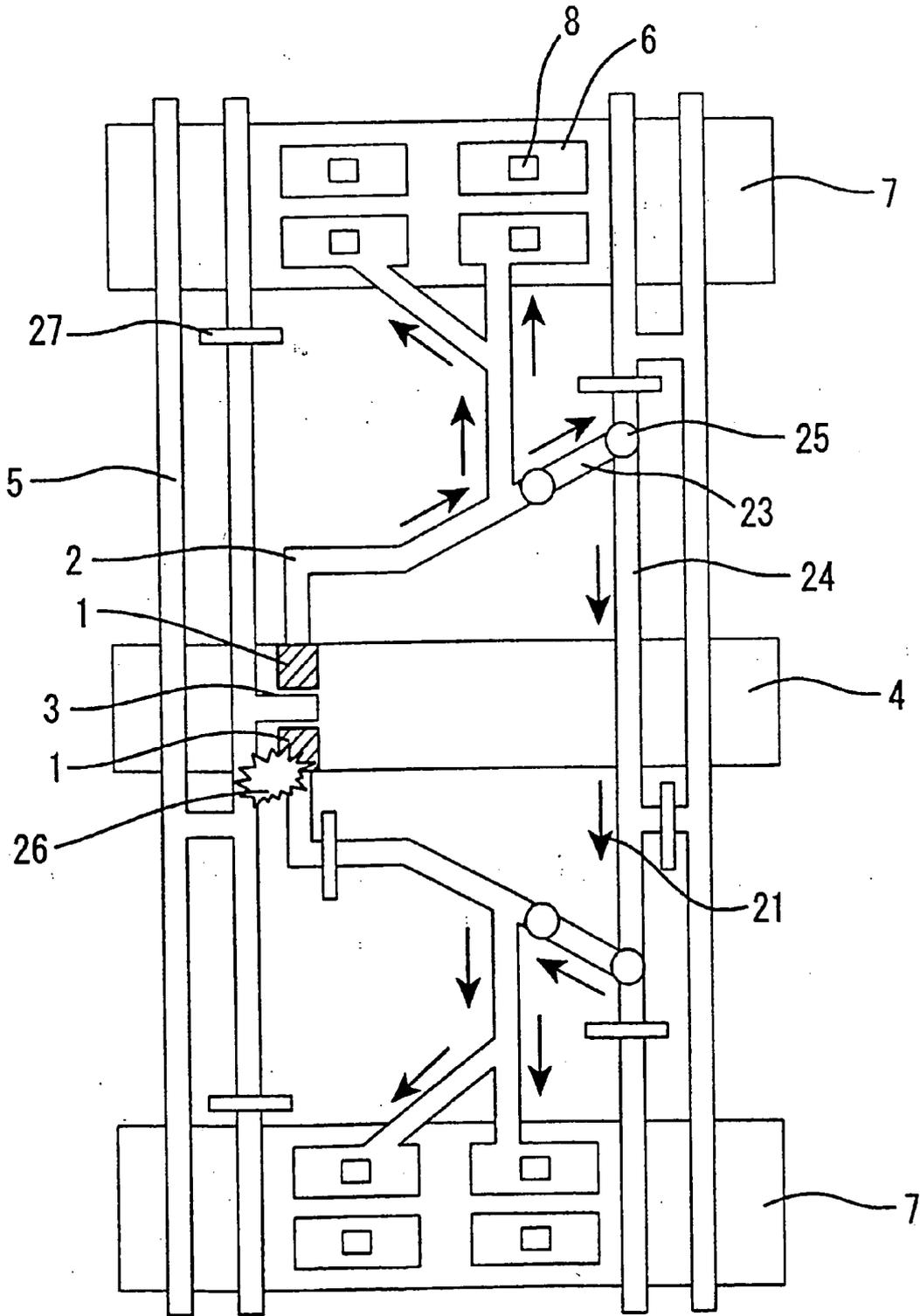


Fig.12-2A

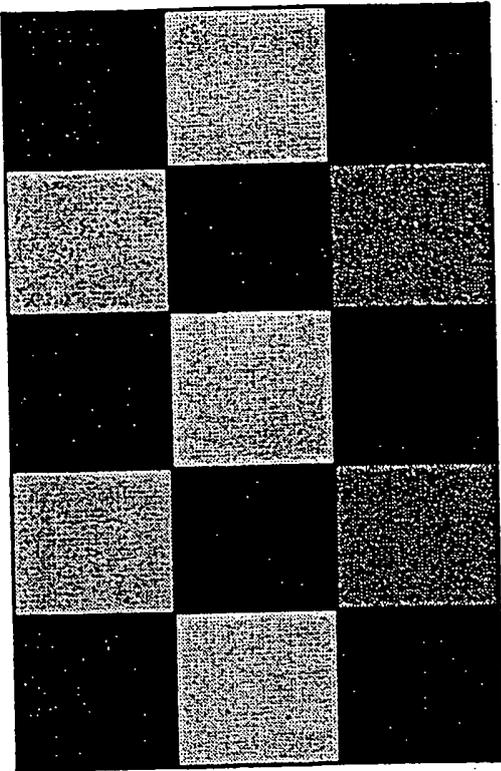


Fig.12-2B

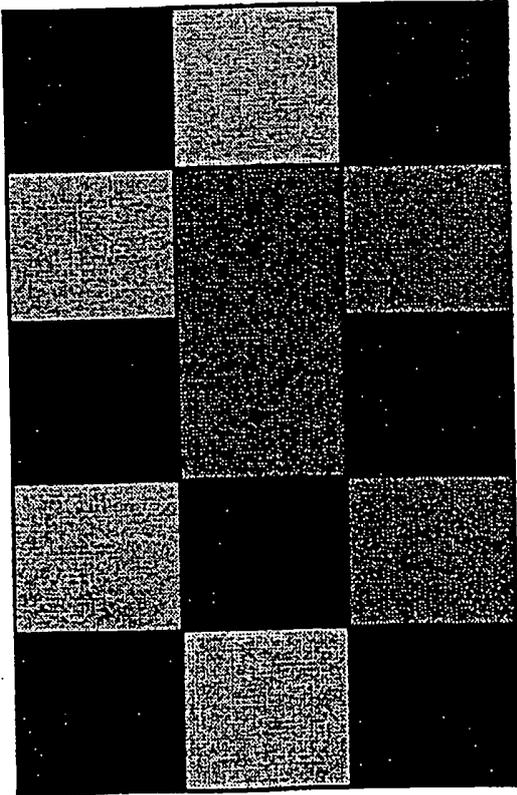


Fig.13-1

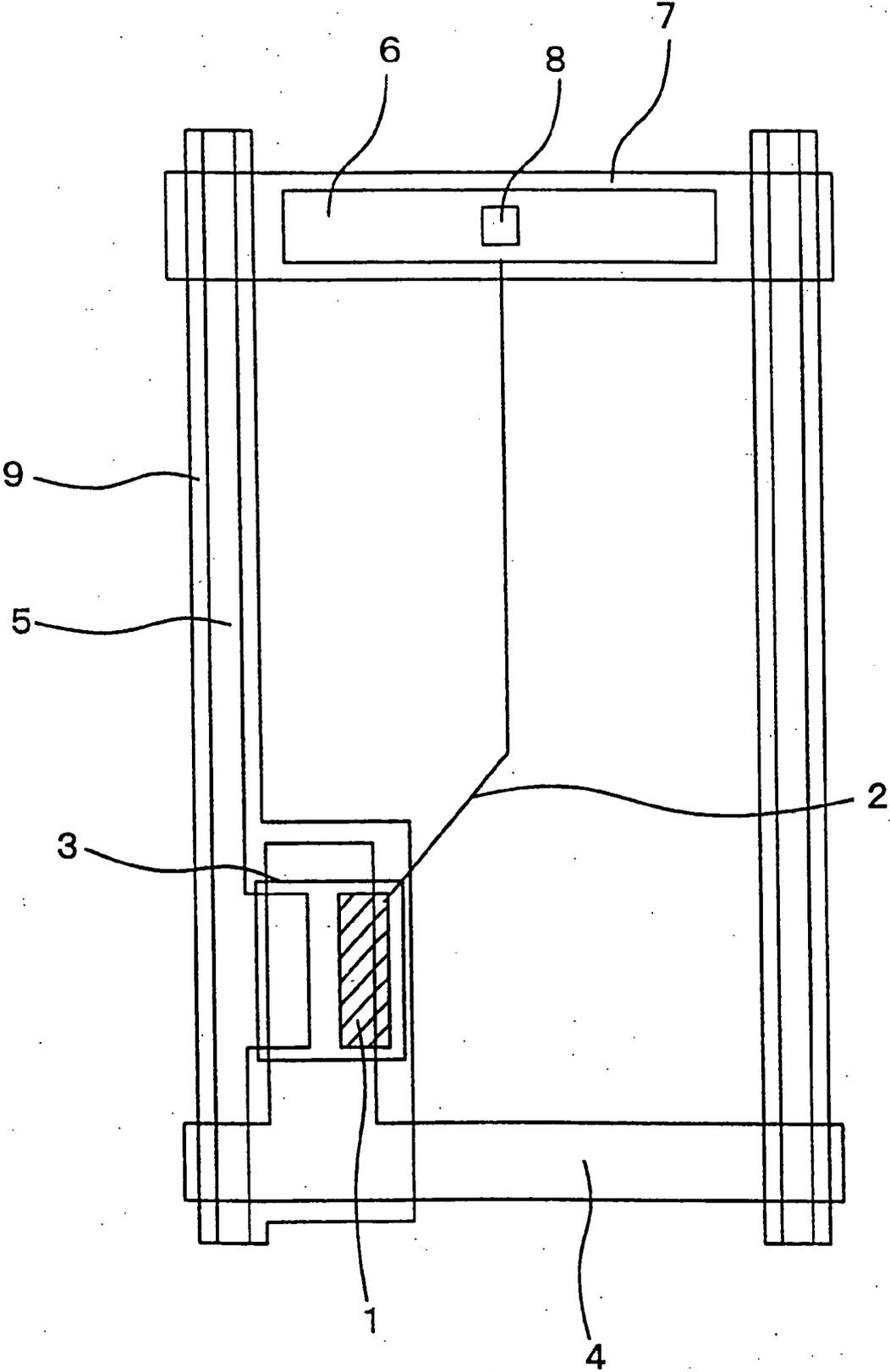
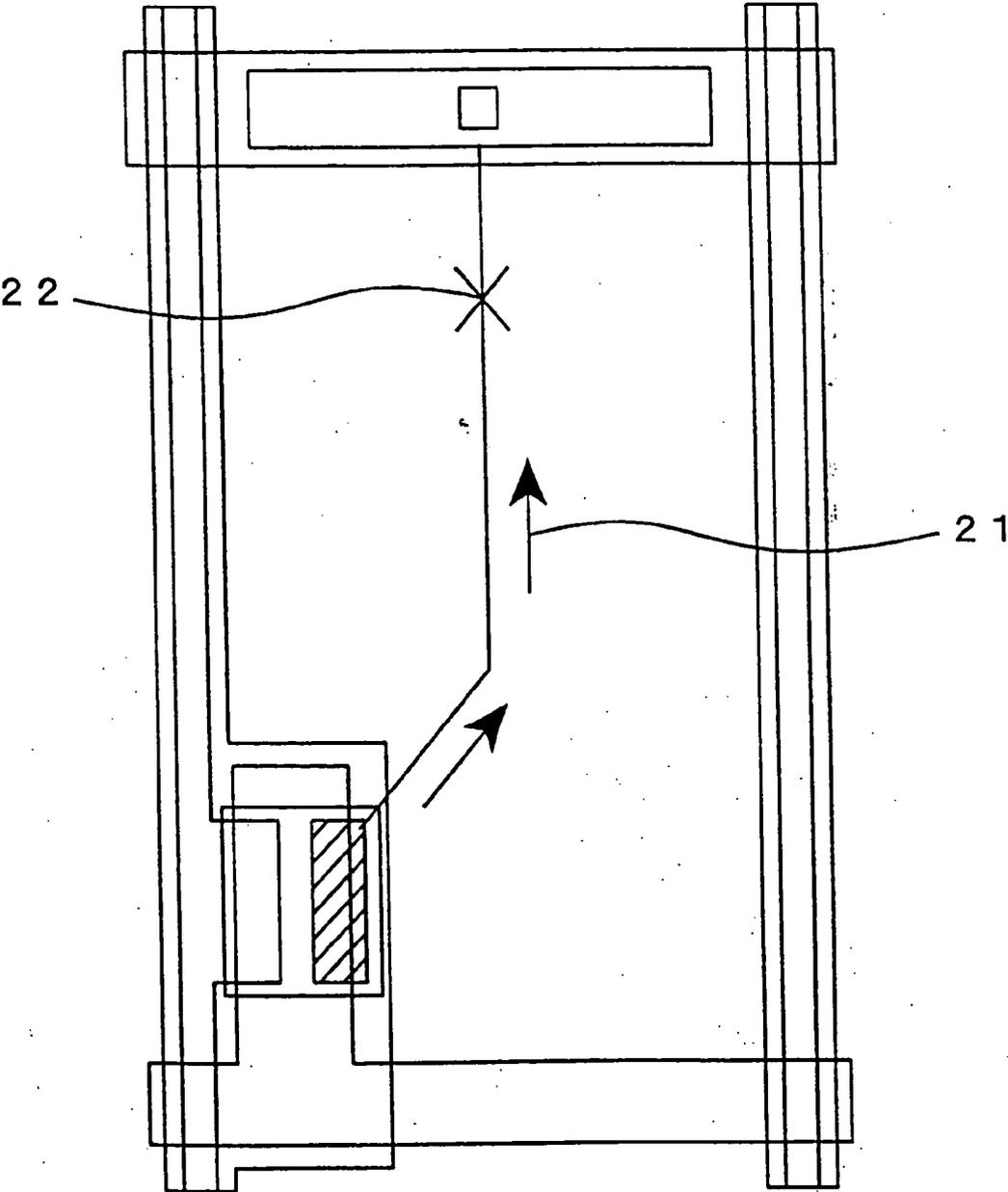


Fig.13-2



## ACTIVE MATRIX SUBSTRATE AND DISPLAY DEVICE

### REFERENCE TO RELATED APPLICATIONS

[0001] This Nonprovisional application claims priority under 35 U.S.C. § 119(a) on patent application Ser. No. 2004-20489 filed in Japan on Jan. 28, 2004 and patent application Ser. No. 2004-349031 filed in Japan on December 1, the entire contents of which are hereby incorporated by reference.

### BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to an active matrix substrate to be used in a display device, such as a liquid crystal display device or EL (electroluminescence) display device. More particularly, it relates to an active matrix substrate suited for use in large-size liquid crystal television or a like liquid crystal display device equipped with a large-size liquid crystal display panel.

[0004] 2. Description of the Related Art

[0005] Active matrix substrates are widely used in active matrix drive type display devices such as liquid crystal display devices and electroluminescence (EL) display devices. In such active matrix drive type display devices, active elements are disposed to form a matrix on respective independent pixel electrodes, and screen displaying is made by the active matrix drive method according to which the pixel electrodes are selectively driven by these active elements. Generally used as the active elements for selective driving of pixel electrodes are TFT (thin film transistors) elements, MIM (metal-insulator-metal) elements, MOS transistor elements, diodes, and varistors, among others, and screen displaying is made by switching the voltage applied to each pixel electrode and the corresponding opposing electrode to thereby optically modulate the display medium, such as a liquid crystal layer, EL display layer or plasma radiation layer, between both the electrodes. Such active matrix drive method enables high contrast displaying and is in practical use in liquid crystal televisions, personal computer terminal display devices, and so forth.

[0006] As the conventional active matrix substrate for use in a liquid crystal display device using such active matrix drive method, one in which the drain electrode of a TFT element is connected to the corresponding pixel electrode via a drain extraction line and a contact hole has been disclosed (cf. e.g. Japanese Kokai Publication H10-20298, pages 3 and 6, drawing 1). In this conventional display device, only one drain extraction line is formed for each pixel on the active matrix substrate and, in case of breaking of this one drain extraction line, the normal display of the corresponding pixel is not made any longer, which leads to the occurrence of an operation failure called pixel defect; the result is a decrease in the yield of liquid display devices. This is explained referring to the drawings. In the conventional active matrix substrate for a liquid display device, as shown in FIG. 13-1, breaking 22 of one drain extraction line, as shown in FIG. 13-2, results in inhibition of a data signal 21 from arriving at a pixel electrode for transmission from a source bus line 5 via a drain electrode 1 and the drain extraction line 2. As a result, a pixel defect occurs, and this

lowers the display quality of the liquid display device and causes a decrease in yield. As the cause of drain extraction line breaking, there may be mentioned, among others, a photo resist pattern defect in wiring pattern formation, and a defect in layer deposition in drain extraction line layer formation by sputtering, for instance.

[0007] As a technology of preventing the occurrence of pixel defects, a liquid crystal display device has been disclosed in which each pixel is provided with a plurality of thin film transistors (cf. e.g. Japanese Kokai Publication H07-199221, pages 3 and 6, drawing 1 and Japanese Kokai Publication 2002-350901, pages 13 and 20, drawing 9). However, to provide each pixel with a plurality of thin film transistors causes a decrease in aperture ratio and an increase in production cost; in these respects, there is room for improvement.

[0008] Further, a liquid crystal display device or the like in which an interconnection line (bridge) is disposed between two neighboring pixel electrodes to cope with the occurrence of a pixel defect by connecting the electrode of the defective pixel to the electrode of the neighboring normal pixel by means of that interconnection line has been disclosed (cf. e.g. Japanese Kokai Publication H02-135320, pages 3 and 4, drawing 1 and Japanese Kokai Publication H08-328035, pages 3 and 5, drawing 1). According to this technology, however, the interconnection line is disposed in a manner stepping across the gate line, so that the gray scale characteristics are deteriorated due to the increase in coupling capacity; in this respect, there is room for improvement.

[0009] In recent years, the liquid display panels in liquid crystal televisions and so forth have become larger and larger in size and, accordingly, the number of pixels has been increased; as a result, there is a tendency for the number of pixel defects to increase. The size of pixels is also increasing with the increase in size of the screen and, therefore, even when an abnormal bright spot, if discovered in the manufacturing process, is converted to a dark spot, as is conventional in the art, users will be able to readily recognize, by the eye, not only the luminescent spot but also the dark spot as a pixel defect. Under such circumstances, a novel technology has been demanded for improving the display quality by effectively inhibiting pixel defects from occurring and thereby improving the yield.

### SUMMARY OF THE INVENTION

[0010] The present invention has been made in view of the problems discussed above. Accordingly, it is an object of the present invention to provide an active matrix substrate in which drain extraction lines of active elements can be prevented from breaking while suppressing the decrease in aperture ratio and the increase in manufacturing cost, and a display device using such substrate.

[0011] As a result of various investigations made by them in an attempt to create an active matrix substrate in which drain extraction lines of active elements can be prevented from breaking, the present inventors came to realize that when each drain extraction line is provided with at least two routes, the possibility of an active element being insulated from the corresponding storage capacitor upper electrode by breaking of a part of the corresponding drain extraction line can be satisfactorily reduced without lowering the aperture

ratio or increasing the manufacturing cost. Based on this finding, the present invention has now been completed.

[0012] Thus, the present invention provides an active matrix substrate comprising an active element connected, via a drain extraction line, to a storage capacitor upper electrode, wherein the drain extraction line has at least two routes.

#### BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1-1 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention.

[0014] FIG. 1-2 is a schematic plan view illustrating a condition of drain line breaking 22 in the active matrix substrate shown in FIG. 1-1.

[0015] FIG. 2 is a schematic sectional view illustrating the section along the broken line A-A' of the active matrix substrate shown in FIG. 1-1.

[0016] FIG. 3 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which the MVA (multi-domain vertical alignment) system is used.

[0017] FIG. 4 is a schematic sectional view illustrating the section along the broken line B-B' of the active matrix substrate shown in FIG. 3.

[0018] FIG. 5-1 is a schematic plan view illustrating another example of the branched structure in the active matrix substrate of the invention.

[0019] FIG. 5-2 is a schematic plan view illustrating the result of drain line breaking 22 in the active matrix substrate shown in FIG. 5-1.

[0020] FIG. 6-1 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which three drain electrodes 1 are provide for each pixel.

[0021] FIG. 6-2 is a schematic plan view illustrating the result of drain line breaking 22 in the active matrix substrate shown in FIG. 6-1.

[0022] FIG. 7-1 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which a dummy TFT element 20 is employed.

[0023] FIG. 7-2 is a schematic plan view illustrating the result of drain line breaking 22 in the active matrix substrate shown in FIG. 7-1.

[0024] FIG. 8 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which drain extraction lines or routes 2 are disposed each below a slit provided in each pixel electrode.

[0025] FIG. 9 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which drain extraction lines or routes 2 are disposed at those sites which are opposite to slits provided in each opposing electrode of a color filter substrate.

[0026] FIGS. 10A to 10F each is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention.

[0027] FIG. 11-1 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which a divided pixel (subpixel) structure is employed.

[0028] FIG. 11-2A is a schematic representation of signal waveforms to be applied to a bright subpixel, FIG. 11-2B is a schematic representation of signal waveforms to be applied to a dark subpixel, and FIG. 11-2C is a schematic representation of signal waveforms to be applied to both subpixels after drain/drain interconnection. In the FIGS. CS1, CS2 and CS:DC denote the Cs signal waveforms to be applied to the bright subpixel, dark subpixel and synthesized subpixel, respectively; Drain 1, Drain 2 and Drain 3 denote the drain signal waveforms to be applied to the bright subpixel, dark subpixel and synthesized subpixel, respectively, and Gate denotes the gate signal waveform.

[0029] FIG. 11-3 is a representation of V-T characteristics of the respective subpixels before drain/drain interconnection and after drain/drain interconnection.

[0030] FIG. 11-4A is an ordinary gray-scale image pattern in the active matrix substrate shown in FIG. 11-1, and FIG. 11-4B is a gray-scale image pattern upon drain/drain interconnection of the subpixel on line 2, column 2 and the subpixel on line 3, column 2.

[0031] FIG. 12-1 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which a divided pixel structure is employed.

[0032] FIG. 12-2A is an ordinary gray-scale image pattern in the active matrix substrate shown in FIG. 12-1, and FIG. 12-2B is a gray-scale image pattern upon drain/drain interconnection of the subpixels in column 2.

[0033] FIG. 13-1 is a schematic plan view illustrating an example of the structure of the drain extraction line 2 in the active matrix substrate constituting the conventional liquid crystal display device.

[0034] FIG. 13-2 is a schematic plan view illustrating the result of drain line breaking 22 in the active matrix substrate shown in FIG. 13-1.

#### EXPLANATION OF SYMBOLS

- [0035] 1: Drain electrode
- [0036] 2: Drain extraction line
- [0037] 3: TFT element
- [0038] 4: Gate bus line
- [0039] 5: Source bus line
- [0040] 6: Storage capacitor upper electrode
- [0041] 7: Cs bus line
- [0042] 8: Contact hole
- [0043] 9: Black matrix (light shielding layer)
- [0044] 10: Active semiconductor layer (i layer)
- [0045] 11: Amorphous silicon layer (n<sup>+</sup> layer)

- [0046] 12: Interlayer insulation layer
- [0047] 13: Gate insulator
- [0048] 14: Transmission pixel-electrode
- [0049] 15: Liquid crystal layer
- [0050] 16: Glass substrate
- [0051] 17: Color layer
- [0052] 18: Counter electrode
- [0053] 19: Alignment controlling protrusion (on color filter substrate side)
- [0054] 20: Dummy TFT element
- [0055] 21: Data signal
- [0056] 22: Drain line breaking
- [0057] 23: Floating island electrode
- [0058] 24: Source ladder
- [0059] 25: Overlapping portion
- [0060] 26: SD leak site
- [0061] 27: Cleaving site
- [0062] 30: Slit provided on pixel electrode (on active matrix substrate side)
- [0063] 40: Slit provided on pixel electrode (on color filter substrate side)
- [0064] 50: Slit provided on pixel electrode (on active matrix substrate side)

#### PREFERRED EMBODIMENTS

[0065] As the above-mentioned active elements, there may be mentioned, among others, TFT (thin film transistor) elements, MIM (metal-insulator-metal) elements, MOS transistor elements, diodes, and varistors. When TFT elements, for instance, are used, they are disposed, to form a matrix, at points of crossing of scanning signal lines and data signal lines, each scanning signal line is connected to each corresponding gate electrode, each data signal line is connected to each corresponding source electrode, and a drain extraction line is connected to the drain electrode. In this way, it is possible to cause scanning signals successively fed to a plurality of scanning signal lines crossing a plurality of data signal lines to sample data signals simultaneously fed to the data signal lines and thus use the active elements as switches for selectively driving pixel electrodes. The material of the drain extraction lines is not particularly restricted but may be any conductive material. Judiciously used are films of such metals as titanium, chromium, aluminum and molybdenum, or alloys of such metals, and laminates thereof. As for the method of forming drain extraction lines, the method comprising forming them by subjecting such a metal layer or laminate as mentioned above to photolithography and etching is judiciously used.

[0066] Suited for use as the storage capacitor upper electrodes are those each of which is provided so as to oppose a storage capacitor lower electrode comprising a storage capacitor line or scanning signal line or the like at least via an insulation layer and constitute a storage capacitor (Cs) element therewith. The storage capacitor element can be

used for storing the data signal fed to the data signal line since the storage capacitor upper electrode is connected to the active element via the drain extraction line.

[0067] The constitution of the active matrix substrate of the present invention is not particularly restricted but may comprise another or other constituent elements provided that it is constituted of those constituent elements mentioned above as essential ones. However, the mode of practice in which each pixel electrode is connected to the corresponding storage capacitor upper electrode via a contact hole is desirable. In this mode of practice, it becomes possible to optically modulate the display medium, such as a liquid crystal layer, EL emission layer or plasma radiation layer, to make screen displaying by applying a voltage switched by each active element between the corresponding pixel electrode and the opposing electrode opposite thereto. To form the contact hole on the storage capacitor upper electrode on the storage capacitor lower electrode pattern is preferred since any further decrease in aperture ratio will not result then.

[0068] In accordance with the present invention, each drain extraction line has at least two routes. As the form of such drain extraction line, there may be mentioned (1) the form in which one drain extraction line connected to the active element is branched into two or more lines and each of them is connected to the storage capacitor upper electrode, (2) the form in which two or more drain extraction lines connected to the active element are joined into one line and connected to the storage capacitor upper electrode, and (3) the form in which two or more drain extraction lines connected to the active element, with or without cross-linking, are connected to the storage capacitor upper electrode. Among them, the form (3) is preferred. By giving such a form to the drain extraction line in accordance with the present invention, it becomes possible to satisfactorily reduce the possibility of the active element being insulated from the storage capacitor upper electrode due to breaking of a part of the drain extraction line, since the signal from the active element is now sent to the storage capacitor upper electrode via two or more conducting routes. The above-mentioned drain extraction line wiring pattern is preferably one connecting the drain electrode of the active element to the storage capacitor upper electrode via two or more routes and, when the active element has two or more drain electrodes, each of the two or more drain electrodes of the active element is preferably connected to the storage capacitor upper electrode via two or more routes. When such active matrix substrates are used as the pixel electrode substrates for use in such display devices as liquid crystal display devices and EL (electroluminescence) display devices, the occurrence of pixel defects in images displayed as resulting from drain extraction line breaking can be effectively prevented, the display quality of the display devices can be prevented from lowering, and the yield can be improved.

[0069] Some preferred embodiments of the active matrix substrate of the invention are described below.

[0070] In the practice of the invention, the drain extraction line is preferably disposed at those sites corresponding to a protrusion and/or an electrode-free area provided on at least one of the active matrix substrate and the substrate facing the active matrix substrate. Thus, in the practice of the invention, the protrusion and/or electrode-free area pattern is

preferably at least partly overlapping the drain extraction line pattern. In cases where the substrate facing the active matrix substrate is provided with protrusions and/or electrode-free areas, it is preferred that the protrusion and/or electrode-free area pattern and the drain extraction wiring pattern be at least partly overlapping with each other in the state of panel alignment of the active matrix substrate and opposite substrate. As the protrusions, there may be mentioned, among others, those formed in the form of ribs, for instance, on the opposing faces of both the substrates. As the electrode-free areas, there may be mentioned, among others, those formed in the form of slits, for instance, in the pixel electrodes on the active matrix substrate or the common electrode on the substrate facing the active matrix substrate. Such forms are judiciously used in applying the active matrix substrate of the present invention to a liquid crystal display device in which liquid crystal molecules are horizontally or vertically aligned between both the active matrix substrate and color filter substrate when no voltage is applied and to a liquid crystal display device under the MVA (multi-domain vertical alignment) system where liquid crystal molecules are vertically aligned between both the substrates when no voltage is applied and each pixel is divided into a plurality of domains and, in this case, the protrusions and electrode-free areas are preferably utilized for controlling the alignment of liquid crystal molecules. By disposing the drain extraction lines at positions corresponding to the protrusions and/or electrode-free areas, which are generally not used effectively as aperture areas, in the practice of the invention, the aperture ratio can be prevented from lowering due to making each drain extraction line have a plurality of routes. In a more preferred embodiment, the drain extraction lines are disposed at positions corresponding to the protrusions. When the drain extraction lines are disposed at positions corresponding to the electrode-free areas in the active matrix substrate, there arise the possibilities of the effect of the electrode-free areas in controlling the alignment of liquid crystal molecules becoming lessened and the speed of response of liquid crystal molecules being reduced.

[0071] The MVA system is a system under which each pixel is divided into a plurality of domains so that the viewing angle characteristics of a vertical alignment type liquid crystal display device may be improved. In the liquid crystal display device on the MVA system, bank-like protrusions (protrusion for alignment control) are generally formed on the respective facing surfaces of two substrates, and the direction of tilting of liquid crystal molecules is specified and the domain border positions are restricted by means of those alignment controlling protrusions.

[0072] In a preferred embodiment of the practice of the invention, each of the active elements has at least two drain electrodes. Such wiring structure of active elements can be appropriately combined with the form in which two or more drain extraction lines are connected to each active element. In such a structure, it is possible to more satisfactorily produce the effects of the invention while preventing the aperture ratio from lowering due to provision of a plurality of active elements for each pixel. In other words, that an active element has two or more drain electrodes is equivalent to the fact that the active element has the same number of, namely two or more, channels as the drain electrodes. Therefore, in this mode of embodiment, even if a defect, such as short circuiting, is found in a certain channel, an attempt can be made to amend the defective pixel by

utilizing another normal channel in the same active element. More specifically, in case of a leak (short circuiting) between the source electrode and drain electrode in a certain channel, for instance, the drain extraction line connected to that channel is cut off from the drain electrode, and the drain extraction line cut off is connected to the drain extraction line connected to a normal channel (drain/drain interconnection), whereby almost the same drain potential can be applied to all the drain extraction lines.

[0073] The number of gate electrodes may be one or two or more.

[0074] From the viewpoint of prevention of the aperture ratio from lowering, one active element is preferably provided in each driving area (pixel or subpixel). In the embodiment in which two or more active elements are provided in each driving area, the drain extraction line pattern is preferably such that each of the drain electrodes of the two or more active elements is connected to the storage capacitor upper electrode via two or more routes.

[0075] The active matrix substrate of the invention preferably has a structure such that a pixel is constituted of at least two subpixels and the pixel electrodes in the at least two subpixels have a structure such that they are connected to the respective different drain electrodes each via a storage capacitor upper electrode and a drain extraction line. Such mode of embodiment in which each pixel (picture element) is constituted of two or more subpixels, namely the mode of embodiment utilizing the so-called divided pixel system, is advantageous from the viewpoint of amendment of defective pixels, such as bright defects.

[0076] In cases where the above divided pixel system is applied, each pixel preferably comprises subpixels differing in brightness. In this mode of embodiment in which both a bright subpixel and a dark subpixel exist in each pixel, intermediate gray scales can be expressed by means of area gradation and, therefore, this mode is suitable for attaining improvements with respect to the whitening on the liquid crystal display panel at oblique viewing angles. Briefly, the area gradation is effected by capacity coupling of the liquid crystal capacity (Clc), the Cs capacity (Ccs), and the polarity and amplitude (Vsd) of Cs, and this is expressed by the formula "capacity of bright subpixel=Vs+K(Vs)×Vsd, K=Ccs/Clc(Vs)+Ccs", where Vs is the voltage value of the signal fed from the source.

[0077] Further, in cases where the divided pixel system is applied, the active matrix substrate of the invention is preferably such that at least two storage capacitor lower electrodes have a structure such that they are overlapping, via an insulation layer, with the respective storage capacitor upper electrodes corresponding to different subpixels. Such mode of embodiment is suitable for forming bright subpixels and dark subpixels. The term "signal voltages opposite in phase to each other to be applied to two or more storage capacitor lower electrodes" means the Cs waveform voltages used for operating the area gradation in each pixel with a divided pixel structure and includes two species, namely the Cs waveform voltage (Cs polarity +) contributing to pushing up the drain signal voltage (Vs) fed from the source at timing for capacity coupling when the gate signal is off, and the Cs waveform voltage (Cs polarity -) contributing to pushing down the Vs. In such divided pixel system (area gradation technology), it is possible to vary the effective

voltage applied to each pixel on a subpixel to subpixel basis by capacity coupling of the Cs waveform voltage, Cs capacity and liquid crystal capacity to thereby form bright and dark subpixels and thus realize multiple driving of these. The details of such divided pixel system (area gradation technology) are disclosed in Japanese Kokai Publication 2004-62146, for instance.

[0078] As the divided pixel structure, there may be mentioned, for example, the 1:1 pixel division structure in which the area of the bright subpixel and the area of the dark area are equal to each other, and the 1:3 pixel division structure in which the area of the bright subpixel is one third the area of the dark subpixel. Among them, the 1:3 pixel division structure is particularly effective as a measure for whitening at oblique viewing angles.

[0079] The active matrix substrate of the invention is preferably one in which there is provided, for each pixel, an interconnection electrode for amendment having a structure overlapping, via an insulation layer, with at least two drain extraction lines connected to respective different drain electrodes. In this mode of embodiment, even when a defect is found in a channel involving a thin film transistor, for instance, it is possible to cut off the drain extraction line connected to that channel from the drain electrode and then connect the drain extraction line cut off to a drain extraction line connected to a normal channel (drain/drain interconnection) to thereby apply almost the same drain potential to the pixel electrode of the subpixel whose defect has been corrected and that of the subpixel used for defect correction. The layer in which the interconnection electrode for amendment is formed is preferably the same layer as that in which the scanning signal line (gate bus line) is formed, and the interconnection electrodes are preferably formed in the form islands simultaneously with the patterning of the scanning signal lines.

[0080] In the above-mentioned mode of embodiment in which interconnection electrodes for amendment are provided, the active matrix substrate of the invention preferably has a structure such that any two of the storage capacitor upper electrodes overlapping, via an insulation layer, with the corresponding storage capacitor lower electrode to which signal voltages opposite in phase to each other are to be applied are interconnected via a drain extraction line and an interconnection electrode for amendment. According to this mode, the storage capacitor upper electrodes overlapping the storage capacitor lower electrode to which Cs signals (electric signals fed to the storage capacitor lower electrode) given as signal voltages opposite in phase to each other are to be applied are connected to each other; therefore, in the synthetic subpixel newly formed by the subpixel whose defect has been corrected and the subpixel used for the amendment, it becomes possible to apply direct current voltage Cs signals to the storage capacitor element synthesized, with the result that gradation characteristics intermediate between both can be obtained and a gray scale equivalent to that of the surrounding ordinary pixels can be obtained.

[0081] In such mode of embodiment, for securing the display quality of the pixel comprising the synthetic subpixel, the storage capacitor upper electrode connected to the drain extraction line and interconnection electrode for amendment is preferably connected to the pixel electrode of

the neighboring subpixel. The storage capacitor lower electrode is preferably provided as an independent wiring pattern (storage capacitor wiring pattern), and this makes it possible to secure the degree of freedom in driving pattern selection.

[0082] The interconnected structure mentioned above is to be formed only partly in those pixels showing a defect but need not be formed in all pixels.

[0083] The active matrix substrate of the invention has a structure such that a scanning signal line is connected to the gate electrode of an active element, and the above-mentioned drain extraction line and interconnection electrode for amendment preferably have a structure not overlapping with the scanning signal line. In this mode of embodiment, the interconnection electrode for amendment does not cross the scanning signal line even after drain/drain interconnection; therefore, the coupling capacity between that electrode and the scanning signal line can be effectively prevented from increasing, and the display quality of the subpixel whose defect has been corrected by drain/drain interconnection can be improved.

[0084] In the practice of the invention, the storage capacitor upper electrode is preferably constituted of at least three divided electrodes in the area facing the corresponding storage capacitor lower electrode. In this mode of embodiment, even in case of short circuiting of the storage capacitor upper electrode with the storage capacitor lower electrode facing thereto via an insulating layer as caused by a conductive foreign matter or a pinhole or in case of short circuiting thereof with the data signal line formed in the same step, it is possible to electrically separate only the divided electrode including the site of short circuiting to thereby allow the remaining divided electrodes effectively and allow the storage capacitor element to maintain the function thereof. Further, both end portions of the storage capacitor upper electrode are generally subject to short circuiting because of the disposition of data signal and other lines. Even in case of two divided electrodes on both ends having been involved in short circuiting, it is possible to allow the remaining divided electrode(s) to function effectively by carrying out an isolation treatment separating only the short-circuiting electrode to thereby maintain the function of the storage capacitor element. Therefore, when such active matrix substrate is used as the pixel electrode substrate in a display device such as a liquid crystal display device, the occurrence of pixel defects in the image displayed as caused by short circuiting of the storage capacitor upper electrode can be effectively inhibited.

[0085] The present invention also provides a display device equipped with the above active matrix substrate. As a result of the use of the above active matrix substrate as the pixel electrode substrate, such display devices can be manufactured in a high yield while the occurrence of pixel defects in displayed images as caused by drain extraction line breaking is effectively suppressed and the display quality is prevented from lowering. The above display device is preferably a liquid crystal display device, among others. Such liquid crystal display device generally comprises a liquid crystal layer sandwiched between the above active matrix substrate and a substrate having a color filter layer formed thereon, and predetermined voltages can be applied to the liquid crystal layer via the active elements.

[0086] The active matrix substrate of the invention has the constitution described hereinabove, and each drain extraction line has at least two routes and, therefore, the signal from the active element is sent to the storage capacitor upper electrode via at least two conducting routes. As a result, the possibility of the active element and storage capacitor upper electrode being insulated as a result of partial drain extraction line breaking can be reduced. When such active matrix substrate is used as the pixel electrode substrate in a display device such as a liquid crystal display device or EL (electroluminescence) display device, the occurrence of pixel defects in displayed images as resulting from drain extraction line breaking can be effectively suppressed, the display quality of the display device can be inhibited from lowering, and the yield can be improved.

[0087] The following examples, which are described referring to the drawings attached hereto, illustrates the present invention in further detail. These examples are, however, by no means limitative of the scope of the invention.

[0088] First, referring to the liquid crystal display devices described in the examples, the active matrix substrate and color filter substrate are described referring to FIGS. 1-1, 2, 3, 4, 5-1, 6-1 and 7-1.

[0089] FIG. 1-1 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention, and FIG. 2 is a schematic sectional view illustrating the section along the broken line A-A' of the active matrix substrate shown in FIG. 1-1. FIG. 3 is a schematic plan view illustrating an example of the branched structure in the active matrix substrate of the invention in which the MVA system is used, and FIG. 4 is a schematic sectional view illustrating the section along the broken line B-B' of the active matrix substrate shown in FIG. 3. FIGS. 5-1, 6-1 and 7-1 each independently is a schematic plan view illustrating another example of the structure of the drain extraction line 2 in the active matrix substrate of the invention.

[0090] (Structure of the Active Matrix Substrate)

[0091] As shown in FIGS. 1-1 and 2, one TFT (thin film transistor) element 3 is disposed, as the active element, for each pixel in the active matrix substrate. A gate bus line 4 as a gate line for feeding a gate signal to the TFT element 3 and a source bus line 5 as a source line for feeding a data signal 21 to the TFT element 3 are disposed each perpendicularly to the TFT element 3 in each pixel. There is also formed a rectangular storage capacitor upper electrode 6 on an extension of a drain electrode 1 of the TFT element 3 and a line (drain extraction line) 2 extracted from the drain electrode 1. Below the storage capacitor upper electrode 6, there is formed, independently of the gate bus line 4 and in parallel to the gate bus line 4, a Cs bus line 7 as a storage capacitor line for forming a storage capacitor Cs with the storage capacitor upper electrode 6. Between the storage capacitor upper electrode 6 and Cs bus line 7, there is formed a gate insulator 13. The storage capacitor upper electrode 6 is electrically connected to the drain electrode 1 and overlapping with the Cs bus line 7 via the gate insulator 13 to form a storage capacitor. A contact hole 8 serves to connect a transmission pixel electrode 14 to the storage capacitor upper electrode 6.

[0092] (Structure of the Color Filter Substrate)

[0093] In the color filter substrate, a color layer 17 is formed on the surface, facing a liquid crystal layer 15, of a color filter side glass substrate 16, and a counter electrode 18 made of a transparent electrode is formed on the liquid crystal layer 15 side surface of the color layer 17, as shown in FIG. 2. In the case of a liquid crystal display device of the MVA system, an alignment controlling protrusion 19 for controlling the alignment of liquid crystal molecules in the liquid crystal layer 15 is formed on the liquid crystal layer 15 side surface of the counter electrode 18, as shown in FIG. 4. The voltage controlled by the TFT element 3 is applied to the transmission pixel electrode 14 via the contact hole 8 by means of the drain extraction line 2 and drives the liquid crystal layer 15 by the potential difference from the counter electrode 18 in the color filter substrate.

[0094] The drain extraction line 2 connected to the storage capacitor upper electrode 6 has two or more routes, as shown in FIG. 1-1. In other words, the drain extraction line 2 is branched into a plurality of lines to form a branch structure. In the case of a liquid crystal display device of the MVA system, the drain extraction line 2 having a branch structure is disposed so as to be located below the alignment controlling protrusion 19, as shown in FIG. 3. In the case of a liquid crystal display device of the MVA system, the drain extraction line 2 in FIG. 5-1, 6-1 or 7-1 is disposed so as to be located below the alignment controlling protrusion 19 in the same manner as shown in FIG. 3.

[0095] In FIG. 1-1 and other figures, TFT elements are used as the active elements of the active matrix substrate but this has no limitative meaning. In FIG. 1-1 and other figures, the number of drain extraction lines 2 connected to the storage capacitor upper electrode 6 is two or three. The number is not limited thereto but may be one or more.

[0096] (Method for Manufacturing the TFT Substrate)

[0097] Now, referring to FIG. 2, a method for manufacturing the active matrix substrate (TFT substrate) using TFT elements as the active elements is described.

[0098] First, using a film of a metal such as titanium, chromium, aluminum or molybdenum or an alloy thereof or a laminate thereof, the gate bus line 4 and Cs bus line 7 are formed on a glass substrate 16, which is an insulator, in one and the same step. Then, on the surfaces of these, a gate insulator 13 made of a silicon nitride, silicon oxide or like insulator layer is formed, followed by formation of a high resistivity semiconductor layer (i layer) 10 of amorphous silicon or polysilicon, for instance, and of a low resistivity semiconductor layer (n<sup>+</sup> layer) 11 of impurity-doped n<sup>+</sup> amorphous silicon, for instance, and further followed by simultaneous patterning of i/n<sup>+</sup> layers. Then, the source bus line 5, drain electrode 1, drain extraction line 2 and storage capacitor upper electrode 6 are formed simultaneously using a film of a metal such as titanium, chromium, aluminum or molybdenum or an alloy thereof or a laminate thereof. On that occasion, the structure of the drain extraction line 2 is patterned in a branch form. Thereafter, the n<sup>+</sup> layer 11 on the TFT element 3 is subjected to etching for source/drain separation. In this step, the TFT element 3 formation is completed.

[0099] Then, an interlayer insulation film 12 is formed of an acrylic resin, silicon nitride, silicon oxide or the like so as to cover all the surface of the glass substrate 16 processed

in such steps as mentioned above. The contact hole **8** is then formed for connecting the transmission pixel electrode **14** to the storage capacitor upper electrode **6** for driving the liquid crystal layer **15** and realizing the connection of the storage capacitor. Thereafter, a transparent electrode (transmission pixel electrode) **14** is formed of a transparent conductive film, such as an ITO (indium tin oxide), IZO (indium zinc oxide), zinc oxide or tin oxide film, followed by patterning for obtaining an independent transmission pixel electrode **14** for each pixel. In this way, the active matrix substrate (TFT substrate) shown in **FIG. 2** can be obtained.

**[0100]** (Method for Manufacturing the Color Filter Substrate)

**[0101]** Referring to **FIG. 2** and **FIG. 4**, a method for manufacturing the color filter substrate is now described.

**[0102]** First, on a glass substrate **16**, which is an insulator, there are formed red, green and blue color layers **17** in each area corresponding to the transmission pixel electrode **14** in the TFT substrate using photosensitive resin compositions prepared by dispersing each pigment in an acrylic resin, and a black matrix **9**, which is a light-shielding layer, is formed in areas corresponding to the gap between the transmission pixel electrodes **14**, source bus line **5** and TFT element **3**. The color layers **17** are formed so as to be disposed without overlapping with one another. Then, the counter electrode **18**, which is a transparent electrode for driving the liquid crystal layer **15**, is formed so as to cover the black matrix **9** and respective color layers **17** utilizing a transparent conductive film, such as an ITO, IZO, zinc oxide or tin oxide film. In the case of a color filter substrate for use in a liquid crystal display device of the MVA system, alignment controlling protrusions **19** are then formed of an inorganic silicon compound, for instance, for the purpose of determining a specified direction of tilting of liquid crystal molecules and of restricting the domain boundary positions.

**[0103]** (Method for Manufacturing the Liquid Display Device)

**[0104]** First, an alignment layer of a polyimide resin is formed on the TFT substrate and color filter substrate obtained as described above. Then, spacers are sprayed at specified positions on the TFT substrate, a sealing material is applied to predetermined sites on the color filter substrate, the two substrates are subjected to panel alignment, and the sealing material is cured. Then, the panel obtained is cut to a predetermined size, and the liquid crystal display panel is manufactured by filling with a liquid crystal material, filling port sealing, panel cleaning, annealing treatment, and polarizer sticking. The liquid crystal display device is completed by further equipment with a liquid crystal driving IC, a power source circuit, a backlight, input and output line systems, etc.

#### EXAMPLE 1

**[0105]** Referring to the active matrix substrate for a liquid crystal display device as obtained in the above manner, the drain extraction line **2** connected to the storage capacitor upper electrode **6** is formed so as to comprise two lines, as shown in **FIG. 1-1**, on the occasion of forming, in each pixel, the branch structure of the drain extraction line **2** branched into a plurality of lines. In this case, the electrical connection between the drain electrode **1** of the TFT element

**3** and the storage capacitor upper electrode **6** can be secured even on the occasion of occurrence of the drain line breaking **22** at one site, as shown in **FIG. 1-2**.

#### EXAMPLE 2

**[0106]** Referring to the active matrix substrate for a liquid crystal display device as obtained in the above manner, the drain extraction line **2** connected to the storage capacitor upper electrode **6** is formed so as to comprise three lines, as shown in **FIG. 5-1**, on the occasion of forming, in each pixel, the branch structure of the drain extraction line **2** branched into a plurality of lines. In this case, the electrical connection between the drain electrode **1** of the TFT element **3** and the storage capacitor upper electrode **6** can be secured even on the occasion of occurrence of the drain line breaking **22** at one site, as shown in **FIG. 5-2**.

#### EXAMPLE 3

**[0107]** Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, three drain electrodes **1** are provided to give a redundant structure in preparation for deviations and errors in finish and the drain extraction lines **2** in each pixel area are all branched into a plurality to give a branch structure such that each drain electrode **1** is connected to the storage capacitor upper electrode **6** via at least two routes, as shown in **FIG. 6-1**, so that the lowering in display quality as caused by parasitic capacitances Cgd may be prevented.

**[0108]** In this case, the electrical connection between the drain electrode **1** of the TFT element **3** and the storage capacitor upper electrode **6** can be secured even on the occasion of occurrence of the drain extraction line breaking **22** at one site, as shown in **FIG. 6-2**.

#### EXAMPLE 4

**[0109]** Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, a dummy TFT element **20** is employed to give a redundant structure in preparation for deviations and errors in finish and the drain extraction lines **2** in each pixel area are all branched into a plurality to give a branch structure such that each drain electrode **1** is connected to the storage capacitor upper electrode **6** via at least two routes, as shown in **FIG. 7-1**, so that the lowering in display quality as caused by parasitic capacitances Cgd may be prevented.

**[0110]** In this case, the electrical connection between the drain electrode **1** of the TFT element **3** and the storage capacitor upper electrode **6** can be secured even on the occasion of occurrence of the drain line breaking **22** at one site, as shown in **FIG. 7-2**.

#### EXAMPLE 5

**[0111]** Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, the drain extraction line **2** is disposed each below a slit **30** prepared in each pixel electrode and the drain extraction line **2** in each pixel area is branched into a plurality to give a branch structure such that the drain electrode **1** is connected to the storage capacitor upper electrode **6** via at least two routes, as shown in **FIG. 8**.

[0112] In this case, the electrical connection between the drain electrode 1 of the TFT element 3 and the storage capacitor upper electrode 6 can be secured even on the occasion of occurrence of the drain line breaking 22 at one site. It is further possible to give a branch structure to the drain extraction line 2 without lowering the aperture ratio of the liquid crystal display device.

#### EXAMPLE 6

[0113] Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, the drain extraction line 2 is disposed at sites opposing slits 40 prepared on the counter electrode of the color filter substrate and the drain extraction line 2 in each pixel area is branched into a plurality to give a branch structure such that the drain electrode 1 is connected to the storage capacitor upper electrode 6 via at least two routes, as shown in FIG. 9.

[0114] In this case, the electrical connection between the drain electrode 1 of the TFT element 3 and the storage capacitor upper electrode 6 can be secured even on the occasion of occurrence of the drain line breaking 22 at one site. It is further possible to give a branch structure to the drain extraction line 2 without lowering the aperture ratio of the liquid crystal display device.

#### EXAMPLES 7-9

[0115] Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, a branch structure is formed in a manner such that the drain electrode 1 is finally connected to the storage capacitor upper electrode 6 via one or two drain extraction lines 2, as shown in FIGS. 10A, 10B and 10C.

[0116] In these cases, the possibility of line breaking between the drain electrode 1 of the TFT element 3 and the storage capacitor upper electrode 6 upon drain line breaking in the drain extraction line 2 can be reduced.

#### EXAMPLES 10-12

[0117] Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, two drain electrodes 1 are provided and a branch structure is formed in a manner such that the drain electrodes 1 are finally connected to the storage capacitor upper electrode 6 via one or two drain extraction lines 2, as shown in FIGS. 10D, 10E and 10F.

[0118] In these cases, the possibility of line breaking between the drain electrode 1 of the TFT element 3 and the storage capacitor upper electrode 6 upon drain line breaking in the drain extraction line 2 can be reduced.

#### EXAMPLE 13

[0119] Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, each TFT element 3 is provided with three drain electrodes 1 and a drain extraction line 2 is formed in a manner such that each of the drain electrodes 1 is connected to the storage capacitor upper electrode 6 on the Cs bus line 7, as shown in FIG. 11-1. The active matrix substrate of this example has three subpixels per pixel and, in each defect-free pixel, the subpixels are driven separately

by respective individual drain electrodes. The storage capacitor upper electrode 6 comprises two divided electrodes in the area facing the corresponding storage capacitor lower electrode 7, so that the drain extraction line 2 is formed to show a branch structure in front of the region for connection to the storage capacitor upper electrode 6.

[0120] In the neighboring Cs bus lines 7, the Cs signals are opposite in phase, as shown in FIGS. 11-2A and 11-2B, and the waveforms of the Cs signals (CS1 and CS2) differ in polarity, so that the drain signals (Drain1 and Drain2) applied differ in waveform. Therefore, from the pixel gray-scale level viewpoint as well, the neighboring subpixels differ in voltage-transmittance (V-T) characteristics as shown in FIG. 11-3, and the Drain 1 side one corresponding to plus writing (the side increasing the voltage amplitude value) serves as a bright subpixel and the Drain 2 side one corresponding to minus writing (the side decreasing the voltage amplitude value) serves as a dark subpixel. In this example, the area proportion between a bright subpixel corresponding to Drain 1, always serving as the "bright" side and being disposed in the middle of the pixel, and a dark subpixel corresponding to Drain 2, always serving as the "dark" side and being disposed on each end portion of the pixel, is 1:3.

[0121] In this case, if there is found drain line breaking 22 in a drain extraction line 2, as shown in FIG. 11-1 and at least one of the plurality of channels is normal, the overlapping portion 25 between a floating island electrode (interconnection electrode for amendment) 23 and the drain extraction line is laser-melted for interconnection of the drain extraction lines 2 of the respective subpixels with each other (drain/drain interconnection) to thereby attain equalization in electric potential. On that occasion, the drain/drain interconnected lines, the waveforms (polarities) of the Cs signals are synthesized so as to negate each other, so that such a Cs signal (CS:DC) with a direct current potential as shown in FIG. 11-2C is applied. As for the V-T characteristics, the V-T curves of both subpixels are synthesized and a V-T curve (Cs0V; basic V-T curve) intermediate between that for the bright subpixel and that for the dark subpixel is obtained. Therefore, in this example, even after drain/drain interconnection, V-T characteristics with an intermediate gray scale, which are visually the same as those of a normal pixel without drain/drain interconnection, can be obtained (the human eye cannot recognize the difference in gray scale between both), as seen in the gray-scale image shown in FIG. 11-4B, and all the subpixels (one pixel) can be driven like a normal pixel.

[0122] Furthermore, according to this example, unlike the case of drain/drain interconnection utilizing the ladder structure of the source bus line 5, no extra increase in coupling capacity (e.g. Csd) will result and, therefore, defect-free amendment (correction of all defects) can be realized while suppressing the variation of the effective voltage applied to the liquid crystal layer.

[0123] Even in case of occurrence of a short circuit (SD leak) between the source bus line 5 (or source electrode) and drain extraction line 2 (or drain electrode 1) in the vicinity of a channel, the channel and drain extraction line 2 involved in leak failure can be electrically separated from each other and the thus-separated drain extraction line 2 can be connected to the drain extraction line 2 from a normal channel for defect correction.

## EXAMPLE 14

[0124] Referring to the active matrix substrate (TFT substrate) for a liquid crystal display device as obtained in the above manner, two drain electrodes **1** are disposed for each TFT element **3**, and a drain extraction line **2** is formed so that each drain electrode **1** is connected to the storage capacitor upper electrode **6** on the Cs bus line **7**, as shown in **FIG. 12-1**. In an area facing the storage capacitor lower electrode **7**, the storage capacitor upper electrode **6** comprises two electrode divisions and, therefore, the drain extraction line **2** is formed so that it shows a branch structure in front of the section for connection to the storage capacitor upper electrode **6**. In the neighboring Cs bus lines **7**, the Cs signals are opposite in phase.

[0125] In this example, the bright and dark subpixels are disposed in an area proportion of 1:1.

[0126] In this case, on the occasion of occurrence of an SD leak, as shown in **FIG. 12-1**, the drain extraction lines **2** are connected to each other (drain/drain interconnection) using a floating island pattern electrode **23** and a source ladder **24** cut off from the source bus line **5** after cleavage at a cleavage site **27**.

[0127] In this way, the same effects as in Example 13 can be obtained. Thus, as shown in the gray-scale images in **FIGS. 12-2A** and **12-2B**, V-T characteristics with an intermediate gray scale which, to the human eye, appears the same as the gray scale of a normal pixel without drain/drain interconnection are obtained. In this example, however, there is an area where the source ladder **24** interconnecting both the drain extraction lines to each other is partly overlapping with a gate bus line **4**, and this results in an increase in coupling capacity and a difference in capacity with the neighboring pixels. Therefore, the effective voltage value (voltage applied to the liquid crystal layer) varies to some extent as compared with the amendment method of Example 13 shown in **FIG. 11-1**.

1. An active matrix substrate comprising an active element connected, via a drain extraction line, to a storage capacitor upper electrode, characterized in that the drain extraction line has at least two routes.

2. The active matrix substrate as claimed in claim 1,

wherein said drain extraction line is disposed at those sites corresponding to a protrusion and/or an electrode-free area provided on at least one of the active matrix substrate and the substrate facing the active matrix substrate.

3. The active matrix substrate as claimed in claim 1,

wherein said active element has at least two drain electrodes.

4. The active matrix substrate as claimed in claim 3,

wherein a pixel is constituted of at least two subpixels and

wherein the pixel electrodes in said at least two subpixels have a structure such that they are connected to the respective different drain electrodes each via a storage capacitor upper electrode and a drain extraction line.

5. The active matrix substrate as claimed in claim 4,

wherein said pixel comprises subpixels differing in brightness.

6. The active matrix substrate as claimed in claim 4,

wherein at least two storage capacitor lower electrodes to which signal voltages opposite in phase to each other are to be applied are provided therein and

wherein said at least two storage capacitor lower electrodes have a structure such that they are overlapping, via an insulation layer, with the respective storage capacitor upper electrodes corresponding to different subpixels.

7. The active matrix substrate as claimed in claim 4 which further comprises an interconnection electrode for amendment having a structure overlapping, via an insulation layer, with at least two drain extraction lines connected to respective different drain electrodes.

8. The active matrix substrate as claimed in claim 7 which further comprises a structure such that any two of the storage capacitor upper electrodes overlapping, via an insulation layer, with the corresponding storage capacitor lower electrode to which signal voltages opposite in phase to each other are to be applied are interconnected via a drain extraction line and an interconnection electrode for amendment.

9. The active matrix substrate as claimed in claim 7,

wherein a scanning signal line is connected to the gate electrode of an active element and

wherein said drain extraction line and interconnection electrode for amendment have a structure not overlapping with said scanning signal line.

10. The active matrix substrate as claimed in claim 1,

wherein said storage capacitor upper electrode comprises at least three divided electrodes in an area facing the corresponding storage capacitor lower electrode.

11. A display device equipped with the active matrix substrate according to claim 1.

12. The display device as claimed in claim 11, said display device being a liquid crystal display device.

\* \* \* \* \*

专利名称(译)	有源矩阵基板和显示装置		
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[标]申请(专利权)人(译)	栗原隆司 久田YUHKO 津幡町俊英 TAKEUCHI MASANORI 大坪友和		
申请(专利权)人(译)	栗原隆司 久田YUHKO 津幡町俊英 TAKEUCHI MASANORI 大坪友和		
当前申请(专利权)人(译)	夏普株式会社		
[标]发明人	KURIHARA RYUJI HISADA YUHKO TSUBATA TOSHIHIDE TAKEUCHI MASANORI OHTSUBO TOMOKAZU		
发明人	KURIHARA, RYUJI HISADA, YUHKO TSUBATA, TOSHIHIDE TAKEUCHI, MASANORI OHTSUBO, TOMOKAZU		
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外部链接	<a href="#">Espacenet</a> <a href="#">USPTO</a>		

#### 摘要(译)

本发明的有源矩阵基板是有源矩阵基板，其中可以防止漏极引出线在没有多个有源元件（例如TFT（薄膜晶体管）元件，MIM（金属-绝缘体-金属）元件）的情况下断开，设置MOS晶体管元件，二极管和变阻器，适用于大尺寸液晶电视或配备有大尺寸液晶显示板的类似液晶显示装置。本发明的有源矩阵基板是有源矩阵基板，包括通过漏极引出线连接到存储电容器上电极的有源元件，其中漏极引出线具有至少两个路径。

