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(54) **CAPACITIVE LOAD DRIVING CIRCUIT AND LIQUID CRYSTAL DISPLAY**

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(57) **ABSTRACT**

An overcurrent is prevented from flowing in an output circuit when a short circuit occurs between an output terminal and a power supply terminal or a ground terminal. For this purpose, provided is an output circuit comprising a power supply terminal, a ground terminal, and an output terminal connected to a capacitive load. Depending on the state of a load control input signal, the output circuit performs selectively a charging-current supplying operation of supplying a charging-current from the power supply terminal to the capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from the capacitive load to the ground terminal. Further, an overcharging-current prevention switch is provided for detecting a short circuit between the output terminal and the ground terminal so as to stop or suppress the charging-current supplying operation. Furthermore, an overdischarging-current prevention switch is provided for detecting a short circuit between the output terminal and the power supply terminal so as to stop or suppress the discharging-current withdrawing operation.

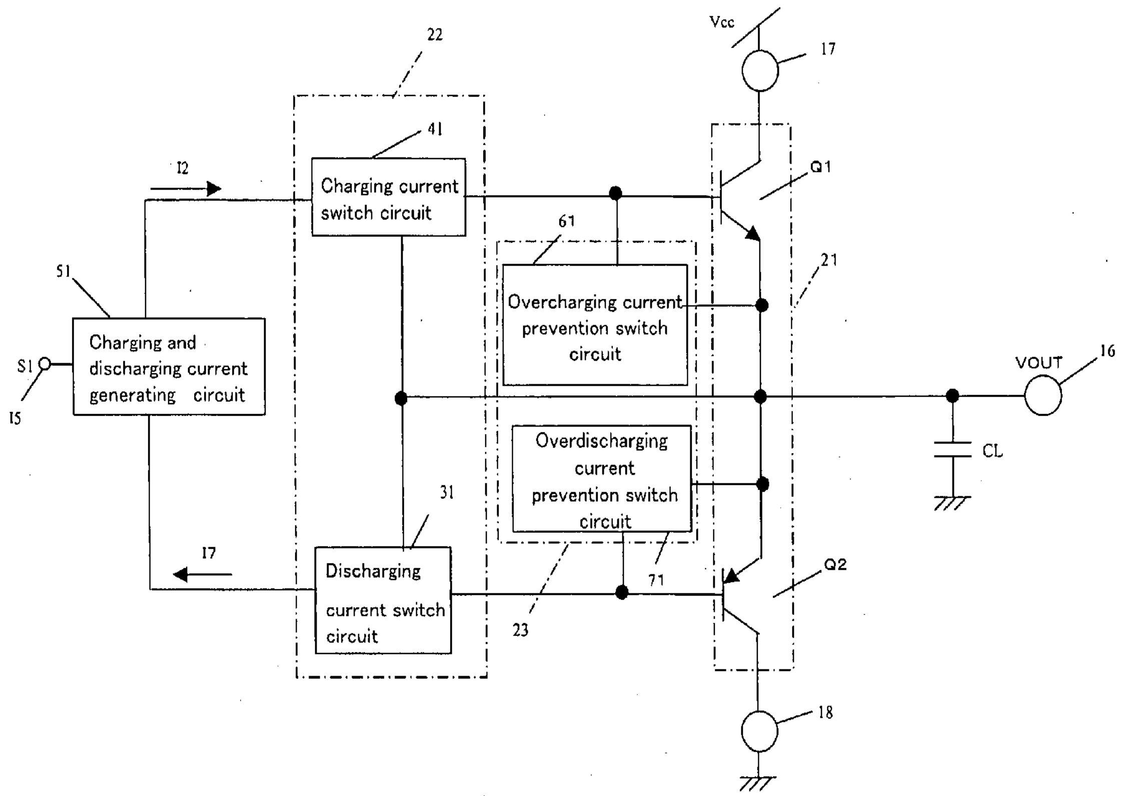


FIG. 1

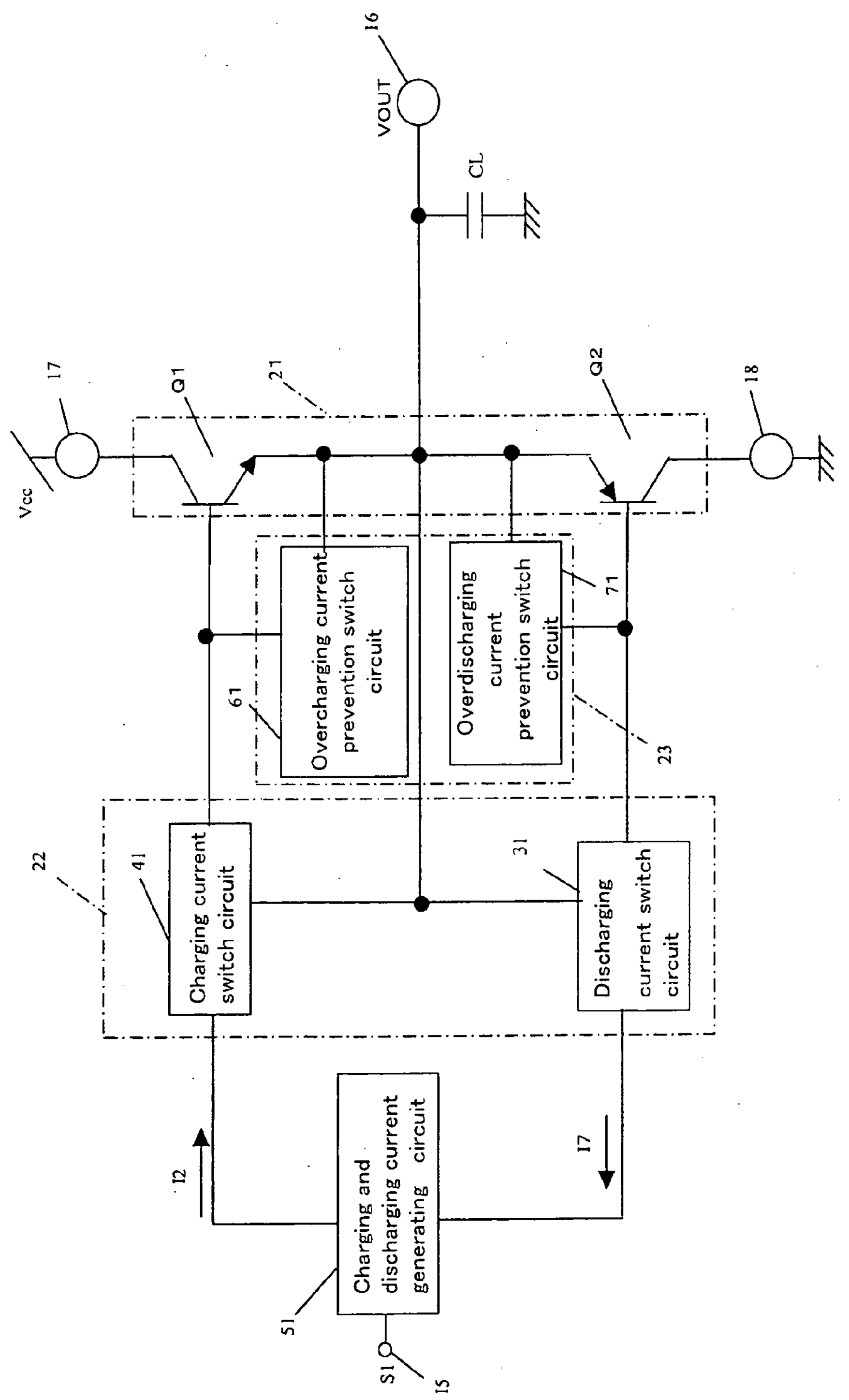
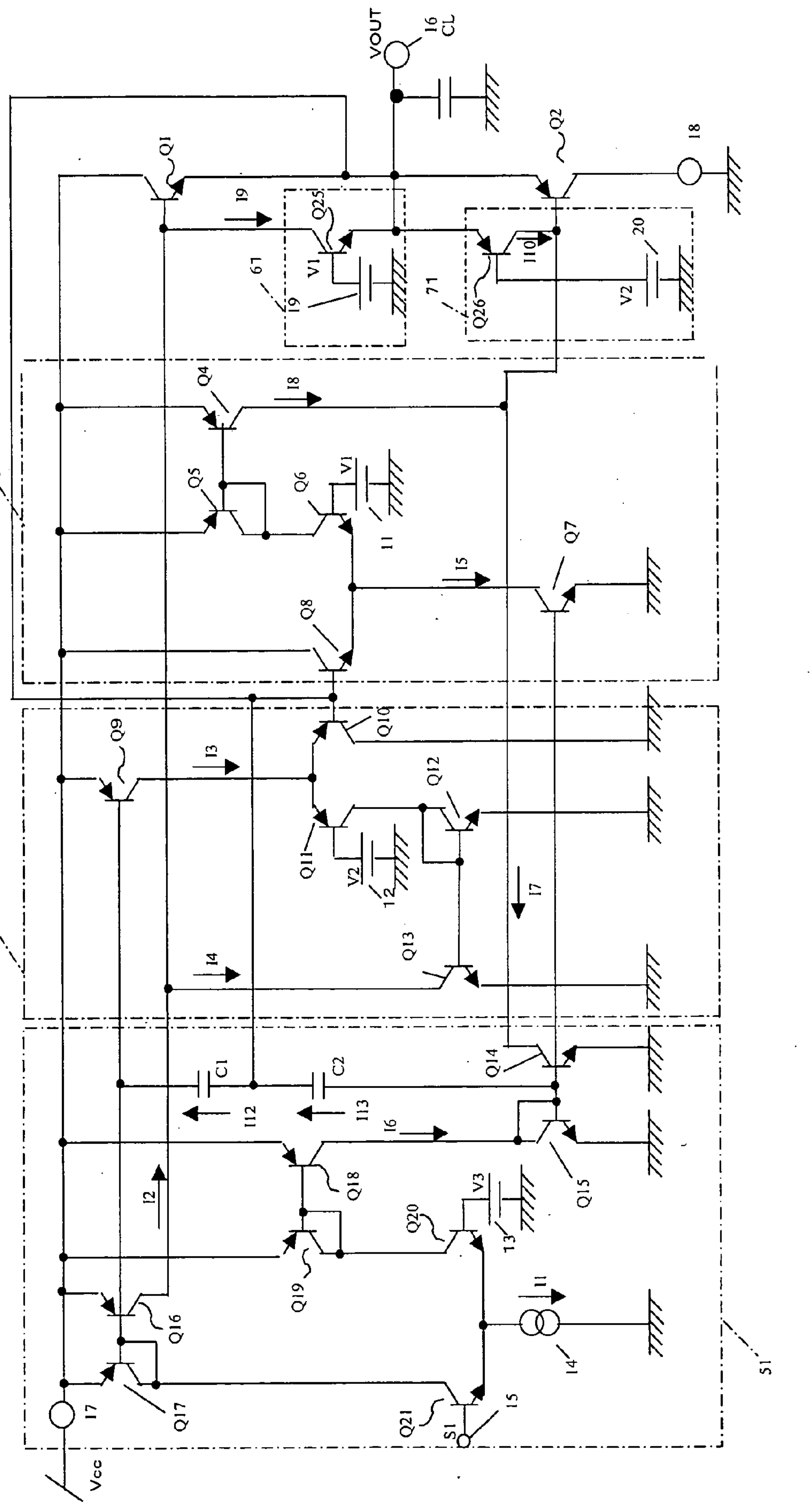

VOUT
16
CL
17
Vcc
Q1
21
Q2
18
Overcharging current prevention switch circuit
Overdischarging current prevention switch circuit
61
71
23
22
41
Charging current switch circuit
31
Discharging current switch circuit
I2
I7
Charging and discharging current generating circuit
51
S1
15

FIG. 2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16
CL
Q1
Q2
18
Q25
Q26
61
71
19
20
V1
V2
I9
I10
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Q4
Q5
Q6
Q7
Q8
I8
I5
11
41
Q9
Q10
Q11
Q12
Q13
I3
I4
I7
12
51
Q14
Q15
Q16
Q17
Q18
Q19
Q20
Q21
C1
C2
I12
I13
I6
I2
I1
V3
13
14
15
S1
17
Vcc

FIG. 3

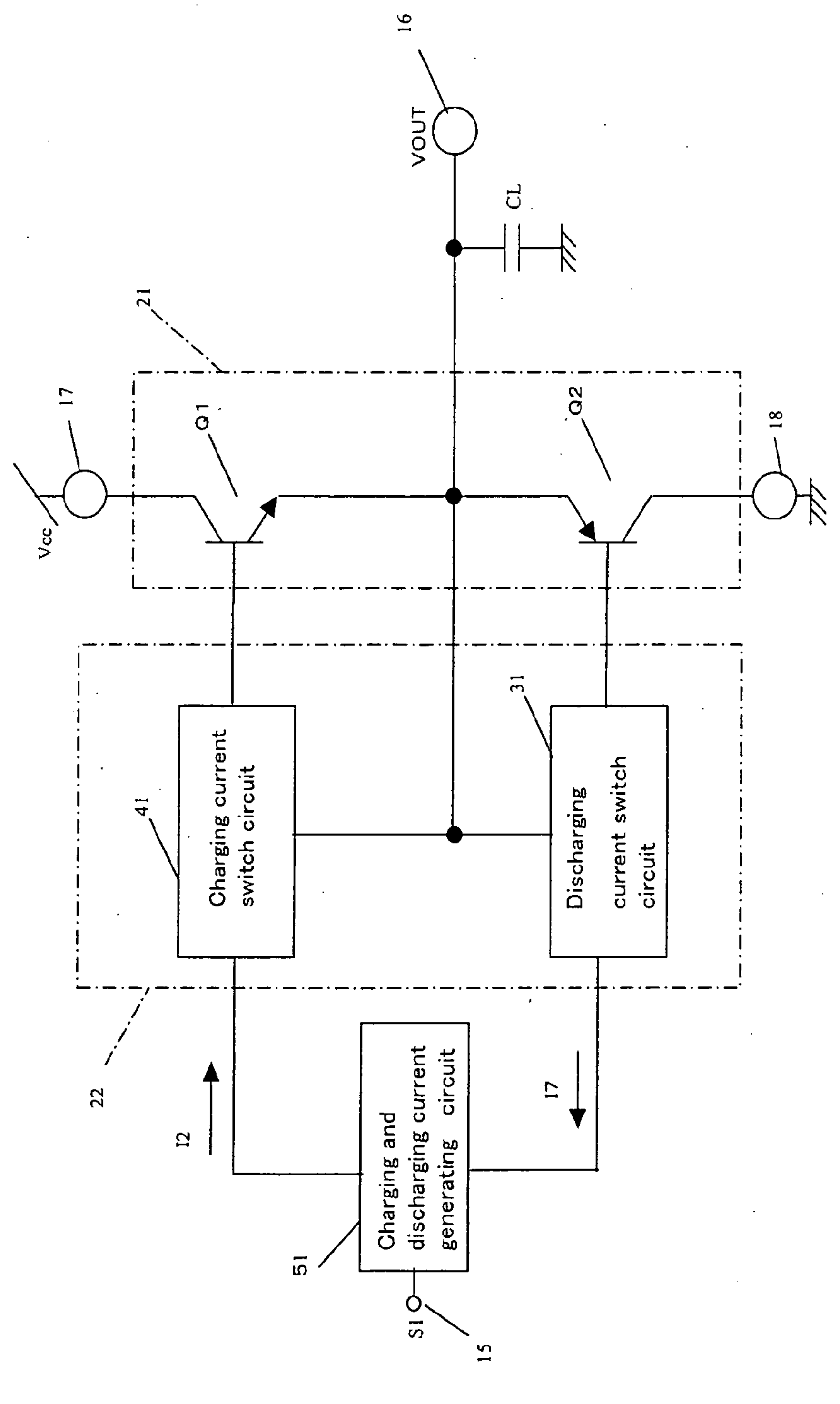
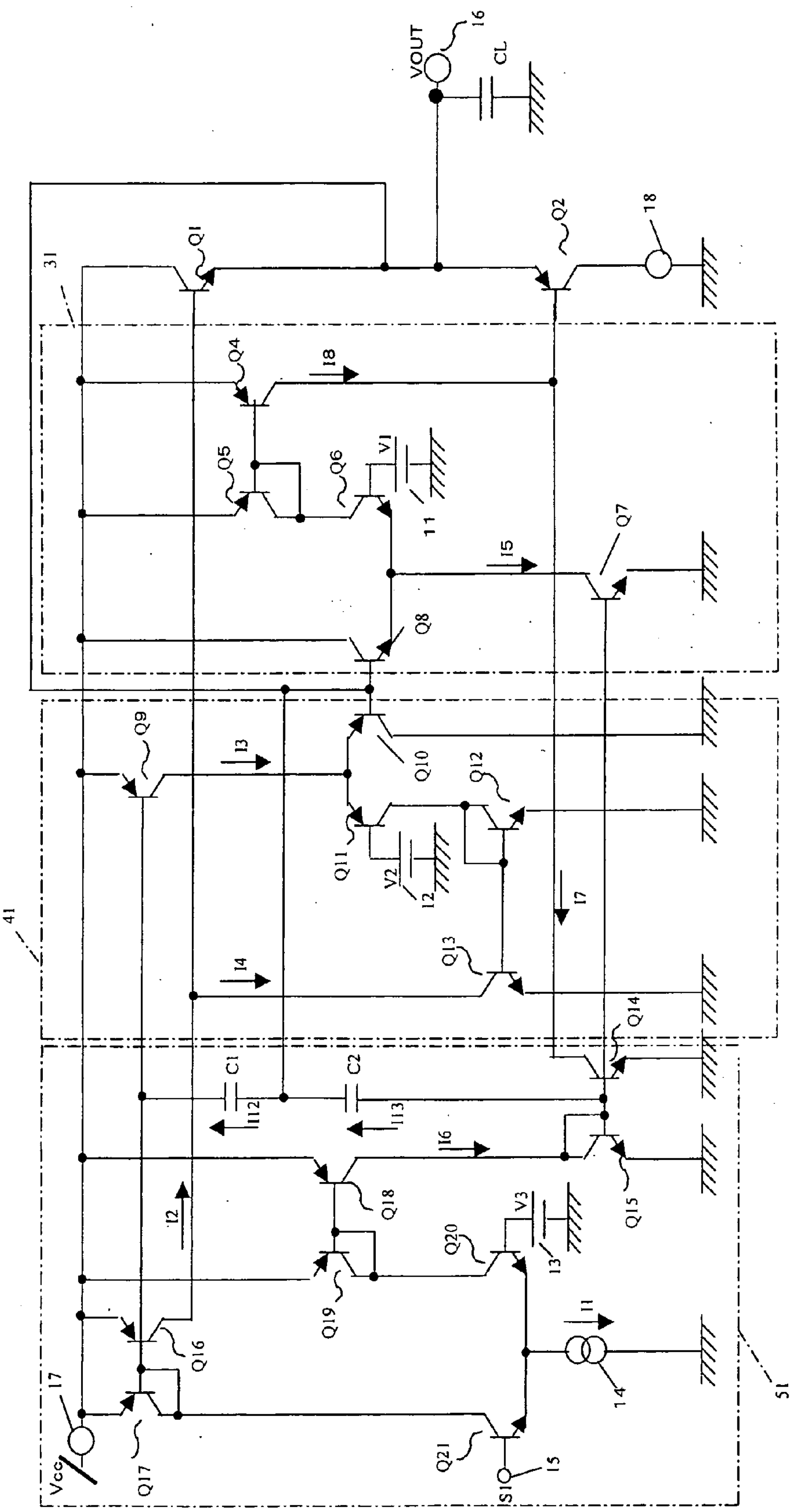
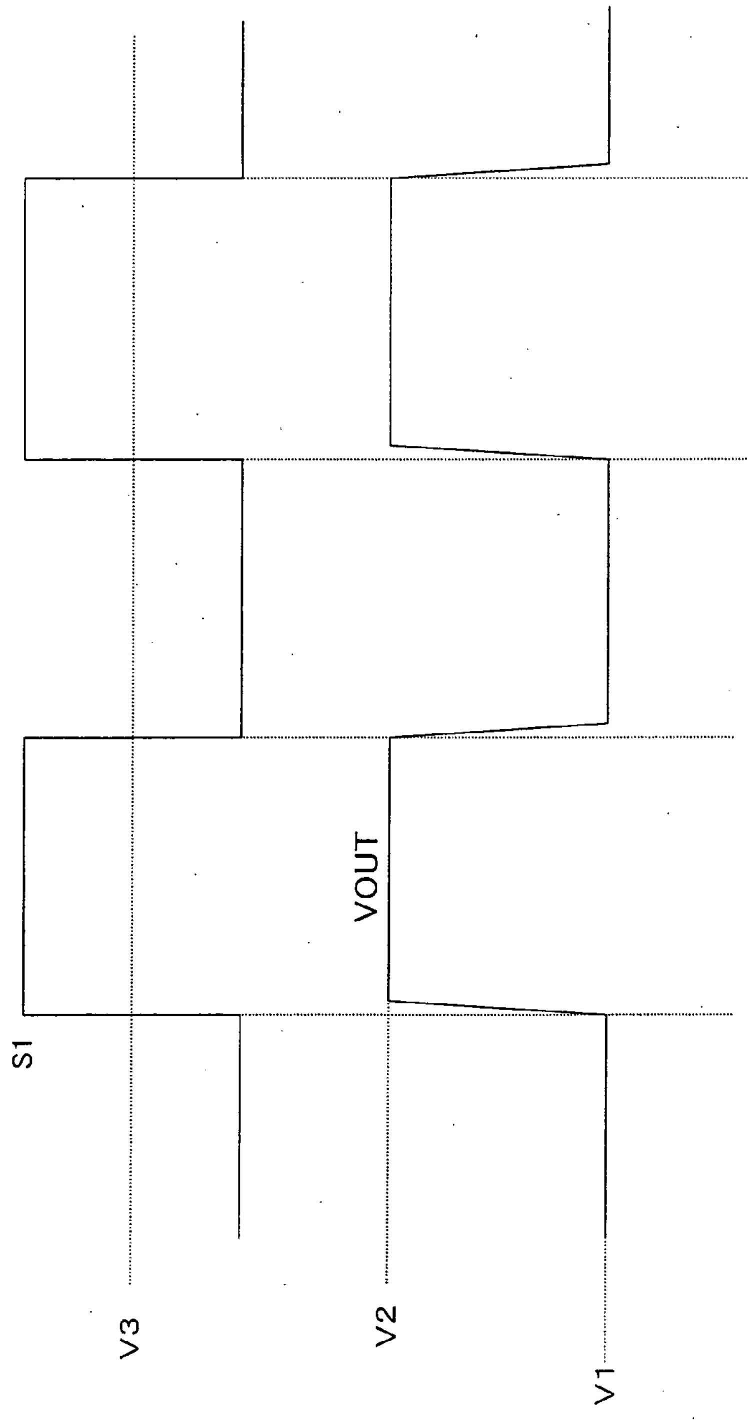

16
VOUT
CL
21
17
Vcc
Q1
Q2
18
31
41
Charging current switch circuit
Discharging current switch circuit
22
I2
I7
Charging and discharging current generating circuit
51
S1
15

FIG. 4



VOUT
16
CL
Q1
Q2
18
31
Q4
I8
Q5
Q6
V1
11
I5
Q7
Q8
Q9
I3
Q10
Q12
Q11
V2
12
I7
41
Q13
I4
Q14
C1
C2
I12
I13
I16
Q15
Q18
I2
V3
Q20
13
Q19
I1
Q16
17
Vcc
Q17
Q21
S1
15
14
51

FIG. 5



CAPACITIVE LOAD DRIVING CIRCUIT AND LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a capacitive load driving circuit for driving a capacitive load with charging and discharging-currents, such as a capacitive load driving circuit for driving a common electrode of a liquid crystal display panel. Further, the invention relates to a liquid crystal display using a capacitive load driving circuit.

[0003] 2. Related Art of the Invention

[0004] An example of a capacitive load driving circuit for driving a capacitive load composed of a common electrode of a liquid crystal display panel is disclosed in JP-A 2000-174601.

[0005] **FIG. 3** is a schematic circuit diagram of a capacitive load driving circuit according to the prior art proposed by the present inventors. In this capacitive load driving circuit, as shown in **FIG. 3**, an output circuit **21** comprises: a power supply terminal **17** connected to a power supply line (Vcc line); a ground terminal **18** connected to a ground line; and an output terminal **16** connected to a capacitive load CL composed, for example, of a common electrode of a liquid crystal display panel.

[0006] The output circuit **21** performs selectively a charging-current supplying operation of supplying a charging-current from the output terminal **16** to the capacitive load CL and a discharging-current withdrawing operation of withdrawing a discharging-current from the capacitive load CL to the output terminal **16**. The charging-current supplying operation and the discharging-current withdrawing operation are performed selectively depending on the state of a load control input signal **S1** the state (high level or low level) of which varies or alternates periodically. The charging-current supplying operation is continued until the voltage of the output terminal **16** reaches an upper amplitude limit. The discharging-current withdrawing operation is continued until the voltage of the output terminal **16** reaches a lower amplitude limit. The output terminal **16**, the power supply terminal **17**, and the ground terminal **18** are formed into terminal pins for external connection when the capacitive load driving circuit is implemented in the form of an integrated circuit.

[0007] **FIG. 4** is a circuit diagram showing a specific configuration of the capacitive load driving circuit of **FIG. 3**.

[0008] In the capacitive load driving circuit, when an earth fault (a short circuit to the ground terminal **18**) occurs in the output terminal **16**, the voltage of the output terminal **16** is always lower than the upper amplitude limit. This causes a large current to flow ceaselessly through a route connecting the power supply terminal **17**, a charging output transistor Q**1**, the output terminal **16**, and the ground terminal **18** in this order, during the period that the load control input signal **S1** is high.

[0009] Similarly, when a sky fault (a short circuit to the power supply terminal **17**) occurs in the output terminal **16**, the voltage of the output terminal **16** is always higher than the lower amplitude limit. This causes a large current to flow ceaselessly through a route connecting the power supply terminal **17**, the output terminal **16**, a discharging output transistor Q**2**, and the ground terminal **18** in this order, during the period that the load control input signal **S1** is low.

[0010] As such, in case of an earth fault or a sky fault, an excessive current or overcurrent flows in the output circuit **21**. This causes the problem of overheat in the output transistors Q**1** and Q**2** constituting the output circuit **21** and hence in the integrated circuit containing the capacitive load driving circuit comprising the output transistors Q**1** and Q**2**.

[0011] Such an earth fault or sky fault occurs, for example, when terminal pins provided in the integrated circuit package containing the capacitive load driving circuit form a short circuit between them. Here, these terminal pins correspond to the output terminal, the power supply terminal, and the ground terminal. Sucha short circuit between the terminal pins occurs, for example, owing to an error during the fabrication or owing to the adhesion of electrically conductive dust or the like to the terminal pins during thus

SUMMARY OF THE INVENTION

[0012] An object of the invention is to provide a capacitive load driving circuit and a liquid crystal display in which an overcurrent is prevented from flowing ceaselessly in an output circuit when a short circuit occurs between an output terminal and a power supply terminal or a ground terminal, so that overheat is avoided in the output circuit.

[0013] A first aspect of the invention is a capacitive load driving circuit for supplying a charging-current to a capacitive load and withdrawing a discharging-current from the capacitive load, comprising an output circuit and an overcurrent protection circuit.

[0014] The output circuit comprises a power supply terminal, a ground terminal, and an output terminal connected to the capacitive load, and performs a charging-current supplying operation of supplying a charging-current from the power supply terminal to the capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from the capacitive load to the ground terminal.

[0015] The overcurrent protection circuit detects a short circuit between the output terminal and the ground terminal so as to stop or suppress the charging-current supplying operation, and detects a short circuit between the output terminal and the power supply terminal so as to stop or suppress the discharging-current withdrawing operation.

[0016] Then, the output circuit selects any one of the charging-current supplying operation and the discharging-current withdrawing operation depending on the state of a control input signal.

[0017] According to this configuration provided with the overcurrent protection circuit, when a short circuit occurs between the output terminal and the ground terminal, the charging-current supplying operation is stopped or suppressed. Further, when a short circuit occurs between the output terminal and the power supply terminal, the discharging-current withdrawing operation is stopped or suppressed. Accordingly, an overcurrent is prevented from flowing ceaselessly in an output circuit when a short circuit occurs between the output terminal and the power supply terminal or the ground terminal, so that overheat is avoided in the output circuit.

[0018] In the capacitive load driving circuit according to the first aspect, it is preferable that the output circuit continues to charge the capacitive load in the charging-current supplying operation until the electric potential of the capacitive load reaches a predetermined upper amplitude limit lower than the electric potential of the power supply terminal, and continues to discharge the capacitive load in the discharging-current withdrawing operation until the electric potential of the capacitive load reaches a predetermined lower amplitude limit higher than the electric potential of the ground terminal.

[0019] According to this configuration, in the charging, when the electric potential of the capacitive load reaches the upper amplitude limit, the charging-current supplying operation is stopped. Further, in the discharging, when the electric potential of the capacitive load reaches the lower amplitude limit, the discharging-current withdrawing operation is stopped. This ensures the constancy of the electric potential of the capacitive load at the upper amplitude limit and the lower amplitude limit in the charging and the discharging, respectively.

[0020] In the capacitive load driving circuit according to the first aspect, the output circuit, for example, comprises: a first NPN transistor the collector of which is connected to the power supply terminal and the emitter of which is connected to the output terminal; and a first PNP transistor the collector of which is connected to the ground terminal and the emitter of which is connected to the output terminal.

[0021] The overcurrent protection circuit, for example, comprises a second NPN transistor and a second PNP transistor. In the second NPN transistor, the collector is connected to the base of the first NPN transistor, the emitter is connected to the output terminal, and the base is connected to a first voltage supply for generating a predetermined electric potential higher than the electric potential of the ground terminal. In the second PNP transistor, the collector is connected to the base of the first PNP transistor, the emitter is connected to the output terminal, and the base is connected to a second voltage supply for generating a predetermined electric potential lower than the electric potential of the power supply terminal.

[0022] The first voltage supply preferably generates a predetermined electric potential higher than the electric potential of the ground terminal and lower than or equal to the lower amplitude limit. The second voltage supply preferably generates a predetermined electric potential lower than the electric potential of the power supply terminal and higher than or equal to the upper amplitude limit.

[0023] According to this configuration, the overcurrent protection circuit is constructed by the second NPN transistor, the second PNP transistor, and the first and second voltage supplies. This realizes an overcurrent protection circuit having simple configuration.

[0024] In the capacitive load driving circuit according to the first aspect, for example, the state of the control input signal alternates periodically.

[0025] A second aspect of the invention is a capacitive load driving circuit for supplying a charging-current to a capacitive load and withdrawing a discharging-current from the capacitive load, comprising an output circuit, a current generation circuit, a charging and discharging control circuit, and an overcurrent protection circuit.

[0026] The output circuit comprises a power supply terminal, a ground terminal, and an output terminal connected to the capacitive load, and performs a charging-current supplying operation of supplying a charging-current from the power supply terminal to the capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from the capacitive load to the ground terminal.

[0027] The current generation circuit selects, depending on the state of a control input signal, any one of a first state where a first current is supplied to the output circuit so as to cause the output circuit to select the charging-current supplying operation and a second state where a second current is supplied to the output circuit so as to cause the output circuit to select the discharging-current withdrawing operation.

[0028] The charging and discharging control circuit detects the electric potential of the capacitive load and thereby controls and causes the output circuit to continue the charging-current supplying operation until the electric potential of the capacitive load reaches a predetermined upper amplitude limit, to stop the charging-current supplying operation when the electric potential reaches the predetermined upper amplitude limit, to continue the discharging-current withdrawing operation until the electric potential of the capacitive load reaches a predetermined lower amplitude limit, and to stop the discharging-current withdrawing operation when the electric potential reaches the predetermined lower amplitude limit.

[0029] The overcurrent protection circuit detects a short circuit between the output terminal and the ground terminal so as to stop or suppress the charging-current supplying operation, and detects a short circuit between the output terminal and the power supply terminal so as to stop or suppress the discharging-current withdrawing operation.

[0030] According to this configuration provided with the overcurrent protection circuit, when a short circuit occurs between the output terminal and the ground terminal, the charging-current supplying operation is stopped or suppressed. Further, when a short circuit occurs between the output terminal and the power supply terminal, the discharging-current withdrawing operation is stopped or suppressed. Accordingly, an overcurrent is prevented from flowing ceaselessly in an output circuit when a short circuit occurs between the output terminal and the power supply terminal or the ground terminal, so that overheat is avoided in the output circuit.

[0031] In the capacitive load driving circuit according to the second aspect, the output circuit, for example, comprises: a first NPN transistor the collector of which is connected to the power supply terminal and the emitter of which is connected to the output terminal; and a first PNP transistor the collector of which is connected to the ground terminal and the emitter of which is connected to the output terminal.

[0032] The overcurrent protection circuit comprises a second NPN transistor and a second PNP transistor. In the second NPN transistor, the collector is connected to the base of the first NPN transistor, the emitter is connected to the output terminal, and the base is connected to a first voltage supply for generating a predetermined electric potential higher than the electric potential of the ground terminal and lower than or equal to the lower amplitude limit. In the second PNP transistor, the collector is connected to the base of the first PNP transistor, the emitter is connected to the output terminal, and the base is connected to a second voltage supply for generating a predetermined electric potential lower than the electric potential of the power supply terminal and higher than or equal to the upper amplitude limit. The charging and discharging control circuit controls the base currents of the first NPN transistor and the first PNP transistor, so as to control the execution and the stop of the charging-current supplying operation and the discharging-current withdrawing operation.

[0033] According to this configuration, the overcurrent protection circuit is constructed by the second NPN transistor, the second PNP transistor, and the first and second voltage supplies. This realizes an overcurrent protection circuit having simple configuration.

[0034] In the capacitive load driving circuit according to the second aspect, the charging and discharging control circuit, for example, comprises: a third voltage supply for generating an electric potential equal to the upper amplitude limit; a fourth voltage supply for generating an electric potential equal to the lower amplitude limit; a charging control differential switch circuit one input terminal of which receives the electric potential of the capacitive load, and the other input terminal of which receives the electric potential of the third voltage supply; and a discharging control differential switch circuit one input terminal of which receives the electric potential of the capacitive load, and the other input terminal of which receives the electric potential of the fourth voltage supply.

[0035] The charging control differential switch circuit performs on-off control of the base current of the first NPN transistor depending on the result of comparison between the electric potential of the capacitive load and the electric potential of the third voltage supply. Further, the discharging control differential switch circuit performs on-off control of the base current of the first PNP transistor depending on the result of comparison between the electric potential of the capacitive load and the electric potential of the fourth voltage supply.

[0036] According to this configuration, the charging control differential switch circuit and the discharging control differential switch circuit for controlling the charging and discharging-currents can shut off completely the charging and discharging-currents supplied to the output circuit. This realizes low electric power consumption. Further, the voltage amplitude appearing in the output terminal is defined by the differential switch circuits, and such differential switch circuits have a good temperature characteristic. This avoids the problem of variation in the voltage amplitude of the output terminal caused by temperature variation.

[0037] In this configuration, it is preferable that the electric potentials of the third and fourth voltage supplies are variable, and that the electric potential of the first voltage supply varies in linkage with the electric potential of the fourth voltage supply while the electric potential of the second voltage supply varies in linkage with the electric potential of the third voltage supply.

[0038] According to this configuration, the electric potential of the first voltage supply varies in linkage with the electric potential of the fourth voltage supply, while the electric potential of the second voltage supply varies in linkage with the electric potential of the third voltage supply. Accordingly, when the electric potential of the third or the fourth voltage supply is adjusted for the purpose of adjusting the upper amplitude limit or the lower amplitude limit of the capacitive load, avoided is the occurrence of mismatching with the electric potential where the overcurrent protection circuit stops the charging-current supplying operation or the discharging-current withdrawing operation. This avoids the occurrence of abnormality in the control operation of the charging control differential switch circuit and the discharging control differential switch circuit.

[0039] In this configuration, it is preferable that the electric potential of the first voltage supply is equal to the electric potential of the fourth voltage supply while the electric potential of the second voltage supply is equal to the electric potential of the third voltage supply.

[0040] In the capacitive load driving circuit according to the second aspect, it is preferable that a frequency-dependent impedance element is provided between the current generation circuit and the output circuit, so that a part of the output current of the output circuit is fed back through the frequency-dependent impedance element to the current generation circuit, so that the through-rate is suppressed at the alternation of the output state of the current generation circuit.

[0041] According to this configuration, even when the through-rate is high in the load control input signal, the frequency-dependent impedance element restricts the through-rate, so as to permit smooth alternation of the charging and discharging-currents. This avoids an overshoot and an undershoot at the alternation of the charging and discharging-currents. This provides a stable output waveform without an overshoot and an undershoot, and hence avoids a steep change in the charging and discharging-currents.

[0042] In the capacitive load driving circuit according to the second aspect, for example, the state of the control input signal alternates periodically.

[0043] A third aspect of the invention is a liquid crystal display comprising a liquid crystal display panel common electrode, an output circuit, and an overcurrent protection circuit.

[0044] The output circuit comprises a power supply terminal, a ground terminal, and an output terminal connected to the liquid crystal display panel common electrode, and performs a charging-current supplying operation of supplying a charging-current from the power supply terminal to the liquid crystal display panel common electrode and a discharging-current withdrawing operation of withdrawing a discharging-current from the liquid crystal display panel common electrode to the ground terminal.

[0045] The overcurrent protection circuit detects a short circuit between the output terminal and the ground terminal so as to stop or suppress the charging-current supplying operation, and detects a short circuit between the output terminal and the power supply terminal so as to stop or suppress the discharging-current withdrawing operation.

[0046] Then, the output circuit selects any one of the charging-current supplying operation and the discharging-current withdrawing operation depending on the state of a control input signal.

[0047] According to this configuration provided with the overcurrent protection circuit, when a short circuit occurs between the output terminal and the ground terminal, the charging-current supplying operation is stopped or suppressed. Further, when a short circuit occurs between the output terminal and the power supply terminal, the discharging-current withdrawing operation is stopped or suppressed. Accordingly, an overcurrent is prevented from flowing ceaselessly in an output circuit when a short circuit occurs between the output terminal and the power supply terminal or the ground terminal, so that overheat is avoided in the output circuit.

[0048] Further, in case that the output circuit and the overcurrent protection circuit are implemented in the form of an IC and attached to a liquid crystal display panel, the above-mentioned configuration avoids the necessity of providing separately a protection circuit between the IC and the liquid crystal display panel common electrode, so as to reduce the number of components. Further, overheat is avoided in the output circuit, so that the safety in the liquid crystal display driving system is improved.

[0049] A fourth aspect of the invention is a liquid crystal display comprising a liquid crystal display panel common electrode, an output circuit, a current generation circuit, a charging and discharging control circuit, and an overcurrent protection circuit.

[0050] The output circuit comprises a power supply terminal, a ground terminal, and an output terminal connected to the liquid crystal display panel common electrode, and performs a charging-current supplying operation of supplying a charging-current from the power supply terminal to the liquid crystal display panel common electrode and a discharging-current withdrawing operation of withdrawing a discharging-current from the liquid crystal display panel common electrode to the ground terminal.

[0051] The current generation circuit selects, depending on the state of a control input signal, any one of a first state where a first current is supplied to the output circuit so as to cause the output circuit to select the charging-current supplying operation and a second state where a second current is supplied to the output circuit so as to cause the output circuit to select the discharging-current withdrawing operation.

[0052] The charging and discharging control circuit detects the electric potential of the liquid crystal display panel common electrode and thereby controls and causes the output circuit to continue the charging-current supplying operation until the electric potential of the liquid crystal display panel common electrode reaches a predetermined upper amplitude limit, to stop the charging-current supplying operation when the electric potential reaches the predetermined upper amplitude limit, to continue the discharging-current withdrawing operation until the electric potential of the liquid crystal display panel common electrode reaches a predetermined lower amplitude limit, and to stop the discharging-current withdrawing operation when the electric potential reaches the predetermined lower amplitude limit.

[0053] The overcurrent protection circuit detects a short circuit between the output terminal and the ground terminal so as to stop or suppress the charging-current supplying operation, and detects a short circuit between the output terminal and the power supply terminal so as to stop or suppress the discharging-current withdrawing operation.

[0054] According to this configuration provided with the overcurrent protection circuit, when a short circuit occurs between the output terminal and the ground terminal, the charging-current supplying operation is stopped or suppressed. Further, when a short circuit occurs between the output terminal and the power supply terminal, the discharging-current withdrawing operation is stopped or suppressed. Accordingly, an overcurrent is prevented from flowing ceaselessly in an output circuit when a short circuit occurs between the output terminal and the power supply terminal or the ground terminal, so that overheat is avoided in the output circuit.

[0055] Further, similarly in the third aspect of the invention, the number of components is reduced, while the safety in the liquid crystal display driving system is improved. Further, electric power consumption is reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

[0056] **FIG. 1** is a circuit diagram showing schematic configuration of a capacitive load driving circuit according to an embodiment of the invention.

[0057] **FIG. 2** is a circuit diagram showing detailed configuration of the capacitive load driving circuit of **FIG. 1**.

[0058] **FIG. 3** is a circuit diagram showing schematic configuration of a capacitive load driving circuit according to the prior art.

[0059] **FIG. 4** is a circuit diagram showing detailed configuration of the capacitive load driving circuit of **FIG. 3**.

[0060] **FIG. 5** is a waveform diagram illustrating the operation of the capacitive load driving circuit of **FIG. 2**.

DETAILED DESCRIPTION OF THE INVENTION

[0061] Embodiments of the invention are described below with reference to the drawings.

[0062] **FIG. 1** is a circuit diagram showing schematic configuration of a capacitive load driving circuit according to an embodiment of the invention. The capacitive load driving circuit has such a configuration that an overcurrent protection circuit **23** is added to the configuration of **FIG. 3**. The other points in the configuration are the same as those of the capacitive load driving circuit of **FIG. 3**.

[0063] The overcurrent protection circuit **23** detects a short circuit (earth fault) between an output terminal **16** and a ground terminal **18** so as to stop or suppress a charging - current supplying operation performed by a charging-current switch circuit **41** of a charging and discharging control circuit **22**. Further the overcurrent protection circuit **23** detects a short circuit (sky fault) between the output terminal **16** and a power supply terminal **17** so as to stop or suppress a discharging-current withdrawing operation performed by a discharging-current switch circuit **31** of the charging and discharging control circuit **22**.

[**0064**] This capacitive load driving circuit is described below in detail.

[**0065**] In the capacitive load driving circuit, as shown in **FIG. 1**, an output circuit **21** comprises: a power supply terminal **17** connected to a power line (Vcc line); a ground terminal **18** connected to a ground line; and an output terminal **16** connected to a capacitive load CL composed, for example, of a common electrode of a liquid crystal display panel.

[**0066**] The output circuit **21** performs selectively a charging-current supplying operation of supplying a charging-current from the output terminal **16** to the capacitive load CL and a discharging-current withdrawing operation of withdrawing a discharging-current from the capacitive load CL to the output terminal **16**. The charging-current supplying operation and the discharging-current withdrawing operation are performed selectively depending on the state of a load control input signal S1 the state (high level or low level) of which varies or alternates periodically. The charging-current supplying operation is continued until the voltage of the output terminal **16** reaches an upper amplitude limit. The discharging-current withdrawing operation is continued until the voltage of the output terminal **16** reaches a lower amplitude limit. The output terminal **16**, the power supply terminal **17**, and the ground terminal **18** are formed into terminal pins for external connection when the capacitive load driving circuit is implemented in the form of an integrated circuit.

[**0067**] For the purpose of the above-mentioned operations, the output circuit **21** comprises two output transistors Q1 and Q2 interconnected in series. The output transistor Q1 is composed of an NPN transistor. The collector is connected to the power supply terminal **17**, while the emitter is connected to the output terminal **16**. The output transistor Q2 is composed of a PNP transistor. The collector is connected to the ground terminal **18**, while the emitter is connected to the output terminal **16**.

[**0068**] The output transistor Q1 the collector of which is connected to the power supply terminal **17** supplies a charging-current from the VCC power line to the capacitive load CL. The output transistor Q2 the collector of which is connected to the ground terminal **18** withdraws a discharging-current from the capacitive load CL to the ground line.

[**0069**] The base current of the output transistor Q1 is supplied through the charging-current switch circuit **41**. The base current of the output transistor Q2 is withdrawn through the discharging-current switch circuit **31**. The discharging-current switch circuit **31** and the charging-current switch circuit **41** are connected to a charging and discharging-current generating circuit **51**.

[**0070**] The charging and discharging-current generating circuit **51** outputs a first current I2 for charging-current generation and a second current I7 ford is charging-current generation. The first current I2 is supplied as a base current to the output transistor Q1. The second current I7 is withdrawn as a base current from the output transistor Q2.

[**0071**] An input terminal **15** of the charging and discharging-current generating circuit **51** receives a pulse-shaped load control input signal S1 the state of which alternates periodically between a high level and a low level.

[**0072**] Depending on the state of the load control input signal S1, the charging and discharging-current generating circuit **51** selects any one of a first state where the first current I2 is supplied to the output circuit **21** so as to cause the output circuit **21** to select the charging-current supplying operation and a second state where the second current I7 is supplied to the output circuit **21** so as to cause the output circuit **21** to select the discharging-current withdrawing operation.

[**0073**] The charging-current switch circuit **41** and the discharging-current switch circuit **31** constitute the charging and discharging control circuit **22**. The charging and discharging control circuit **22** monitors or detects the electric potential of the capacitive load CL, and thereby controls the output circuit **21** as follows. That is, the charging and discharging control circuit **22** controls and causes the output circuit **21** to continue the charging-current supplying operation until the electric potential of the capacitive load CL reaches a predetermined upper amplitude limit V2, and to stop the charging-current supplying operation when the electric potential reaches the predetermined upper amplitude limit V2. Further, the charging and discharging control circuit **22** controls and causes the output circuit **21** to continue the discharging-current withdrawing operation until the electric potential of the capacitive load CL reaches a predetermined lower amplitude limit V1, and to stop the discharging-current withdrawing operation when the electric potential reaches the predetermined lower amplitude limit V1.

[**0074**] More specifically, the charging and discharging control circuit **22** controls the base currents of the output transistors Q1 and Q2, so as to control the execution and the stop of the charging-current supplying operation and the discharging-current withdrawing operation.

[**0075**] As described above, the electric potential of the output terminal **16** is monitored by the discharging-current switch circuit **31** and the charging-current switch circuit **41**. The charging-current switch circuit **41** shuts off the charging-current from the output transistor Q1 in such a manner that the electric potential VOUT of the output terminal **16** does not go higher than the predetermined upper amplitude limit V2. The discharging-current switch circuit **31** shuts off the discharging-current from the output transistor Q2 in such a manner that the electric potential VOUT of the output terminal **16** does not go lower than the predetermined lower amplitude limit The overcurrent protection circuit **23** comprises: an overcharging-current prevention switch circuit **61** for detecting a short circuit (earth fault) between the output terminal **16** and the ground terminal **18** so as to stop or suppress the charging-current supplying operation performed by the charging-current switch circuit **41** of the charging and discharging control circuit **22**; and an overdischarging-current prevention switch circuit **71** for detecting a short circuit (sky fault) between the output terminal **16** and the power supply terminal **17** so as to stop or suppress the discharging-current withdrawing operation performed by the discharging-current switch circuit **31** of the charging and discharging control circuit **22**.

[**0076**] In this overcurrent protection circuit **23**, when a short circuit (sky fault) occurs between the output terminal

16 and the power supply terminal **17**, the overdischarging-current prevention switch circuit **71** shuts off or restricts the current I7, which is the base current of the discharging output transistor Q2, so as to prevent an overdischarging-current from flowing ceaselessly through the output transistor Q2. When a short circuit (earth fault) occurs between the output terminal **16** and the ground terminal **18**, the over-charging-current prevention switch circuit **61** shuts off or restricts the current I2, which is the base current of the charging output transistor Q1, so as to prevent an over charging-current from flowing ceaselessly through the output transistor Q1. This avoids overheat in the output circuit.

[**0077**] **FIG. 2** is a circuit diagram showing detailed configuration of the capacitive load driving circuit of **FIG. 1**. Difference from **FIG. 4** is that the over charging-current prevention switch circuit **61** and the overdischarging-current prevention switch circuit **71** are added. The other points are the same as those of **FIG. 4**.

[**0078**] In **FIG. 2**, like parts to **FIG. 1** are designated by like numerals. The charging-current switch circuit **41** comprises transistors Q9, Q**10**, Q**11**, Q**12**, and Q**13** and a constant voltage supply **12** for generating an electric potential defining the upper amplitude limit V2. More specifically, the constant voltage supply **12** generates an electric potential equal to the upper amplitude limit V2. In an exemplary case that the voltage applied to the power supply terminal **17** is 12 V, the upper amplitude limit V2 is set, for example, at approximately 10 V. In case that the capacitive load CL is composed, for example, of a common electrode of a liquid crystal display panel, the upper amplitude limit V2 is not fixed but variable in some cases for the purpose of adjustment of the visibility of the liquid crystal display panel. That is, the constant voltage supply **12** is replaced by a variable voltage supply in some cases.

[**0079**] The current I3 is the collector current of the transistor Q9. This current is set to be twice the current I2, and flows into the charging control differential switch circuit constructed by the transistors Q**10** and Q**11**. The current I4 is the collector current of the transistor Q13. The current I3 satisfies the relation I3=2×I4. The transistors Q12 and Q13 constitute a current mirror circuit.

[**0080**] In the charging control differential switch circuit, one input terminal receives the electric potential of the capacitive load CL, that is, the electric potential VOUT of the output terminal **16**. The other input terminal receives the electric potential of the constant voltage supply **12**. Then, depending on the result of comparison between the electric potential of the capacitive load CL and the electric potential of the constant voltage supply **12**, the charging control differential switch circuit performs on-off control of the base current of the output transistor Q1, that is, the first current I2.

[**0081**] The discharging-current switch circuit **31** comprises transistors Q**4**, Q**5**, Q**6**, Q**7**, and Q**8** and a constant voltage supply **11** for generating an electric potential defining the lower amplitude limit V1. More specifically, the constant voltage supply **11** generates an electric potential equal to the lower amplitude limit V1. In an exemplary case that the voltage applied to the power supply terminal **17** is 12 V, the lower amplitude limit V1 is set, for example, at approximately 2 V. In case that the capacitive load CL is composed, for example, of a common electrode of a liquid crystal display panel, the lower amplitude limit V1 is not fixed but variable in some cases for the purpose of adjustment of the visibility of the liquid crystal display panel. That is, the constant voltage supply **11** is replaced by a variable voltage supply in some cases.

[**0082**] The current I**5** is the collector current of the transistor Q7. This current is set to be twice the current I7, and flows out from the discharging control differential switch circuit constructed by the transistors Q6 and Q8. The current I8 is the collector current of the transistor Q4. The current I5 satisfies the relation I5=2×I8. The transistors Q4 and Q5 constitute a current mirror circuit.

[**0083**] In the discharging control differential switch circuit, one input terminal receives the electric potential of the capacitive load CL, that is, the electric potential VOUT of the output terminal **16**. The other input terminal receives the electric potential of the constant voltage supply **11**. Then, depending on the result of comparison between the electric potential of the capacitive load CL and the electric potential of the constant voltage supply **11**, the discharging control differential switch circuit performs on-off control of the base current of the output transistor Q2, that is, the second current I7.

[**0084**] The charging and discharging-current generating circuit **51** comprises: transistors Q14, Q15, Q16, Q17, Q18, Q19, Q**20**, and Q21; capacitors Cl and C2 serving as frequency-dependent impedance elements or capacitive impedance elements; a constant voltage supply **13**; and a constant current supply **14**. The combination of the transistors Q14 and Q15, the combination of the transistors Q**16** and Q17, and the combination of the transistors Q18 and Q**19** constitute current mirror circuits respectively.

[**0085**] The transistors Q**20** and Q21 constitute a differential switch circuit. In this differential switch circuit, one input terminal receives the electric potential of the load control input signal S1, while the other input terminal receives the electric potential V3 of the constant voltage supply **13**. The emitters of the transistors Q**20** and Q**21** are connected to the constant current supply **14**. The differential switch circuit compares the electric potential of the load control input signal S1 with the electric potential V3 of the constant voltage supply **13**, and thereby determines the state (high level or low level) of the load control input signal S1 so as to switch the path through which the current I1 of the constant current supply **14** flows, depending on the determination result.

[**0086**] **FIG. 5** shows output waveforms of the capacitive load driving circuit of **FIGS. 1 and 2**. **FIG. 5** is wave form diagrams showing the load control input signal S1 and the voltage VOUT appearing in the output terminal **16**. When the threshold voltage where the on-off state alternates in the charging-current switch circuit **41** is denoted by V2, and when the threshold voltage where the on-off state alternates in the discharging-current switch circuit **31** is denoted by V1, the load control input signal S1 is inputted to the input terminal **15**, while the electric potential VOUT is obtained in the output terminal **16**.

[**0087**] The operation of the circuit of **FIG. 2** is described below in detail with reference to **FIG. 5**. Described below is a charging period where the load control input signal S1 applied to the input terminal **15** alternates from a low level to a high level.

[0088] When the voltage applied to the input terminal **15**, that is, the electric potential of the load control input signal S1, goes higher than the electric potential V3 of the constant voltage supply **13**, the transistor Q**21** goes on. At this time, all of the current I1 of the constant current supply **14** flows through the transistor Q**21**. The transistor Q**21** is connected to the current mirror circuit constructed by the transistors Q**17** and Q**16**. This current mirror circuit allows the transistor Q**16** to output the current I2 as the collector current. The amount of the current I2 is the same as the current I1 in a stationary state.

[0089] The collector of the transistor Q**16** is connected to the base of the charging output transistor Q1 and the collector of the transistor Q**13**. In general, when the load control input signal S1 applied to the input terminal **15** alternates from a low level to a high level, the electric potential of the output terminal **16** is lower than the electric potential V2 of the constant voltage supply **12**. Accordingly, in the charging control differential switch circuit constructed by the transistors Q**10** and Q**11**, the transistor Q**10** is on. Thus, no current flows through the transistor Q**11**. Since the transistor Q**13** is connected to the transistor Q**11** via the current mirror circuit, no current flows through the transistor Q**13**. As a result, the collector current I4 of the transistor Q**13** is zero.

[0090] Consequently, all of the current I2 serves as the base current of the charging output transistor Q1.

[0091] Since the current I2 flows into the charging output transistor Q1 as the base current, this transistor supplies the emitter current in an amount of hfe-times the base current, to the capacitive load CL. At that time, since no base current is supplied to the discharging output transistor Q2, all of the emitter current of the charging output transistor Q1 flows into the capacitive load CL. This current causes the electric potential VOUT of the output terminal **16** to go higher as shown in **FIG. 5**.

[0092] When the electric potential VOUT of the output terminal **16** becomes equal to the electric potential V2 of the constant voltage supply **12**, the same amount of currents flow respectively through the transistors Q**10** and Q**11**. The amount of each current is half of the collector current I3 of the transistor Q9. However, in this circuit, the current I3 is set to be twice the current I2. As a result, a current of the same amount as the current I2 flows through the transistor Q**11**.

[0093] The current flowing through the transistor Q**11** flows through the current mirror circuit constructed by the transistors Q**12** and Q**13**, and thereby causes the collector current I4 of the transistor Q**13**. Since the amount of the current I4 is the same as the current I2, all of the collector current I2 provided by the transistor Q**16** flows into the transistor Q**13**, so that the supply of the base current to the output transistor Q1 is stopped. When the supply of the base current is stopped, the output transistor Q1 stops the supply of the charging-current to the capacitive load CL. As a result, the electric potential VOUT of the output terminal **16** is set to be the electric potential V2 of the constant voltage supply **12**.

[0094] Described below next is a discharging period where the load control input signal S1 applied to the input terminal **15** as shown in **FIG. 5** alternates from a high level to a low level.

[0095] When the voltage applied to the input terminal **15**, that is, the electric potential of the load control input signal S1, goes lower than the electric potential V3 of the constant voltage supply **13**, the transistor Q**20** goes on. At this time, all of the current I1 of the constant current supply **14** flows through the transistor Q**20**. The transistor Q**20** is connected to the current mirror circuit constructed by the transistors Q**18** and Q**19**. This current mirror circuit allows the transistor Q**18** to output the collector current I**6**. The amount of the collector current I**6** is the same as the current I1 of the constant current supply **14**. The transistor Q**18** is connected to the current mirror circuit constructed by the transistors Q**14** and Q**15**. This current mirror circuit causes the collector current I**7** through the transistor Q**14**. The amount of the current I**6** is the same as the current I**7** in a stationary state.

[0096] The collector of the transistor Q**14** is connected to the base of the discharging output transistor Q2 and the collector of the transistor Q4. In general, when the load control input signal S1 applied to the input terminal **15** alternates from a high level to a low level, the electric potential of the output terminal **16** is higher than the electric potential V1 of the constant voltage supply **11**. Accordingly, in the charging control differential switch circuit constructed by the transistors Q**6** and Q**8**, the transistor Q**8** is on. Thus, no current flows through the transistor Q**6**. Since the transistor Q4 is connected to the transistor Q**6** via the current mirror circuit, no current flows through the transistor Q4. As a result, the collector current I**8** of the transistor Q4 is zero.

[0097] Consequently, all of the current I**7** serves as the base current of the discharging output transistor Q2.

[0098] Since the current I**7** flows out from the discharging output transistor Q2 as the base current, this transistor withdraws the emitter current in an amount of hfe-times the base current, from the capacitive load CL. At that time, since no base current is supplied to the charging output transistor Q1, all of the emitter current of the discharging output transistor Q2 is supplied from the capacitive load CL. This current causes the electric potential VOUT of the output terminal **16** to go lower as shown in **FIG. 5**.

[0099] When the electric potential VOUT of the output terminal **16** becomes equal to the electric potential V1 of the constant voltage supply **11**, the same amount of currents flow respectively through the transistors Q**6** and Q**8**. The amount of each current is half of the collector current I**5** of the transistor Q7. However, in this circuit, the current I**5** is set to be twice the current I**7**. As a result, a current of the same amount as the current I**7** flows through the transistor Q**6**.

[0100] The current flowing through the transistor Q**6** flows through the current mirror circuit constructed by the transistors Q4 and Q5, and thereby causes the collector current I**8** of the transistor Q4. Since the amount of the current I**8** is the same as the current I**7**, all of the collector current I**7** provided by the transistor Q**14** flows out from the transistor Q4, so that the supply of the base current to the output transistor Q2 is stopped. When the supply of the base current is stopped, the output transistor Q2 stops the withdrawal of the discharging-current from the capacitive load CL. As a result, the electric potential VOUT of the output terminal **16** is set to be the electric potential V1 of the constant voltage supply **11**.

[0101] As described above, the configuration that the charging and discharging control circuit **22** is constructed by the charging-current switch circuit **41** and the discharging-current switch circuit **31** permits the complete shut-off of the charging and discharging-currents supplied to the output circuit **21**, and thereby realizes low electric power consumption. This allows the capacitive load driving circuit to be easily built in a driver integrated circuit for driving a liquid crystal display panel.

[0102] Further, the output voltage amplitude of the output circuit **21** is defined by the charging-current switch circuit **41** and the discharging-current switch circuit **31**, and the charging-current switch circuit **41** and the discharging-current switch circuit **31** are composed respectively of the charging-current control differential switch circuit and the discharging-current control differential switch circuit having a good temperature characteristic. This avoids the problem of variation in the output voltage amplitude of the output circuit **21** caused by temperature variation.

[0103] Described below is the operation of the capacitors Cl and C2 provided in the charging and discharging-current generating circuit **51**. According to this configuration comprising the capacitors Cl and C2, even when the through-rate is high in the load control input signal S1, a steep change in the base current I2 is alleviated by the impedance of the capacitor Cl which is proportional to the frequency component. Similarly, a steep change in the base current I7 is alleviated by the impedance of the capacitor C2 which is proportional to the frequency component. This avoids a steep change in the charging and discharging-currents, and hence provides a stable output waveform without an overshoot and an undershoot.

[0104] This point is described below in detail. In case that the capacitors Cl and C2 are not provided, the operation becomes as follows.

[0105] When the load control input signal S1 applied to the input terminal **15** is a pulse signal having a high through-rate, the change in the base currents of the charging and discharging output transistors Q1 and Q2 becomes steep. Thus, in the charging, in case that a time difference occurs between the time when the electric potential VOUT of the output terminal **16** reaches the electric potential V2 of the constant voltage supply **12** and the time when the supply of the base current to the output transistor Q1 is stopped, an overcharging-current is supplied to the capacitive load CL. In the discharging, in case that a time difference occurs between the time when the electric potential VOUT of the output terminal **16** reaches the electric potential V1 of the constant voltage supply **11** and the time when the supply of the base current to the output transistor Q2 is stopped, an overdischarging-current is withdrawn from the capacitive load CL. This causes an overshoot and an undershoot where the amplitude of the electric potential VOUT of the output terminal **16** goes outside the lower amplitude limit V1 and the upper amplitude limit V2 which are set by the constant voltage supplies **11** and **12**, respectively.

[0106] In the circuit of **FIGS. 1 and 2**, a part of the output current of the output circuit **21** is fed back to the charging and discharging-current generating circuit **51** via the capacitors C1 and C2 serving as frequency-dependent impedance elements provided between the charging and discharging-current generating circuit **51** and the output circuit **21**, so that the through-rate is suppressed at the alternation of the output state of the charging and discharging-current generating circuit **51**, so that the supply of an overcharging-current and an overdischarging-current is avoided.

[0107] The operation in the charging is described below first. When a current I2 is suddenly supplied as the base current to the charging output transistor Q1, the output transistor Q1 suddenly tries to supply a charging-current to the capacitive load CL. This current flows also through the capacitor C1 as a current I12. The capacitor C1 is connected to the collector of the transistor Q21 for supplying the current I2, so that the current I12 constitutes a part of the collector current of the transistor Q21.

[0108] The sudden change in the charging-current flowing through the output transistor Q1 indicates that a large amount of high-frequency component current is contained. Thus, the reactance of the capacitor C1 becomes smaller for the current I12. Accordingly, a more sudden change causes a larger amount of current I12. Since the amount of the collector current of the transistor Q17 is equal to I1–I12, a larger amount of the current I12 causes a smaller amount of the collector current of the transistor Q17. The transistor Q17, together with the transistor Q16, constitutes a current mirror circuit, so as to supply the base current I2 to the output transistor Q1. Thus, a decrease in the collector current of the transistor Q17 causes a decrease in the current I2 serving as the base current of the output transistor Q1, and hence reduces the amount of the charging-current. As a result, no steep change occurs in the charging-current.

[0109] The operation in the discharging is described next. When a current I7 is suddenly supplied as the base current to the discharging output transistor Q2, the output transistor Q2 suddenly tries to withdraw a discharging-current from the capacitive load CL. This current flows also through the capacitor C2 as a current I13. The capacitor C2 is connected to the collector of the transistor Q18 for supplying the current I7, so that the current I13 constitutes a part of the collector current of the transistor Q18.

[0110] The sudden change in the discharging-current flowing through the output transistor Q2 indicates that a large amount of high-frequency component current is contained. Thus, the reactance of the capacitor C2 becomes smaller for the current I13. Accordingly, a more sudden change causes a larger amount of current I13. Since the amount of the collector current of the transistor Q15 is equal to I6—I13, a larger amount of the current I13 causes a smaller amount of the collector current of the transistor Q15. The transistor Q15, together with the transistor Q14, constitutes a current mirror circuit, so as to supply the base current I7 to the output transistor Q2. Thus, a decrease in the collector current of the transistor Q15 causes a decrease in the base current I7 of the output transistor Q2, and hence reduces the amount of the discharging-current. As a result, no steep change occurs in the discharging-current.

[0111] By virtue of these operation, even when the load control input signal S1 applied to the input terminal **15** is a pulse signal having a high through-rate, no overcharging-current and no overdischarging-current is supplied to the capacitive load CL.

[0112] As such, in this capacitive load driving circuit, even when the through-rate is high in the load control input signal S1, the capacitors C1 and C2 serving as frequency-dependent impedance elements restrict the through-rate, so as to permit smooth alternation of the charging and discharging-currents. This avoids an overshoot and an undershoot at the alternation of the charging and discharging-currents. This provides a stable output waveform without an overshoot and an undershoot, and hence avoids a steep change in the charging and discharging-currents.

[0113] The electric potential V1 and V2 generated by the constant voltage supplies **11** and **12** in the above-mentioned description may be generated arbitrarily by a resistor type voltage divider circuit for dividing a power supply voltage, or alternatively may be inputted as arbitrary voltage values through external electrodes. In order that these values be variable, the resistor type voltage divider circuit can be implemented using a variable resistor as the divider resistor.

[0114] As shown in **FIG. 2**, the overcharging-current prevention switch circuit **61** is composed of an NPN transistor Q**25** the collector of which is connected to the base of the output transistor Q**1**, and the emitter of which is connected to the output terminal **16**, and further the base of which is connected to a constant voltage supply **19**. The constant voltage supply **19** generates a predetermined electric potential higher than the electric potential of the ground terminal **17** and lower than or equal to the lower amplitude limit V**1**. In this embodiment, this generated electric potential is equal to the lower amplitude limit V**1**.

[0115] The overdischarging-current prevention switch circuit **71** is composed of an PNP transistor Q**26** the collector of which is connected to the base of the output transistor Q**2**, and the emitter of which is connected to the output terminal **16**, and further the base of which is connected to a constant voltage supply **20**. The constant voltage supply **20** generates a predetermined electric potential lower than the electric potential of the power supply terminal **17** and higher than or equal to the upper amplitude limit V**2**. In this embodiment, this generated electric potential is equal to the upper amplitude limit V**2**.

[0116] In this case, the constant voltage supplies **19** and **20** may be replaced by variable voltage supplies for generating variable voltages, so that these variable voltage supplies may operate in linkage with the changes in the electric potentials of other variable voltage supplies used in place of the constant voltage supplies **11** and **12**.

[0117] According to this configuration, when the electric potential of the constant voltage supply **11** or **12** is adjusted for the purpose of adjusting the upper amplitude limit V**2** or the lower amplitude limit V**1** of the capacitive load CL, avoided is the occurrence of mismatching with the electric potential where the overcurrent protection circuit **23** stops the charging-current supplying operation or the discharging-current withdrawing operation. This avoids the occurrence of abnormality in the control operation of the charging control differential switch circuit and the discharging control differential switch circuit.

[0118] The above-mentioned abnormality is described below in detail. When the voltage of the constant voltage supply **20** is lower than the upper amplitude limit V**2** by an amount of the emitter-base voltage Veb of the PNP transistor Q**26** or more, the PNP transistor Q**26** serves as a voltage clipping circuit, so that the voltage of the output terminal **16** does not reach the predetermined upper amplitude limit V**2**, but stays at a voltage of V**20**+Vbe. Here, V**20** indicates the voltage of the constant voltage supply **20**.

[0119] When the voltage of the constant voltage supply **19** is higher than the lower amplitude limit V**1** by an amount of the emitter-base voltage Veb of the NPN transistor Q**25** or more, the PNP transistor Q**25** serves as a voltage clipping circuit, so that the voltage of the output terminal **16** does not reach the predetermined lower amplitude limit V**1**, but stays at a voltage of V**19**−Vbe. Here, V**19** indicates the voltage of the constant voltage supply **19**.

[0120] The operation of the overcharging-current prevention switch circuit **61** and the overdischarging-current prevention switch circuit **71** is described below in detail with reference to **FIG. 2**.

[0121] When the electric potential of the input terminal **15** is high, all of the current I**1** flows through the transistor Q**21**. The current I**1** flows through the current mirror circuit constructed by the transistors Q**16** and Q**17**, so as to cause a current I**2** serving as the base current of the output transistor Q**1** which flows into the base of the output transistor Q**1**. When receiving the base current, the output transistor Q**1** supplies a charging-current from the emitter to the capacitive load CL. This charging-current flows ceaselessly until the electric potential VOUT of the output terminal **16** reaches the upper amplitude limit V**2** so as to cause the charging-current switch circuit **41** to shut off the base current. When the electric potential of the input terminal **15** is high, no base current is supplied to the discharging output transistor Q**2**, so that the discharging output transistor Q**2** is off.

[0122] In this case, when a short circuit (earth fault) occurs between the output terminal **16** and the ground terminal **18**, the electric potential VOUT of the output terminal **16** becomes a value sufficiently lower than the lower amplitude limit V**1**. This causes the NPN transistor Q**25** to be on, so that a collector current I**9** flows. At this time, all of the current I**2** serves as the current I**9**. Thus, the base current of the output transistor Q**1** is shut off, so that the supply of the charging-current to the output terminal **16** is stopped. As a result, an overcharging-current is prevented from flowing ceaselessly through the output transistor Q**1** when an earth fault occurs in the output terminal **16**.

[0123] In the configuration of the circuit of **FIG. 2**, the current I**9** flowing through the NPN transistor Q**25** flows into the capacitive load CL. However, this current is equivalent to the base current of the output transistor Q**1**, and hence negligible small. In case that the overcharging-current prevention switch circuit **61** is constructed by differential transistors in place of a single NPN transistor, the current equivalent to the current I**9** is prevented from flowing into the capacitive load CL.

[0124] On the contrary, when the electric potential of the input terminal **15** is low, all of the current I**1** flows through the transistor Q**20**. The current I**1** flows through the current mirror circuit constructed by the transistors Q**18** and Q**19** and the current mirror circuit constructed by the transistors Q**14** and Q**15**, so as to cause a current I**7** serving as the base current of the output transistor Q**2** which is withdrawn from the base of the output transistor Q**2**. When the base current is withdrawn, the output transistor Q**2** withdraws a discharging-current from the capacitive load CL via the emitter. This discharging-current flows ceaselessly until the electric potential VOUT of the output terminal **16** reaches the lower amplitude limit V**1** so as to cause the discharging-current switch circuit **31** to shut off the base current. When the electric potential of the input terminal **15** is low, no base current is supplied to the charging output transistor Q**1**, so that the charging output transistor Q**1** is off.

[0125] In this case, when a short circuit (sky fault) occurs between the output terminal **16** and the power supply terminal **17**, the electric potential VOUT of the output terminal **16** becomes a value sufficiently higher than the upper amplitude limit V**2**. This causes the PNP transistor Q**26** to be on, so that a collector current I**10** flows. At this time, all of the current I**7** serves as the current I**10**. Thus, the base current of the output transistor Q**2** is shut off, so that the withdrawal of the discharging-current from the output terminal **16** is stopped. As a result, an overdischarging-current is prevented from flowing ceaselessly through the output transistor Q**2** when an sky fault occurs in the output terminal **16**.

[0126] When the capacitive load driving circuit according to the invention is used for driving a liquid crystal display panel common electrode, high driving performance is obtained, while a circuit for preventing an overcurrent is built in. This avoids the necessity of a buffer circuit and a protection circuit having been attached externally in the prior art, and hence reduces the number of components.

[0127] Furthermore, the present configuration that the charging and discharging-currents are shut off when predetermined upper amplitude limit are lower amplitude limit are reached realizes low electric power consumption.

[0128] **FIG. 1**

[0129] **31** Discharging current switch circuit

[0130] **41** Charging current switch circuit

[0131] **51** Charging and discharging-current generating circuit

[0132] **61** Overcharging current prevention switch circuit

[0133] **71** Overdischarging-current prevention switch circuit

What is claimed is:

1. A capacitive load driving circuit for supplying a charging-current to a capacitive load and withdrawing a discharging-current from said capacitive load, comprising:

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said capacitive load, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from said capacitive load to said ground terminal; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation; wherein

said output circuit selects any one of said charging-current supplying operation and said discharging-current withdrawing operation depending on the state of a control input signal.

2. A capacitive load driving circuit according to claim 1, wherein said output circuit continues to charge said capacitive load in said charging-current supplying operation until the electric potential of said capacitive load reaches a predetermined upper amplitude limit lower than the electric potential of said power supply terminal, and continues to discharge said capacitive load in said discharging-current withdrawing operation until the electric potential of said capacitive load reaches a predetermined lower amplitude limit higher than the electric potential of said ground terminal.

3. A capacitive load driving circuit according to claim 1, wherein

said output circuit comprises: a first NPN transistor the collector of which is connected to said power supply terminal and the emitter of which is connected to said output terminal; and a first PNP transistor the collector of which is connected to said ground terminal and the emitter of which is connected to said output terminal; and wherein

said overcurrent protection circuit comprises: a second NPN transistor the collector of which is connected to the base of said first NPN transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a first voltage supply for generating a predetermined electric potential higher than the electric potential of said ground terminal; and a second PNP transistor the collector of which is connected to the base of said first PNP transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a second voltage supply for generating a predetermined electric potential lower than the electric potential of said power supply terminal.

4. A capacitive load driving circuit according to claim 2, wherein

said output circuit comprises: a first NPN transistor the collector of which is connected to said power supply terminal and the emitter of which is connected to said output terminal; and a first PNP transistor the collector of which is connected to said ground terminal and the emitter of which is connected to said output terminal; and wherein

said overcurrent protection circuit comprises: a second NPN transistor the collector of which is connected to the base of said first NPN transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a first voltage supply for generating a predetermined electric potential that is higher than the electric potential of said ground terminal and lower than or equal to said lower amplitude limit; and a second PNP transistor the collector of which is connected to the base of said first PNP transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a second voltage supply for generating a predetermined electric potential that is lower than the electric potential of said power supply terminal and higher than or equal to said upper amplitude limit.

5. A capacitive load driving circuit according to claim 1, wherein the state of said control input signal alternates periodically.

6. A capacitive load driving circuit for supplying a charging-current to a capacitive load and withdrawing a discharging-current from said capacitive load, comprising:

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said capacitive load, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said capacitive load and a discharging-current withdrawing operation of withdrawing a discharging-current from said capacitive load to said ground terminal;

a current generation circuit for selecting, depending on the state of a control input signal, any one of a first state where a first current is supplied to said output circuit so as to cause said output circuit to select said charging-current supplying operation and a second state where a second current is supplied to said output circuit so as to cause said output circuit to select said discharging-current withdrawing operation;

a charging and discharging control circuit for detecting the electric potential of said capacitive load and thereby controlling and causing said output circuit to continue said charging-current supplying operation until the electric potential of said capacitive load reaches a predetermined upper amplitude limit, to stop said charging-current supplying operation when said electric potential reaches said predetermined upper amplitude limit, to continue said discharging-current withdrawing operation until the electric potential of said capacitive load reaches a predetermined lower amplitude limit, and to stop said discharging-current withdrawing operation when said electric potential reaches said predetermined lower amplitude limit; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation.

7. A capacitive load driving circuit according to claim 6, wherein

said output circuit comprises: a first NPN transistor the collector of which is connected to said power supply terminal and the emitter of which is connected to said output terminal; and a first PNP transistor the collector of which is connected to said ground terminal and the emitter of which is connected to said output terminal; wherein

said overcurrent protection circuit comprises: a second NPN transistor the collector of which is connected to the base of said first NPN transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a first voltage supply for generating a predetermined electric potential that is higher than the electric potential of said ground terminal and lower than or equal to said lower amplitude limit; and a second PNP transistor the collector of which is connected to the base of said first PNP transistor, and the emitter of which is connected to said output terminal, and further the base of which is connected to a second voltage supply for generating a predetermined electric potential that is lower than the electric potential of said power supply terminal and higher than or equal to said upper amplitude limit; and wherein

said charging and discharging control circuit controls the base currents of said first NPN transistor and said first PNP transistor, so as to control the execution and the stop of said charging-current supplying operation and said discharging-current withdrawing operation.

8. A capacitive load driving circuit according to claim 7, wherein said charging and discharging control circuit comprises: a third voltage supply for generating an electric potential equal to said upper amplitude limit; a fourth voltage supply for generating an electric potential equal to said lower amplitude limit; a charging control differential switch circuit one input terminal of which receives the electric potential of said capacitive load, and the other input terminal of which receives the electric potential of said third voltage supply; and a discharging control differential switch circuit one input terminal of which receives the electric potential of said capacitive load, and the other input terminal of which receives the electric potential of said fourth voltage supply; and wherein said charging control differential switch circuit performs on-off control of the base current of said first NPN transistor depending on the result of comparison between the electric potential of said capacitive load and the electric potential of said third voltage supply, while said discharging control differential switch circuit performs on-off control of the base current of said first PNP transistor depending on the result of comparison between the electric potential of said capacitive load and the electric potential of said fourth voltage supply.

9. A capacitive load driving circuit according to claim 8, wherein the electric potentials of said third and fourth voltage supplies are variable, and wherein the electric potential of said first voltage supply varies in linkage with the electric potential of said fourth voltage supply, while the electric potential of said second voltage supply varies in linkage with the electric potential of said third voltage supply.

10. A capacitive load driving circuit according to claim 8, wherein the electric potential of said first voltage supply is equal to the electric potential of said fourth voltage supply, while the electric potential of said second voltage supply is equal to the electric potential of said third voltage supply.

11. A capacitive load driving circuit according to claim 6, wherein a frequency-dependent impedance element is provided between said current generation circuit and said output circuit, so that a part of the output current of said output circuit is fed back through said frequency-dependent impedance element to said current generation circuit, so that the through-rate is suppressed at the alternation of the output state of said current generation circuit.

12. A capacitive load driving circuit according to claim 6, wherein the state of said control input signal alternates periodically.

13. A liquid crystal display comprising:

a liquid crystal display panel common electrode;

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said liquid crystal display panel common electrode, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said liquid crystal display panel common electrode and a discharging-current withdrawing operation of withdrawing a discharging-current from said liquid crystal display panel common electrode to said ground terminal; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation; wherein

said output circuit selects any one of said charging-current supplying operation and said discharging-current withdrawing operation depending on the state of a control input signal.

14. A liquid crystal display comprising:

a liquid crystal display panel common electrode;

an output circuit which comprises a power supply terminal, a ground terminal, and an output terminal connected to said liquid crystal display panel common electrode, and which performs a charging-current supplying operation of supplying a charging-current from said power supply terminal to said liquid crystal display panel common electrode and a discharging-current withdrawing operation of withdrawing a discharging-current from said liquid crystal display panel common electrode to said ground terminal;

a current generation circuit for selecting, depending on the state of a control input signal, any one of a first state where a first current is supplied to said output circuit so as to cause said output circuit to select said charging-current supplying operation and a second state where a second current is supplied to said output circuit so as to cause said output circuit to select said discharging-current withdrawing operation;

a charging and discharging control circuit for detecting the electric potential of said liquid crystal display panel common electrode and thereby controlling and causing said output circuit to continue said charging-current supplying operation until the electric potential of said liquid crystal display panel common electrode reaches a predetermined upper amplitude limit, to stop said charging-current supplying operation when said electric potential reaches said predetermined upper amplitude limit, to continue said discharging-current withdrawing operation until the electric potential of said liquid crystal display panel common electrode reaches a predetermined lower amplitude limit, and to stop said discharging-current withdrawing operation when said electric potential reaches said predetermined lower amplitude limit; and

an overcurrent protection circuit for detecting a short circuit between said output terminal and said ground terminal so as to stop or suppress said charging-current supplying operation, and for detecting a short circuit between said output terminal and said power supply terminal so as to stop or suppress said discharging-current withdrawing operation.

* * * * *

专利名称(译)	电容负载驱动电路和液晶显示器		
公开(公告)号	US20040169980A1	公开(公告)日	2004-09-02
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[标]申请(专利权)人(译)	天野YUJI NIRASAWA YOSHIO HAMAGUCHI HIDEO		
申请(专利权)人(译)	天野YUJI NIRASAWA YOSHIO HAMAGUCHI HIDEO		
当前申请(专利权)人(译)	天野YUJI NIRASAWA YOSHIO HAMAGUCHI HIDEO		
[标]发明人	AMANO YUJI NIRASAWA YOSHIO HAMAGUCHI HIDEO		
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摘要(译)

当在输出端子和电源端子或接地端子之间发生短路时，防止过电流流入输出电路。为此目的，提供了一种输出电路，包括电源端子，接地端子和连接到电容性负载的输出端子。根据负载控制输入信号的状态，输出电路选择性地执行从电源端子向电容性负载提供充电电流的充电电流提供操作和提取放电电流的放电电流提取操作。从容性负载到接地端子。此外，提供过充电电流防止开关，用于检测输出端子和接地端子之间的短路，以便停止或抑制充电电流供应操作。此外，提供过放电电流防止开关，用于检测输出端子和电源端子之间的短路，以便停止或抑制放电电流提取操作。