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(54) SHIFT REGISTER HAVING FEWER LINES THEREIN, AND LIQUID CRYSTAL DISPLAY HAVING THE SAME

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(57) **ABSTRACT**

A shift register has m stages which store one of two states, where m is an integer more than 1, each stage including clock input terminals at which n-phase clock signals are input, where n is an integer more than 1, and an input terminal, and an output terminal. The input terminal of one stage receives the signal delivered from an input terminal of the shift register or from the output terminal of the previous stage. The signal output at the output terminal of one stage is passed to the input terminal of the subsequent stage or to an output terminal of the shift register. Each stage receives an initial state level from one of the clock input terminals. The initial state level is used to initialize the state of each stage.

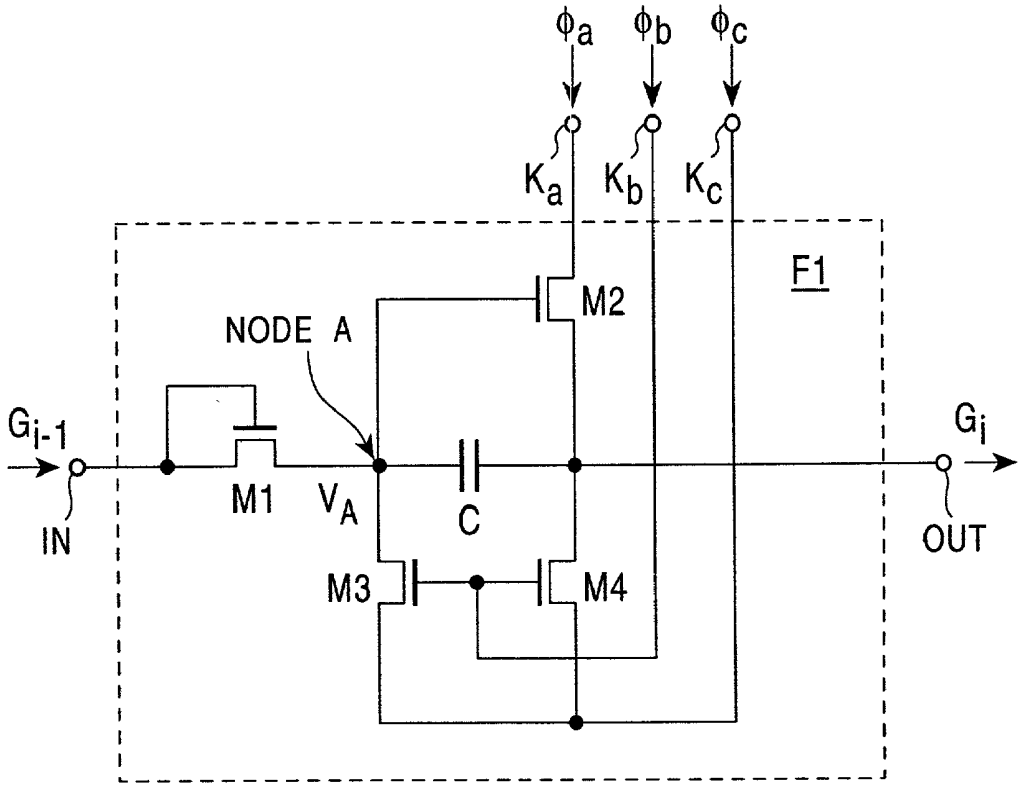


FIG. 1

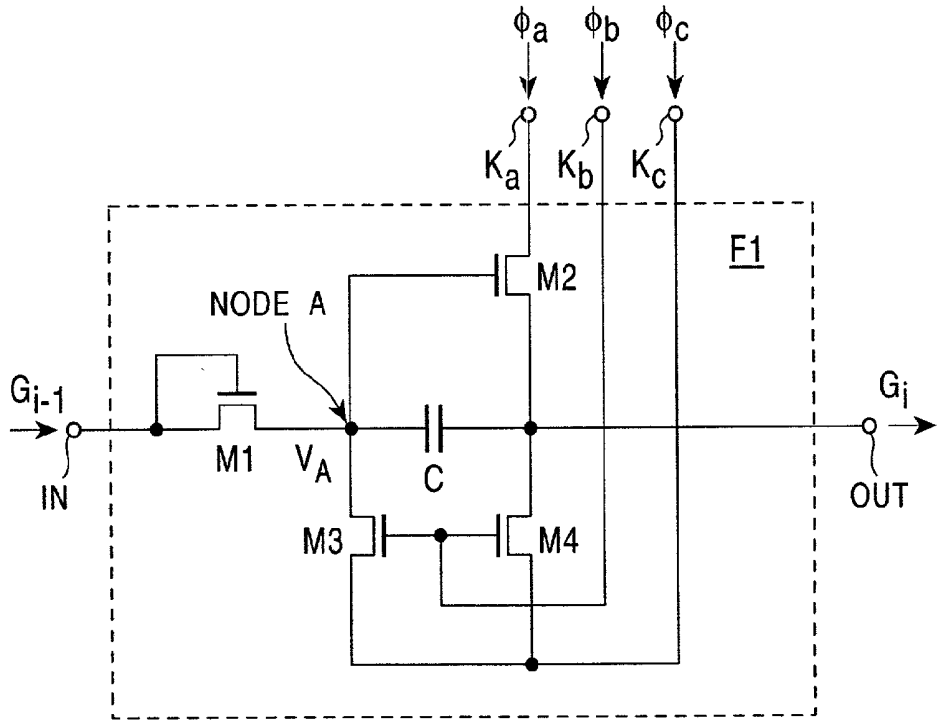


FIG. 2

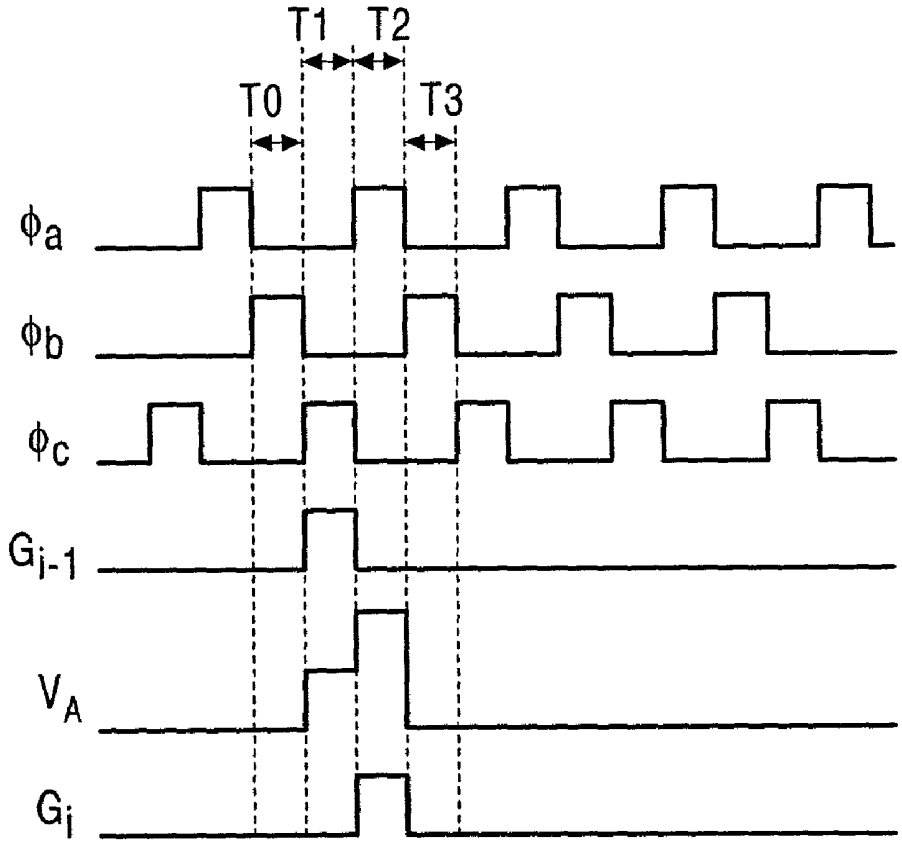


FIG. 3

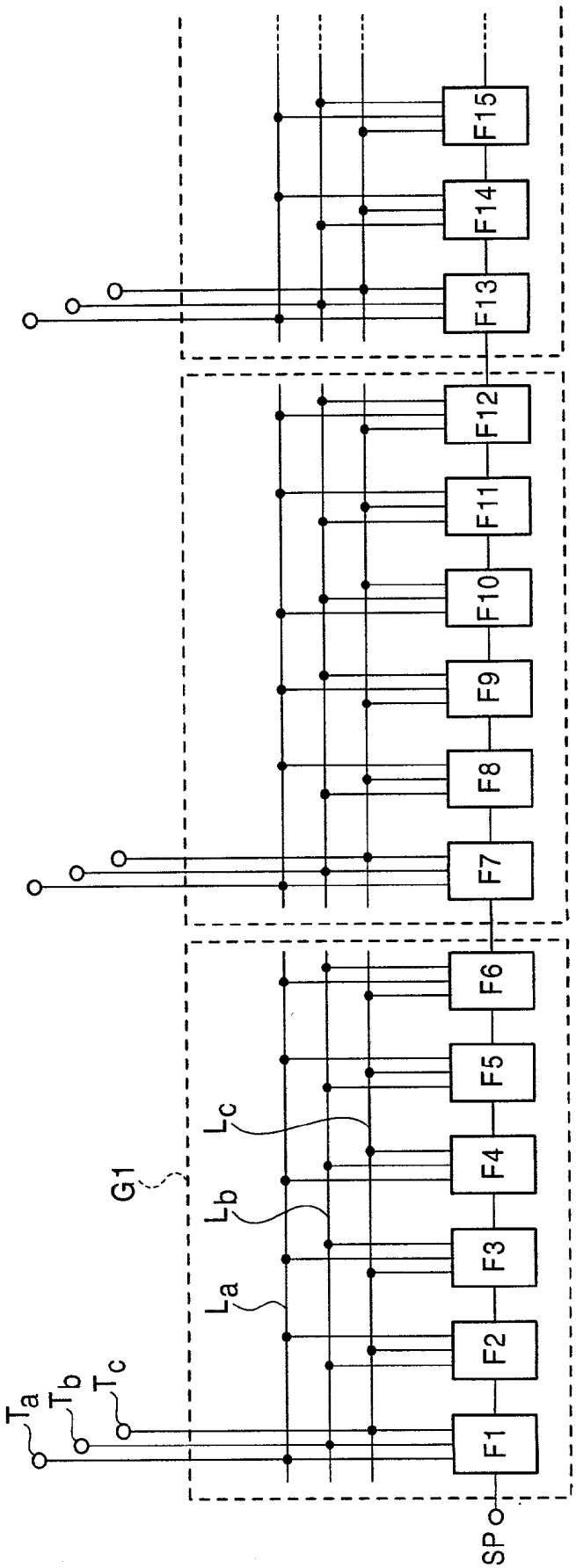

F15
F14
F13
F12
F11
F10
F9
F8
F7
F6
F5
F4
F3
F2
F1
Lc
Lb
La
G1
Ta
Tb
Tc
SP

FIG. 4

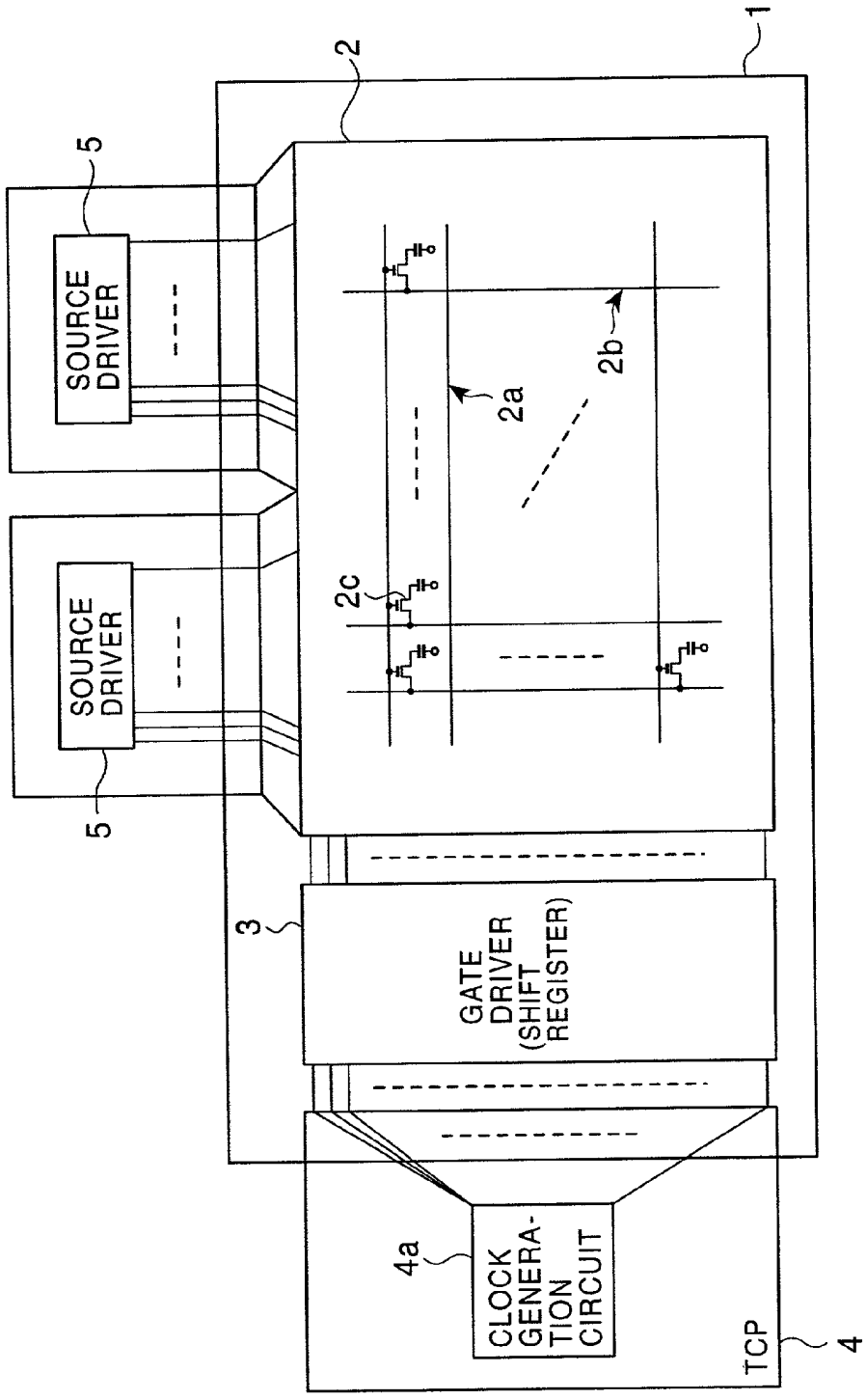

1
2
5
SOURCE DRIVER
SOURCE DRIVER
5
2a
2b
2c
3
GATE DRIVER (SHIFT REGISTER)
4a
CLOCK GENERA-TION CIRCUIT
TCP
4

FIG. 5

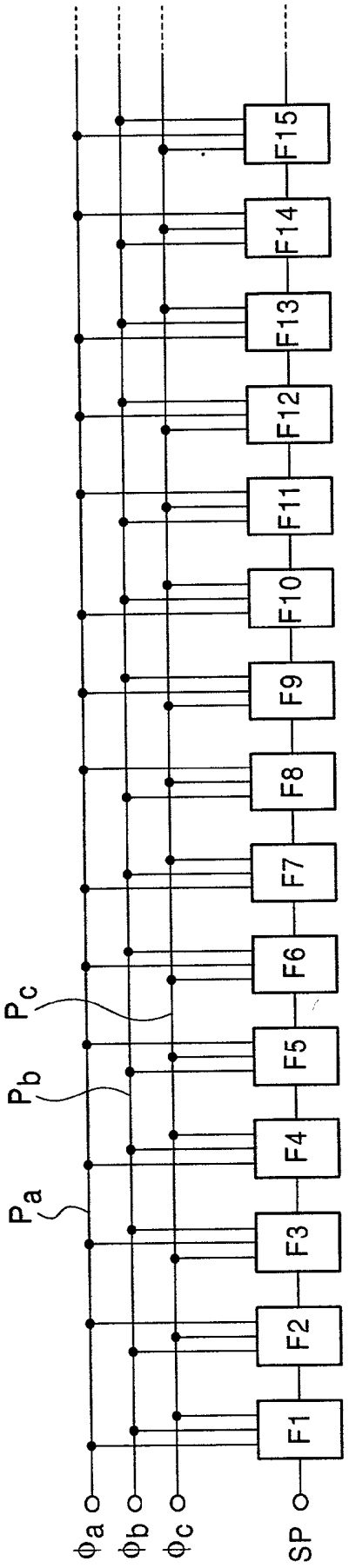

F15
F14
F13
F12
F11
F10
F9
F8
F7
F6
F5
F4
F3
F2
F1
Pc
Pb
Pa
φa
φb
φc
SP

FIG. 6

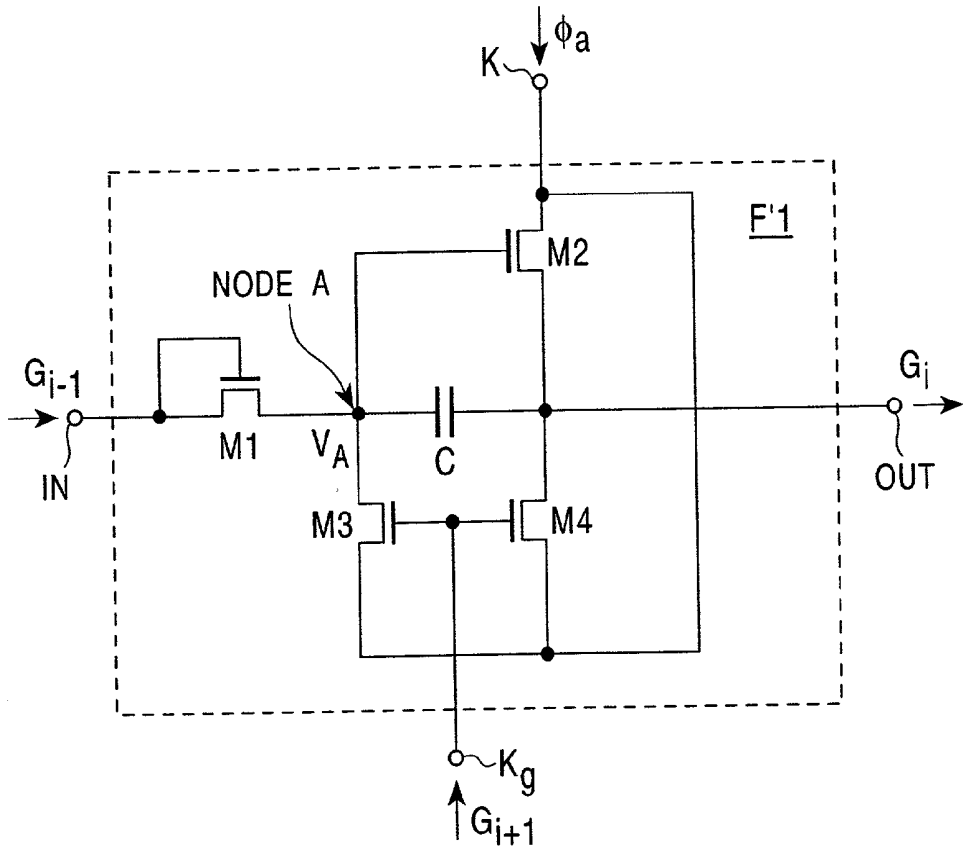


FIG. 7

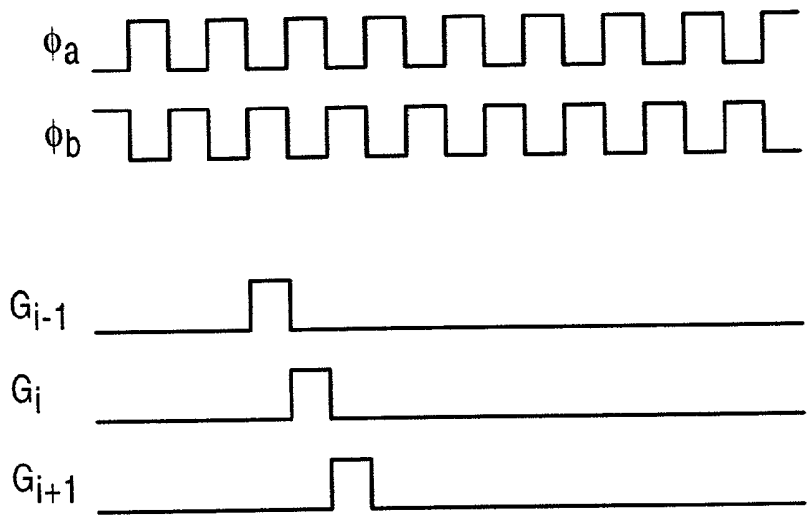


FIG. 8

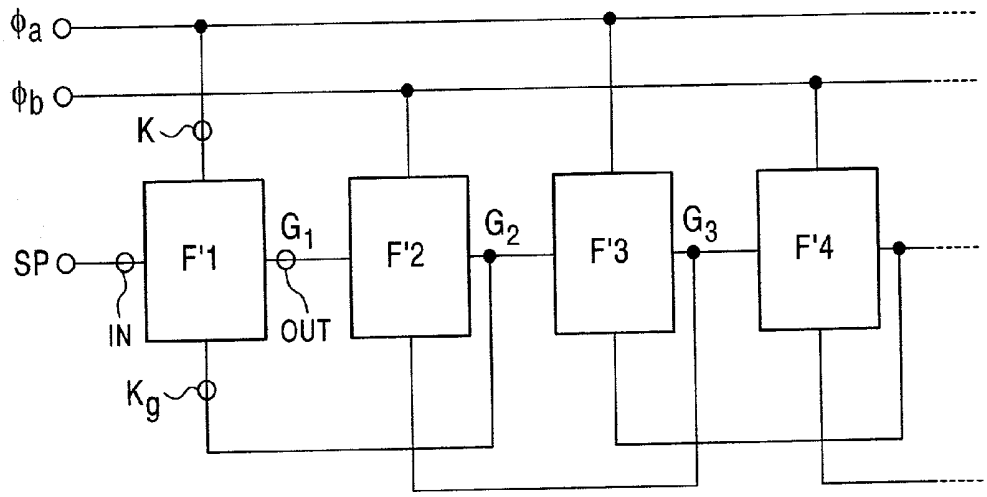

φa
φb
K
SP
IN
F'1
G1
OUT
F'2
G2
F'3
G3
F'4
Kg

FIG. 9

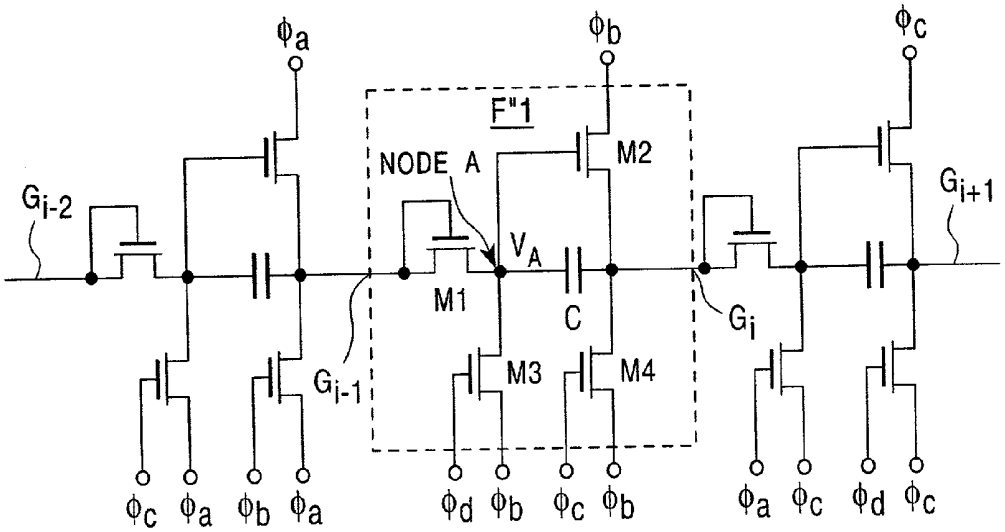

φa
φb
φc
F"1
NODE A
M2
Gi-2
VA
Gi+1
M1
C
Gi
Gi-1
M3
M4
φc φa φb φa
φd φb φc φb
φa φc φd φc

FIG. 10

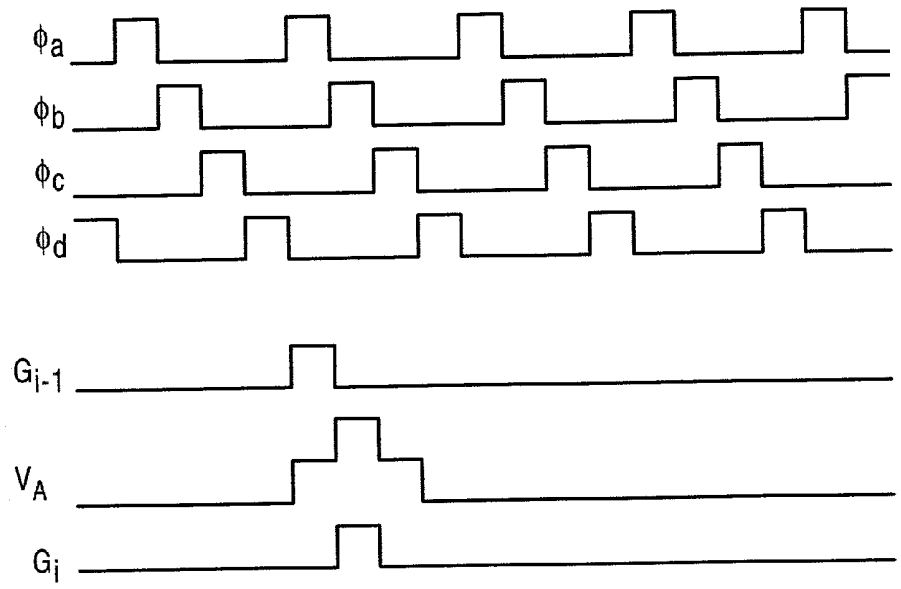


FIG. 11

	COMPARATIVE EXAMPLE	EMBODIMENT 1	EMBODIMENT 2	EMBODIMENT 3
R (PER LINE)	1200 Ω	90 kΩ	1200 Ω	63 kΩ
C (PER LINE)	860 pF	11 pF	860 pF	16 pF
LINE WIDTH	80 μm	≪1 μm	80 μm	≪1μm
LINE NUMBER	4 (INCLUDING GND)	3	3	2

FIG. 12

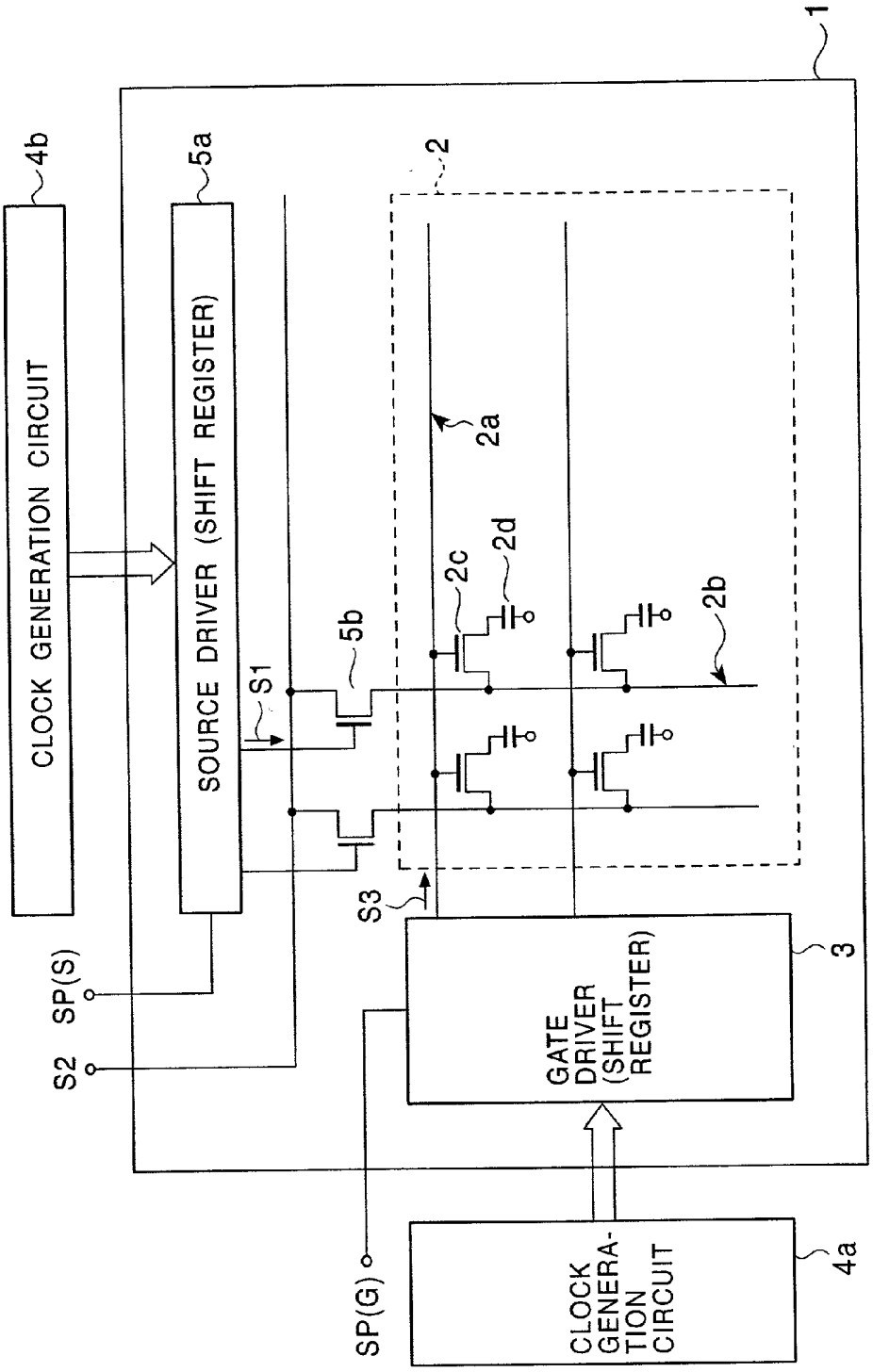

1
4b
5a
2
CLOCK GENERATION CIRCUIT
SOURCE DRIVER (SHIFT REGISTER)
2a
2c
2d
2b
5b
S1
S3
SP(S)
S2
SP(G)
GATE DRIVER (SHIFT REGISTER)
3
CLOCK GENERA-TION CIRCUIT
4a

FIG. 13

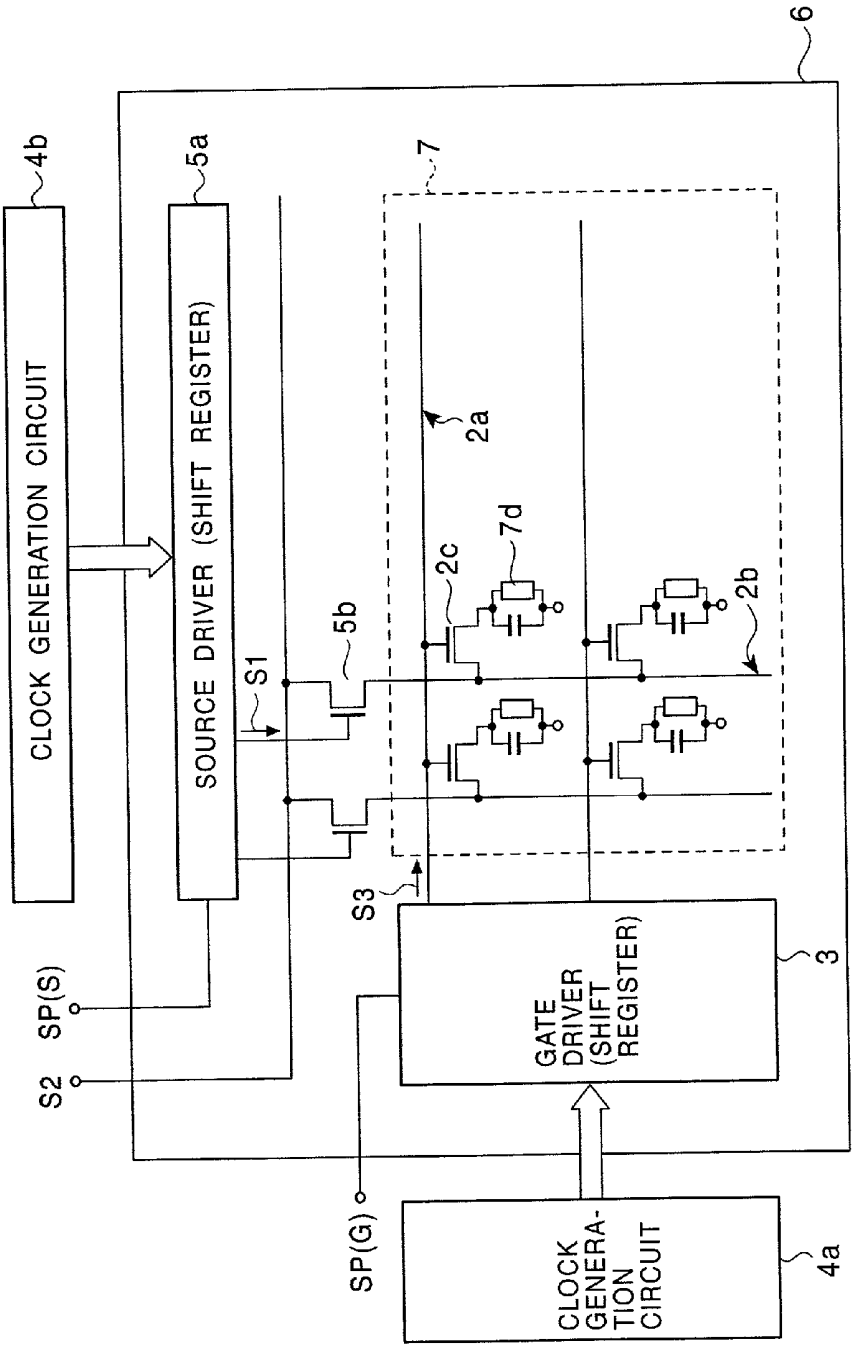

6
4b
5a
7
CLOCK GENERATION CIRCUIT
SOURCE DRIVER (SHIFT REGISTER)
2a
7d
2c
2b
5b
S1
S3
SP(S)
S2
GATE DRIVER (SHIFT REGISTER)
3
SP(G)
CLOCK GENERA-TION CIRCUIT
4a

FIG. 14
PRIOR ART

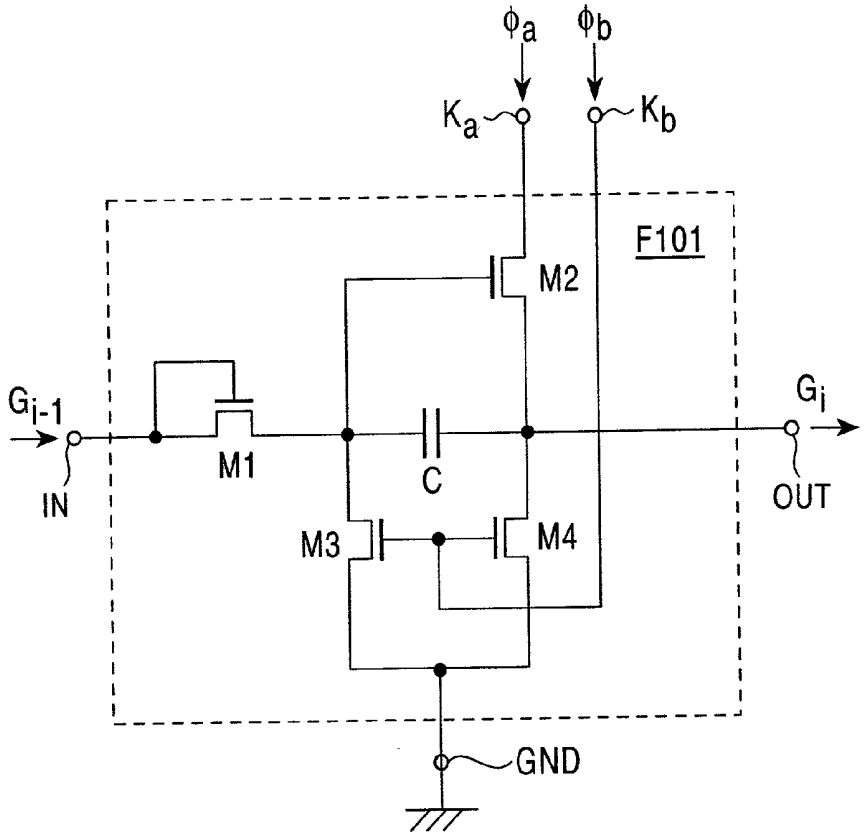
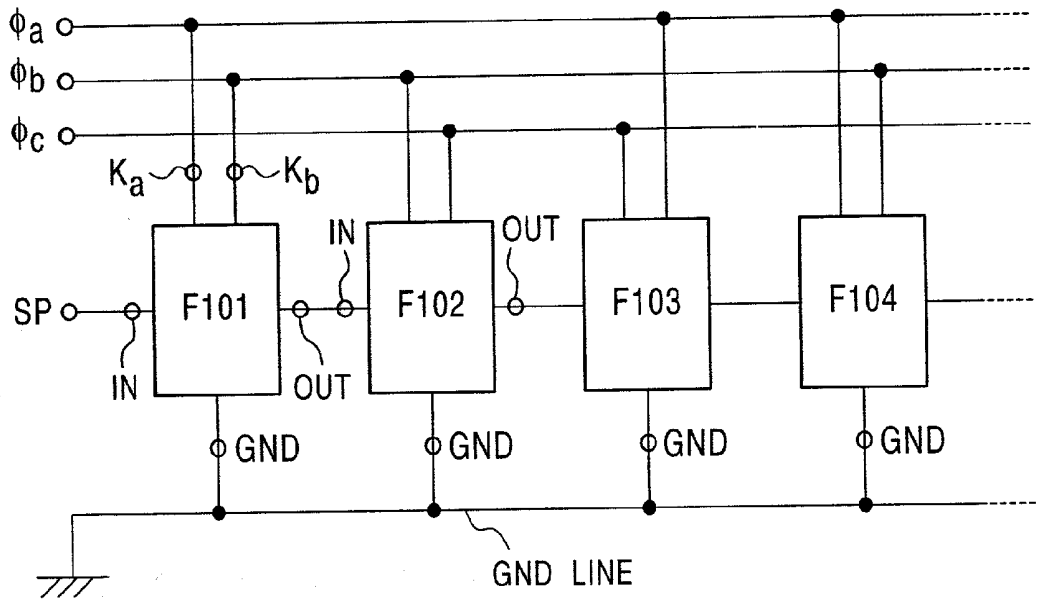


FIG. 15
PRIOR ART



SHIFT REGISTER HAVING FEWER LINES THEREIN, AND LIQUID CRYSTAL DISPLAY HAVING THE SAME

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a shift register and a device, such as a display or an image sensor, using the same.

[0003] 2. Description of the Related Art

[0004] **FIG. 14** is a circuit diagram which illustrates the internal circuitry of a stage F**101** incorporated in a conventional exemplary shift register. The stage F**101** includes an input terminal IN at which a signal G_{i-1} output from a previous stage is input, an output terminal OUT at which a signal G_i is output to a subsequent stage, clock input terminals K_a and K_b at which clock signals ϕ_a and ϕ_b are input, respectively, and a ground terminal GND connected to a ground potential.

[0005] **FIG. 15** is an overall view of the conventional exemplary shift register. The shift register is formed of a plurality of stages F**101**, F**102**, F**103**, and the like. The internal circuitry of the stages F**102**, F**103**, and the like is the same as that of the stage F**101** shown in **FIG. 14**. The stages F**101**, F**102**, F**103**, and the like are connected to each other in the cascade configuration. For example, the output terminal OUT of the stage F**101** is connected to the input terminal IN of the next stage F**102**. As above described, the stages F**102**, F**103**, and the like have the same circuitry as the stage F**101**, and the stages F**101**, F**102**, F**103**, and the like each have ground terminals GND which are connected to the ground potential via a ground line. As used herein, ground potential refers to the initial state level of the internal components of the stages F**101**, F**102**, F**103**, and the like. That is, in the initial state, a ground potential is output from the output terminal OUT of each of the stages F**101**, F**102**, F**103**, and the like.

[0006] However, the conventional shift register has the following problems; it requires a line, such as a ground line, which supplies the initial state level to each stage in the shift register, so that the number of lines in the shift register increases, leading to an increase in size of the area required for wiring.

SUMMARY OF THE INVENTION

[0007] Accordingly, it is an object of the present invention to provide a shift register having fewer lines to reduce the size of area required for wiring, and to provide a display using the shift register.

[0008] To this end, in one aspect of the present invention, a shift register has m stages which store one of two states, where m is an integer more than 1, each stage including clock input terminals at which n-phase clock signals are input, where n is an integer more than 1, and an input terminal, and an output terminal. The input terminal of one stage receives the signal delivered from an input terminal of the shift register or from the output terminal of the previous stage. The signal output at the output terminal of one stage is passed to the input terminal of the subsequent stage or to an output terminal of the shift register. Each stage receives an initial state level from one of the clock input terminals. The initial state level is used to initialize the state of each stage.

[0009] Since the initial state level is input from one of the clock input terminals, a line, such as a ground line, which supplies the initial state level is eliminated. Therefore, fewer lines are connected to the shift register, thereby reducing the size of area required for wiring.

[0010] Two- to four-phase clock signals would provide optimum number of clock signal lines, thereby reducing the size of area required for wiring.

[0011] Preferably, the stages in the shift register are divided into a plurality of groups, and the in-phase clock input terminals of the stages in each group are all connected to each other.

[0012] This allows the clock input terminals of the stages in each group to be integrated into one system, and each group is provided with a set of clock input terminals. Thus, the clock signal lines in the shift register may not extend across the shift register. Therefore, the length of the clock signal lines in the shift register may be reduced, thereby reducing a delay of the clock signals due to the line capacitance or the line resistance.

[0013] preferably, each stage further includes a storage unit for storing one of two states, and an initializing unit for initializing the state stored by the storage unit to the initial state level input from one of the clock input terminals.

[0014] The initializing unit (a transistor in an illustrated embodiment) may be used to initialize one of the two states, i.e., HIGH level or LOW level, which is stored in the storage unit (a capacitor in the illustrated embodiment) to the initial state level (the ground potential in the illustrated embodiment) which is input from one of the clock input terminals. Thus, a line, such as a ground line, which supplies the initial state level is not necessary in order to initialize the state of each stage in the shift register.

[0015] Preferably, the initializing unit is an MIS transistor, and MIS transistors contained in each stage, including that MIS transistor, are of the same channel type.

[0016] All of the MIS transistors are of the same channel type, thereby making the production process simplified. The MIS transistors of the same channel type would be achieved using multiphase clock signals.

[0017] Preferably, the MIS transistors are made of a material containing amorphous silicon or polycrystalline silicon.

[0018] When a voltage is applied in the same direction to a MIS transistor made of a material containing amorphous silicon or polycrystalline silicon, the reliability of the MIS transistor may be reduced in general. According to the present invention, however, the initial state level is input to the MIS transistor, or the initializing unit, from one of the clock input terminals having a time-varying potential, rather than a line having a potential which is always fixed at the initial state level. Thus, the direction of the voltage applied to the MIS transistor varies over time, and is not fixed to the same direction. Accordingly, the reliability of the MIS transistor is improved.

[0019] The outputs of the stages in the shift register may correspond to scan signals of an active matrix circuit having

switching elements formed at intersections between signal lines and scan lines. Preferably, MIS transistors contained in the active matrix circuit, and the MIS transistors contained in each of the stages in the shift register are of the same channel type, and are made of a material containing amorphous silicon or polycrystalline silicon.

[0020] Since the outputs of the stages in the shift register correspond to scan signals of the active matrix circuit, that is, a gate driver or a source driver of the active matrix circuit is formed of the shift register, fewer lines are required for the gate driver or the source driver. The size of area required for the lines in the gate driver or the source driver is therefore reduced.

[0021] Preferably, the shift register is formed together with the active matrix circuit on the same substrate.

[0022] Since the shift register and the active matrix circuit formed on the same substrate, the line extending between the shift register and the active matrix circuit can be shortened. The MIS transistors which are formed on the same substrate may be formed using the same production process, and the MIS transistors in the shift register and the active matrix circuit may be of the same channel type, and may be made of the same material.

[0023] In another aspect of the present invention, a display uses the shift register in accordance with the present invention as a gate driver and/or a source driver.

[0024] Fewer lines are required for a shift register used as a gate driver and/or a source driver, thereby reducing the size of area required for wiring. This results in a compact display having a smaller wiring area than a conventional display without any influence on display capabilities.

BRIEF DESCRIPTION OF THE DRAWINGS

[0025] **FIG. 1** is a circuit diagram which illustrates the internal circuitry of a stage F1 incorporated in a shift register according to a first embodiment of the present invention;

[0026] **FIG. 2** is a timing chart of the stage F1 shown in **FIG. 1**;

[0027] **FIG. 3** is an overall view of the shift register according to the first embodiment;

[0028] **FIG. 4** is a schematic view of a display in an embodiment which uses the shift register in accordance with the first embodiment as a gate driver;

[0029] **FIG. 5** is an overall view of a shift register according to a second embodiment of the present invention;

[0030] **FIG. 6** is a circuit diagram which illustrates the internal circuitry of a stage F'1 incorporated in a shift register according to a third embodiment of the present invention;

[0031] **FIG. 7** is a timing chart of the stage F'1 shown in **FIG. 6**;

[0032] **FIG. 8** is an overall view of the shift register according to the third embodiment;

[0033] **FIG. 9** is an overall view of a shift register according to a fourth embodiment of the present invention;

[0034] **FIG. 10** is a timing chart of a stage F"1 incorporated in the shift register according to the fourth embodiment;

[0035] **FIG. 11** is a comparative table which illustrates the effect of reducing a delay with respect to the clock signals in the display;

[0036] **FIG. 12** is a schematic view of a display in an embodiment of the present invention which uses the shift register in accordance with the present invention as a gate driver or a source driver;

[0037] **FIG. 13** is a schematic view of an image sensor which uses the shift register in accordance with the present invention as a gate driver or a source driver;

[0038] **FIG. 14** is a circuit diagram which illustrates the internal circuitry of a stage F101 incorporated in a conventional exemplary shift register; and

[0039] **FIG. 15** is an overall view of the conventional shift register.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0040] **FIG. 1** is a circuit diagram which illustrates the internal circuitry of a stage F1 incorporated in a shift register according to a first embodiment of the present invention. The stage F1 includes an input terminal IN at which a signal G_{i-1} output from a previous stage is input, an output terminal OUT at which a signal G_i is output to a subsequent stage, and three clock input terminals K_a, K_b, and K_c at which three-phase clock signals ϕ_a, ϕ_b, and ϕ_c are input, respectively.

[0041] The input terminal IN is connected to a first end (node A) of a capacitor C serving as a storage element via an MIS (metal-insulator-semiconductor) transistor M1 serving as a diode. A second end of the capacitor C is connected to the output terminal OUT. The clock input terminal K_a is connected to the drain of an MIS transistor M2, the clock input terminal K_b is connected to the gates of MIS transistors M3 and M4, and the clock input terminal K_c is connected to the sources of the MIS transistors M3 and M4. The first end (node A) of the capacitor C is connected to the gate of the MIS transistor M2 and the drain of the MIS transistor M3. The second terminal of the capacitor C, i.e., the output terminal OUT, is connected to the source of the MIS transistor M2 and the drain of the MIS transistor M4.

[0042] **FIG. 2** is a timing chart of the stage F1. The stage F1 retains the input signal G_{i-1} input from the input terminal IN in the capacitor C used as a storage element, and outputs the output signal G_i from the output terminal OUT.

[0043] In a period T0 of the timing chart, since the clock signal ϕ_b is at a high level (HIGH), the MIS transistors M3 and M4 are turned on. In turn, the first and second ends of the capacitor C are short-circuited, and the capacitor C would be discharged if it had been charged. Since the clock signal ϕ_c is at a low level (LOW) in the period T0, the MIS transistor M4 is turned on while the clock signal ϕ_c is LOW, so that the output signal G_i goes LOW. Since the MIS transistor M3 is also turned on, the potential V_A at the node A goes LOW, so that the MIS transistor M2 is turned off.

[0044] In the next period T1, the clock signal ϕ_b goes LOW, and the MIS transistors M3 and M4 are turned off.

The clock signal ϕ_c is HIGH in the period T1, but has no influence on the potential V_A and the output signal G_i because the MIS transistors M3 and M4 are turned off. In this state, the input signal G_{i-1} goes HIGH, and the potential V_A also goes HIGH. As the potential V_A goes HIGH, the MIS transistor M2 is turned on. Since the clock signal ϕ_a is LOW in the period T1, the output signal G_i is also LOW. The output signal G_i at the low level and the potential V_A at the high level allow the capacitor C between the output signal G_i and the potential V_A to be charged. Then, the potential V_A is fixed at the high level. This ensures that the MIS transistor M2 remains in the ON state.

[0045] In the next period T2, as the clock signal ϕ_a goes HIGH, the output signal G_i also goes HIGH because the MIS transistor M2 is still ON. This causes the potential V_A to be boosted (bootstrapped) to a potential that is substantially double the high level. Then, the ON state of the MIS transistor M2 is strengthened.

[0046] In the next period T3, the clock signal ϕ_b goes HIGH, and the MIS transistors M3 and M4 are turned on. Then, the first and second ends of the capacitor C are short-circuited, allowing the capacitor C that has been charged to be discharged. Since the clock signal ϕ_c is at the low level, the MIS transistor M4 is turned on while the clock signal ϕ_c is LOW, so that the output signal G_i goes LOW again. Since the MIS transistor M3 is also turned on, the potential V_A goes LOW, so that the MIS transistor M2 is turned off. Accordingly, without a ground line that is always kept at the low level (LOW) being connected to the stage F1, the signal G_i output from the output terminal OUT is allowed to go LOW again.

[0047] **FIG. 3** is an overall view of the shift register according to the first embodiment. The shift register is formed of a plurality of stages F1, F2, F3, and the like. The internal circuitry of the stages F2, F3, and the like is the same as that of the stage F1 shown in **FIG. 1**. The stages F1, F2, F3, and the like are connected to each other in the cascade configuration. For example, the output terminal OUT of the stage F1 is connected to the input terminal IN of the next stage F2.

[0048] A group is formed of six successive stages of the stages F1, F2, F3, and the like. For example, a group G1 is formed of the stages F1 to F6. The in-phase clock input terminals of the stages in one group are all connected to each other, and are then connected to three clock input terminals, respectively, a set of which is provided for that group. Specifically, the clock input terminals K_a, K_b, and K_c of each of the stages F1 to F6 in the group G1 are connected to clock signal lines L_a, L_b, and L_c, respectively, and the clock signal lines L_a, L_b, and L_c are connected to clock input terminals T_a, T_b, and T_c, respectively, a set of which is provided for the group G1. It is noted that the clock signal lines L_a, L_b, and L_c are not connected to clock signal lines of another group. Therefore, clock signal lines of one group do not extend across the shift register.

[0049] Specifically, the clock signal lines of a group (for example, the clock signal lines L_a, L_b, and L_c of the group G1) are formed on a TFT (thin film transistor) substrate (glass substrate), and provide great line resistance. On the other hand, the lines extending to a set of clock input terminals of a group (for example, the set of clock input terminals T_a, T_b, and T_c of the group G1) are mounted on a TCP (tape carrier package), and may be made of a lower resistance material. This makes it possible to reduce a delay of the clock signals due to the line resistance.

[0050] **FIG. 4** is a schematic view of a display in one embodiment which uses the shift register in accordance with the first embodiment as a gate driver. The display includes a TFT substrate (glass substrate) **1**, a display area **2** formed on the TFT substrate **1**, and a gate driver (shift register) **3** positioned on a side of the display area **2** for driving scan lines **2***a* within the display area **2**. That is, the display area **2** and the gate driver (shift register) **3** are formed on the same TFT substrate (glass substrate) **1** by the same production process. Therefore, MIS transistors **2***c* formed at intersections between the scan lines **2***a* and signals lines **2***b* within the display area **2**, and the MIS transistors in the gate driver (shift register) **3** are of the same channel type (for example, n-channel transistors). The MIS transistors are made of the same material, and the MIS transistors formed on the glass substrate are preferably made of a material containing amorphous silicon or polycrystalline silicon.

[0051] If a voltage is always applied in the same direction across the gate and source of an MIS transistor which is made of a material containing amorphous silicon or polycrystalline silicon, the reliability of the MIS transistor may be reduced.

[0052] In the conventional shift register, the clock signal ϕ_b having a high level potential or a ground potential is input to the gates of the MIS transistors M3 and M4, and the ground line that is always kept at the ground potential is connected to the sources thereof. This enables the potential of the gates to be always equal to or higher than the potential of the sources, so that a constant direction of the gate-source voltage can always be maintained.

[0053] On the other hand, in the first embodiment, the clock signal ϕ_b having a high level potential or a ground potential is input to the gates of the MIS transistors M3 and M4, and the clock signal ϕ_c having a high level potential or a ground potential is input to the sources thereof. Since the clock signals ϕ_b and ϕ_c have different phases, the direction of the gate-source voltage varies over time and does not always remain in the same direction. The reliability of the MIS transistors M3 and M4 is thus improved.

[0054] The clock signals ϕ_a, ϕ_b, and ϕ_c are supplied from a clock generation circuit **4***a* formed on a TCP **4** to the gate driver (shift register) **3**. Source drivers **5** drive the signal lines **2***b* within the display area **2**. The shift register according to the first embodiment may be implemented as a source driver of the display.

[0055] For example, if the display is a 6-inch VGA panel, the gate driver (shift register) **3** which drives the scan lines **2***a* has 480 stages. According to the first embodiment, since the stages of the shift register are divided into groups each consisting of six stages, 480 stages are divided into 80 groups each consisting of six stages. Thus, the length of the clock signal lines in each group is reduced to 1/80 length of clock signal lines when the stages are not divided into groups. The line capacitance and the line resistance of the clock signal lines in each group are also reduced to 1/80. Then, the delay of the clock signals, which is determined by substantially multiplying the line capacitance by the line resistance, is reduced to 1/6400.

[0056] **FIG. 5** is an overall view of a shift register according to a second embodiment of the present invention. The internal circuitry of stages F1, F2, F3, and the like in the shift register is the same as in the first embodiment. In the second embodiment, the stages F1, F2, F3, and the like in the shift register are not divided into blocks, and the clock signals ϕ_a, ϕ_b, and ϕ_c are supplied to each stage via clock signal lines P_a, P_b, and P_c of a single system. If it is possible that the clock signal lines P_a, P_b, and P_c are made of a material having sufficiently small line capacitance or line resistance, the structure of the second embodiment would be achieved. This structure requires fewer terminals (clock input terminals) connected to external components, thereby making the production process simplified, while improving the reliability.

[0057] **FIG. 6** is a circuit diagram which illustrates the internal circuitry of a stage F'1 incorporated in a shift register according to a third embodiment of the present invention. In **FIG. 6**, the same reference numerals are assigned to the same components of the stage F1 shown in **FIG. 1**, and the description thereof is omitted. The stage F'1 in the third embodiment has a terminal K_g at which a signal G_{i+1} output from the next stage is input. The terminal K_g is connected to the gates of the MIS transistors M3 and M4. The stage F'1 uses only one clock input terminal K as the clock input terminal. One clock signal ϕ_a of the two-phase clock signals ϕ_a and ϕ_b is input to the clock input terminal K. The clock input terminal K is connected to the drain of the MIS transistor M2, and is further connected to the sources of the MIS transistors M3 and M4.

[0058] **FIG. 7** is a timing chart of the stage F'1 shown in **FIG. 6**. The stage F'1 receives one of the two-phase clock signals ϕ_a and ϕ_b, i.e., the clock signal ϕ_a, and the signal G_{i+1} output from the next stage, and works similarly to the stage F1 according to the first embodiment.

[0059] **FIG. 8** is an overall view of the shift register according to the third embodiment. The shift register is formed of a plurality of stages F'1, F'2, F'3, and the like, and the two-phase clock signals ϕ_a and ϕ_b are alternately input to the stages F'1, F'2, F'3, and the like in turn. For example, the clock signal ϕ_a is input to the stage F'1, and the clock signal ϕ_b is input to the stage F'2. A signal output from the next stage is input to the terminal K_g of each of the stages F'1, F'2, F'3, and the like. For example, a signal G_2 output from the next stage F'2 is input to the terminal K_g of the stage F'1. This structure only requires the two-phase clock signals ϕ_a and ϕ_b to drive the shift register, thereby further reducing the number of lines in the shift register, while simplifying the clock generation circuit.

[0060] **FIG. 9** is an overall view of a shift register according to a fourth embodiment of the present invention. Three out of four-phase clock signals ϕ_a, ϕ_b, ϕ_c, and ϕ_d are supplied to each stage in the shift register. For example, the clock signals ϕ_b, ϕ_c, and ϕ_d are supplied to a stage F"1.

[0061] **FIG. 10** is a timing chart of the stage F"1 shown in **FIG. 9**. The stage F"1 receives three of the four-phase clock signals ϕ_a, ϕ_b, ϕ_c, and ϕ_d, i.e., the clock signals ϕ_b, ϕ_c, and ϕ_d, and works similarly to the stage F1 according to the first embodiment.

[0062] **FIG. 11** is a comparative table which illustrates the effect of reducing a delay with respect to the clock signals in the display. It is assumed that the display is a 6-inch VGA panel, and a gate driver (shift register) for driving scan lines has 480 stages with the overall length of approximately 91 mm. It is further assumed that the line material has a sheet resistance of 1 Ω per square, the parasitic capacitance (per unit width) of the gates of the TFTs is $2\times10^{(-11)}$ F/cm, and the MIS transistors M1, M2, and M4 each have a TFT dimension (W/L) of (600 μm/3 μm), and the MIS transistor M3 has a TFT dimension (W/L) of (1500 μm/3 μm). In the first, second, and third embodiments of the present invention, in comparison with the conventional shift register, the number of lines decreases, and the line capacitance C and the line resistance R are reduced.

[0063] In **FIG. 11**, the line capacitance C and the line resistance R in the first and third embodiments represent values in each group consisting of six stages. With respect to the line width in the first and third embodiments, the minimum line width is typically 3 to 10 μm due to the process limitation.

[0064] **FIG. 12** is a schematic view of a display in an embodiment of the present invention which uses the shift register in accordance with one of the illustrated embodiments as a gate driver or a source driver. In the display, a clock signal output by a clock generation circuit **4***a* is supplied to a gate driver **3** formed on a TFT substrate (display substrate) **1**, and the gate driver **3** drives scan lines **2***a* within a display area **2**. A clock signal output by a clock generation circuit **4***b* is supplied to a source driver **5***a* formed on the TFT substrate (display substrate) **1** to apply scan signals S1 output by the source driver **5***a* to the gates of transistors **5***b*. The transistors **5***b* turn on or off the supplying of a source signal S2 to signal lines **2***b* within the display area in response to the scan signals S1.

[0065] The shift register according to the present invention may be implemented as the gate driver **3** which supplies scan signals S3 to the scan lines **2***a*, and may also be implemented as the source driver **5***a* which applies the scan signals S1 to the gates of the transistors **5***b*.

[0066] **FIG. 13** is a schematic view of an image sensor using the shift register in accordance with the present invention as a gate driver or a source driver. The image sensor includes photo detectors **7***d* in a sensor area **7** formed on a TFT substrate (image sensor substrate) **6** in place of display elements **2***d* in the display area **2** on the TFT substrate (display substrate) **1** shown in **FIG. 12**. The structure of other components is the same as that in the display shown in **FIG. 12**.

[0067] While the present invention has been described through illustration of its preferred forms, it is to be understood that the described embodiments are only illustrative and various changes and modifications may be imparted thereto without departing from the scope of the present invention which is limited solely by the appended claims.

What is claimed is:

1. A shift register having m stages which store any one of two states, where m is an integer more than 1, each stage comprising, as terminals:

clock input terminals at which n-phase clock signals are input, where n is an integer more than 1;

an input terminal at which a signal delivered from an input terminal of the shift register or from an output terminal of the previous stage is input; and

an output terminal at which a signal is output to the input terminal of the subsequent stage or to an output terminal of the shift register,

wherein said each stage receives an initial state level from any one of said clock input terminals, the initial state level being used to initialize the state of said each stage.

2. A shift register according to claim 1,

wherein the stages of the shift register are divided into a plurality of groups, and the in-phase clock input terminals of the stages in each group are all connected to each other.

3. A shift register according to claim 1, said each stage comprising:

storage means for storing any one of two states; and

initializing means for initializing the state stored by said storage means to the initial state level input from any one of said clock input terminals.

4. A shift register according to claim 2, said each stage comprising:

storage means for storing any one of two states; and

initializing means for initializing the state stored by said storage means to the initial state level input from any one of said clock input terminals.

5. A shift register according to claim 4, wherein said initializing means comprises an MIS transistor, and MIS transistors contained in said each stage, including said MIS transistor, are MIS transistors of the same channel type.

6. A shift register according to claim 3, wherein said initializing means comprises an MIS transistor, and MIS transistors contained in said each stage, including said MIS transistor, are MIS transistors of the same channel type.

7. A shift register according to claim 5, wherein the MIS transistors are made of a material containing amorphous silicon or polycrystalline silicon.

8. A shift register according to claim 6, wherein the MIS transistors are made of a material containing amorphous silicon or polycrystalline silicon.

9. A shift register according to claim 5, wherein the outputs of the stages in the shift register correspond to scan signals of an active matrix circuit having switching elements formed at intersections between signal lines and scan lines, and

MIS transistors contained in the active matrix circuit, and the MIS transistors contained in said each stage constituting the shift register are MIS transistors of the same channel type, and are made of a material containing amorphous silicon or polycrystalline silicon.

10. A shift register according to claim 6, wherein the outputs of the stages in the shift register correspond to scan signals of an active matrix circuit having switching elements formed at intersections between signal lines and scan lines, and

MIS transistors contained in the active matrix circuit, and the MIS transistors contained in said each stage constituting the shift register are MIS transistors of the same channel type, and are made of a material containing amorphous silicon or polycrystalline silicon.

11. A shift register according to claim 7, wherein the outputs of the stages in the shift register correspond to scan signals of an active matrix circuit having switching elements formed at intersections between signal lines and scan lines, and

MIS transistors contained in the active matrix circuit, and the MIS transistors contained in said each stage constituting the shift register are MIS transistors of the same channel type, and are made of a material containing amorphous silicon or polycrystalline silicon.

12. A shift register according to claim 8, wherein the outputs of the stages in the shift register correspond to scan signals of an active matrix circuit having switching elements formed at intersections between signal lines and scan lines, and

MIS transistors contained in the active matrix circuit, and the MIS transistors contained in said each stage constituting the shift register are MIS transistors of the same channel type, and are made of a material containing amorphous silicon or polycrystalline silicon.

13. A shift register according to claim 9, wherein the shift register is formed together with the active matrix circuit on the same substrate.

14. A shift register according to claim 10, wherein the shift register is formed together with the active matrix circuit on the same substrate.

15. A shift register according to claim 11, wherein the shift register is formed together with the active matrix circuit on the same substrate.

16. A shift register according to claim 12, wherein the shift register is formed together with the active matrix circuit on the same substrate.

17. A display using a shift register according to claim 1 as a gate driver.

18. A display using a shift register according to claim 1 as a source driver.

* * * * *

专利名称(译)	移位寄存器中具有较少的线，并且具有相同的液晶显示器		
公开(公告)号	US20020097829A1	公开(公告)日	2002-07-25
申请号	US10/038181	申请日	2001-10-23
[标]申请(专利权)人(译)	阿尔卑斯电气株式会社		
申请(专利权)人(译)	阿尔普电子有限公司		
当前申请(专利权)人(译)	ONANOVICH集团股份公司，有限责任公司		
[标]发明人	KAWAHATA KEN		
发明人	KAWAHATA, KEN		
IPC分类号	G02F1/133 G09G3/20 G09G3/36 G11C19/00 G11C19/18 G11C19/28 H01L27/146 H04N5/335 H04N5/369 H04N5/66		
CPC分类号	G11C19/18		
优先权	2000323612 2000-10-24 JP		
其他公开文献	US6621886		
外部链接	Espacenet USPTO		

摘要(译)

移位寄存器具有m级，其存储两种状态中的一种，其中m是大于1的整数，每级包括输入n相时钟信号的时钟输入端子，其中n是大于1的整数，以及输入终端和输出终端。一级的输入端接收从移位寄存器的输入端或前一级的输出端传送的信号。在一级输出端输出的信号传递到后级的输入端或移位寄存器的输出端。每个级从一个时钟输入端接收初始状态级。初始状态级别用于初始化每个阶段的状态。