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(54) **COMMON VOLTAGE GENERATION CIRCUIT AND LIQUID CRYSTAL DISPLAY COMPRISING THE SAME**

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(57) **ABSTRACT**

A common voltage generation circuit includes a common voltage adjusting circuit adjusting a level of a common voltage in response to a compensation signal and providing the adjusted common voltage to a liquid crystal panel, and a common voltage compensating circuit including a resistor producing potential differences between the adjusted common voltage and each of the positive and negative polarity data voltages, a first voltage detector detecting a potential difference between the adjusted common voltage and the negative polarity data voltage, a second voltage detector detecting a potential difference between the adjusted common voltage and the positive polarity data voltage, and a voltage comparator comparing output signals of the first and second voltage detectors and feeding the compensation signal back to the common voltage adjusting circuit.

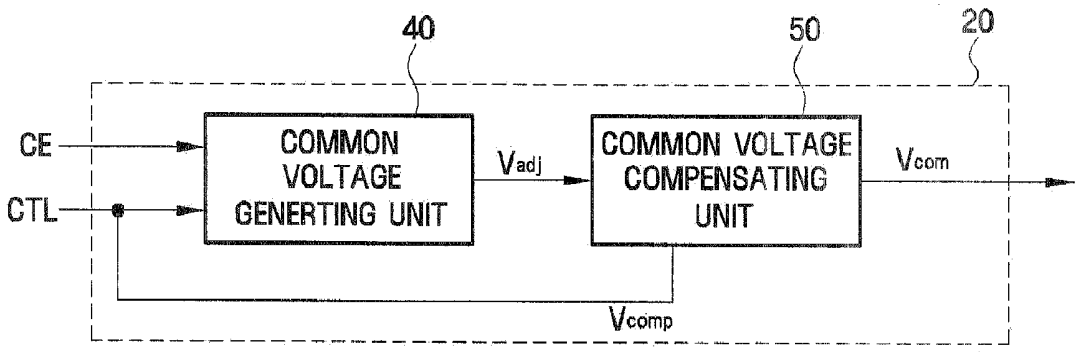


FIG. 1

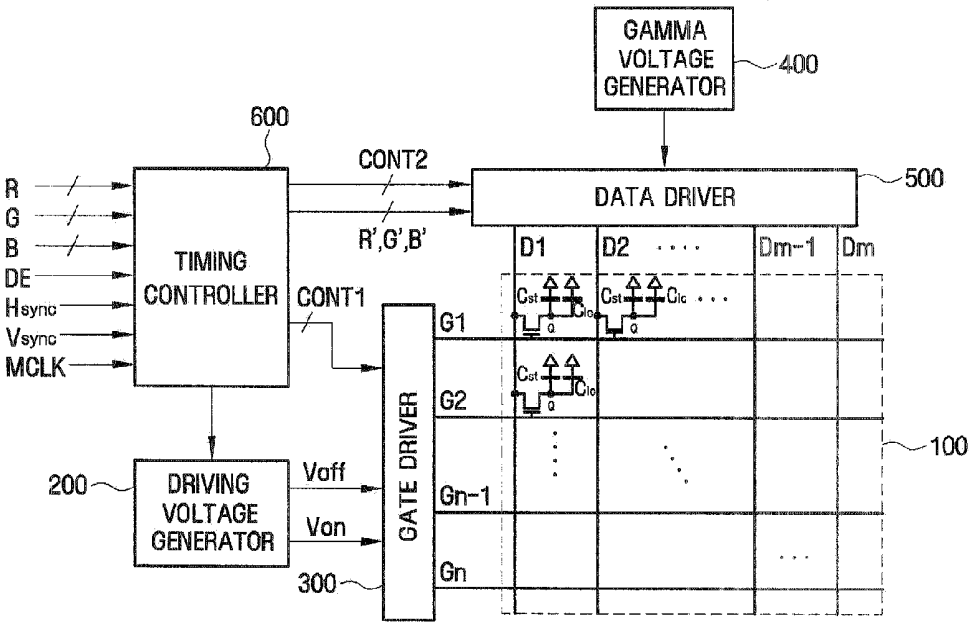

GAMMA VOLTAGE GENERATOR
400
600
CONT2
R
G
B
DE
Hsync
Vsync
MCLK
TIMING CONTROLLER
R',G',B'
DATA DRIVER
500
D1
D2
Dm-1
Dm
CONT1
G1
G2
Gn-1
Gn
GATE DRIVER
100
200
DRIVING VOLTAGE GENERATOR
Voff
Von
300

FIG. 2

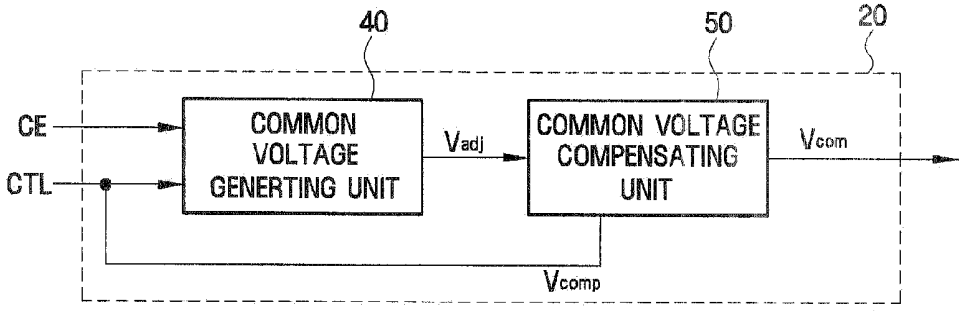

40
50
20
CE
CTL
COMMON VOLTAGE GENERTING UNIT
Vadj
COMMON VOLTAGE COMPENSATING UNIT
Vcom
Vcomp

FIG. 3

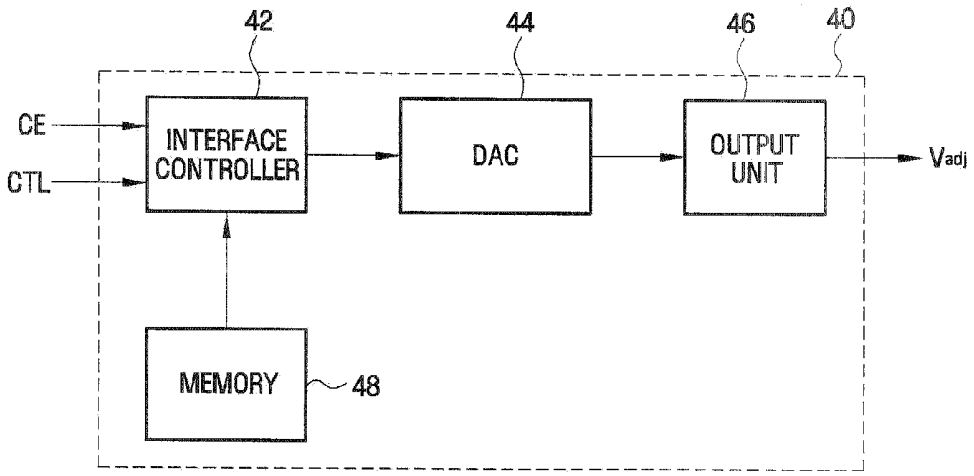

42
44
46
40
CE
CTL
INTERFACE CONTROLLER
DAC
OUTPUT UNIT
Vadj
MEMORY
48

FIG. 4

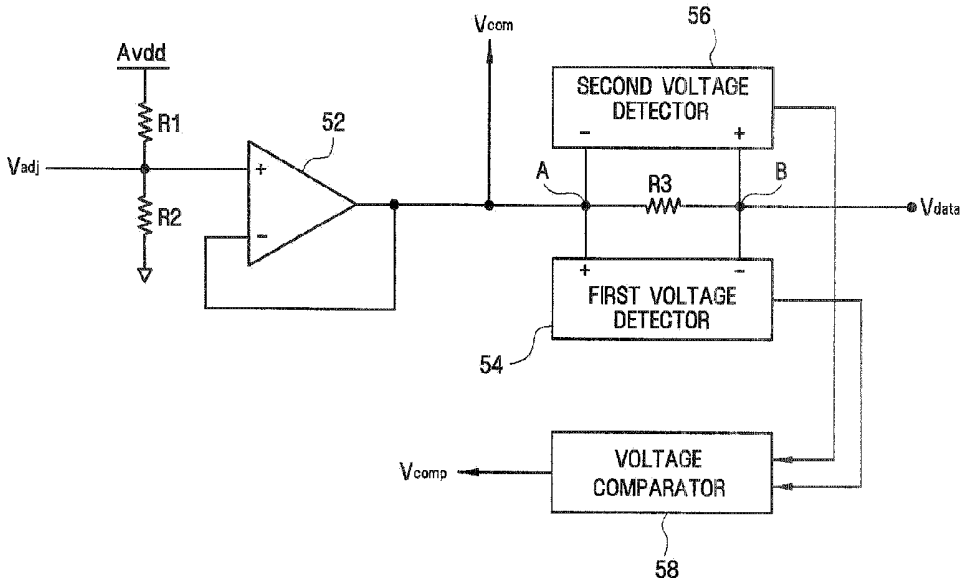

Vcom
56
Avdd
R1
52
Vadj
R2
SECOND VOLTAGE DETECTOR
A
R3
B
Vdata
FIRST VOLTAGE DETECTOR
54
Vcomp
VOLTAGE COMPARATOR
58

FIG. 5

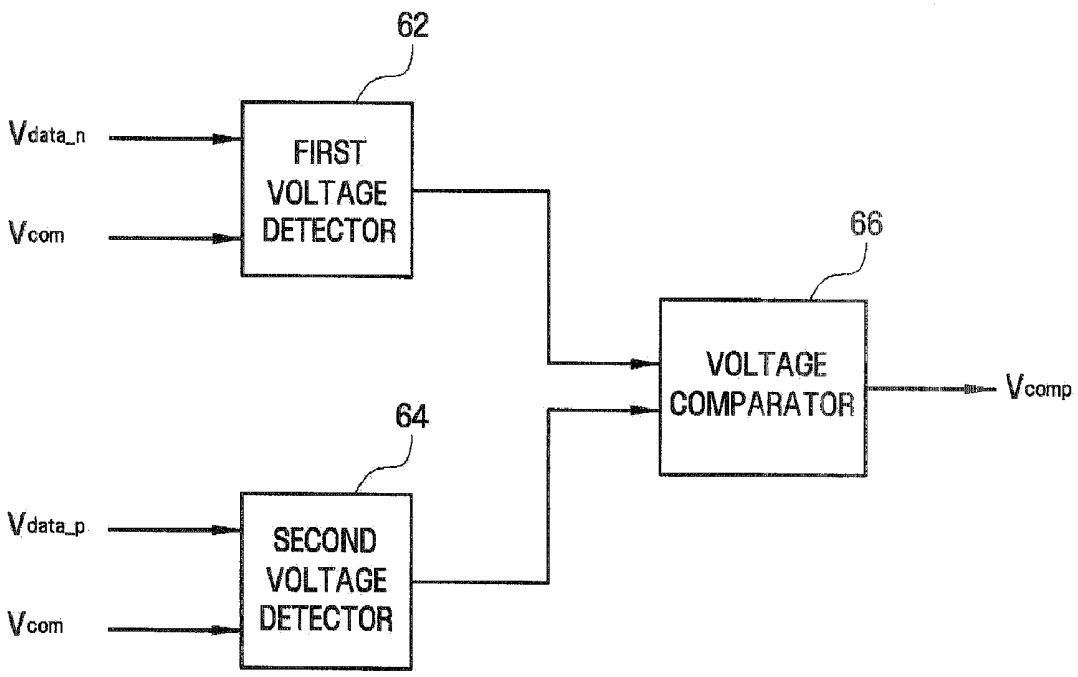

62
Vdata_n
Vcom
FIRST VOLTAGE DETECTOR
66
VOLTAGE COMPARATOR
Vcomp
64
Vdata_p
Vcom
SECOND VOLTAGE DETECTOR

FIG. 6

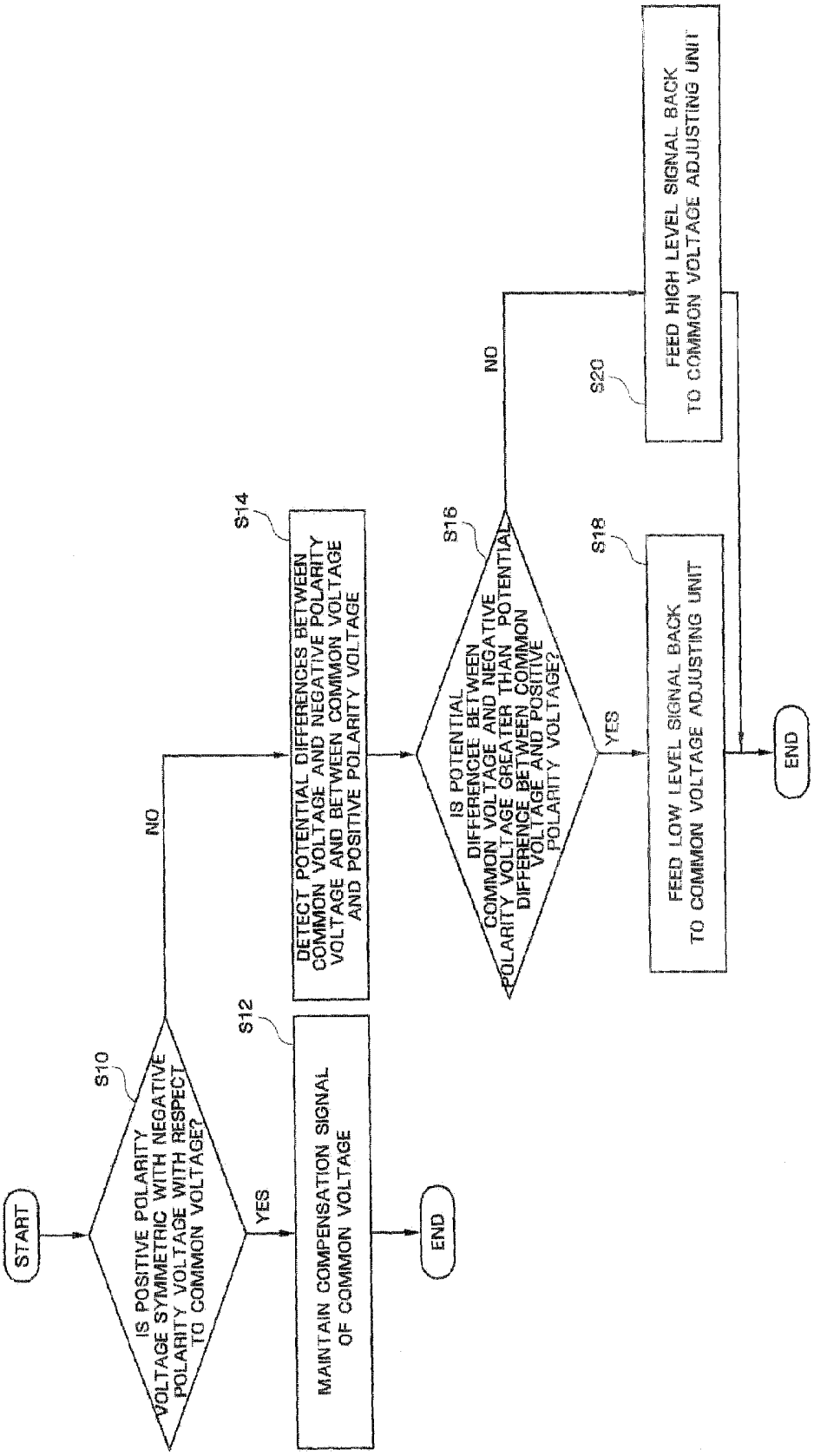

START
S10
IS POSITIVE POLARITY VOLTAGE SYMMETRIC WITH NEGATIVE POLARITY VOLTAGE WITH RESPECT TO COMMON VOLTAGE?
YES
NO
S12
MAINTAIN COMPENSATION SIGNAL OF COMMON VOLTAGE
END
S14
DETECT POTENTIAL DIFFERENCES BETWEEN COMMON VOLTAGE AND NEGATIVE POLARITY VOLTAGE AND BETWEEN COMMON VOLTAGE AND POSITIVE POLARITY VOLTAGE
S16
IS POTENTIAL DIFFERENCE BETWEEN COMMON VOLTAGE AND NEGATIVE POLARITY VOLTAGE GREATER THAN POTENTIAL DIFFERENCE BETWEEN COMMON VOLTAGE AND POSITIVE POLARITY VOLTAGE?
YES
NO
S18
FEED LOW LEVEL SIGNAL BACK TO COMMON VOLTAGE ADJUSTING UNIT
S20
FEED HIGH LEVEL SIGNAL BACK TO COMMON VOLTAGE ADJUSTING UNIT
END

FIG. 7

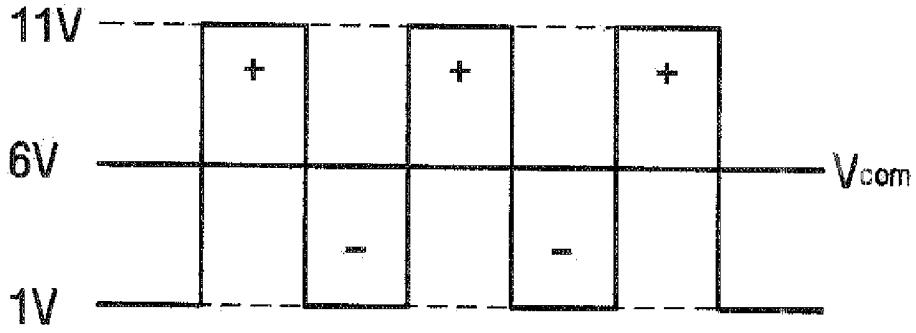


FIG. 8

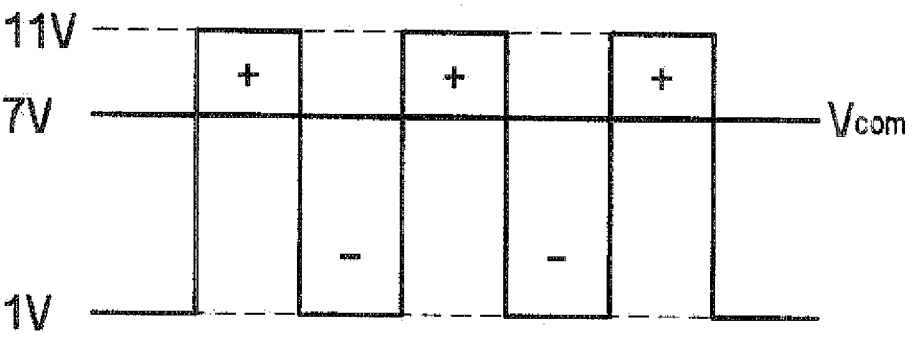


FIG. 9

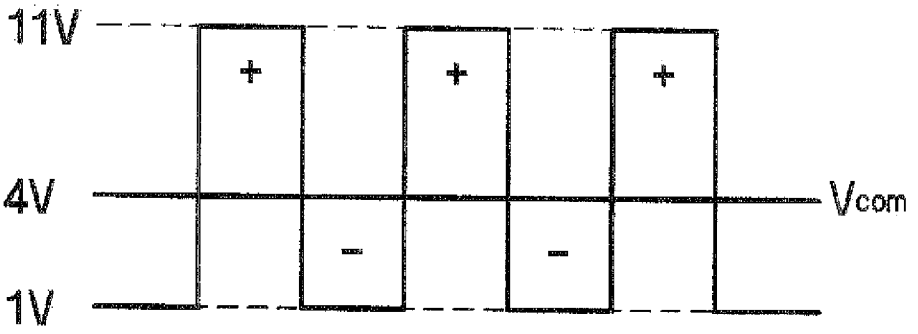
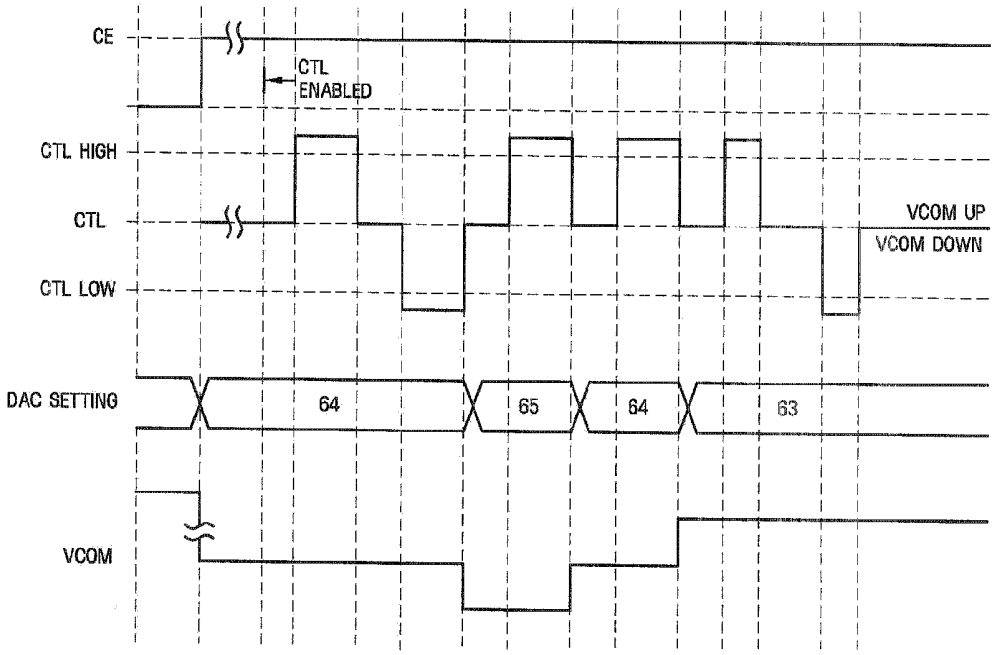


FIG. 10


CE
CTL ENABLED
CTL HIGH
CTL
CTL LOW
VCOM UP
VCOM DOWN
DAC SETTING
64
65
64
63
VCOM

COMMON VOLTAGE GENERATION CIRCUIT AND LIQUID CRYSTAL DISPLAY COMPRISING THE SAME

CROSS-REFERENCE TO RELATED PATENT APPLICATION

[0001] This application claims priority to Korean Patent Application No. 10-2006-0005928, filed on Jan. 19, 2006, the disclosure of which is herein incorporated by reference in its entirety

BACKGROUND OF THE INVENTION

[0002] 1. Technical Field

[0003] The present disclosure relates to a common voltage generation circuit and a liquid crystal display circuit comprising the same.

[0004] 2. Discussion of Related Art

[0005] A liquid crystal display (LCD) is a type of flat panel display for displaying images using liquid crystals. In general, LCDs feature low power consumption, slim, lightweight design, with low driving voltage.

[0006] A conventional LCD includes a color fitter display panel having reference electrodes and color filters, a thin film transistor (TFT) substrate having TFTs and pixel electrodes, and a liquid crystal layer sandwiched between the color filter display substrate and the TFT substrate. An LCD displays images by applying electric potentials to the pixel electrodes and the reference electrodes to generate an electric field in the liquid crystal layer to control the alignment of the liquid crystal molecules and the quantity of light transmitted is controlled.

[0007] In conventional LCDs, in order to reduce or prevent deterioration of a liquid crystal layer, polarity inversion of a liquid crystal voltage is periodically performed within each frame, which is called a frame inversion driving method. The liquid crystal voltage is determined by a data voltage applied to a data driver and a common voltage corresponding to the data voltage.

[0008] In recent years, several attempts have been made to improve the display quality of LCD devices. In polarity inversion, a positive-polarity voltage and a negative-polarity voltage: for a gray scale, are applied alternately to each pixel. Polarity inversion, however, necessitates different common voltages for the respective liquid crystal panels, due to various reasons, such as parasitic capacitance generated during fabrication of a thin film transistor, characteristics of the thin film transistor, voltage uniformity in common voltage generating electrodes, or a structural difference between each of the circuit components.

[0009] A flicker phenomenon occurs due to a data voltage distortion, that is, the positive-polarity data voltage and the negative-polarity data voltage being asymmetric with respect to the common voltage. To minimize the occurrence of the flicker phenomenon a common voltage generation circuit may employ a digital variable resistor to enable an inspector to adjust a flickering level directly at an inspection stage. The time for adjusting the flickering level may vary depending on the inspector's skill. In addition, since the flickering level is observed with the naked eyes, quantitative control of the flickering level is less than satisfactory. Further, measurement errors may be introduced due to an inspector's physical fatigue or other ambient conditions.

SUMMARY OF THE INVENTION

[0010] According to an exemplary embodiment of the present invention, there is provided a common voltage generation circuit including a common voltage adjusting circuit adjusting a level of a common voltage in response to a compensation signal and providing the adjusted common voltage to a liquid crystal panel, and a common voltage compensating circuit including a resistor producing potential differences between the adjusted common voltage and each of the positive and negative polarity data voltages, a first voltage detector detecting a potential difference between the adjusted common voltage and the negative polarity data voltage, a second voltage detector detecting a potential difference between the adjusted common voltage and the positive polarity data voltage, and a voltage comparator comparing output signals of the first and second voltage detectors and feeding the compensation signal back to the common voltage adjusting circuit.

[0011] According to an exemplary embodiment of the present invention, there is provided a liquid crystal display comprising a liquid crystal panel including a plurality of unit pixels defined at an intersecting area of each of a plurality of gate lines and each of a plurality of data lines, a timing controller generating control signals for controlling the liquid crystal panel, a driving voltage generator receiving the control signals and generating a plurality of driving voltages, wherein the driving voltage generator includes a common voltage adjusting circuit adjusting a level of a common voltage in response to a compensation signal and providing the adjusted common voltage to a liquid crystal panel and a resistor producing potential differences between the adjusted common voltage and each of the positive and negative polarity data voltages, a first voltage detector detecting a potential difference between the adjusted common voltage and the negative polarity data voltage, a second voltage detector detecting a potential difference between the adjusted common voltage and the positive polarity data voltage, and a voltage comparator comparing output signals of the first and second voltage detectors and feeding the compensation signal back to the adjusted common voltage adjusting circuit, a gate driver receiving the driving voltage and applying the driving voltage to the plurality of the gate lines; and a data driver applying the data voltage to the plurality of the data lines.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The present invention will become readily apparent to those of ordinary skill in the art when descriptions of exemplary embodiments thereof are read with reference to the accompanying drawings.

[0013] FIG. **1** is a block diagram of a liquid crystal display according to an exemplary embodiment of the present invention.

[0014] FIG. **2** is a block diagram of a common voltage generator according to an exemplary embodiment of the present invention.

[0015] FIG. **3** is an internal block diagram of a common voltage adjusting unit according to an exemplary embodiment of the present invention.

[0016] FIG. **4** is an internal block diagram of a common voltage compensating unit according to an exemplary embodiment of the present invention.

[0017] FIG. **5** is an internal block diagram of a common voltage compensating unit according to an exemplary embodiment of the present invention.

[0018] FIG. **6** is a flow chart showing operations of the common voltage adjusting unit according to an exemplary embodiment of the present invention;

[0019] FIGS. **7** through **9** are waveform diagrams of data voltages according to an exemplary embodiment of the present invention.

[0020] FIG. **10** is a timing diagram of the common voltage adjusting unit according to an exemplary embodiment of the present invention.

DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0021] Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. Like reference numerals refer to similar or identical elements throughout the description of the figures.

[0022] Hereinafter, a liquid crystal display (LCD) according to an exemplary embodiment of the present invention will be described with reference to FIG. **1**.

[0023] FIG. **1** is a block diagram of a LCD according to an exemplary embodiment of the present invention. Referring to FIG. **1**, the LCD includes a liquid crystal panel **100**, a driving voltage generator **200**, a gate driver **300**, a gamma voltage generator **400**, a data driver **500**, and a timing controller **600**.

[0024] As shown in FIG. **1**, the liquid crystal panel **100** includes a plurality of unit pixels which are electrically connected to a plurality of display signal lines G**1**-Gn and D**1**-Dm and arranged substantially in the form of a matrix. The display signal lines G**1**-Gn and D**1**-Dm include a plurality of gate lines G**1**-Gn transmitting gate signals and a plurality of data lines D**1**-Dm transmitting data signals. The gate lines G**1**-Gn extend substantially in a row direction in FIG. **1** and are substantially parallel to each other, while the data lines D**1**-Dm extend substantially in a column direction and are substantially parallel to each other.

[0025] Each of the plurality of pixels comprises a switching element Q, which is electrically connected to a corresponding one of the plurality of display signal lines G**1**-Gn and D**1**-Dm, and a liquid crystal capacitor C_{lc}. Each of the plurality of pixels may include a storage capacitor C_{st} which is electrically connected to the switching element Q. If desired, the storage capacitor C_{st} may not be formed.

[0026] The switching element Q is provided on a thin film transistor (TFT) substrate. The switching element Q includes a control terminal which is electrically connected to one of the gate lines G**1**-Gn, an input terminal which is electrically connected to one of the data lines D**1**-Dm, and an output terminal which is electrically connected to both the liquid crystal capacitor C_{lc} and the storage capacitor C_{st}.

[0027] The liquid crystal capacitor C_{lc} includes a pixel electrode provided on the TFT substrate and a common electrode provided on a color filter substrate. A liquid crystal layer disposed between the two electrodes functions as the dielectric of the liquid crystal capacitor C_{lc}. The pixel electrode is electrically connected to the switching element Q. The common electrode, which is electrically connected to the common voltage V_{com}, may be formed on the entire surface of the color filter substrate. The common electrode may be provided on the TFT substrate, and both electrodes may be bar or stripe shaped.

[0028] The storage capacitor C_{st} may be defined by the overlap of the pixel electrode and a separate wire (not shown) provided on the TFT substrate and applied with a predetermined voltage such as the common voltage V_{com} (separate wire type). The storage capacitor C_{st} may be defined by the overlap of the pixel electrode and its previous gate line via an insulator (previous gate type).

[0029] For color display each pixel can represent a color by providing one of a plurality of red (R), green (G) and blue (B) color filters in an area corresponding to the pixel electrode. The color filter may be provided in the corresponding area of the color filter substrate. The color filters may be provided on or under the pixel electrode on the TFT substrate.

[0030] A polarizer or polarizers (not shown) may be attached to either or both of the TFT substrate and the color filter substrate of the liquid crystal panel **100**.

[0031] The driving voltage generator **200** generates a plurality of driving voltages. For example, the driving voltage generator **200** generates a gate-on voltage Von, a gate-off voltage Voff, and a common voltage V_{com}. The driving voltage generator **200** may further comprise a common voltage generator **20** including a common voltage adjusting unit **40** and a common voltage compensating unit **50**. The common voltage adjusting unit **40** adjusts a voltage level of the common voltage V_{com} in response to a compensation signal. The common voltage compensating unit **50** compares the positive polarity voltage with the negative polarity voltage to determine whether the positive polarity voltage and the negative polarity voltage are symmetric with respect to the common voltage V_{com}, and feeds a comparison result back to the common voltage adjusting unit **40**. This will be described in more detail later in this disclosure with reference to FIG. **2**.

[0032] The gate driver **300**, which is electrically connected to the gate lines G**1**-Gn of the liquid crystal panel **100**, applies gate signals from an external device to the gate lines G**1**-Gn, each gate signal being a combination of a gate-on voltage Von and a gate-off voltage Voff.

[0033] The gamma voltage generator **400** generates two sets of a plurality of gray-scale voltages related to the transmittance of the pixels. The data voltages in one set have a positive polarity with respect to the common voltage V_{com}, while those in the other set have a negative polarity with respect to the common voltage V_{com}. The positive-polarity data voltages and negative-polarity data voltages are alternately supplied to the liquid crystal panel **100** during inversion driving.

[0034] The data driver **500**, which is electrically connected to the data lines D**1**-Dm of the liquid crystal panel **100**, selects the gray-scale voltages from the gamma voltage generator **400** for application as data signals to the data lines D**1**-Dm. The data driver **500** may include a plurality of integrated circuits (ICs).

[0035] The timing controller **600** generates control signals for controlling the gate driver **300**, the data driver **500**, and other components, and supplies the generated control signals to the corresponding elements.

[0036] Hereinafter, operations of the LCD will be described in detail.

[0037] The timing controller **600** receives RGB image signals R, G and B and input control signals controlling the display thereof, such as for example, a vertical synchronization signal V_{sync}, a horizontal synchronization signal H_{sync}, a main clock CLK and a data enable signal DE, from an external graphic controller (not shown). The timing controller **600** generates a plurality of gate control signals CONT**1**, and a plurality of data control signals CONT**2**, and processes the image signals R, G and B for the liquid crystal panel **100** on the basis of the input control signals. The timing controller **600** provides the gate control signals CONT**1** for the gate driver **400**, the data control signals CONT**2** and the processed image signals R', G' and B' for the data driver **500**.

[0038] The gate control signals CONT**1** include a vertical synchronization start signal STV for informing of start of a frame, a gate clock signal CPV for controlling the output time of the gate-on voltage Von and an output enable signal OE for defining the widths of the gate-on voltage Von.

[0039] The data control signals CONT**2** include a horizontal synchronization start signal STH for informing of start of a horizontal period, a load signal LOAD for instructing to apply the appropriate data voltages to the data lines D**1**-Dm, an inversion control signal RVS for reversing the polarity of the data voltages with respect to the common voltage V_{com}, and a data clock signal HCLK.

[0040] The data driver **500** receives a packet of the image data R', G' and B' for a pixel row from the timing controller **600** in response to the data control signal CONT**2** received from the timing controller **600** and converts the image data R', G' and B' into data voltages selected from the gray-scale voltages.

[0041] Responsive to the gate control signals CONT**1** from the timing controller **600**, the gate driver **300** applies the gate-on voltage Von to the gate line G**1**-Gn, thereby turning on the switching elements Q connected thereto.

[0042] The data driver **500** applies the data voltages to the corresponding data lines D**1**-Dm during a turn-on time of the switching elements Q due to the application of the gate-on voltage Von to the gate lines G**1**-Gn that are electrically connected to the switching elements Q, which is called "one horizontal period" or "1H" and is equal to one period of the horizontal synchronization signal H_{sync}, the data enable signal DE, and the data clock signal CPV. Then, the data voltages are supplied to the corresponding pixels via the turned-on switching elements Q.

[0043] The liquid crystal molecules in the liquid crystal capacitor C_{lc} have orientations depending on the variation of the electric field that is generated by the pixel electrode and the common electrode, and the molecular orientations determine the polarization of light passing through the liquid crystal layer. A polarizer or polarizers (not shown) may be attached to either or both of the TFT substrate and the color fitter substrate.

[0044] By repeating this procedure, all of the gate lines G**1**-Gn are sequentially supplied with the gate-on voltage Von during a frame, thereby applying the data voltages to all pixels. When the next frame starts after finishing one frame, the inversion control signal RVS applied to the data driver **500** may be controlled such that the polarity of the data voltages is reversed, which is called "frame inversion". The inversion control signal RVS may be controlled such that the polarity of the data voltages flowing in a data line in one frame is reversed, which is called "line inversion", or such that the polarity of the data voltages in one packet is reversed, which is called "dot inversion".

[0045] FIG. **2** is a block diagram of a common voltage generator **20** according to an embodiment of the invention. Referring to FIG. **2**, the common voltage generator **20** includes a common voltage adjusting unit **40** and a common voltage compensating unit **50**.

[0046] At an initial operating stage, the common voltage adjusting unit **40** receives a control enable signal CE and a control signal CTL from an external device and is initialized for operation. Once the operation of the common voltage adjusting unit **40** is initialized, the common voltage adjusting unit **40** adjusts the common voltage V_{com} in response to a compensation signal V_{comp}, which is output from the common voltage compensating unit **50**, and provides the adjusted result, that is, the common voltage Vcom of the common voltage compensating unit **50**, to the liquid crystal panel **100**.

[0047] The common voltage compensating unit **50** receives the common voltage adjusted signal V_{adj} which is output from the common voltage adjusting unit **40**, compares the positive polarity voltage with the negative polarity voltage to determine whether the positive polarity voltage and the negative polarity voltage are symmetric with respect to the output signal V_{adj}, and feeds a comparison result back to the common voltage adjusting unit **40**. In an exemplary embodiment of the present invention, the output signal V_{adj} of the common voltage adjusting unit **40** is the same as the common voltage V_{com}.

[0048] FIG. **3** is an internal block diagram of a common voltage adjusting unit **40** according to an exemplary embodiment of the present invention. Referring to FIG. **3**, the common voltage adjusting unit **40** includes an interface controller **42**, a digital-to-analog converter (DAC) **44**, an output unit **46**, and a memory **48**.

[0049] At an initial operating stage, the interface controller **42** receives a control enable signal CE and a control signal CTL from an external device, reads intermediate data stored in the memory **48** according to the control signal CTL, and delivers the read data to the DAC **44**. Once the operation of the interface controller **42** is initialized, the interface controller **42** delivers the intermediate data stored in the memory **48** to the DAC **44** according to the compensation signal V_{comp} which is output from the common voltage compensating unit **50**. In addition, the interface controller **42** may modify the intermediate data stored in the memory **48** according to the control signal CTL.

[0050] The control enable signal CE enables the common voltage adjusting unit **40** and is connected to an operating voltage V_{DD}(not shown). At this time, to disable the common voltage adjusting unit **40**, the control enable signal CE is connected to a ground terminal. At an initial operating stage, the control signal CTL is applied from the timing controller **600**. The control signal CTL and the compensation signal V_{comp} are pulse signals having a logic high level and a logic low level.

[0051] At an initial operating stage, the DAC **44** outputs an analog voltage value corresponding to the intermediate data read in the memory **48** according to the control signal CTL. Once the operation of the DAC **44** is initialized, the DAC **44** outputs analog voltage values according to the

compensation signal V_{comp}, which is output from the common voltage compensating unit **50**.

[0052] The output unit **46** amplifies the analog voltage values and outputs the amplified voltage values, that is, the adjusted output signal V_{adj}.

[0053] The memory **48** stores the intermediate data of bit data, for example, "1000000" as intermediate data of 7-bit data, at an initial stage. The memory **48** is a programmable memory. In an exemplary embodiment of the present invention, the memory **48** is an Electrically Erasable Programmable Read Only Memory (EEPROM).

[0054] FIG. **4** is an internal block diagram of a common voltage compensating unit **50** according to an exemplary embodiment of the present invention. Referring to FIG. **4**, the common voltage compensating unit **50** includes an amplifier **52**, first and second voltage detectors **54** and **56**, and a voltage comparator **58**.

[0055] The amplifier **52** comprises an operating amplifier OP**1** including resistors R**1** and R**2** connected to the non-inverting terminal (+). The non-inverting terminal (+) of the operating amplifier OP**1** is supplied with a driving voltage A_{vdd} and a dropped voltage of the adjusted output signal V_{adj} which is output from the common voltage adjusting unit **40**. The inverting terminal (−) of the operating amplifier OP**1** is connected to the output terminal of the amplifier **52**, and the output signal of the amplifier **52** is fed back to the operating amplifier OP**1** through the inverting terminal (−) thereof. Here, the amplifier **52** amplifies the output signal of the common voltage adjusting unit **40**, that is, the adjusted output signal V_{adj}, which is the same as the common voltage V_{com} applied to the liquid crystal panel **100**.

[0056] When the positive polarity data voltage and the negative polarity data voltage are symmetric with respect to the common voltage, no potential difference is created between opposite ends A and B of a resistor R**3**. On the other hand, when the positive polarity data voltage and the negative polarity data voltage are not symmetric with respect to the common voltage, a potential difference is created between the opposite ends A and B of the resistor R**3**. Here, the first and second voltage detectors **54** and **56** detect the potential difference created between the opposite ends A and B of the resistor R**3**.

[0057] The first voltage detector **54** detects and outputs a difference between the common voltage V_{com} of the adjusted level output from the common voltage adjusting unit **40** and the negative polarity data voltage which is output from the data driver **500**. One end of the resistor R**3** is connected to the output terminal of the amplifier **52** and the other end thereof is connected to the output terminal V_{data} of the data driver **500**.

[0058] The second voltage detector **56** detects and outputs a difference between the common voltage V_{com} of the adjusted level output from the common voltage adjusting unit **40** and the positive polarity data voltage which is output from the data driver **500**.

[0059] Here, in order to determine an order of detecting by the first and second voltage detectors **54** and **56**, a switch (not shown) may be disposed between the first and second voltage detectors **54** and **56**.

[0060] The voltage comparator **58** compares output signals of the first and second voltage detectors **54** and **56**, and feeds a comparison result that is, a compensation signal V_{comp}, back to the common voltage adjusting unit **40**. If the output compensation signal V_{comp} is at a logic high level, the logic high level signal is fed back as the control signal CTL of the common voltage adjusting unit **40**, so that the common voltage adjusting unit **40** pulls-up the level of the common voltage V_{com} according to the compensation signal V_{comp}. Conversely, if the output compensation signal V_{comp} is at a logic low level, the logic low level signal is fed back as the control signal CTL of the common voltage adjusting unit **40**, so that the common voltage adjusting unit **40** pulls-down the level of the common voltage V_{com} according to the compensation signal V_{comp}.

[0061] As described above, in an exemplary embodiment of the present invention, the common voltage V_{com}, the positive polarity data voltage, and the negative polarity data voltage are compared with one another, and a compensation signal is output as the comparison result, which is fed back to the common voltage adjusting unit **40**, thereby automatically optimizing the common voltage V_{com} such that the positive polarity data voltage and the negative polarity data voltage are symmetric with respect to the common voltage V_{com}. In an exemplary embodiment of the present invention since the common voltage V_{com} is automatically optimized, a flicker phenomenon that occurs due to asymmetry of the positive polarity data voltage and the negative polarity data voltage with respect to the common voltage V_{com} can be automatically adjusted.

[0062] FIG. **5** is an internal block diagram of a common voltage compensating unit **50** according to an exemplary embodiment of the present invention. Referring to FIG. **5**, the common voltage compensating unit **50** includes first and second voltage detectors **62** and **64** and a voltage comparator **66**.

[0063] The first voltage detector **62** detects and outputs a difference between the common voltage V_{com} of the adjusted level output from the common voltage adjusting unit **40** and the negative polarity data voltage V_{data_n} that is output from the data driver **500**.

[0064] The second voltage detector **64** detects and outputs a difference between the common voltage V_{com} of the adjusted level output from the common voltage adjusting unit **40** and the positive polarity data voltage V_{data_p} that is output from the data driver **500**.

[0065] The voltage comparator **66** compares output signals of the first and second voltage detectors **62** and **64** and feeds a comparison result, that is, a compensation signal V_{comp}, back to the common voltage adjusting unit **40**.

[0066] FIG. **6** is a flow chart showing operations of the common voltage adjusting unit **40** according to an exemplary embodiment of the present invention. FIGS. **7** through **9** are waveform diagrams of data voltages according to an exemplary embodiment of the present invention.

[0067] As shown in FIG. **6**, in operation S**10**, the positive polarity voltage is compared with the negative polarity voltage to determine whether data voltages that are output from the data driver **500** are symmetric with respect to the common voltage V_{com} of the adjusted level output from the common voltage adjusting unit **40**. If a comparison result shows that the positive polarity voltage and the negative polarity voltage are symmetric with each other with respect to the common voltage V_{com} as shown in FIG. **7** the compensation signal V_{comp}, which is output from the common voltage compensating unit **50**, is maintained in operation S**12**.

[0068] However, when the positive polarity voltage and the negative polarity voltage are not symmetric with each

other with respect to the common voltage V_{com} as shown in FIGS. **8** and **9**, a potential difference is created between opposite ends A and B of the resistor R**3** shown in FIG. **4**. In operation S**14**, a difference between the common voltage V_{com} and the negative polarity data voltage is detected by the first voltage detector **54**, and white a difference between the common voltage V_{com} and the positive polarity data voltage is detected by the second voltage detector **56**.

[0069] In operation S**16**, output signals of the first and second voltage detectors **54** and **56** are compared with each other to determine whether the output signal of the first voltage detector **54** is greater than that of the second voltage detector **56**. If the comparison result of operation S**16** shows that the output signal of the first voltage detector **54** is greater than that of the second voltage detector **56**, as shown in FIG. **8**, the voltage comparator **58** outputs the compensation signal V_{comp} of a logic tow level, which is then fed back to the common voltage adjusting unit **40** to pull-down the voltage level of the common voltage V_{com} in operation S**18**. Meanwhile, if the output signal of the second voltage detector **56** is greater than that of the first voltage detector **54**, as shown in FIG. **9**, the voltage comparator **58** outputs the compensation signal V_{comp} of a logic high level, which is then fed back to the common voltage adjusting unit **40** to pull-up the voltage level of the common voltage V_{com} as shown in FIG. **71** in operation S**20**.

[0070] FIG. **10** is a timing diagram of the common voltage adjusting unit according to an exemplary embodiment of the present invention.

[0071] As shown in FIG. **10**, the common voltage adjusting unit **40** receives a control enable signal CE and a control signal CTL from an external device, the control signal CTL is enabled with a lapse of a predetermined delay time. The control signal CTL is a pulse signal having a logic high level and a logic low level. In an exemplary embodiment of the present invention, the operating voltage VDD has a range of about 2.6 V to about 3.6 V, and the control signal CTL has a logic high level and a logic low level on the basis of $V_{DD}/2$. For example, the logic high level of the control signal CTL may have a minimum value of V_{DD}*0.70 and a maximum value of V_{DD}*0.82, while the logic low level of the control signal CTL may have a minimum value of V_{DD}*0.20 and a maximum value of V_{DD}*0.32.

[0072] Upon receiving the control signal CTL, the interface controller **42** receives a control enable signal CE and a control signal CTL from an external device at an initial operating stage, reads intermediate data stored in the memory **48** according to the control signal CTL, and delivers the read data to the DAC **44**. Once the operation of the interface controller **42** is initialized, the interface controller **42** delivers the intermediate data stored in the memory **48** to the DAC **44** according to the compensation signal V_{comp} which is output from the common voltage compensating unit **50**.

[0073] The DAC **44** outputs an analog voltage value corresponding to the intermediate data read in the memory **48** according to the control signal CTL. The DAC **44** outputs analog voltage values according to the compensation signal V_{comp} which is output from the common voltage compensating unit **50**. As shown in FIG. **10**, DAC SETTING indicates intermediate data converted by the DAC **44**. Here, the intermediate data of bit data, for example, "1000000" as intermediate data of 7-bit data, is stored in the memory **48** at an initial stage. Accordingly, the first data value of the DAC SETTING is 64. Since the compensation signal V_{comp} which is output from the common voltage compensating unit **50** is a logic low level signal, the internal resistance of the DAC **44** increases, so that the second data value of the DAC SETTING is lowered. In addition, since the compensation signal V_{comp} which is output from the common voltage compensating unit **50** is a logic high level signal, the internal resistance of the DAC **44** decreases, so that the third data value of the DAC SETTING rises.

[0074] As described above, in the common voltage generation circuit according to an exemplary embodiment of the present invention, the common voltage, the positive polarity data voltage, and the negative polarity data voltage are compared with one another, and a compensation signal is output as the comparison result which is fed back to a common voltage adjusting unit, thereby automatically optimizing the common voltage such that the positive polarity data voltage and the negative polarity data voltage are symmetric with respect to the common voltage. In an exemplary embodiment of the present invention, since the common voltage is automatically optimized, a flicker phenomenon that occurs due to asymmetry of the positive polarity data voltage and the negative polarity data voltage with respect to the common voltage can be automatically adjusted.

[0075] Although exemplary embodiments of the present invention have been described in detail with reference to the accompanying drawings for the purpose of illustration, it is to be understood that the inventive processes and apparatus should not be construed as limited thereby. It will be readily apparent to those of ordinary skill in the art that various modifications to the foregoing exemplary embodiments may be made without departing from the scope of the invention as defined by the appended claims, with equivalents of the claims to be included therein.

What is claimed is:

1. A common voltage generation circuit comprising:

a common voltage adjusting circuit adjusting a level of a common voltage in response to a compensation signal and providing the adjusted common voltage to a liquid crystal panel; and

a common voltage compensating circuit including a resistor producing potential differences between the adjusted common voltage and each of positive and negative polarity data voltages, a first voltage detector detecting a potential difference between the adjusted common voltage and the negative polarity data voltage, a second voltage detector detecting a potential difference between the adjusted common voltage and the positive polarity data voltage, and a voltage comparator comparing output signals of the first and second voltage detectors and feeding the compensation signal back to the common voltage adjusting circuit.

2. The common voltage generation circuit of claim **1**, wherein feeding the compensation signal back to the common voltage adjusting circuit comprises comparing the positive polarity voltage with the negative polarity voltage to determine whether the positive polarity voltage and the negative polarity voltage are symmetric with respect to the adjusted common voltage.

3. The common voltage generation circuit of claim **1**, further comprising an amplifier amplifying and outputting the adjusted common voltage.

4. The common voltage generation circuit of claim 1, wherein when the compensation signal is at a logic low level, the level of the adjusted common voltage is pulled down.

5. The common voltage generation circuit of claim 1, wherein, when the compensation signal is at a logic high level, the level of the adjusted common voltage is pulled up.

6. A liquid crystal display comprising:

a liquid crystal panel including a plurality of unit pixels defined at an intersecting area of each of a plurality of gate lines and each of a plurality of data lines;

a timing controller generating control signals for controlling the liquid crystal panel;

a driving voltage generator receiving the control signals and generating a plurality of driving voltages,

wherein the driving voltage generator includes a common voltage adjusting circuit adjusting a level of a common voltage in response to a compensation signal and providing an adjusted common voltage to the liquid crystal panel and a resistor producing potential differences between the adjusted common voltage and each of the positive and negative polarity data voltages, a first voltage detector detecting a potential difference between the adjusted common voltage and the negative polarity data voltage, a second voltage detector detecting a potential difference between the adjusted common voltage and the positive polarity data voltage, and a voltage comparator comparing output signals of the first and second voltage detectors and feeding the compensation signal back to the common voltage adjusting circuit;

a gate driver receiving the driving voltage and applying the driving voltage to the plurality of the gate lines; and

a data driver applying the data voltage to the plurality of the data lines.

7. The liquid crystal display of claim 6, wherein feeding the compensation signal back to the common voltage adjusting circuit comprises comparing the positive polarity voltage with the negative polarity voltage to determine whether the positive polarity voltage and the negative polarity voltage are symmetric with respect to the adjusted common voltage.

8. The liquid crystal display of claim 6, further comprising an amplifier amplifying and outputting the adjusted common voltage.

9. The liquid crystal display of claim 6, wherein, when the compensation signal is at a logic low level, the level of the adjusted common voltage is pulled down.

10. The liquid crystal display of claim 6, wherein, when the compensation signal is at a logic high level, the level of the adjusted common voltage is pulled up.

* * * * *

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摘要(译)

公共电压产生电路包括：公共电压调节电路，响应于补偿信号调节公共电压的电平并将调节的公共电压提供给液晶面板;以及公共电压补偿电路，包括产生电位差的电阻器。调节的公共电压和每个正极性和负极性数据电压，第一电压检测器检测调节的公共电压和负极性数据电压之间的电位差，第二电压检测器检测调节的公共电压和正极性之间的电位差极性数据电压和电压比较器，比较第一和第二电压检测器的输出信号，并将补偿信号反馈到公共电压调节电路。