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(54) **LOW POWER DRIVING IN A LIQUID CRYSTAL DISPLAY**

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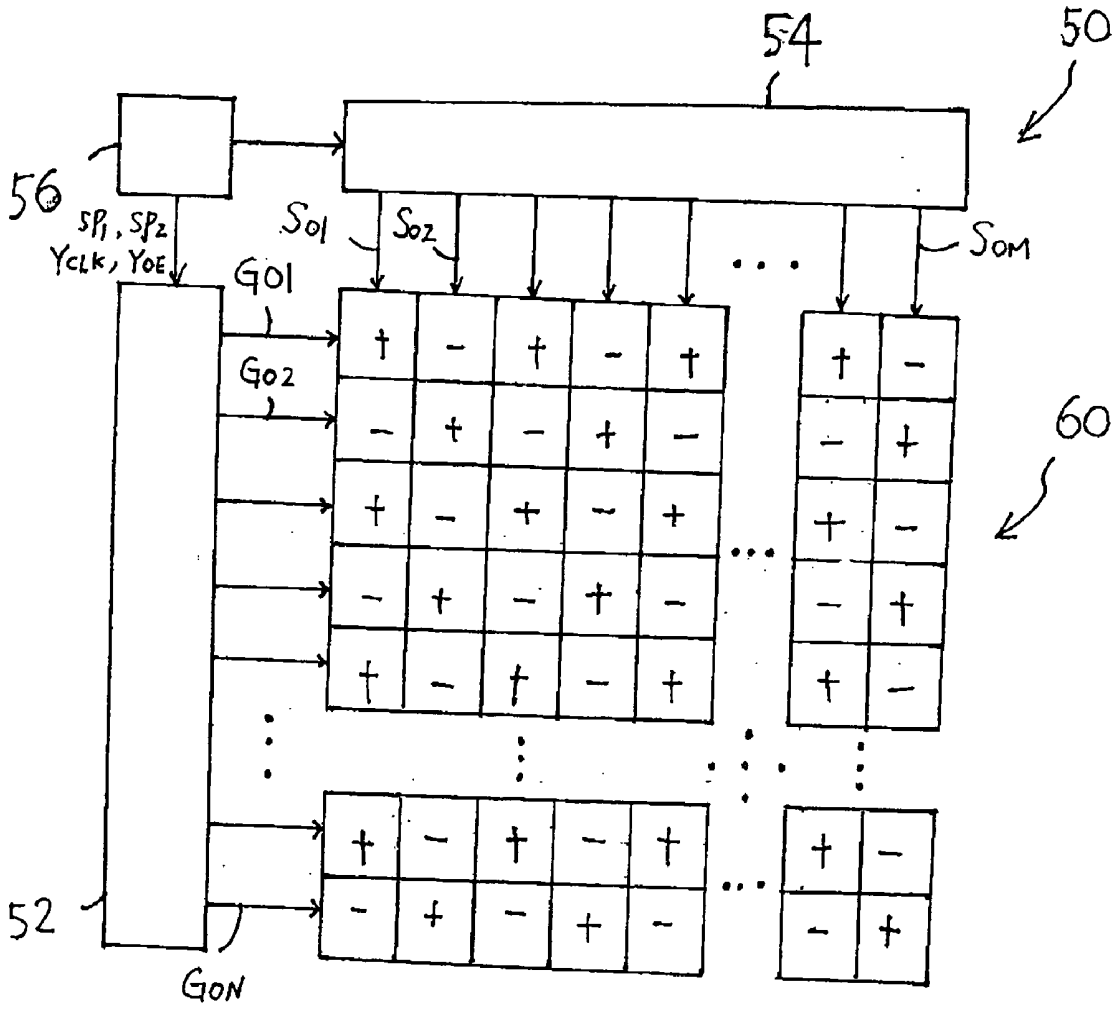
(57) **ABSTRACT**

A drive method for a liquid crystal display device that comprises providing an array of pixels formed in rows and columns, sequentially scanning odd-numbered rows of pixels during a first half of a frame period, and sequentially scanning even-numbered rows of pixels during a second half of the frame period.



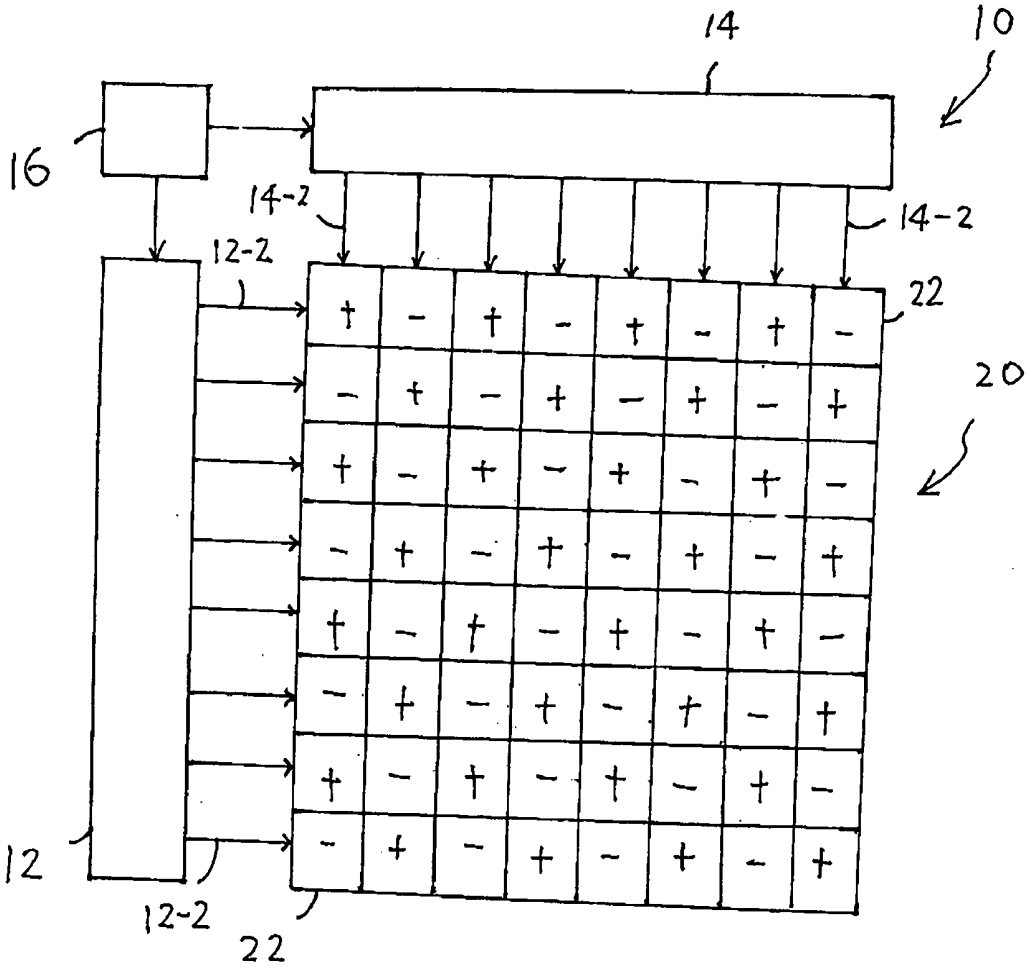


FIG. 1A (PRIOR ART)

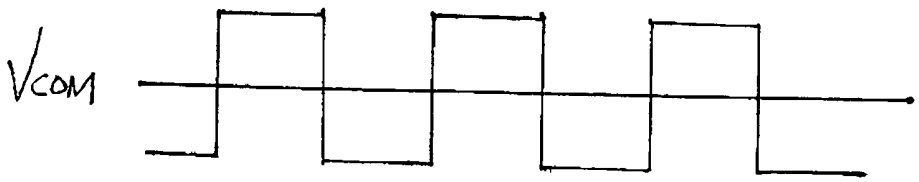


FIG. 1C (PRIOR ART)

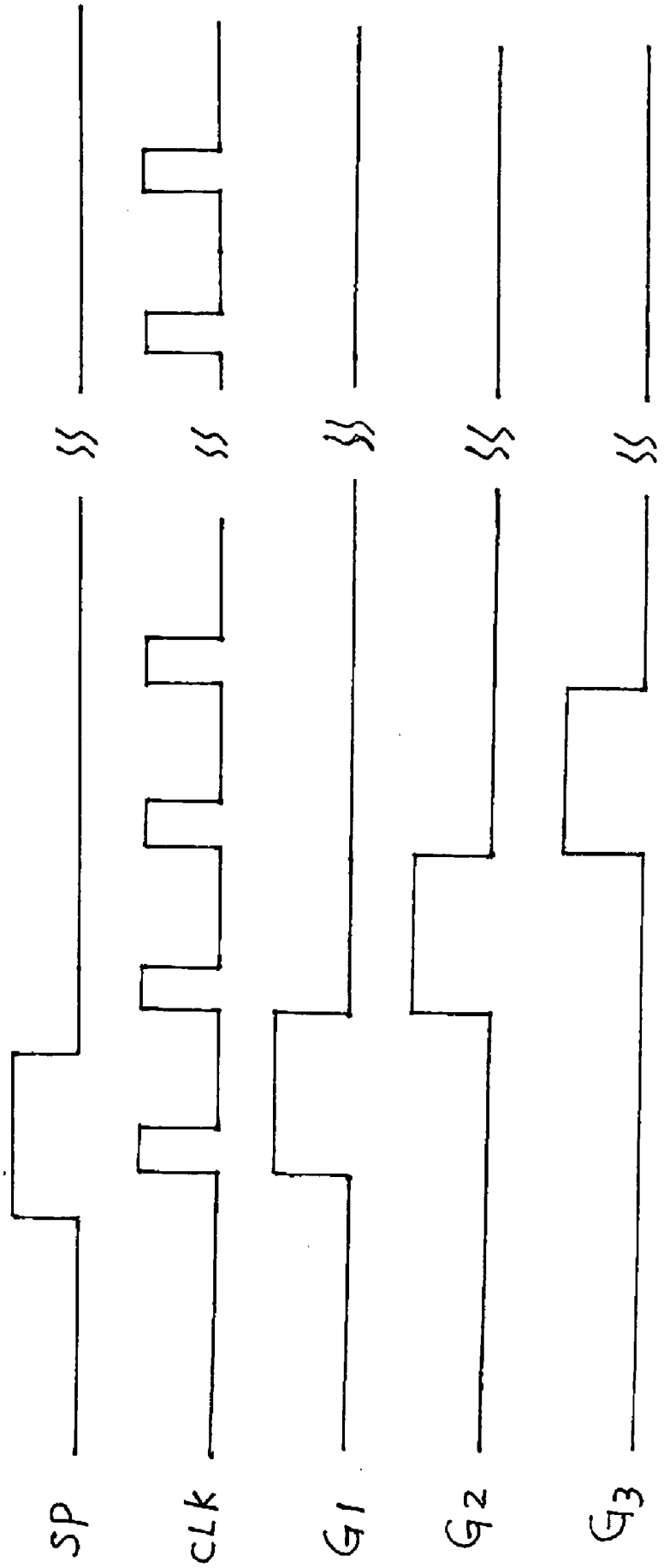


FIG. 1B (PRIOR ART)

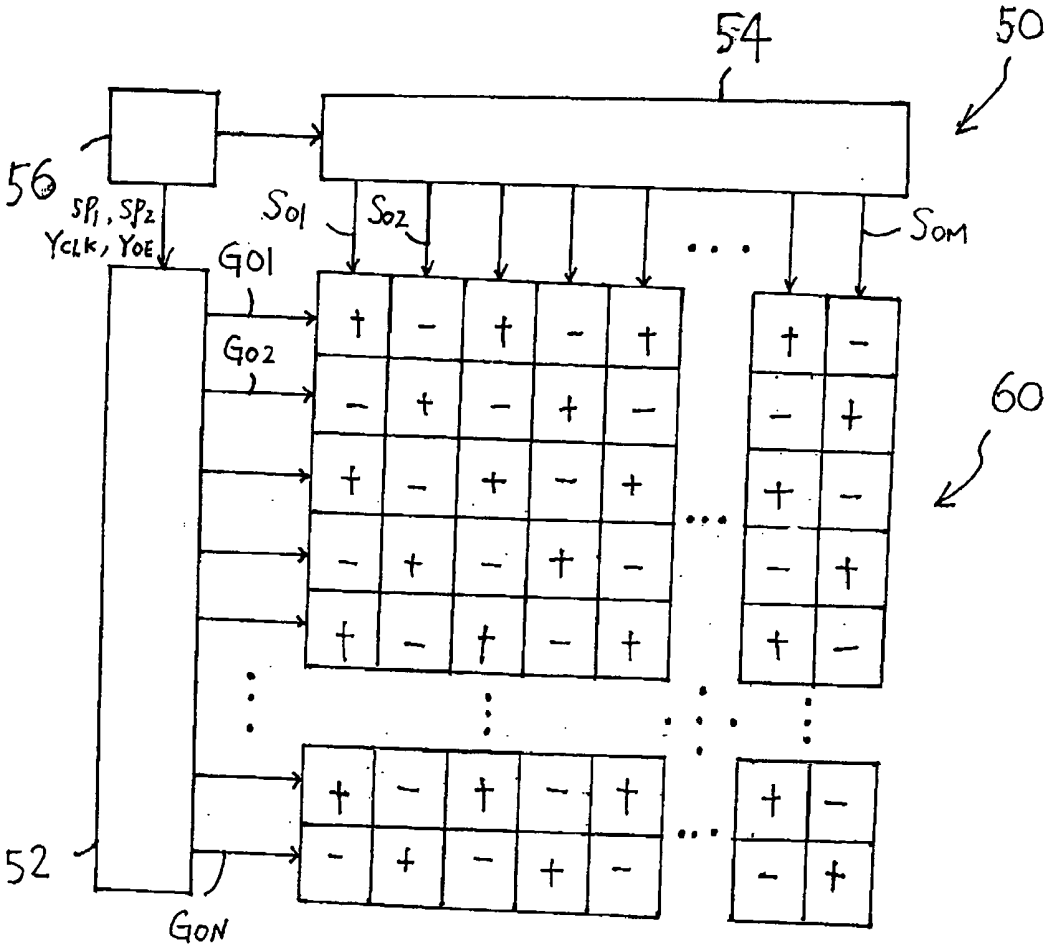

54
50
56
SP1, SP2
YCLK, YOE
S01
S02
SOM
G01
G02
60
52
GON

FIG. 2A

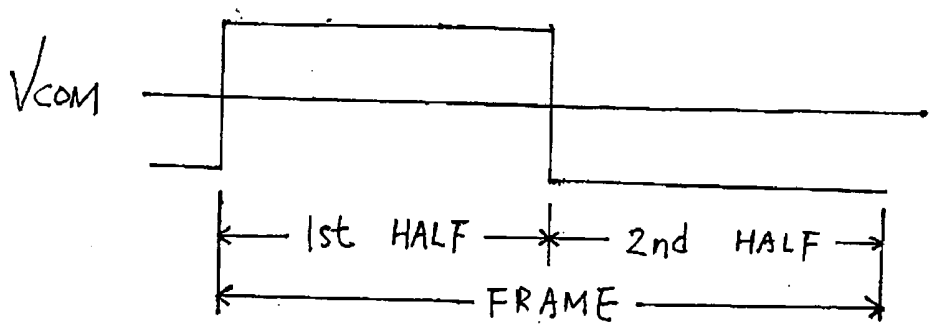

VCOM
1st HALF
2nd HALF
FRAME

FIG. 2C

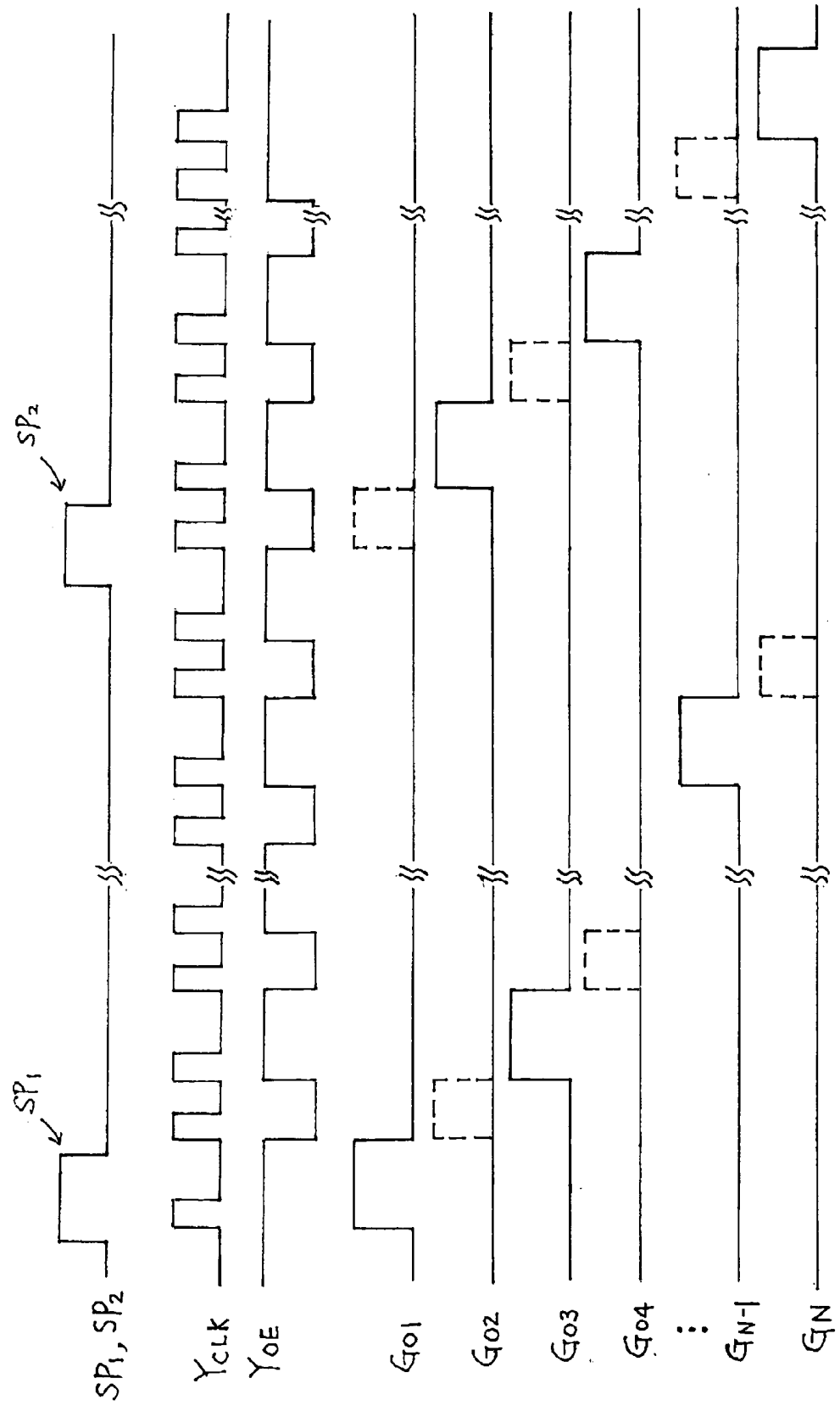


FIG. 2B

LOW POWER DRIVING IN A LIQUID CRYSTAL DISPLAY

DESCRIPTION OF THE INVENTION

[0001] 1. Field of the Invention

[0002] This invention relates in general to a liquid crystal display ("LCD") device and, more particularly, to a drive method and a drive circuit for an LCD device.

[0003] 2. Background of the Invention

[0004] A liquid crystal display ("LCD") device in the art may be driven by line inversion or dot inversion. In driving an LCD device with line inversion, the polarity of a source signal is inverted every line of gates during a frame time. In driving an LCD device with dot inversion, the polarity of a source signal is inverted not only every line of the gates, but also every line of sources during a frame time.

[0005] **FIG. 1A** is a schematic diagram of a drive circuit **10** in the art for an LCD device **20**. For simplicity, it is assumed that LCD device **20** uses a dot inversion scheme and includes an 8×8 matrix of pixels **22**. In reality, for example, a display area of a LCD device may include 1280×1024 pixels elements, respectively the horizontal and vertical resolutions of the LCD device. Drive circuit **10** includes a gate driver **12**, a source driver **14**, and a controller **16**. Although not specifically shown, an exemplary pixel **22** is formed adjacent to an intersection of one of gate lines **12-2** and one of source lines **14-2** formed approximately orthogonal to the gate lines **12-2**. Each of the pixels **22** is driven by a corresponding transistor (not shown) including a gate (not shown) coupled to a corresponding gate line **12-2** and a source (not shown) coupled to a corresponding source line **14-2**. In the particular embodiment, since dot inversion is used, a "+" or "−" sign shown to pixels **22** indicates a polarity, that is, positive or negative polarity of a source signal to be applied upon one of pixels **22** with respect to a common voltage V_{COM}.

[0006] **FIG. 1B** is a schematic timing diagram of drive circuit **10** shown in **FIG. 1A**. Controller **16** provides a start pulse SP to initiate a frame period. A clock signal CLK is generated in response to the start pulse SP. Pixels **22** are activated successively row by row through gate lines **12-2** in response to a rising edge of a clock signal CLK. Specifically, first, second, third gate lines G_1, G_2, G_3 and so forth are selected in sequence. Whenever a row of pixels **22** are activated, source signals are provided from source driver **14** to the row of pixels **22**. A display corresponding to the source signal provided during the frame period is accordingly provided.

[0007] **FIG. 1C** is a diagram showing an output signal of source driver **14** of drive circuit **10** shown in **FIG. 1A**. For line inversion and dot inversion alike, the transition of the polarity of a source signal is required at every gate line. However, frequent transition of voltage polarity may adversely result in large power consumption.

SUMMARY OF THE INVENTION

[0008] Accordingly, the present invention is directed to a display device and a method of display that obviate one or more of the problems due to limitations and disadvantages of the related art.

[0009] To achieve these and other advantages, and in accordance with the purpose of the invention as embodied and broadly described, there is provided a drive method for a liquid crystal display device that comprises providing an array of pixels formed in rows and columns, sequentially scanning odd-numbered rows of pixels during a first half of a frame period, and sequentially scanning even-numbered rows of pixels during a second half of the frame period.

[0010] In one aspect, the method further comprises providing a signal of a first polarity to the odd-numbered rows of pixels in sequence during the first half, and providing a signal of a second polarity to the even-numbered rows of pixels in sequence during the second half.

[0011] In another aspect, the method further comprises during the first half providing a signal of a first polarity in sequence to the odd-numbered rows of pixels at odd-numbered columns, and providing a signal of a second polarity in sequence to the odd-numbered rows of pixels at even-numbered columns.

[0012] In still another aspect, the method further comprises during the second half providing a signal of a first polarity in sequence to the even-numbered rows of pixels at even-numbered columns, and providing a signal of a second polarity in sequence to the even-numbered rows of pixels at odd-numbered columns.

[0013] Also in accordance with the present invention, there is provided a drive method for a liquid crystal display device that comprises providing an array of pixels formed in rows and columns, providing a first signal to activate a first half of a frame period, providing a plurality of first pulses and a plurality of second pulses, each of the second pulses following a corresponding one of the first pulses, sequentially activating odd-numbered rows of pixels during the first half in response to a corresponding one of the first pulses, sequentially inactivating even-numbered rows of pixels during the first half in response a corresponding one of the second pulses, providing a second signal to activate a second half of the frame period, sequentially activating even-numbered rows of pixels during the second half in response to a corresponding one of the first pulses, and sequentially inactivating odd-numbered rows of pixels during the second half in response a corresponding one of the second pulses.

[0014] Still in accordance with the present invention, there is provided a drive circuit for a liquid crystal display device including an array of pixels formed in rows and columns that comprises at least one source driver further comprising a plurality of source lines formed in parallel to each other, each of the source lines being coupled to a corresponding column of pixels, at least one gate driver further comprising a plurality of gate lines formed in parallel to each other and orthogonal to the source lines, each of the gate lines being coupled to a corresponding row of pixels, and a controller providing a first signal to sequentially activate a scan of odd-numbered rows of pixels through corresponding gate lines during a first half of a frame period, and providing a second signal to sequentially activate a scan of even-numbered rows of pixels through corresponding gate lines during a second half of the frame period.

[0015] Additional objects and advantages of the invention will be set forth in part in the description which follows, and in part will be obvious from the description, or may be

learned by practice of the invention. The objects and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the appended claims.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

[0017] The accompanying drawings, which are incorporated in and constitute a part of this specification, illustrate several embodiments of the invention and together with the description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] **FIG. 1A** is a schematic diagram of a conventional drive circuit for a liquid crystal display ("LCD") device;

[0019] **FIG. 1B** is a schematic timing diagram of the drive circuit shown in **FIG. 1A**;

[0020] **FIG. 1C** is a diagram showing an output signal of a source driver of the drive circuit shown in **FIG. 1A**;

[0021] **FIG. 2A** is a schematic diagram of a drive circuit for a liquid crystal display ("LCD") device in accordance with one embodiment of the present invention;

[0022] **FIG. 2B** is a schematic timing diagram of the drive circuit shown in **FIG. 2A** in accordance with one embodiment of the present invention; and

[0023] **FIG. 2C** is a diagram showing an output signal of a source driver of the drive circuit shown in **FIG. 1A** in accordance with one embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

[0024] Reference will now be made in detail to the present embodiment of the invention, an example of which is illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0025] **FIG. 2A** is a schematic diagram of a drive circuit **50** for a liquid crystal display ("LCD") device in accordance with one embodiment of the present invention. Drive circuit **50** serves to drive a matrix of pixels **60** of a LCD device formed in N rows and M columns, N and M being integers. Drive circuit **50** includes at least one gate driver **52**, at least one source driver **54** and a controller **56**. Gate driver **52** includes a plurality of gate lines G_{01}, G_{02} . . . G_N formed in parallel to each other. Each of gate lines G_{01}, G_{02} . . . G_N is coupled to a corresponding row of pixels **60**. Source driver **54** includes a plurality of source lines S_{01}, S_{02} . . . S_M formed in parallel to each other and orthogonal to gate lines G_{01}, G_{02} . . . G_N. Each of source lines S_{01}, S_{02} . . . S_M is coupled to a corresponding column of pixels **60**. Controller **16** provides a first signal SP_1 to sequentially activate a scan of odd-numbered rows of pixels **60** through corresponding gate lines **52** during a first half of a frame period, and provides a second signal SP_2 to sequentially activate a scan of even-numbered rows of pixels **60** through corresponding gate lines **52** during a second half of the frame period.

[0026] Controller **56** also provides a clock signal Y_{CLK} and an output enable signal Y_{OE} to enable the selection of odd-numbered rows of pixels **60** during the first half and selection of even-numbered rows of pixels **60** during the second half, as will be discussed in detail below with reference to **FIG. 2B**. **FIG. 2B** is a schematic timing diagram of drive circuit **50** shown in **FIG. 2A** in accordance with one embodiment of the present invention. The signal Y_{CLK} includes first pulses **70** and second pulses **80**. Each of second pulses **80** follows a corresponding one of first pulses **70**. The signal Y_{OE} is logically high in response to one of first pulses **70**, and becomes logically low in response to one of second pulses **80**. The logically high level of the signal Y_{OE} enables selection of a corresponding gate line G_{01}, G_{02} . . . or G_N, and the logically low level of the signal Y_{OE} disables selection of a corresponding gate line G_{01}, G_{02} . . . or G_N. Specifically, for example, during the first half activated in response to the first signal SP_1, a first gate line G_{01} is selected in response to a first pulse **70** and a high level Y_{OE}, and a second gate line G_{02} is not selected (shown in dotted lines) in response to a low level Y_{OE}. During the second half activated in response to the second signal SP_2, a first gate line G_{01} is not selected (shown in dotted lines) in response to a low level Y_{OE}, and a second gate line G_{02} is selected in response to a first pulse **70** and a high level Y_{OE}.

[0027] **FIG. 2C** is a diagram showing an output signal of source driver **54** of drive circuit **50** shown in **FIG. 2A** in accordance with one embodiment of the present invention. For line inversion, source driver **54** provides a signal of a first polarity to odd-numbered rows of pixels **60** in sequence during the first half, and provides a signal of a second polarity to even-numbered rows of pixels **60** in sequence during the second half. An output of source driver **54** during the first half is kept at the first polarity, for example, a positive voltage level with respect to a common voltage V_{COM}, and during the second half is kept at the second polarity, for example, a negative voltage level with respect to V_{COM}.

[0028] For dot inversion, during the first half source driver **54** provides a signal of a first polarity in sequence to the odd-numbered rows of pixels **60** at odd-numbered columns, and provides a signal of a second polarity in sequence to the odd-numbered rows of pixels **60** at even-numbered columns. During the second half source driver **54** provides a signal of a first polarity in sequence to the even-numbered rows of pixels **60** at even-numbered columns, and provides a signal of a second polarity in sequence to the even-numbered rows of pixels **60** at odd-numbered columns. As a result, outputs of source driver **54** do not change their polarities during the first half until the second half occurs, and are kept at the inverse polarities during the second half.

[0029] The present invention also provides a drive method for an LCD device. An array of pixels **60** formed in rows and columns are provided. A first signal SP, is provided to activate a first half of a frame period. A plurality of first pulses **70** and a plurality of second pulses **80** are provided. Each of second pulses **80** follows a corresponding one of first pulses **70**. Odd-numbered rows of pixels **60** are sequentially activated during the first half in response to a corresponding one of first pulses **70**. Even-numbered rows of pixels **60** are sequentially inactivated during the first half in response a corresponding one of second pulses **80**. After all of the odd-numbered rows of pixels **60** are selected, a second signal SP_2 is provided to activate a second half of the frame period. The even-numbered rows of pixels **60** are sequentially activated during the second half in response to a

corresponding one of first pulses **70**. The odd-numbered rows of pixels **60** are sequentially inactivated during the second half in response a corresponding one of second pulses **80**.

[**0030**] In one embodiment according to the present invention using line inversion, a signal of a first polarity is provided to the odd-numbered rows of pixels **60** in sequence during the first half, and a signal of a second polarity is provided to the even-numbered rows of pixels **60** in sequence during the second half.

[**0031**] In another embodiment according to the present invention using dot inversion, during the first half a signal of a first polarity is provided in sequence to the odd-numbered rows of pixels **60** at odd-numbered columns, and a signal of a second polarity is provided in sequence to the odd-numbered rows of pixels **60** at even-numbered columns. During the second half a signal of a first polarity is provided in sequence to the even-numbered rows of pixels **60** at even-numbered columns, and a signal of a second polarity is provided in sequence to the even-numbered rows of pixels **60** at odd-numbered columns.

[**0032**] Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A drive method for a liquid crystal display device comprising:

providing an array of pixels formed in rows and columns;

sequentially scanning odd-numbered rows of pixels during a first half of a frame period; and

sequentially scanning even-numbered rows of pixels during a second half of the frame period.

2. The method of claim 1 further comprising providing a signal of a first polarity to the odd-numbered rows of pixels in sequence during the first half, and providing a signal of a second polarity to the even-numbered rows of pixels in sequence during the second half.

3. The method of claim 1 further comprising during the first half providing a signal of a first polarity in sequence to the odd-numbered rows of pixels at odd-numbered columns, and providing a signal of a second polarity in sequence to the odd-numbered rows of pixels at even-numbered columns.

4. The method of claim 1 further comprising during the second half providing a signal of a first polarity in sequence to the even-numbered rows of pixels at even-numbered columns, and providing a signal of a second polarity in sequence to the even-numbered rows of pixels at odd-numbered columns.

5. The method of claim 1 further comprising providing a first signal to activate the first half, and a second signal to activate the second half.

6. The method of claim 1 further comprising generating a signal including first pulses and second pulses, wherein each of the second pulses follows a corresponding one of the first pulses.

7. The method of claim 6 further comprising sequentially activating a scan of the odd-numbered rows of pixels during the first half in response to a corresponding one of the first pulses.

8. The method of claim 6 further comprising sequentially activating a scan of the even-numbered rows of pixels during the second half in response to a corresponding one of the first pulses.

9. The method of claim 6 further comprising sequentially inactivating a scan of the even-numbered rows of pixels during the first half in response to a corresponding one of the second pulses.

10. The method of claim 6 further comprising sequentially inactivating a scan of the odd-numbered rows of pixels during the second half in response to a corresponding one of the second pulses.

11. A drive method for a liquid crystal display device comprising:

providing an array of pixels formed in rows and columns;

providing a first signal to activate a first half of a frame period;

providing a plurality of first pulses and a plurality of second pulses, each of the second pulses following a corresponding one of the first pulses;

sequentially activating odd-numbered rows of pixels during the first half in response to a corresponding one of the first pulses;

sequentially inactivating even-numbered rows of pixels during the first half in response a corresponding one of the second pulses;

providing a second signal to activate a second half of the frame period;

sequentially activating even-numbered rows of pixels during the second half in response to a corresponding one of the first pulses; and

sequentially inactivating odd-numbered rows of pixels during the second half in response a corresponding one of the second pulses.

12. The method of claim 11 further comprising providing a signal of a first polarity to the odd-numbered rows of pixels in sequence during the first half, and providing a signal of a second polarity to the even-numbered rows of pixels in sequence during the second half.

13. The method of claim 11 further comprising during the first half providing a signal of a first polarity in sequence to the odd-numbered rows of pixels at odd-numbered columns, and providing a signal of a second polarity in sequence to the odd-numbered rows of pixels at even-numbered columns.

14. The method of claim 11 further comprising during the second half providing a signal of a first polarity in sequence to the even-numbered rows of pixels at even-numbered columns, and providing a signal of a second polarity in sequence to the even-numbered rows of pixels at odd-numbered columns.

15. The method of claim 11 further comprising providing a signal including a first state corresponding to the first pulses, and a second state corresponding to the second pulses.

16. A drive circuit for a liquid crystal display device including an array of pixels formed in rows and columns comprising:

at least one source driver further comprising a plurality of source lines formed in parallel to each other, each of the source lines being coupled to a corresponding column of pixels;

at least one gate driver further comprising a plurality of gate lines formed in parallel to each other and orthogonal to the source lines, each of the gate lines being coupled to a corresponding row of pixels; and

a controller providing a first signal to sequentially activate a scan of odd-numbered rows of pixels through corresponding gate lines during a first half of a frame period, and providing a second signal to sequentially activate a scan of even-numbered rows of pixels through corresponding gate lines during a second half of the frame period.

17. The circuit of claim 16, the source driver providing a signal of a first polarity to the odd-numbered rows of pixels in sequence during the first half, and providing a signal of a second polarity to the even-numbered rows of pixels in sequence during the second half.

18. The circuit of claim 16, during the first half the source driver providing a signal of a first polarity in sequence to the odd-numbered rows of pixels at odd-numbered columns, and providing a signal of a second polarity in sequence to the odd-numbered rows of pixels at even-numbered columns.

19. The circuit of claim 16, during the second half the source driver providing a signal of a first polarity in sequence to the even-numbered rows of pixels at even-numbered columns, and providing a signal of a second polarity in sequence to the even-numbered rows of pixels at odd-numbered columns.

20. The circuit of claim 16, the controller further providing a signal including first pulses and second pulses, wherein each of the second pulses follows a corresponding one of the first pulses.

21. The circuit of claim 20 wherein the odd-numbered rows of pixels are sequentially selected during the first half in response to the first pulses, and the even-numbered rows of pixels are sequentially selected during the second half in response to the first pulses.

22. The circuit of claim 20 wherein the even-numbered rows of pixels are sequentially inactivated during the first half in response to the second pulses.

23. The circuit of claim 20 wherein the odd-numbered rows of pixels are sequentially inactivated during the second half in response to the second pulses.

24. The circuit of claim 16, the controller further providing a signal including a first state corresponding to the first pulses, and a second state corresponding to the second pulses.

* * * * *

专利名称(译)	液晶显示器中的低功率驱动		
公开(公告)号	US20050174310A1	公开(公告)日	2005-08-11
申请号	US10/747068	申请日	2003-12-30
[标]申请(专利权)人(译)	友达光电股份有限公司		
申请(专利权)人(译)	友达光电股份有限公司		
当前申请(专利权)人(译)	友达光电股份有限公司		
[标]发明人	HUANG JIH FONG LI HUAN HSIN		
发明人	HUANG, JIH-FONG LI, HUAN-HSIN		
IPC分类号	G02F1/133 G09G3/20 G09G3/36		
CPC分类号	G09G3/3614 G09G2310/0213 G09G3/3674		
外部链接	Espacenet USPTO		

摘要(译)

一种用于液晶显示装置的驱动方法，包括：提供以行和列形成的像素阵列，在帧周期的前半部分顺序扫描奇数行像素，以及在a期间顺序扫描偶数行像素。帧周期的后半部分。