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(54) **SEMICONDUCTOR ELEMENT AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME**

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(52) **U.S. Cl.** **349/43**

(57) **ABSTRACT**

To prevent an n-channel thin-film transistor from being deteriorated by hot holes generated in a gate-negative pulse mode. A thin polysilicon film **10** is provided with a p-type semiconductor region **13** in contact with a channel region **14**. The p-type semiconductor region **13** is electrically connected to nowhere except the channel region **14**. Holes induced on the surface due to a gate-negative pulse are further supplied from the p-type semiconductor region **13**. An electric field established by the gate-negative pulse is relaxed by the holes, fewer hot holes are injected into the gate oxide film, and the TFT characteristics are less deteriorated.

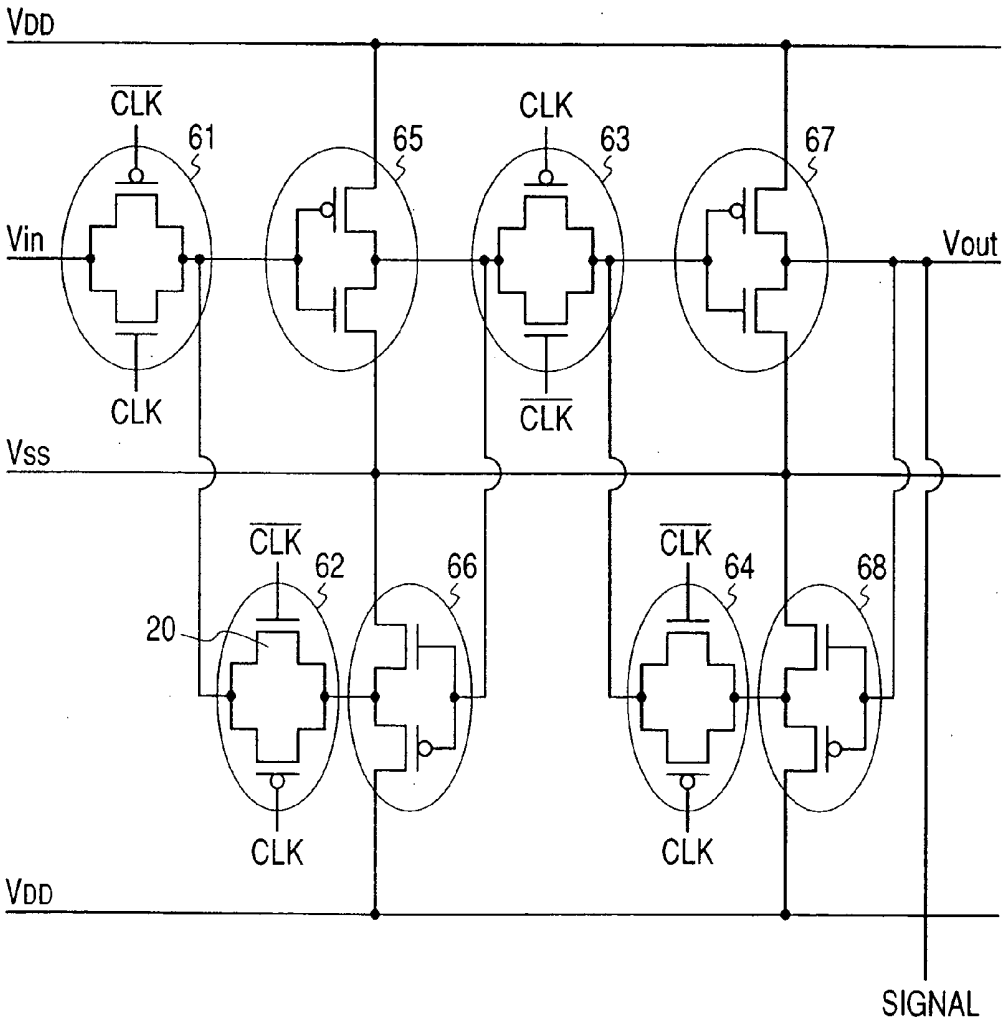


FIG. 1

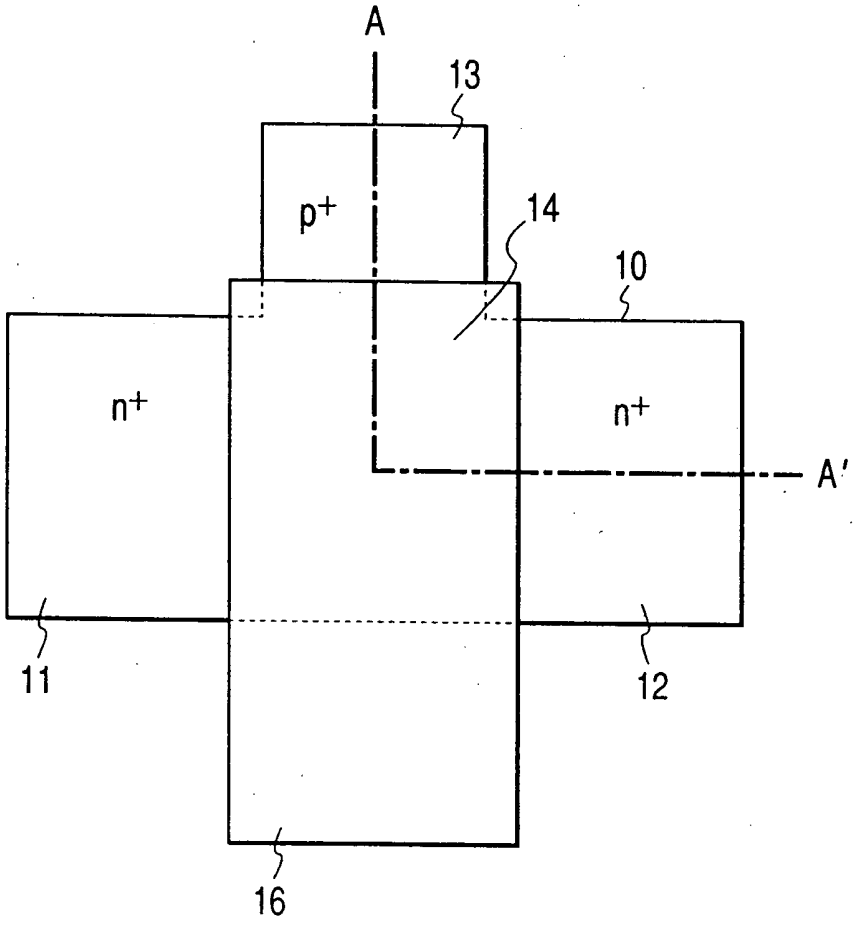


FIG. 2

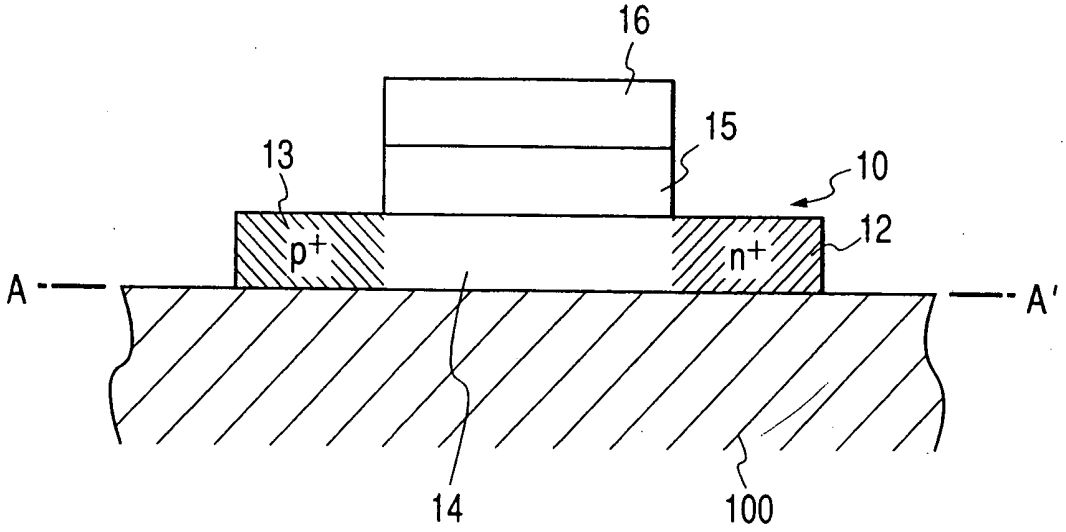


FIG. 3(a)

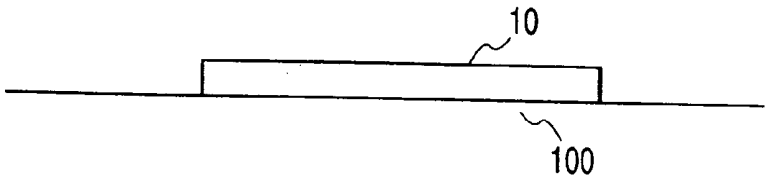


FIG. 3(b)

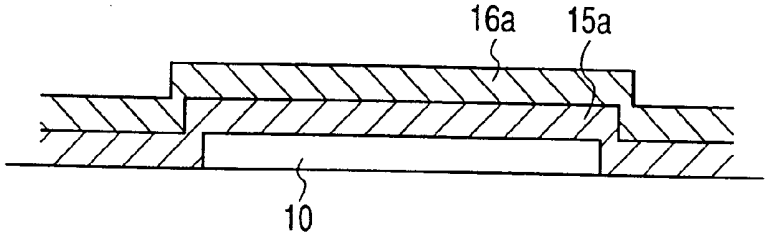


FIG. 3(c)

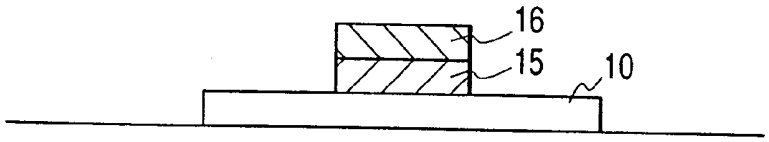


FIG. 3(d)

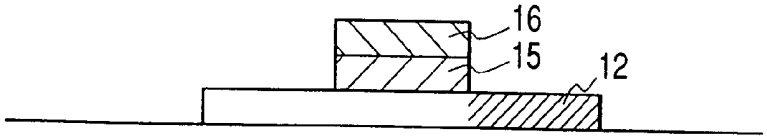


FIG. 3(e)

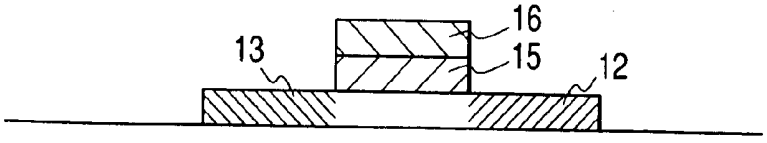


FIG. 4

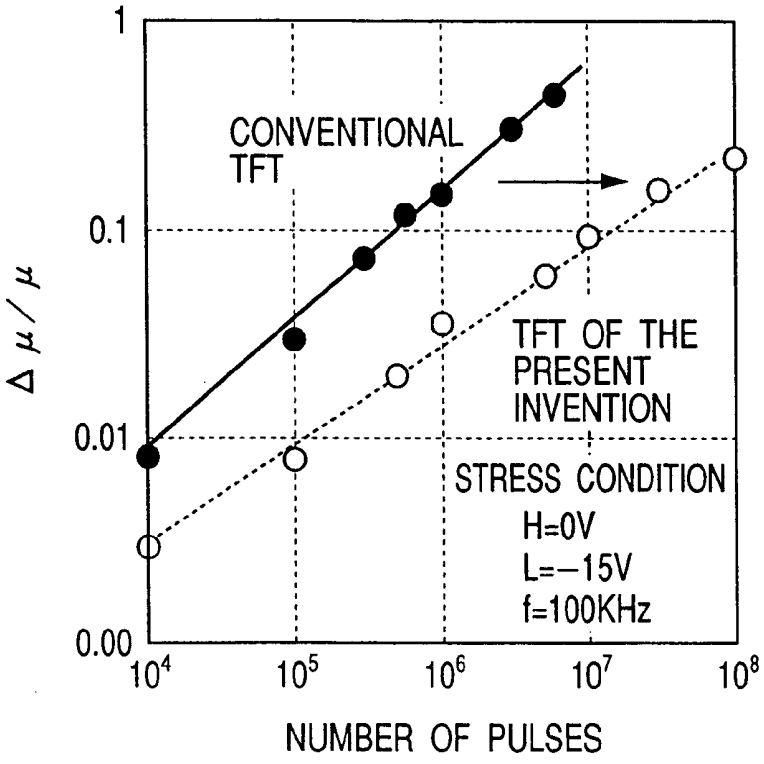

1
0.1
0.01
0.00
Δμ/μ
CONVENTIONAL TFT
TFT OF THE PRESENT INVENTION
STRESS CONDITION
H=0V
L=−15V
f=100KHz
10^4
10^5
10^6
10^7
10^8
NUMBER OF PULSES

FIG. 5

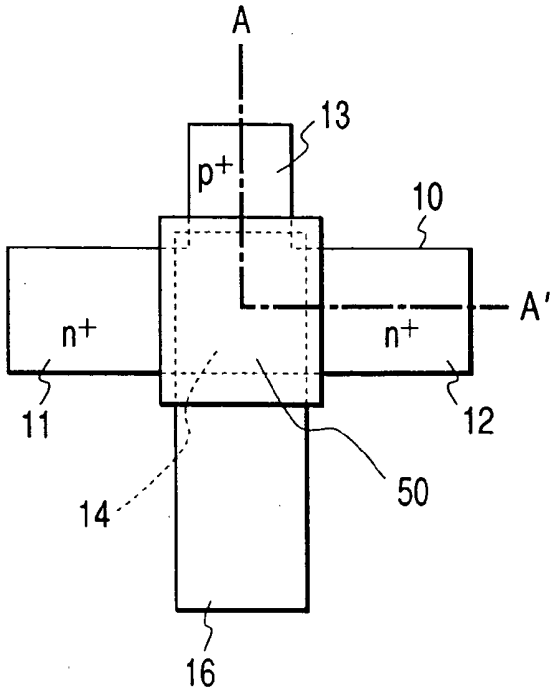

A
13
p+
10
A'
n+
n+
11
12
14
50
16

FIG. 6

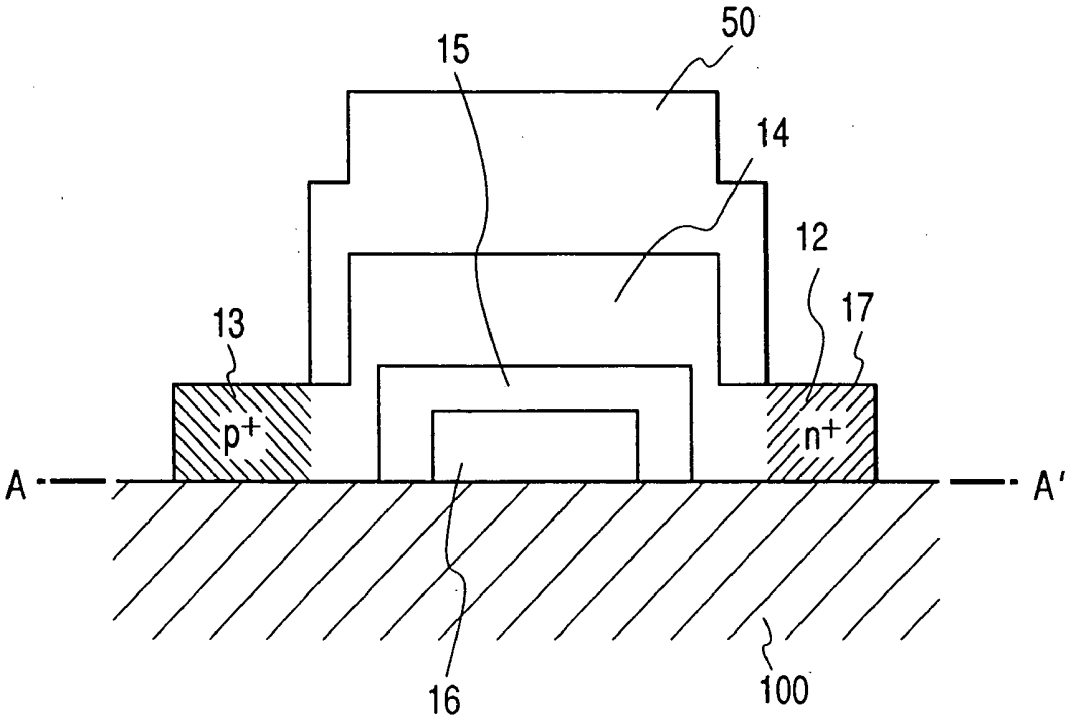


FIG. 7

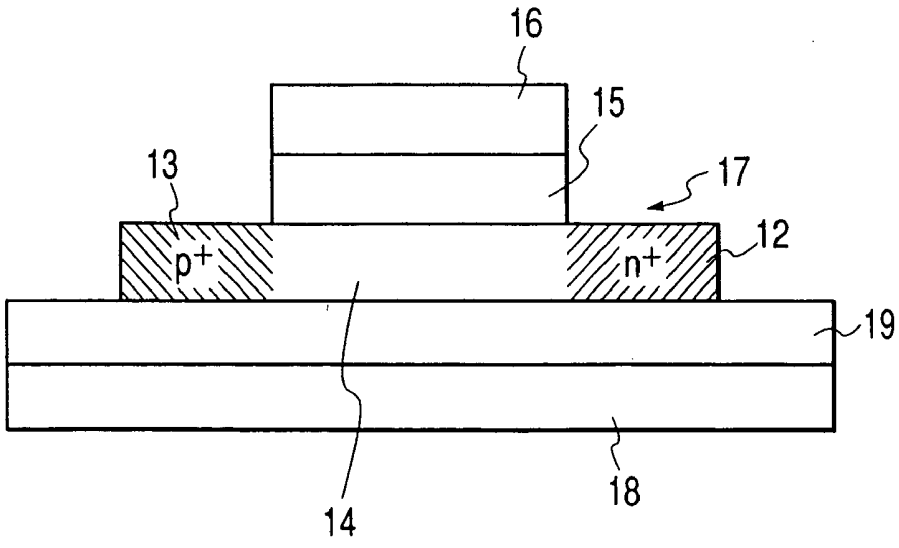


FIG. 8

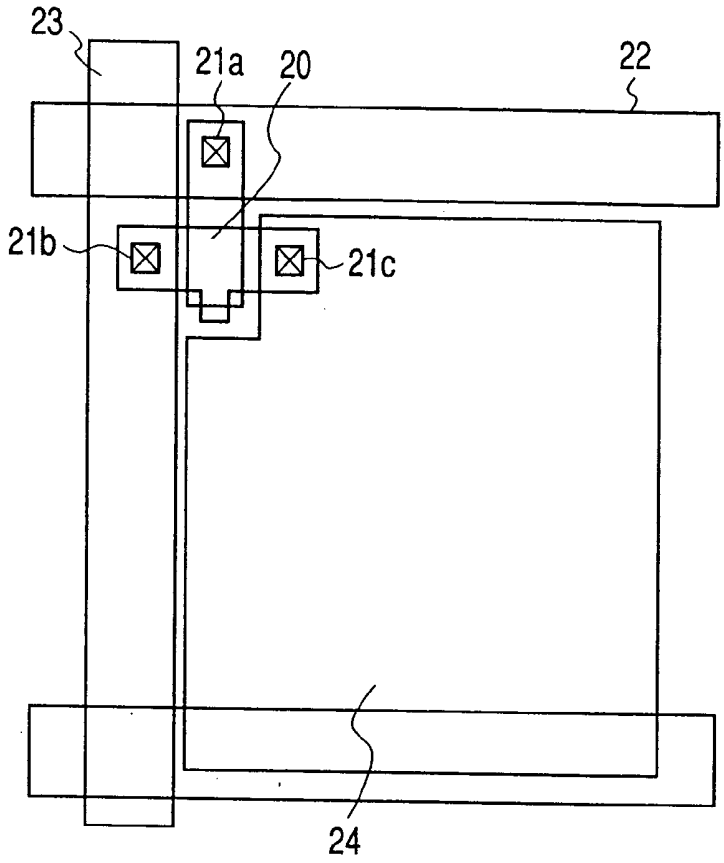


FIG. 9

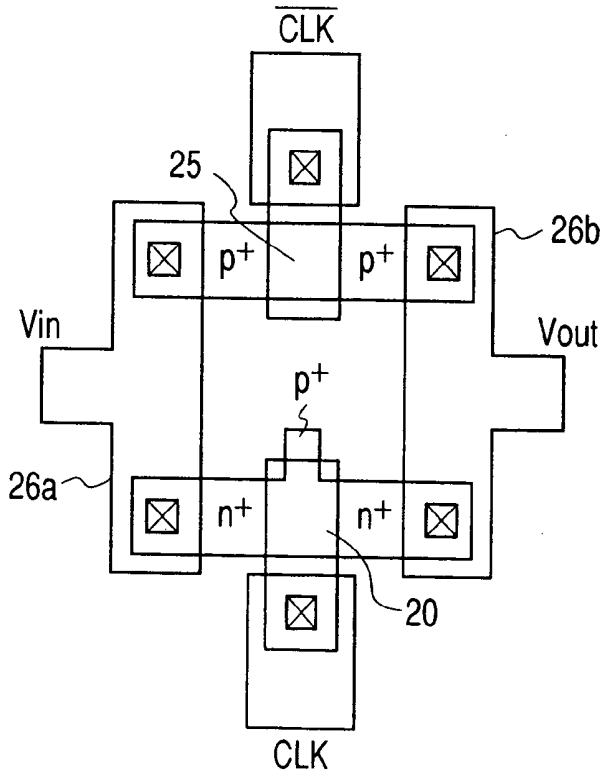


FIG. 10

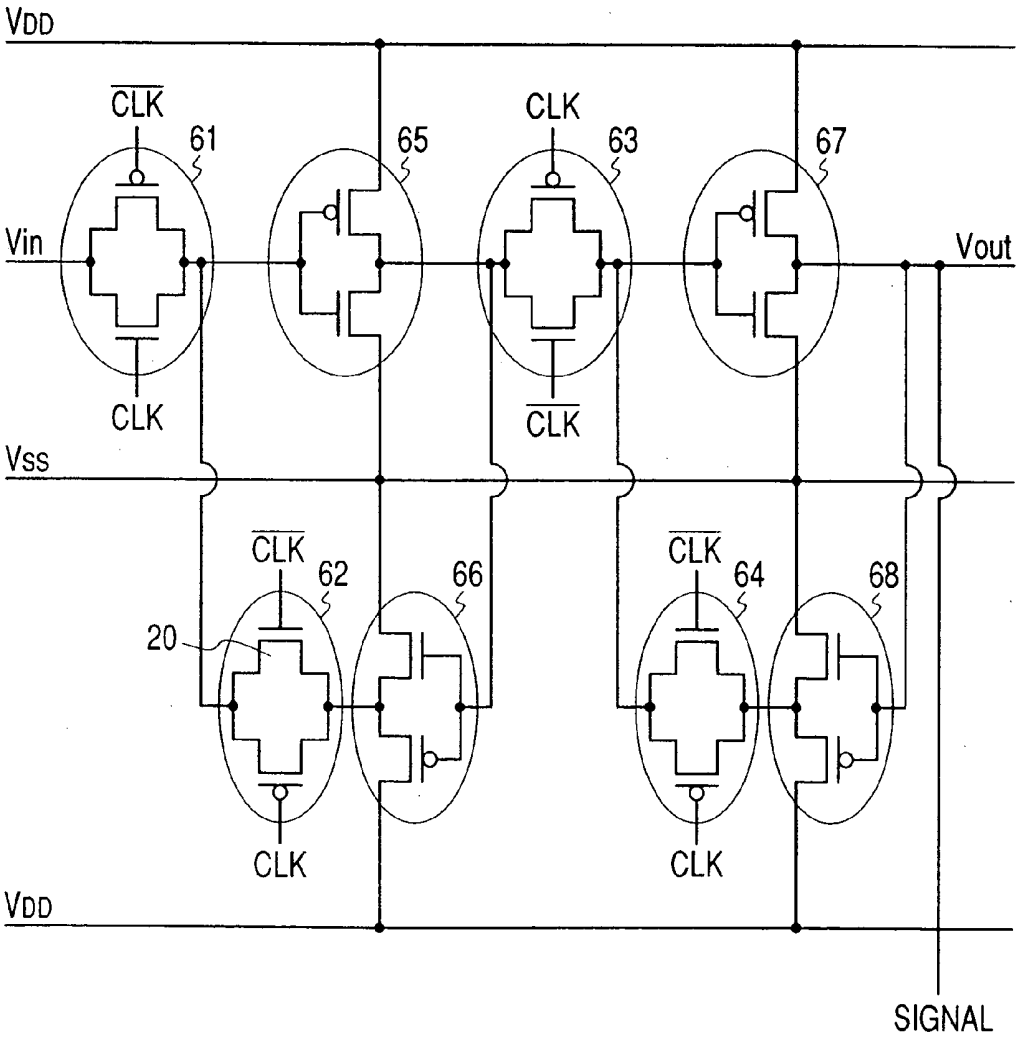

VDD
CLK
61
65
CLK
63
67
Vin
Vout
CLK
CLK
Vss
CLK
62
66
CLK
64
68
20
CLK
CLK
VDD
SIGNAL

FIG. 11

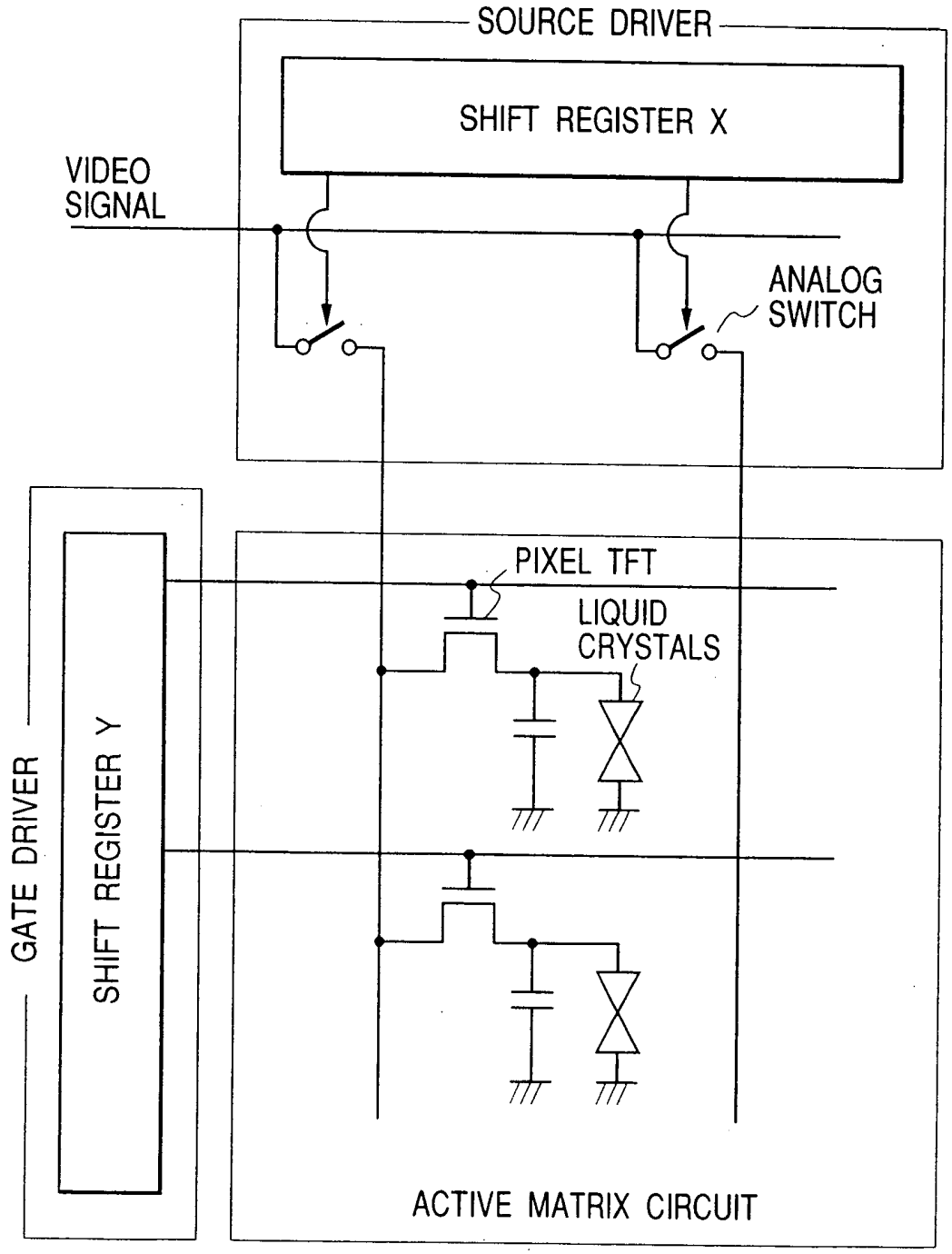
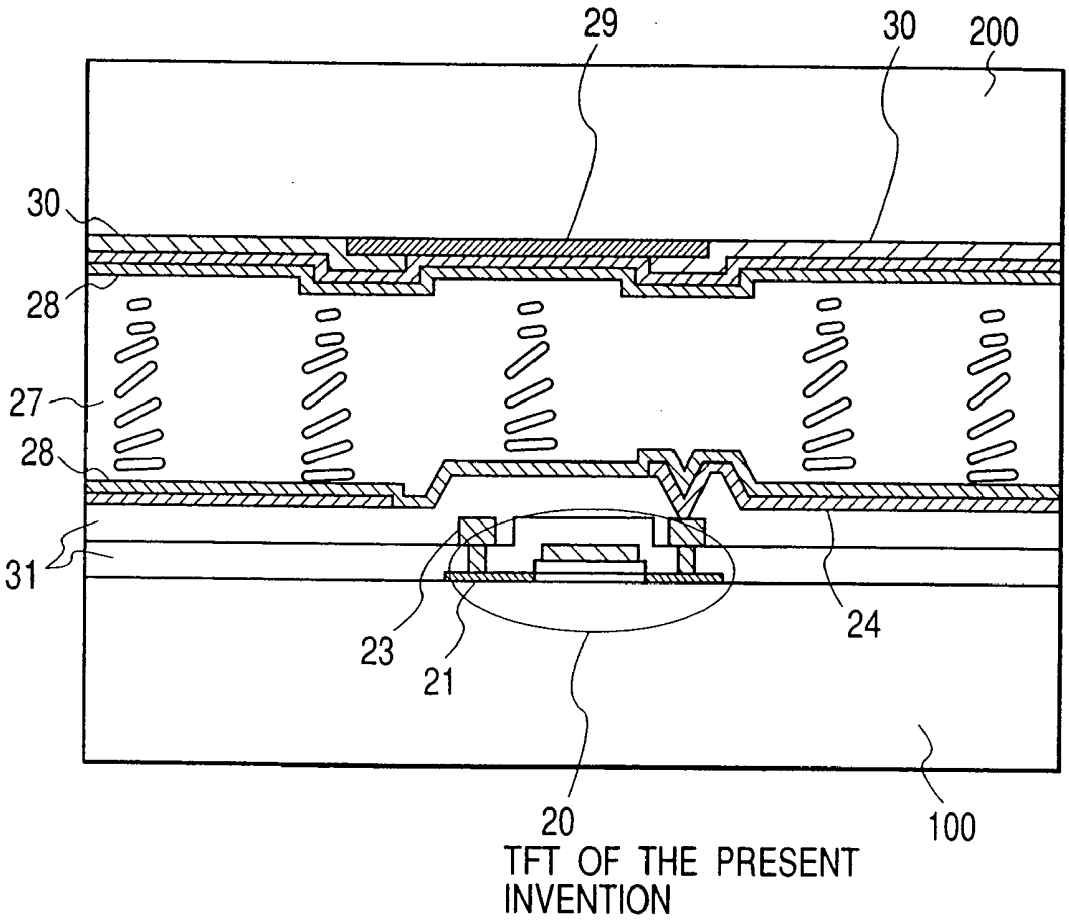

SOURCE DRIVER
SHIFT REGISTER X
VIDEO SIGNAL
ANALOG SWITCH
PIXEL TFT
LIQUID CRYSTALS
GATE DRIVER
SHIFT REGISTER Y
ACTIVE MATRIX CIRCUIT

FIG. 12



TFT OF THE PRESENT INVENTION

FIG. 13

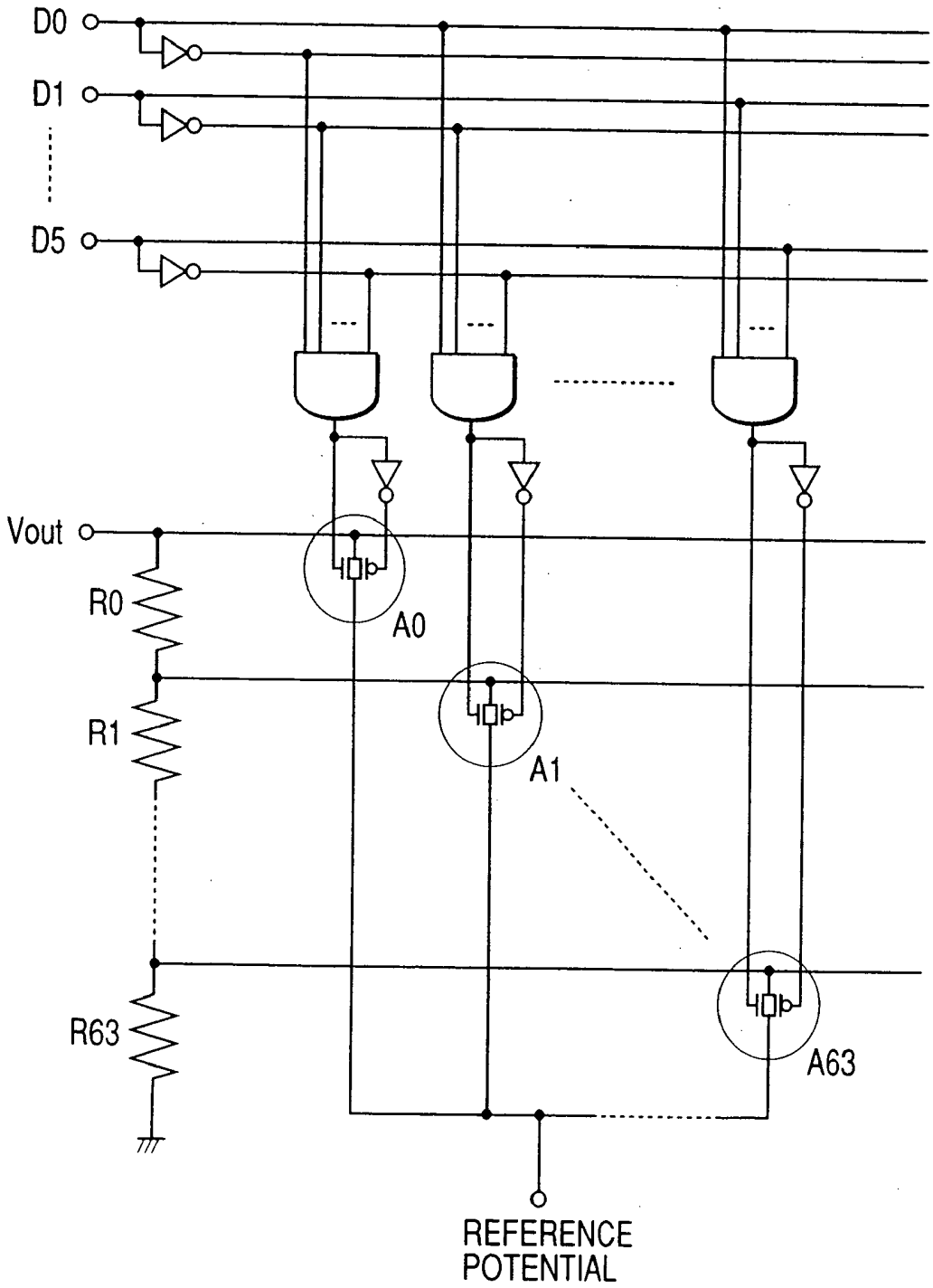
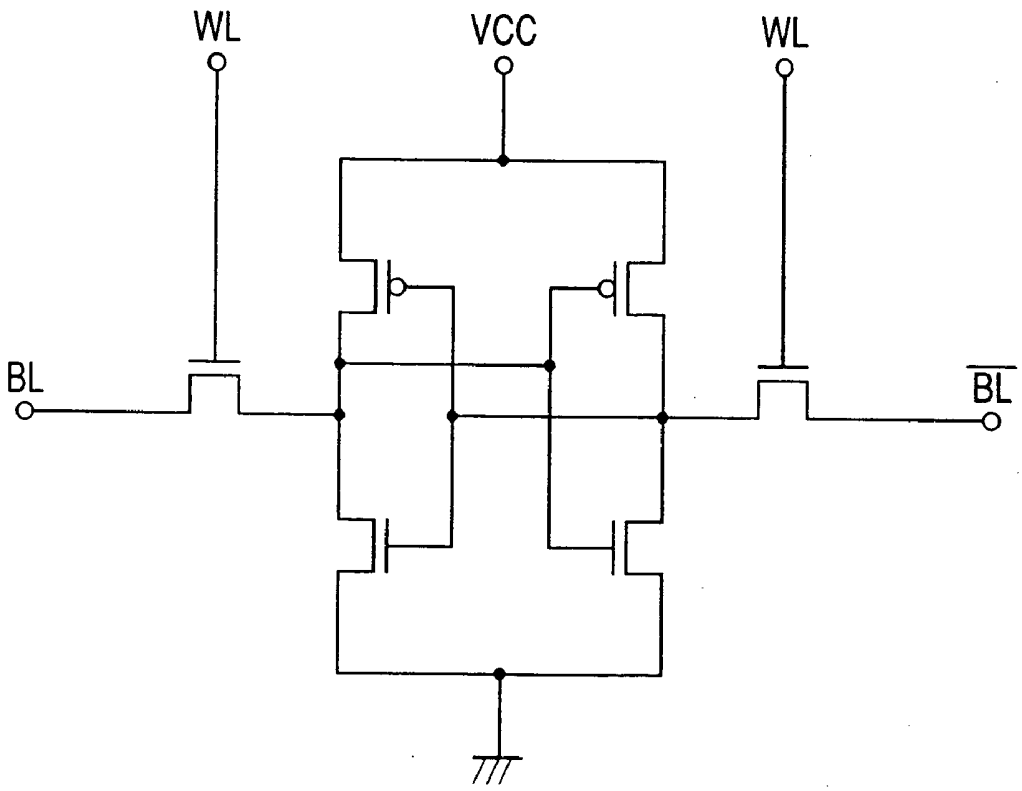


FIG. 14



SEMICONDUCTOR ELEMENT AND LIQUID CRYSTAL DISPLAY DEVICE USING THE SAME

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a liquid crystal display device of an active matrix type used for displaying image data and character data from 0A equipment or the like, and to the structure of an n-channel thin-film transistor used for this device.

[0002] A thin-film transistor (hereinafter abbreviated as TFT) has heretofore been used for driving liquid crystals of a pixel in a panel of a liquid crystal display device of the directly-viewing type. A simple switching element suffices for the performance of the TFT and, hence, amorphous silicon has been used as a semiconductor thin film. On the other hand, a liquid crystal display device of the projection type requires a high degree of brightness, and the TFT must be realized in a small size to increase the transmission factor. However, it was not allowed to decrease the size of the TFT formed by amorphous silicon since its current driving ability was so small. Therefore, so-called high-temperature polysilicon has been developed featuring an increased current driving ability by using quartz glass as a substrate and polycrystallizing amorphous silicon at a temperature as high as 900° C. or higher.

[0003] However, quartz glass is very expensive and drives up the cost of production. Therefore, so-called low-temperature polysilicon has been developed by using an inexpensive glass substrate and polycrystallizing amorphous silicon by the irradiation with a laser beam.

[0004] In recent years, strikingly improved performance has been exhibited by the TFT formed by using the low-temperature polysilicon. Under such circumstances, it is becoming a tendency to utilize the TFT not only as a switching element for driving the pixels of a panel in a liquid crystal display device but also for the peripheral drive circuits in the liquid crystal display device. Moreover, a liquid crystal display device such as system-in-display is emerging being furnished with a memory function as well as various functions of CPU, interface, I/O and input by pen by using TFTs. In these cases, the role played by the TFT is not only limited to that of a simple switching element; i.e., performance and reliability are required by taking the logic circuits into account.

[0005] When the TFT is used as a logic element, eight kinds of voltage patterns will be applied to the three terminals of gate, source and drain as tabulated below, wherein "H" denotes a high level and "L" denotes a low level.

		Patterns							
		1	2	3	4	5	6	7	8
electrode	Gate	H	L	H	L	H	L	L	H
	Source	H	H	L	L	L	H	L	H
	Drain	L	L	H	H	L	H	L	H

[0006] So far, the TFT has been used for driving a liquid crystal pixel, and the above-mentioned patterns 1 to 4 have been exclusively used, i.e., relations of potential difference across the source and the drain have been exclusively used. When a potential difference develops across the source and the drain, a high electric field is established in the TFT, and a carrier having abnormally high energy (hereinafter referred to as hot carrier) is generated. The hot carrier that is injected into the gate oxide film causes a problem of deterioration in the characteristics of TFT.

[0007] It has heretofore been attempted to solve the problem of hot carrier that generates when a high electric field is applied across the source and the drain. As a means for solving this problem, there have been proposed a lightly doped drain (LDD) structure and a double drain structure as disclosed in "Submicron Device 2", by Mitsumasa Koyanagi, Maruzen Co., 1995, p. 187. According to these structures, a high electric field applied across the source and the drain is relaxed to prevent the generation of hot carrier. These structures are with the case when a single crystal is used as a semiconductor. The same, however, also holds true even in the case of TFT.

SUMMARY OF THE INVENTION

[0008] However, there is almost no description concerning the problem of deterioration caused by a voltage application pattern 6 that is tabulated above. This is because, in the conventional TFT for simply driving the liquid crystal pixel, such a voltage application pattern has seldom occurred. When a peripheral circuit is fabricated by using the TFTs, however, the voltage application pattern 6 tabulated above occurs in an analog switch used, for example, for a shift register.

[0009] In an n-channel TFT in which the source is assuming "H" and the drain is assuming "H", in particular, the on-current drastically decreases and the TFT characteristics are deteriorated when a stress is applied to the gate, i.e., when "L" and "H" are alternatingly input to the gate (hereinafter, this stress mode is referred to as gate-negative pulse mode). The cause of deteriorating the TFT characteristics in the gate-negative pulse mode is as described below. When the gate voltage changes from "H" into "L", the channel region changes from a depletion layer in which no carrier is present into an accumulated layer in which holes are present in an excess amount. In this case, holes are induced on the surface of the semiconductor thin film from the channel region of the semiconductor thin film. Here, it is considered that the holes gain high energy due to an electric field of a gate-negative pulse and turn into hot holes which are then injected into the gate oxide film, whereby an interface level generates on the surface of the semiconductor device to greatly deteriorate the TFT. characteristics.

[0010] The object of the present invention is to provide a TFT of a structure of which the characteristics are not deteriorated in the gate-negative pulse mode.

[0011] Moreover, the object of the present invention is to provide a liquid crystal display device which features a simplified circuitry and improved display quality by employing a TFT which is less deteriorated in the gate-negative pulse mode, for a liquid crystal display device of which the circuitry is becoming complex or of which the display quality is becoming poor due to limitation on the range when utilizing the TFT which is deteriorated in the gate-negative pulse mode.

[0012] Furthermore, it is the object of the present invention to provide a liquid crystal display device equipped with a shift register having improved reliability by employing a TFT which is less deteriorated in the gate-negative pulse mode, for the shift register.

[0013] Moreover, it is the object of the present invention to provide a liquid crystal display device using an analog switch having improved reliability by utilizing a TFT which is less deteriorate in the gate-negative pulse mode, for the analog switch.

[0014] According to the present invention, the above-mentioned objects are accomplished by providing a semiconductor thin film of the TFT with a p-type semiconductor region that is in contact with a channel region but is electrically connected to nowhere except the channel region. Upon employing this structure, holes induced on the surface by the gate-negative pulses are further supplied from the p-type semiconductor region. The holes supplied from the p-type semiconductor region relax the electric field established by the gate-negative pulse. Therefore, the hot holes are less injected into the gate oxide film, and the TFT characteristics are less deteriorated. Besides, the p-type semiconductor region needs be connected to nowhere except the channel region and can, hence, be replaced by the conventional TFT, and an increase in the TFT area is confined to the p-type semiconductor region only.

[0015] According to the present invention, furthermore, the above-mentioned objects are accomplished by using the above-mentioned TFTs as the n-channel insulated gate thin-film transistors used for the liquid crystal display device, by using the above-mentioned TFTs as the n-channel insulated gate thin-film transistors to constitute shift registers in the peripheral circuit, and by using the above-mentioned TFTs as the n-channel insulated gate thin-film transistors to constitute analog switches in the peripheral circuit.

[0016] That is, the present invention is concerned with an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a semiconductor thin film formed on an insulating substrate and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except the channel region.

[0017] The present invention is further concerned with an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a gate electrode formed on an insulating substrate and a semiconductor thin film formed on said gate electrode via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just over the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with said channel region, and said p-type semiconductor region is electrically connected to nowhere except the channel region.

[0018] Moreover, the present invention is concerned with an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising an insulating film formed on a semiconductor substrate, a semiconductor thin film formed on said insulating layer and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except the channel region.

[0019] The present invention is further concerned with a liquid crystal display device comprising:

[0020] an active matrix including a plurality of scanning electrodes formed on an insulating substrate, a plurality of video signal electrodes formed so as to intersect the scanning electrodes, thin-film transistors connected to the scanning electrodes and to the video signal electrodes, and pixel electrodes connected to said thin-film transistors;

[0021] a peripheral circuit formed on said insulating substrate by the same method as that of forming said thin-film transistors;

[0022] an opposing substrate opposed to said insulating substrate; and

[0023] liquid crystals held between said insulating substrate and said opposing substrate;

[0024] wherein said n-channel insulated gate thin-film transistors are used as said thin-film transistors.

[0025] In the liquid crystal display device, the TFT characteristics are little deteriorated when the above-mentioned n-channel insulated gate thin-film transistors are used for the shift registers in the peripheral circuit and, particularly, when the above-mentioned n-channel insulated gate thin-film transistors are used to play the role of analog switches in the shift registers in the peripheral circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0026] **FIG. 1** is a schematic plan view of a TFT according to the present invention;

[0027] **FIG. 2** is a schematic sectional view along a line A-A' in **FIG. 1**;

[0028] **FIG. 3** is a diagram illustrating the steps for producing the TFT according to the present invention;

[0029] **FIG. 4** is a diagram comparing the degrees of degradation of when stress is applied to the TFT of the present invention and to the TFT of a conventional structure;

[0030] **FIG. 5** is a schematic plan view illustrating a bottom gate type TFT according to the present invention;

[0031] **FIG. 6** is a schematic sectional view along a line A-A' in **FIG. 5**;

[0032] **FIG. 7** is a schematic sectional view of an n-channel SOI-MOSFET according to the present invention;

[0033] **FIG. 8** is a plan view of a unit pixel in a liquid crystal display device using the TFT of the present invention;

[0034] **FIG. 9** is a plan view of an analog switch using the TFT of the present invention;

[0035] **FIG. 10** is a diagram of a static shift register circuit using the TFTs of the present invention;

[0036] **FIG. 11** is a block diagram of a peripheral circuit and an active matrix circuit in the liquid crystal display device constituted by using the TFTs of the present invention;

[0037] **FIG. 12** is a schematic sectional view of a liquid crystal display device constituted by using the TFTs of the present invention;

[0038] **FIG. 13** is a circuit diagram of a DA converter constituted by using the TFTs of the present invention; and

[0039] **FIG. 14** is a circuit diagram of a static random access memory cell constituted by using the TFTs of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0040] Embodiments of the present invention will now be described with reference to the drawings.

Embodiment 1

[0041] **FIG. 1** is a schematic plan view illustrating a TFT according to the present invention, and **FIG. 2** is a schematic sectional view along a line A-A' in **FIG. 1**. A substrate is a glass **100**. A first layer is a thin polysilicon film **10**. The thin polysilicon film **10** is constituted by a source **11** and a drain **12** which are n-type semiconductor regions, a p-type semiconductor region **13**, and a channel region **14** just under a gate **16** which is an intrinsic semiconductor region. A second layer is a gate insulating film **15** which insulates the gate **16** and the thin polysilicon film **10** from each other. A third layer is the gate **16** having the same shape as the gate insulating film **15**. Upon applying a positive voltage to the gate **16**, an inverted layer in which the electrons are present in an excess amount is formed in the channel region **14** to form a channel, whereby the source **11** and the drain **12** are rendered conductive to each other to obtain a switching operation.

[0042] In the TFT structure of this embodiment, the holes induced on the surface due to a gate-negative pulse are further supplied from the p-type semiconductor region **13**. The holes supplied from the p-type semiconductor region **13** relax the electric field established by the gate-negative pulse. Therefore, fewer hot holes are injected into the gate insulating film **15**, and the TFT characteristics are less deteriorated.

[0043] **FIG. 3** illustrates the steps for producing the above-mentioned TFT. The sectional views of **FIG. 3** correspond to a cross section along the line A-A' in **FIG. 1**. A thin amorphous silicon film is deposited maintaining a thickness of 60 nm on the glass substrate **100**. Upon irradiating the thin film with a laser beam, amorphous silicon is polycrystallized to form a so-called low-temperature polysilicon. Depending upon the photolithographic technology, furthermore, polysilicon is etched to form a thin polysilicon film **10** of the form of an island (**FIG. 3**(*a*)). Next, a silicon oxide **15***a* is grown in vapor phase to form a gate insulating film. Then, a metal **16***a* such as aluminum is deposited to form a gate (**FIG. 3**(*b*)). Next, the gate and the gate insulating film are etched relying upon the photolithographic technology to form a gate **16** and a gate insulating film **15** (**FIG. 3**(*c*)). Then, impurities of the Group **5** of periodic table, such as phosphorus ions, are implanted into the thin polysilicon film by, for example, the ion-doping method to form n-type semiconductor regions that form a source **11** and a drain **12** (**FIG. 3**(*d*)). Then, impurities of the Group **3** of periodic table, such as boron ions, are implanted into the thin polysilicon film by, for example, the ion-doping method to form a p-type semiconductor region (**FIG. 3**(*e*)). Thus, the TFT of the present invention is produced.

[0044] **FIG. 4** illustrates the degrees of degradation of when pulse stress of "L" and "H" is applied to the gate of the TFT of the present invention having the p-type semiconductor region **13** and to the gate of the conventional TFT without p-type semiconductor region with their source potential being maintained at "H" and drain potential being maintained at "H", and with "L" and "H" pulse stress applied to the gate. The "L" level is set to be −15 V, the "H" level is set to be 0 V, and the pulse width is set to be 10 μs. In **FIG. 4**, the ordinate represents the amount obtained by dividing an amount of change $\Delta\mu$ in the mobility of TFT by an initial mobility μ. When the life of the element is defined to be an amount of deterioration in the mobility $\Delta\mu/\mu$=0.2, it will then be obvious from **FIG. 4** that the TFT of the present invention exhibits a life extended into 50 times as long as that of the conventional TFT.

[0045] In this embodiment, the thin semiconductor film is formed of polysilicon. It, however, may be formed of amorphous silicon, single crystalline silicon, single crystalline germanium or the like.

Embodiment 2

[0046] **FIG. 5** is a schematic plan view of a bottom gate type TFT according to the present invention, and **FIG. 6** is a schematic sectional view along a line A-A' in **FIG. 5**. A substrate is a glass **100**. A first layer is a gate **16**. A second layer is a gate insulating film **15** which insulates the gate **16** and a thin polysilicon film **10** from each other. A third layer is the thin polysilicon film **10**. In the thin polysilicon film **10** are formed a source **11** and a drain **12** which are n-type semiconductor regions, a p-type semiconductor region **13**, and a channel region **14** which is an intrinsic semiconductor region just over the gate electrode. A fourth layer is a channel protection film **50** for protecting the channel. Upon applying a positive voltage to the gate **16**, an inverted layer in which the electrons are present in an excess amount is formed in the channel region **14** thereby to form a channel, whereby the source **11** and the drain **12** are rendered conductive relative to each other to obtain a switching operation. ,In the TFT of this embodiment, when a negative pulse is applied to the gate, holes are supplied into the channel region **14** from the p-type semiconductor region **13**, and the TFT characteristics are prevented from being deteriorated.

Embodiment 3

[0047] **FIG. 7** is a schematic sectional view of an SOI-MOSFET according to the present invention. **FIG. 7** corresponds to **FIG. 2** and **FIG. 6**, and in which are appearing a drain **12** and a p-type semiconductor region **13** in a semiconductor film **17**. An insulating layer **19** is formed on a

semiconductor substrate **18**, and the semiconductor film **17** which is the first layer is formed on the insulating layer **19**. The semiconductor film **17** is formed by, for example, single crystalline silicon or a single crystal of gallium-arsenic. The semiconductor film **17** is constituted by a source and a drain **12** which are n-type semiconductor regions, a p-type semiconductor region **13**, and a channel region **14** which is an intrinsic semiconductor region just under the gate. A second layer is a gate insulating film **15** which insulates the gate **16** and the semiconductor film **10** from each other. A third layer is the gate **16** having the same shape as the gate insulating film **15**. Upon applying a positive voltage to the gate **16**, an inverted layer in which the electrons are present in an excess amount is formed in the channel region **14** thereby to form a channel, whereby the source and the drain **12** are rendered conductive relative to each other to obtain a switching operation. In the SOI-MOSFET structure of this embodiment, holes induced on the surface due to a gate-negative pulse are further supplied from the p-type semiconductor region **13**. The holes supplied from the p-type semiconductor region **13** relax the electric field established by the gate-negative pulse. Therefore, fewer hot holes are injected into the gate-insulating film **15**, and the SOI-MOSFET characteristics are less deteriorated.

Embodiment 4

[**0048**] Described below is an embodiment in which an active matrix circuit and a peripheral circuit in the liquid crystal display device are fabricated by using n-channel FETs of the present invention.

[**0049**] **FIG. 8** is a plan view illustrating a unit pixel in the liquid crystal display device constituted by using the n-channel TFT of the present invention. A scanning electrode **22** and the gate of a TFT **20** of the present invention are connected together through a hole **21***a*, a signal electrode **23** and the drain of the TFT **20** of the present invention are connected together through a hole **21***b*, and a pixel electrode **24** and the source of the TFT **20** of the present invention are connected together through a hole **21***c*. The TFT **20** is turned on when a selection signal is input to the scanning electrode **22** and a voltage is applied to the gate of the TFT **20**. A video signal voltage is input to the signal electrode.**23** while the TFT **20** is turned on, and is transmitted from the drain of the TFT **20** to the source thereof and is applied to the pixel electrode **24** to drive the liquid crystal. By using the TFT **20** of the present invention as a pixel drive element, a drive waveform of a gate-negative pulse can be input to the pixel.

[**0050**] **FIG. 9** is a plan view of an analog switch constituted by using the n-channel TFT of the present invention. This is a constitution in which the drain of the n-channel TFT **20** of the present invention and the drain of the p-channel TFT **25** are connected together through a wiring electrode **26***a* to form Vin, the source of the n-channel TFT **20** of the present invention and the source of the p-channel TFT **25** are connected together through a wiring electrode **26***b* to form Vout, and clocks having phases different by 180 degrees from each other are applied to the gate of the n-channel TFT **20** of the present invention and to the gate of the p-channel TFT **25**. This is a switching circuit in which a signal input to Vin is directly transmitted to Vout when the clock is assuming "H" and a signal input to Vin is interrupted when the clock is assuming "L". In this circuit, a gate-negative pulse mode is applied to the n-channel TFT **20** of the present invention when Vin and Vout are assuming "H". Even in such a case, the n-channel TFT **20** of the present invention is not deteriorated unlike the conventional n-channel TFT, and a stable analog switch can be constituted.

[**0051**] **FIG. 10** is a diagram illustrating one stage of a static shift register circuit constituted by using the n-channel TFTs of the present invention. One stage of the static shift register is constituted by four analog switches **61**, **62**, **63**, **64**, four inverters **65**, **66**, **67**, **68**, and power source lines V_{DD} and V_{SS} for supplying electric power to the inverters. One stage of the shift register works to delay a pulse wave input to Vin by one clock and to send it to Vout and to the signal. The analog switches shown in **FIG. 9** are used as the analog switches **61** to **64**. In particular, a gate-negative pulse mode is frequently applied to the n-channel TFT **20** that constitutes the analog switch **62** in **FIG. 10**. Even in such a case, however, the n-channel TFT **20** of the present invention is not deteriorated unlike the conventional TFT, and a stable static shift register is realized.

[**0052**] **FIG. 11** is a block diagram illustrating a peripheral circuit and an active matrix circuit in the liquid crystal display device constituted by using the n-channel TFTs of the present invention. A gate driver works to successively select the scanning electrodes connected to the gates of the unit pixel TFTs constituting the active matrix. The gate driver is constituted chiefly by the shift register. On the other hand, the source driver works to supply a signal voltage to the pixel electrodes that constitute the active matrix circuit and is chiefly constituted by the shift register and the analog switch. By constituting the source driver and the gate driver by using at least the n-channel TFTs of the present invention, it is made possible to constitute a peripheral circuit and an active matrix circuit which are highly reliable.

[**0053**] **FIG. 12** is a schematic sectional view of the liquid crystal display device of the present invention. Liquid crystals **27** are sandwiched between the lower glass substrate **100** including the active matrix circuit and an upper opposing glass substrate **200**. Though not diagramed, scanning electrodes and signal electrodes **23** are formed like a matrix on the glass substrate **100** that includes the active matrix circuit, and a pixel electrode **24** is driven via an n-channel TFT **20** of the present invention formed near an intersecting point thereof. Here, an interlayer insulating film **31** maintains the electric insulation between the pixel electrode and the TFT of the present invention and among the electrodes. On the opposing glass substrate **200** are formed a color filter **30** and a light-shielding film **29** that forms a black matrix pattern for shielding the light. The liquid crystals are in contact with an orientation film **28** so as to possess tilted angles.

[**0054**] **FIG. 13** is a circuit diagram of a basic 6-bit DA converter for converting a digital signal into an analog signal when a video signal is, for example, a digital signal. Six-bit digital signals D**0** to D**5** that are input are analyzed by a decoder, and the voltages are applied by the analog switches A**0** to A**63** to the resistors R**0** to R**63** so as to be converted into analog voltage signals and are output to Vout. By using the TFTs of the present invention as the n-channel TFTs to constitute the analog switches A**0** to A**63**, it is allowed to highly enhance the reliability of the analog switches.

[**0055**] **FIG. 14** is a diagram illustrating a unit cell in a static random access memory (SRAM) when the liquid

crystal display device is equipped with, for example, a memory that is simply constituted by using n-channel TFTs and p-channel TFTs. The circuit itself is constituted in a customary manner. When a word line (WL) is selected to assume the "H" level, the data of a bit line (BL) is stored in the SRAM. Here, by using the TFTs of the present invention as the n-channel TFTs, it is allowed to realize the SRAM having high reliability.

[0056] According to the present invention, the n-channel TFT has the p-type semiconductor region which is in contact with the channel region. Therefore, the TFT is less deteriorated in the gate-negative pulse mode, and the reliability is improved. According to the TFT of the present invention having the p-type semiconductor region in contact with the channel region, furthermore, the TFT is less deteriorated in the gate-negative pulse mode, making it possible to obtain a liquid crystal display device featuring improved reliability.

[0057] In **FIG. 1**:

[0058] **13**—p-type semiconductor region

[0059] **14**—channel portion (intrinsic semiconductor region)

[0060] **10**—thin polysilicon film

[0061] **12**—drain (n-type semiconductor region)

[0062] **16**—gate

[0063] **11**—source (n-type semiconductor region)

[0064] In **FIG. 2**:

[0065] **16**—gate **15**—gate insulating film

[0066] **12**—drain **100**—glass substrate

[0067] **13**—p-type semiconductor region

[0068] In **FIG. 3**:

[0069] **10**—thin polysilicon film **100**—glass substrate

[0070] **12**—drain **13**—p-type semiconductor region

[0071] In **FIG. 4**:

[0072] **1**—conventional TFT **2**—TFT of the present invention

[0073] **3**—Number of pulses

[0074] In **FIG. 5**:

[0075] **13**—p-type semiconductor region

[0076] **10**—thin polysilicon film **12**—drain

[0077] **50**—channel protection film **16**—gate

[0078] **14**—channel region **11**—source

[0079] In **FIG. 6**:

[0080] **50**—channel protection film

[0081] **14**—channel region **12**—drain

[0082] **17**—semiconductor film **100**—glass substrate

[0083] **13**—p-type semiconductor region **16**—gate

[0084] **15**—gate insulating film

[0085] In **FIG. 7**:

[0086] **16**—gate **15**—gate insulating film

[0087] **17**—semiconductor film **12**—drain

[0088] **19**—insulating layer **18**—semiconductor substrate

[0089] **13**—p-type semiconductor region

[0090] In **FIG. 8**:

[0091] **23**—signal electrode **20**—TFT of the present invention

[0092] **22**—scanning electrode **21***c*—through hole

[0093] **24**—pixel electrode

[0094] In **FIG. 9**:

[0095] **25**—p-channel type TFT

[0096] **20**—TFT of the present invention

[0097] In **FIG. 10**:

[0098] **1**—signal

[0099] In **FIG. 11**:

[0100] **1**—video signal **2**—source driver

[0101] **3**—shift register X **4**—analog switch

[0102] **5**—pixel TFT **6**—liquid crystals

[0103] **7**—active matrix circuit **8**—gate driver

[0104] **9**—shift register Y

[0105] In **FIG. 12**:

[0106] **20**—TFT of the present invention

[0107] In **FIG. 13**:

[0108] **1**—reference potential

What is claimed is:

1. A static random access memory comprising a plurality of word lines, a plurality of data lines and a plurality of memory cells respectively located at intersections of said word lines and said data lines, wherein each of said memory cells includes an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising a semiconductor thin film formed on an insulating substrate and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except said channel region.

2. A static random access memory according to claim 1, wherein said semiconductor thin film is formed of polysilicon.

3. A static random access memory comprising a plurality of word lines, a plurality of data lines and a plurality of memory cells respectively located at intersections of said word lines and said data lines, wherein each of said memory cells includes an n-channel insulated gate thin-film transistor

using electrons as a main current carrier and comprising a gate electrode formed on an insulating substrate and a semiconductor thin film formed on said gate electrode via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just over the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with sad channel region, and said p-type semiconductor region is electrically connected to nowhere except said channel region.

4. A static random access memory comprising a plurality of word lines, a plurality of data lines and a plurality of memory cells respectively located at intersections of said word lines and said data lines, wherein each of said memory cells includes an n-channel insulated gate thin-film transistor using electrons as a main current carrier and comprising an insulating film formed on a semiconductor substrate, a semiconductor thin film formed on said insulating layer and a gate electrode formed on said semiconductor thin film via a gate insulating film, said semiconductor thin film having a source region and a drain region which are n-type semiconductor regions formed therein sandwiching a channel region which is an intrinsic semiconductor region just under the gate electrode, wherein said semiconductor thin film has a p-type semiconductor region in contact with the channel region, and said p-type semiconductor region is electrically connected to nowhere except said channel region.

* * * * *

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摘要(译)

为了防止n沟道薄膜晶体管被栅极负脉冲模式中产生的热空穴劣化。薄的多晶硅膜10设置有与沟道区14接触的p型半导体区13.除了沟道区14之外，p型半导体区13电连接到任何地方。由于栅极而在表面上引起的孔从p型半导体区域13进一步提供负脉冲。由栅极负脉冲建立的电场被空穴放松，较少的热空穴注入到栅极氧化膜中，并且TFT特性较少劣化。