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(54) LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING METHOD OF THE SAME

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(57) ABSTRACT

A driving method of a liquid crystal display device, even when a vertical retrace interval varies, can prevent contention between a driving signal transmitted to a driving circuit within the vertical retrace interval and a driving signal transmitted to the driving circuit within the display period of the next frame after the vertical retrace interval. The device has pixels, signal lines, and a driving circuit outputting the gray scale voltage to the signal lines. In the method, letting M be a value obtained by dividing the vertical retrace interval by a regular horizontal scanning time and rounding up a fraction after the decimal point, and letting N be an integer of 1 or more, the gray scale voltage is outputted from the driving circuit to the signal lines by a number of times between twice and (M−N) times within the vertical retrace interval.

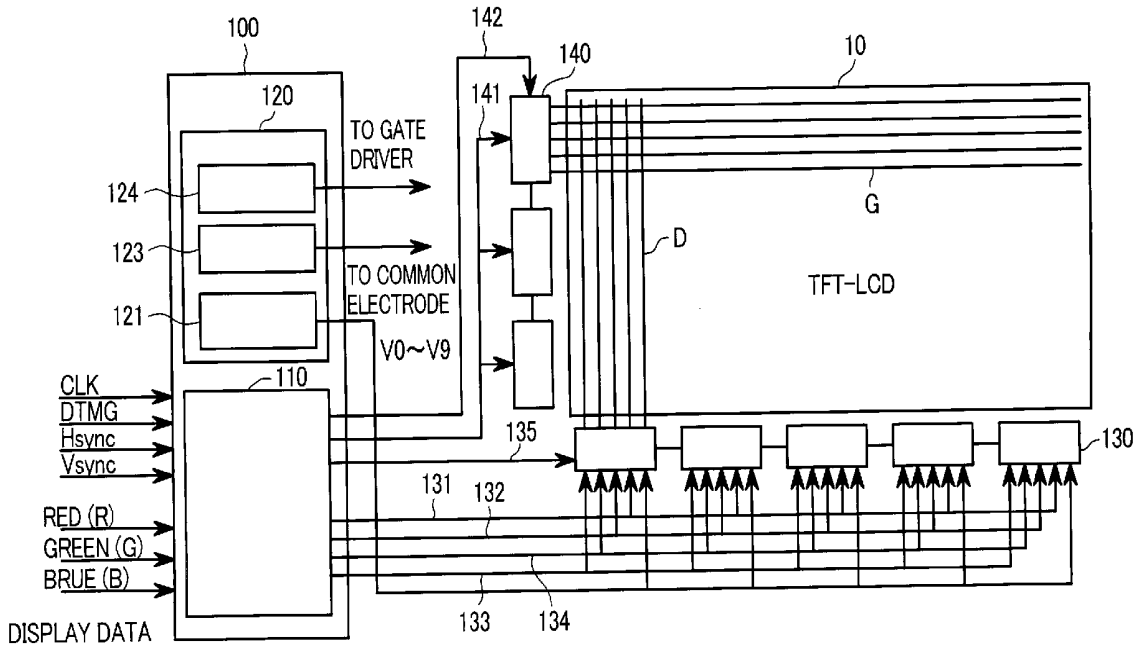


FIG. 1

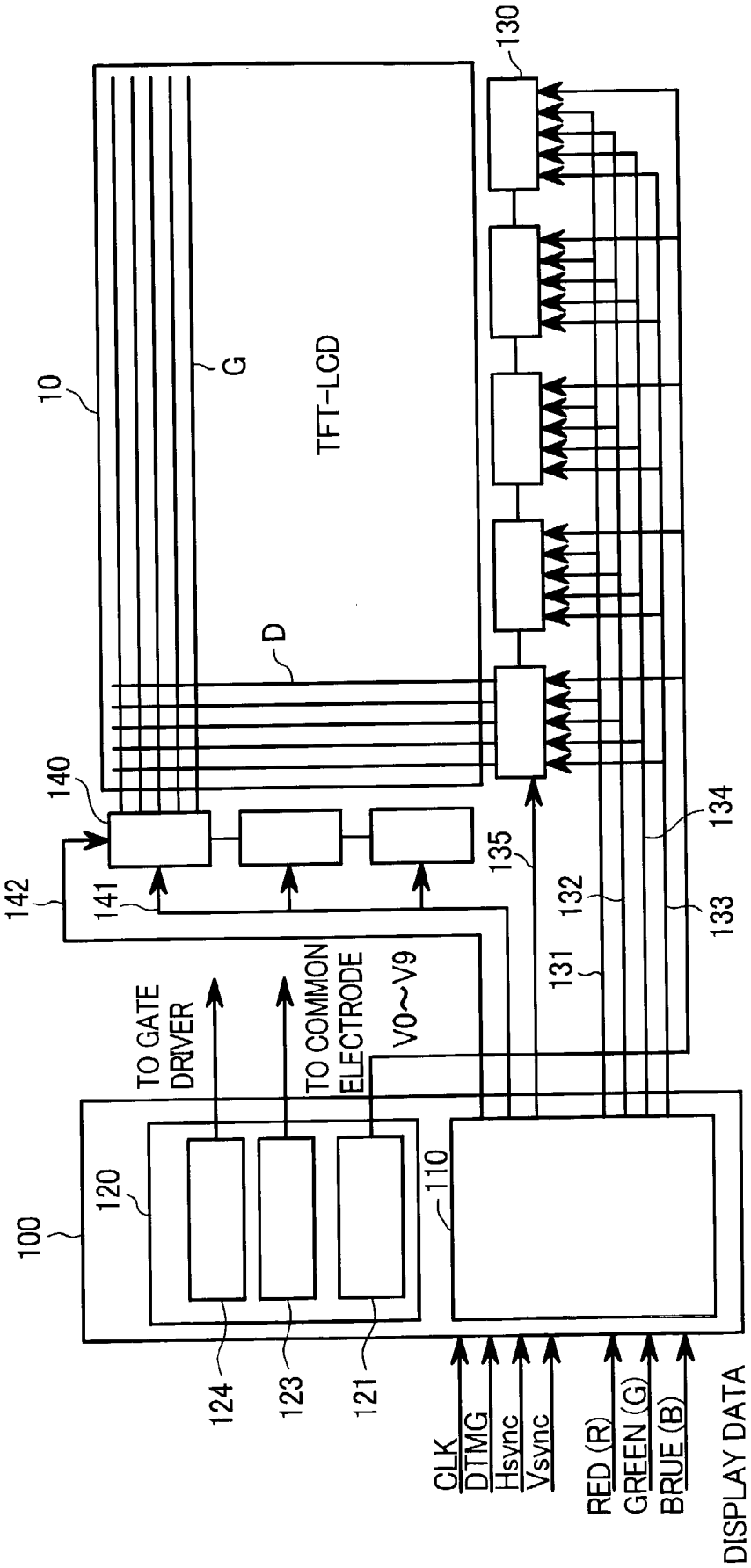

10
G
TFT-LCD
D
130
140
142
141
135
134
132
133
131
TO GATE DRIVER
TO COMMON ELECTRODE
V0~V9
100
120
110
124
123
121
CLK
DTMG
Hsync
Vsync
RED (R)
GREEN (G)
BRUE (B)
DISPLAY DATA

FIG. 2

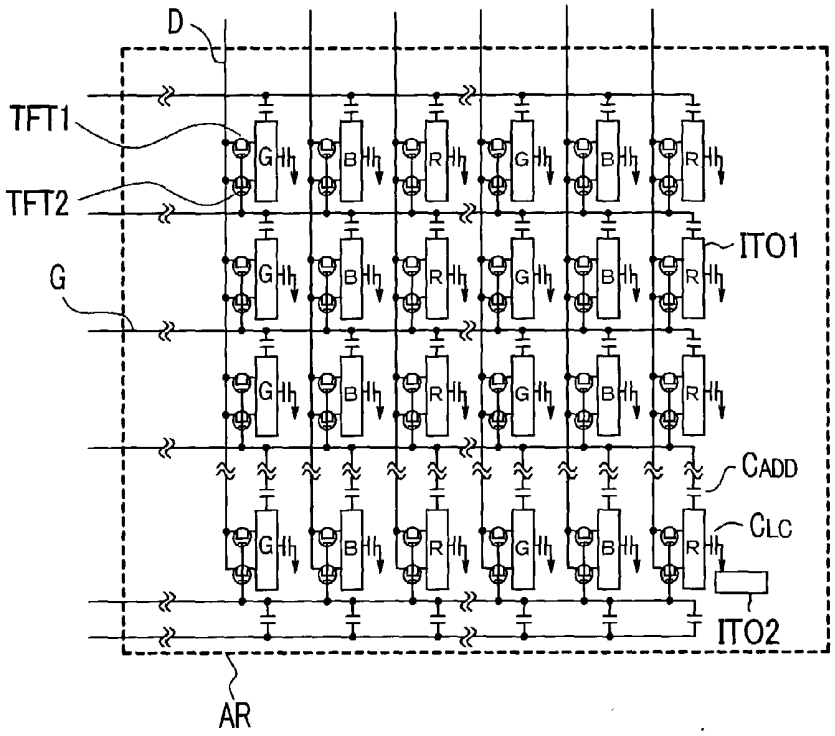

D
TFT1
TFT2
G
ITO1
CADD
CLC
ITO2
AR

FIG. 3

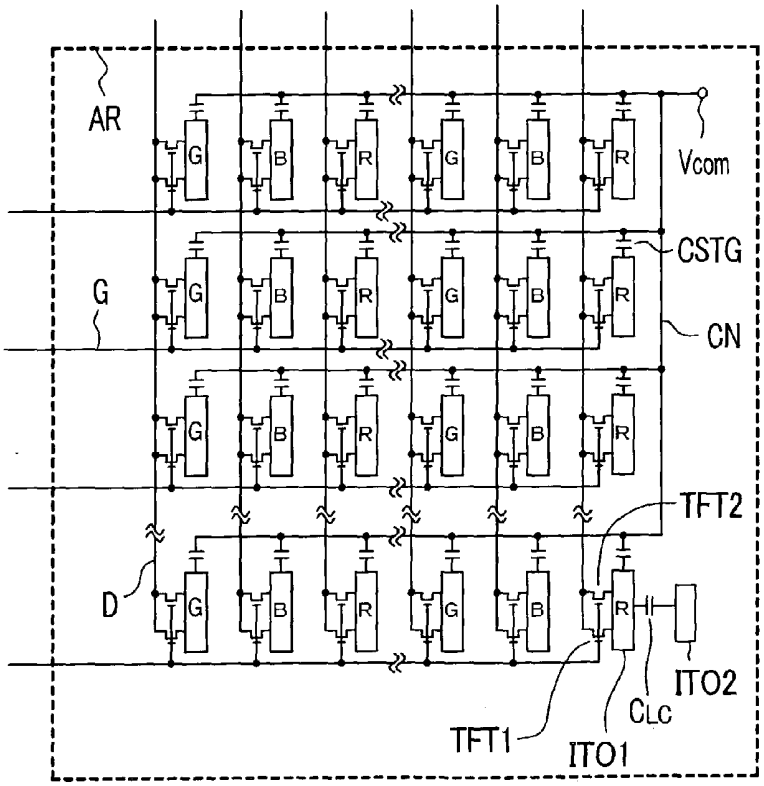

AR
G
D
Vcom
CSTG
CN
TFT2
ITO2
CLC
TFT1
ITO1

FIG. 4

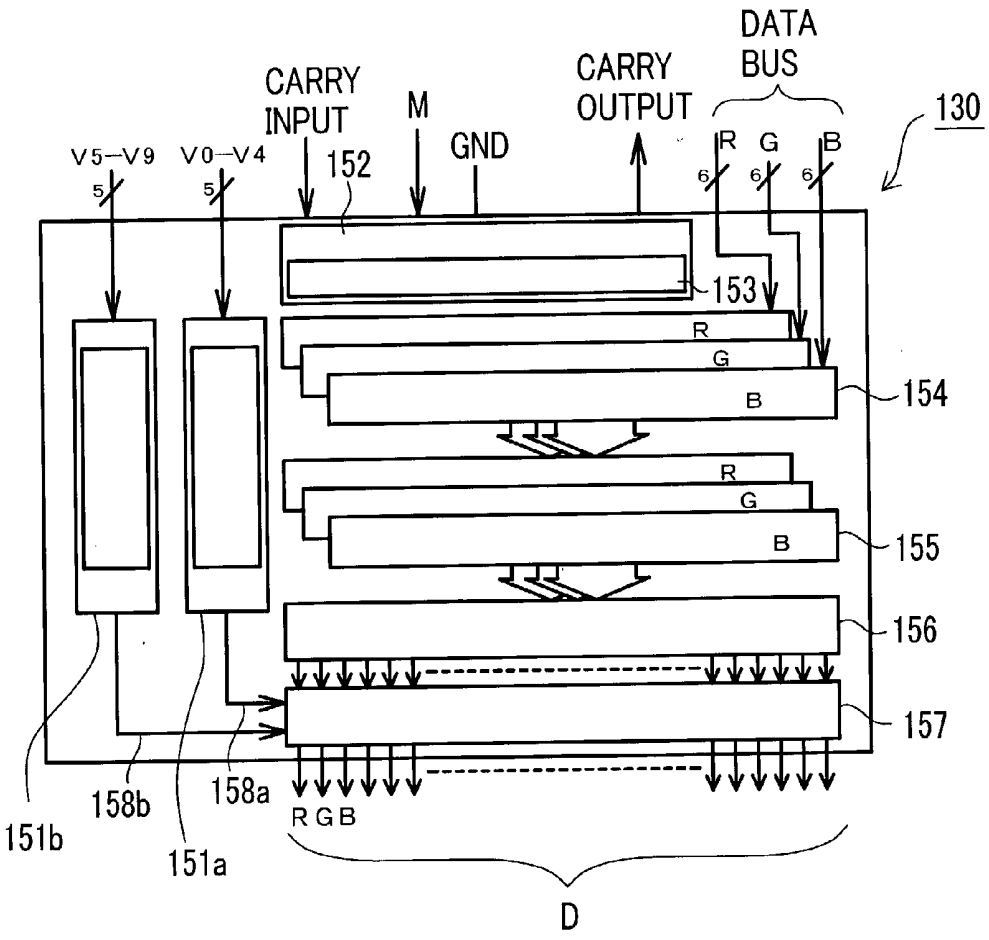

DATA
BUS
CARRY
INPUT
M
CARRY
OUTPUT
130
V5—V9
V0—V4
GND
152
R G B
153
154
155
156
157
158b
158a
151b
151a
RGB
D

FIG. 5

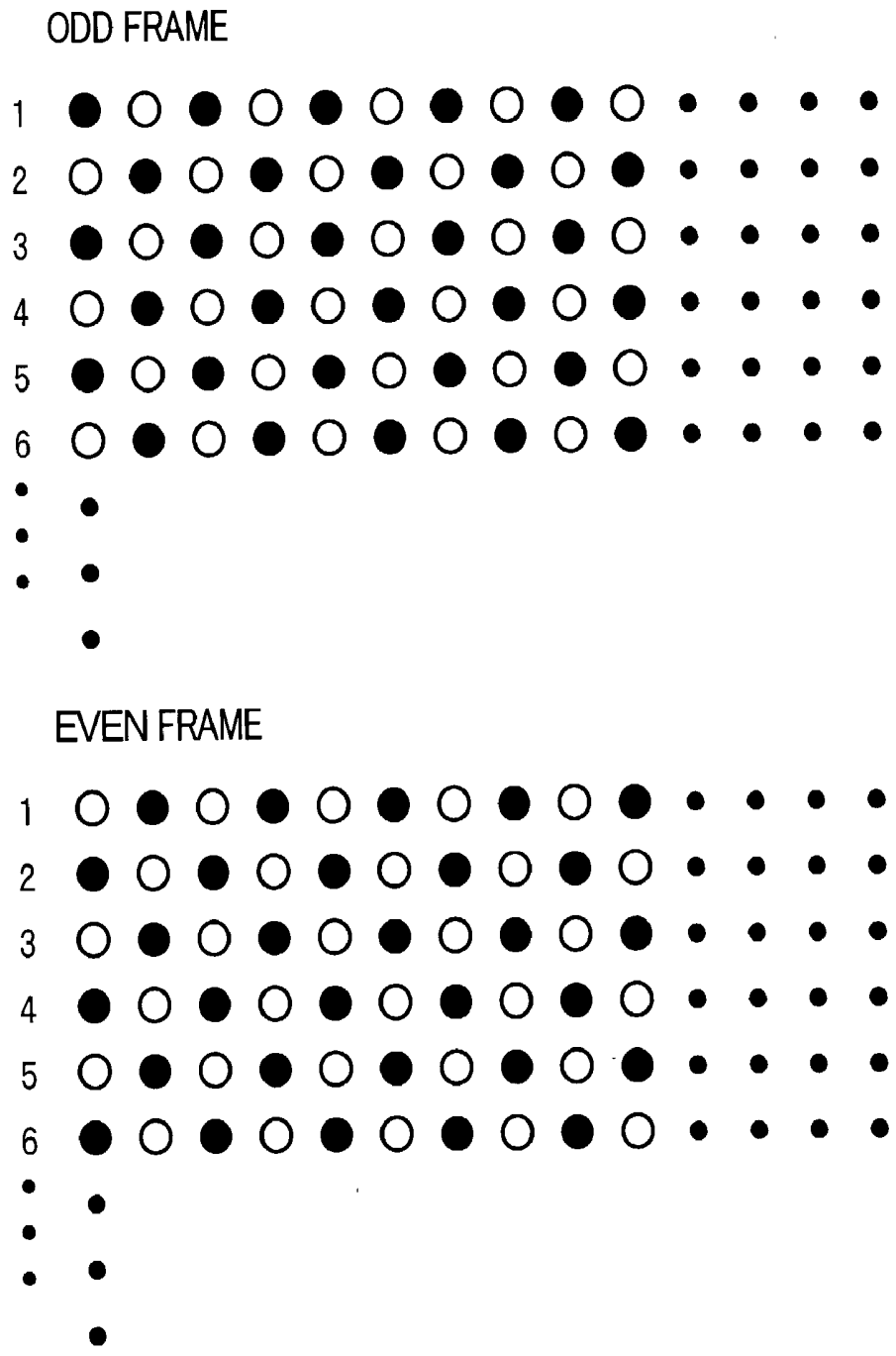
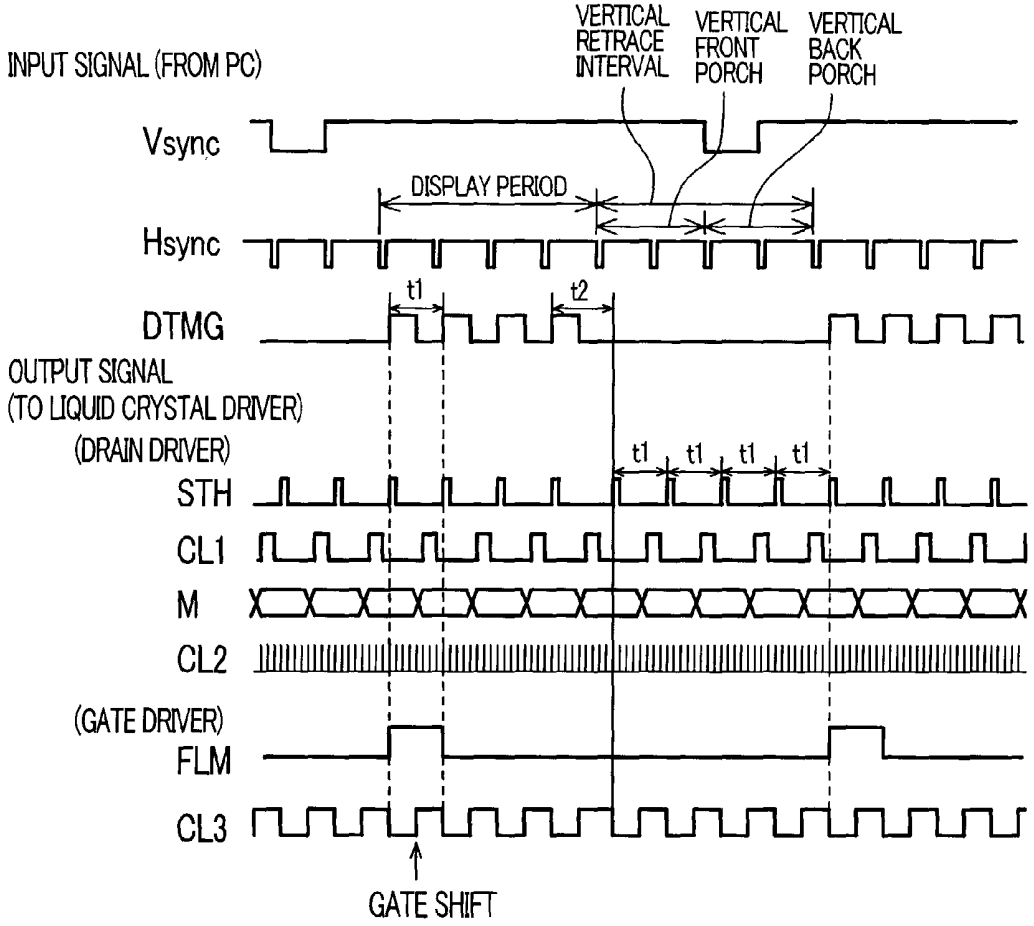


FIG. 6




SEQUENCE OF THE LIQUID CRYSTAL DIRVER (EXAMPLE)

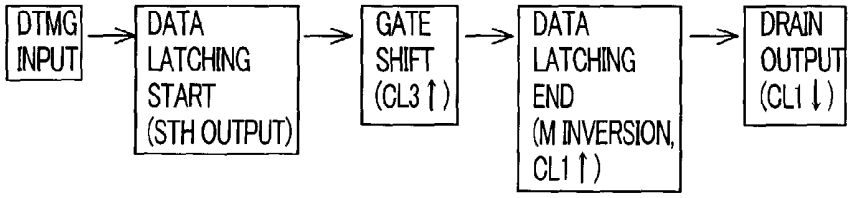


FIG. 7

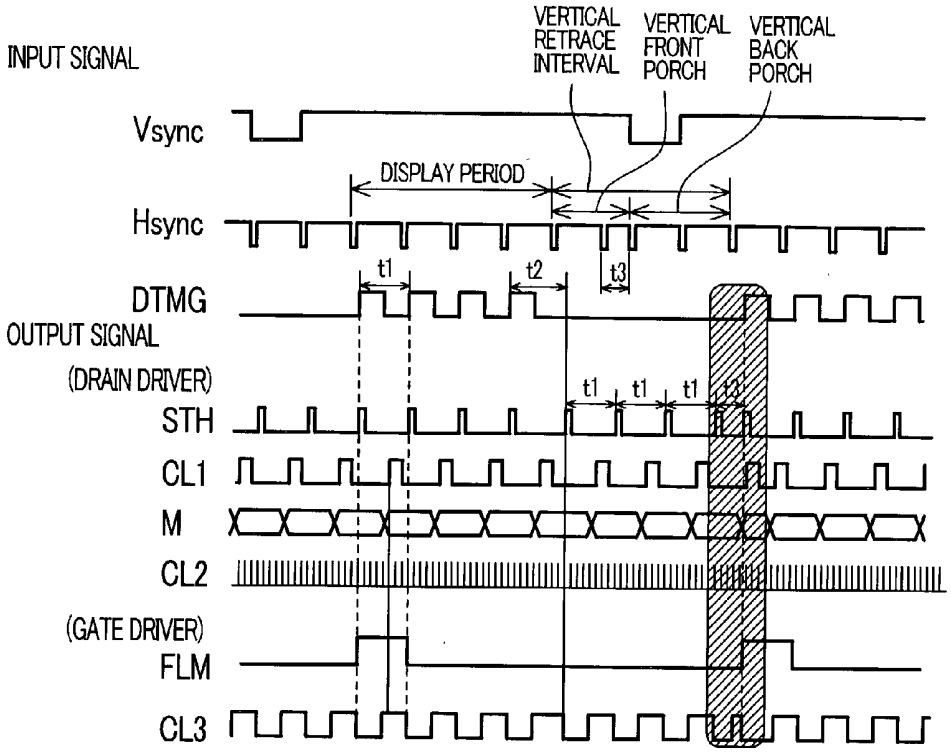

INPUT SIGNAL
VERTICAL RETRACE INTERVAL
VERTICAL FRONT PORCH
VERTICAL BACK PORCH
Vsync
DISPLAY PERIOD
Hsync
t1
t2
t3
DTMG
OUTPUT SIGNAL
(DRAIN DRIVER)
STH
CL1
M
CL2
(GATE DRIVER)
FLM
CL3

FIG. 8

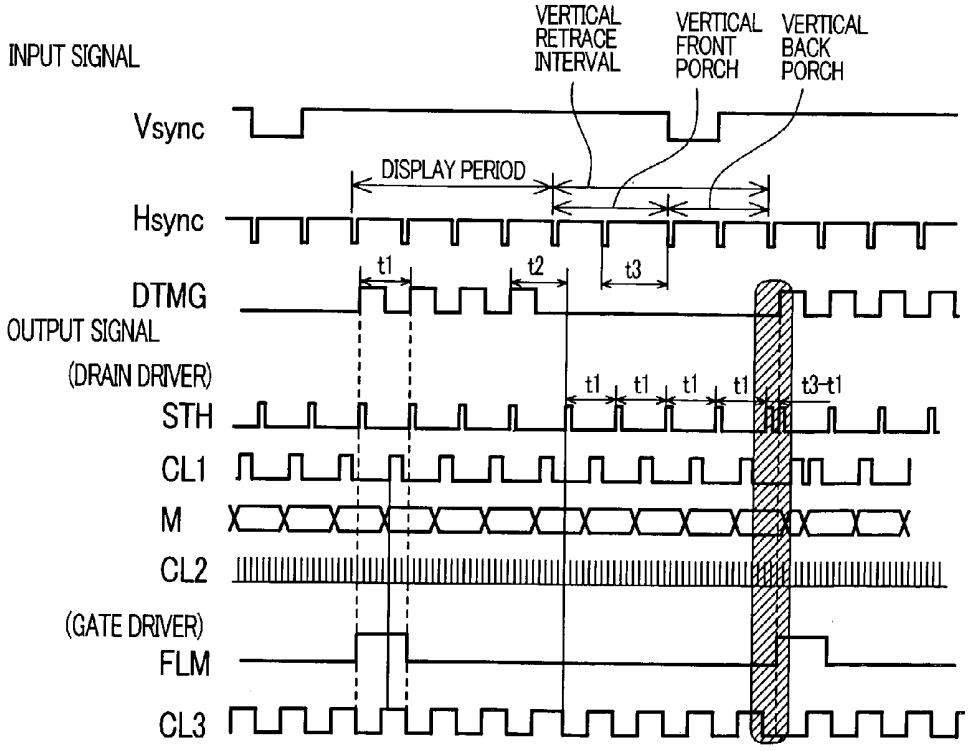

INPUT SIGNAL
VERTICAL RETRACE INTERVAL
VERTICAL FRONT PORCH
VERTICAL BACK PORCH
Vsync
DISPLAY PERIOD
Hsync
t1
t2
t3
DTMG
OUTPUT SIGNAL
(DRAIN DRIVER)
t3-t1
STH
CL1
M
CL2
(GATE DRIVER)
FLM
CL3

FIG. 9

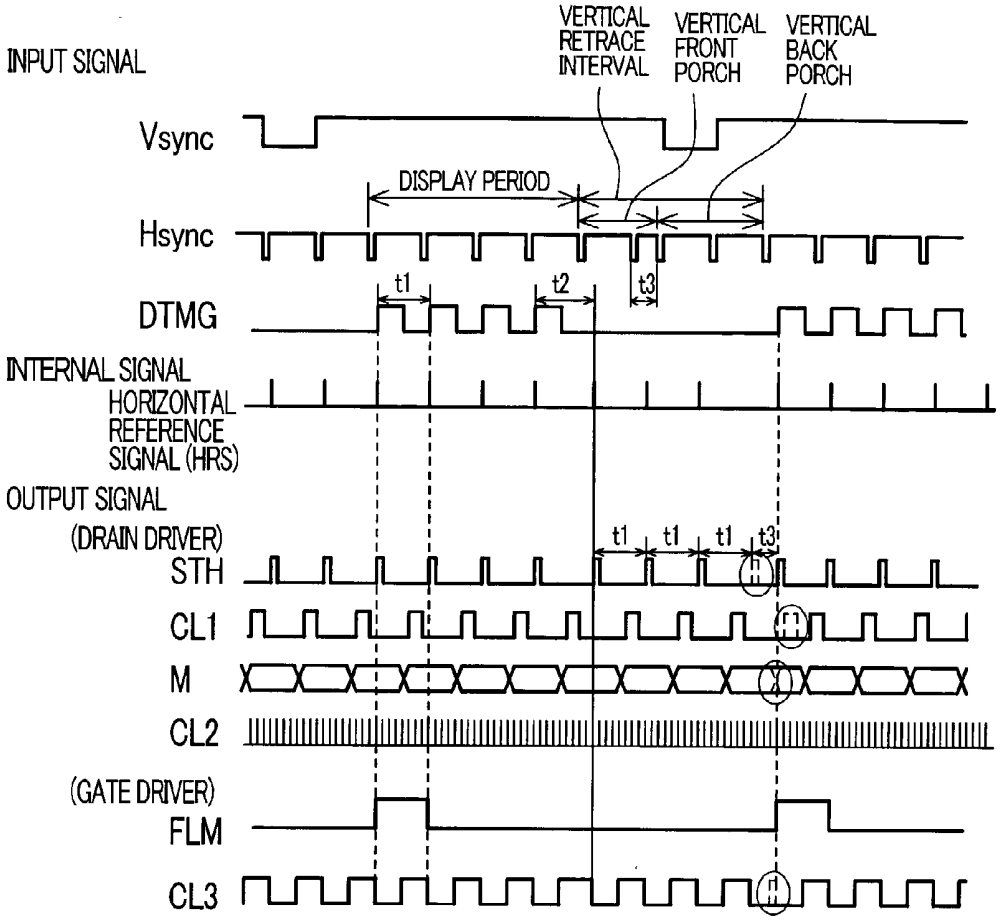

INPUT SIGNAL
VERTICAL RETRACE INTERVAL
VERTICAL FRONT PORCH
VERTICAL BACK PORCH
Vsync
DISPLAY PERIOD
Hsync
t1
t2
t3
DTMG
INTERNAL SIGNAL
HORIZONTAL REFERENCE SIGNAL (HRS)
OUTPUT SIGNAL
(DRAIN DRIVER)
STH
CL1
M
CL2
(GATE DRIVER)
FLM
CL3

FIG. 10

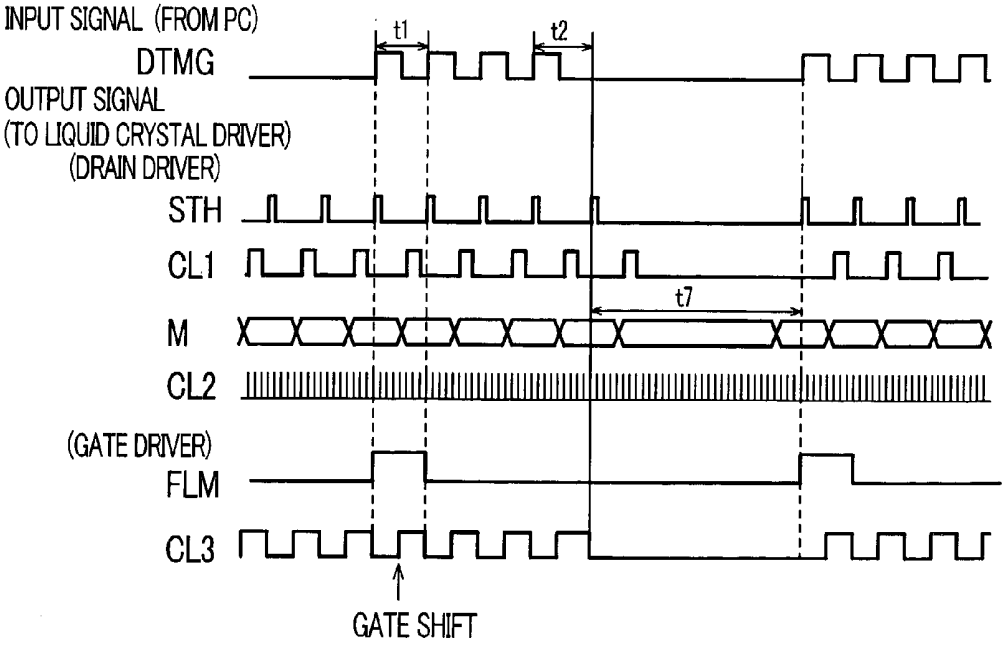

INPUT SIGNAL (FROM PC)
DTMG
t1
t2
OUTPUT SIGNAL
(TO LIQUID CRYSTAL DRIVER)
(DRAIN DRIVER)
STH
CL1
t7
M
CL2
(GATE DRIVER)
FLM
CL3
GATE SHIFT

FIG. 11

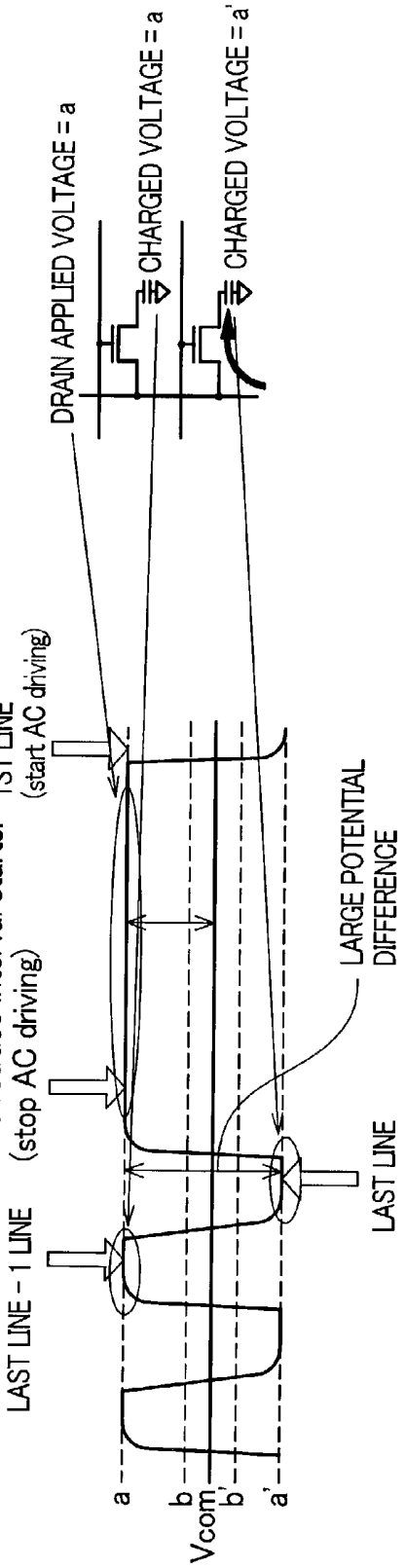

DRAIN APPLIED VOLTAGE = a
CHARGED VOLTAGE = a
CHARGED VOLTAGE = a'
1ST LINE
(start AC driving)
The retrace interval starts.
(stop AC driving)
LAST LINE - 1 LINE
LARGE POTENTIAL
DIFFERENCE
LAST LINE
a
b
Vcom
b'
a'

FIG. 12

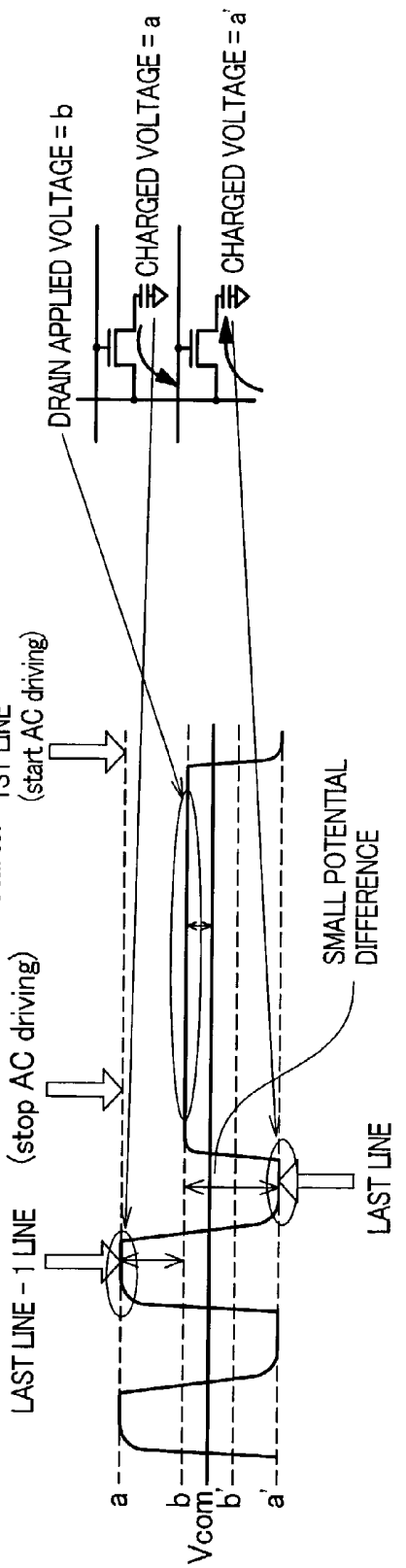

DRAIN APPLIED VOLTAGE = b
CHARGED VOLTAGE = a
CHARGED VOLTAGE = a'
1ST LINE
(start AC driving)
The retrace interval starts.
(stop AC driving)
LAST LINE - 1 LINE
SMALL POTENTIAL
DIFFERENCE
LAST LINE
a
b
Vcom
b'
a'

FIG. 13

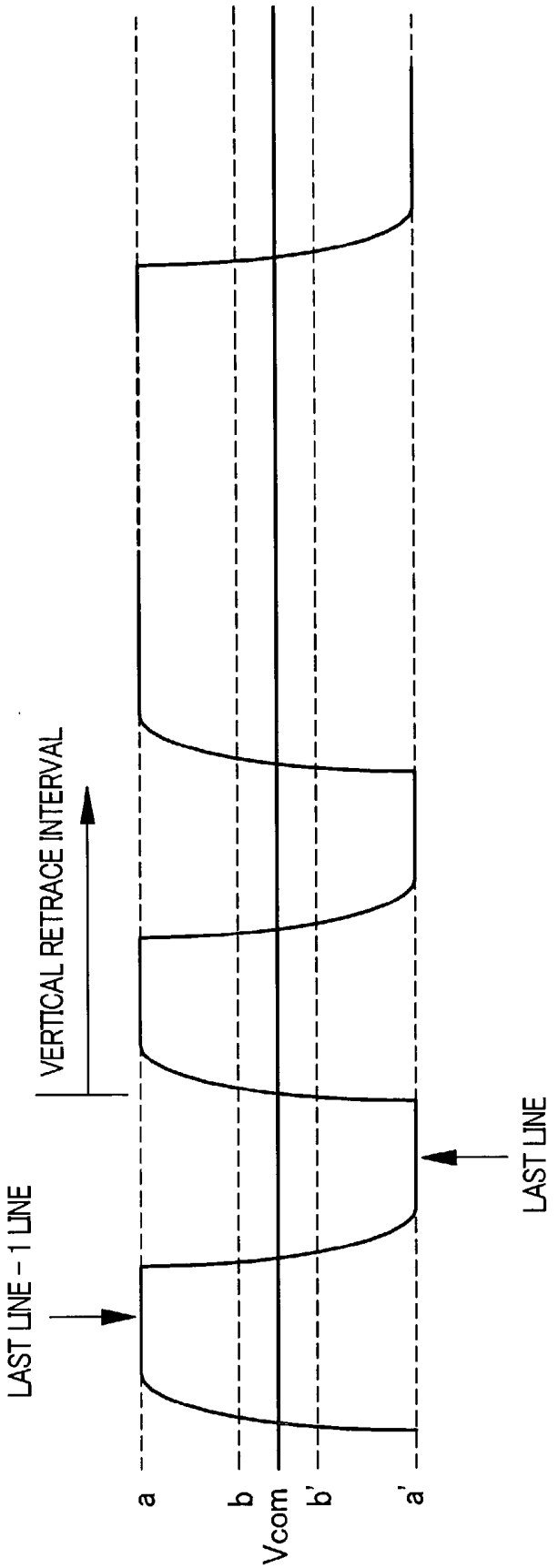

VERTICAL RETRACE INTERVAL
LAST LINE – 1 LINE
LAST LINE
a
b
Vcom
b'
a'

FIG. 14

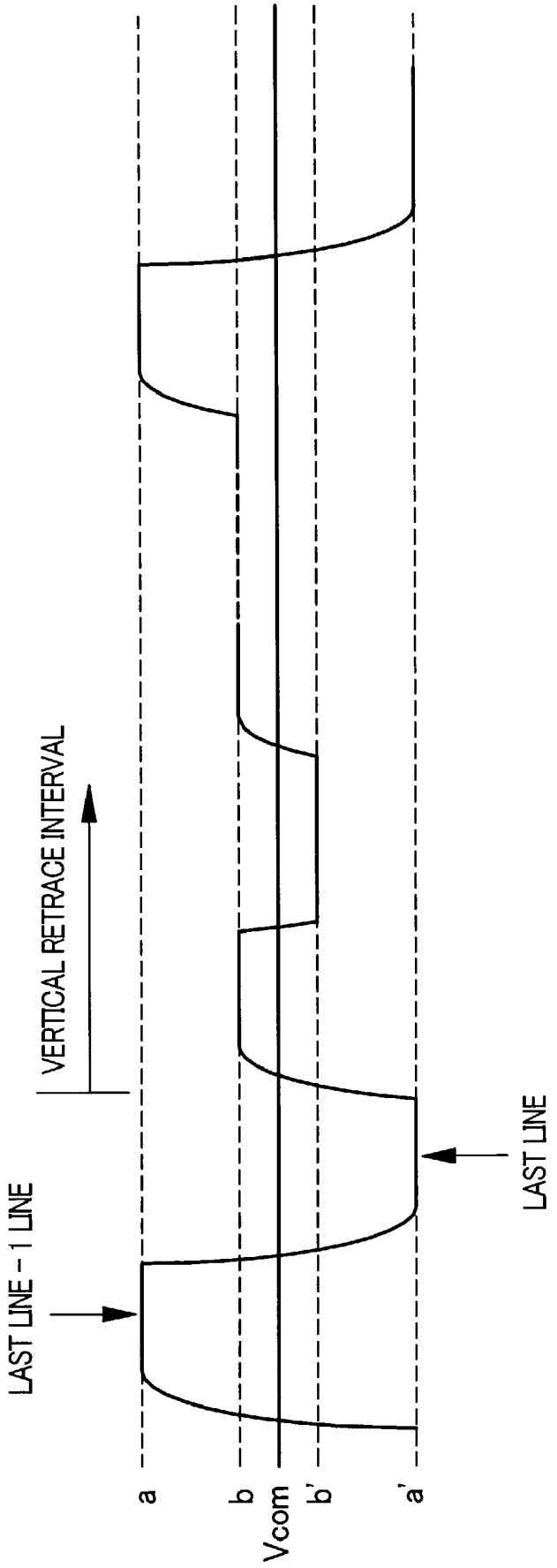

VERTICAL RETRACE INTERVAL
LAST LINE - 1 LINE
LAST LINE
a
b
Vcom
b'
a'

FIG. 15

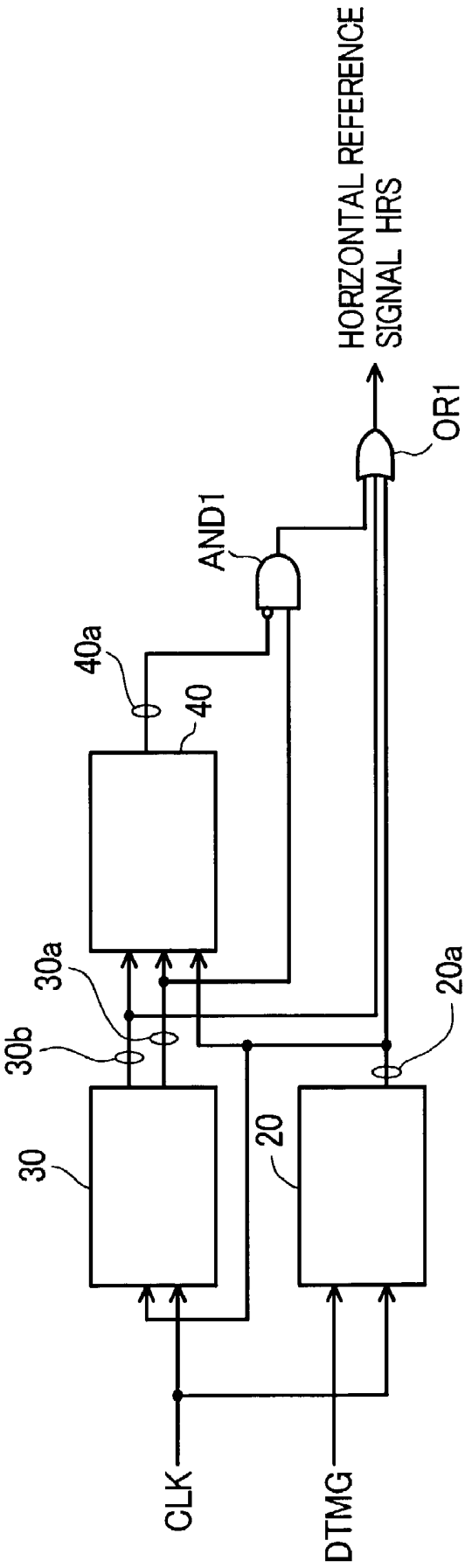

HORIZONTAL REFERENCE SIGNAL HRS
OR1
AND1
40a
40
30a
30b
20a
30
20
CLK
DTMG

FIG. 16

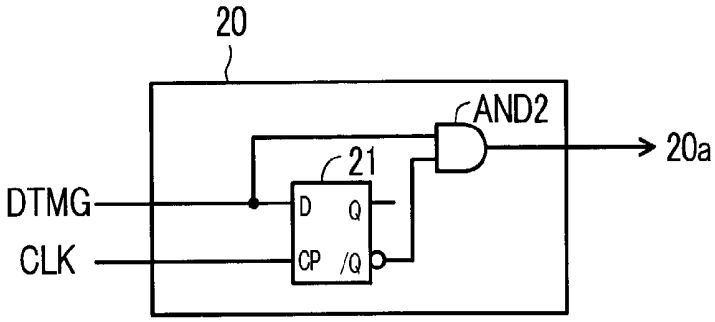

20
AND2
20a
21
DTMG
D
Q
CLK
CP
/Q

FIG. 17

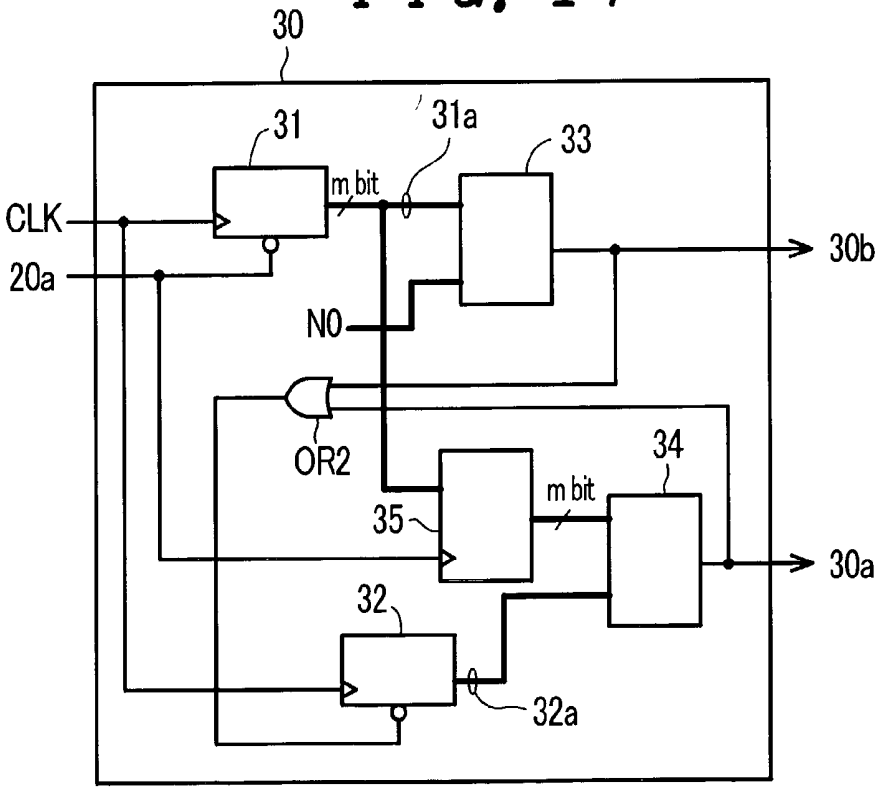

30
31
31a
33
m bit
CLK
20a
30b
N0
OR2
34
m bit
35
30a
32
32a

FIG. 18

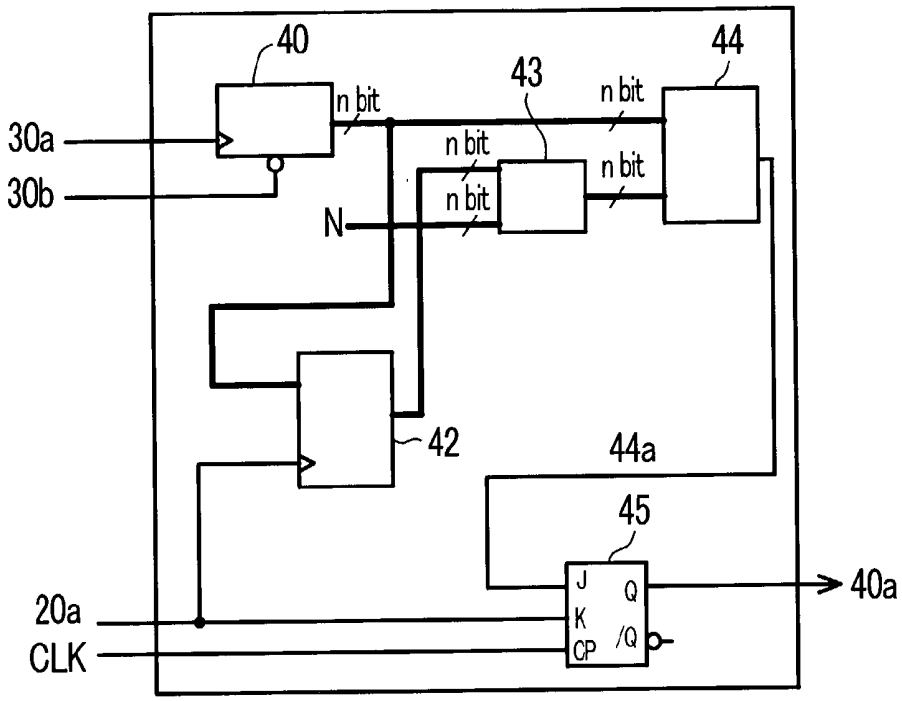

40
44
43
n bit
n bit
30a
30b
n bit
n bit
n bit
N
42
44a
45
J
Q
K
CP
/Q
40a
20a
CLK

FIG. 19

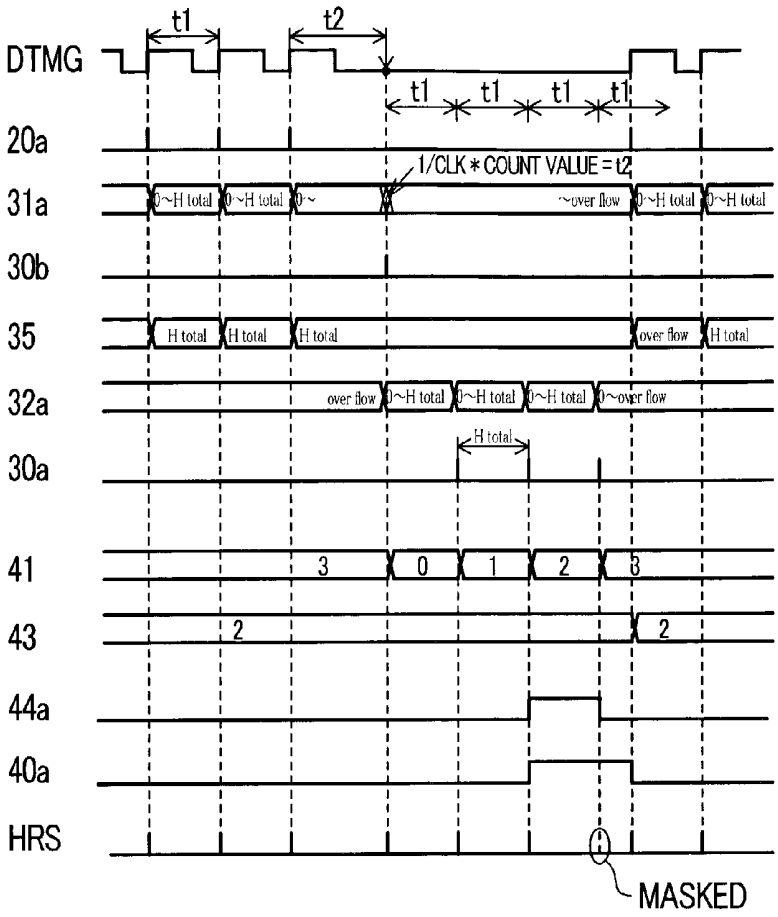

t1
t2
DTMG
t1
t1
t1
t1
20a
1/CLK * COUNT VALUE = t2
31a
0~H total
0~H total
0~
~over flow
0~H total
0~H total
30b
35
H total
H total
H total
over flow
H total
32a
over flow
0~H total
0~H total
0~H total
0~over flow
H total
30a
41
3
0
1
2
3
43
2
2
44a
40a
HRS
MASKED

FIG. 20

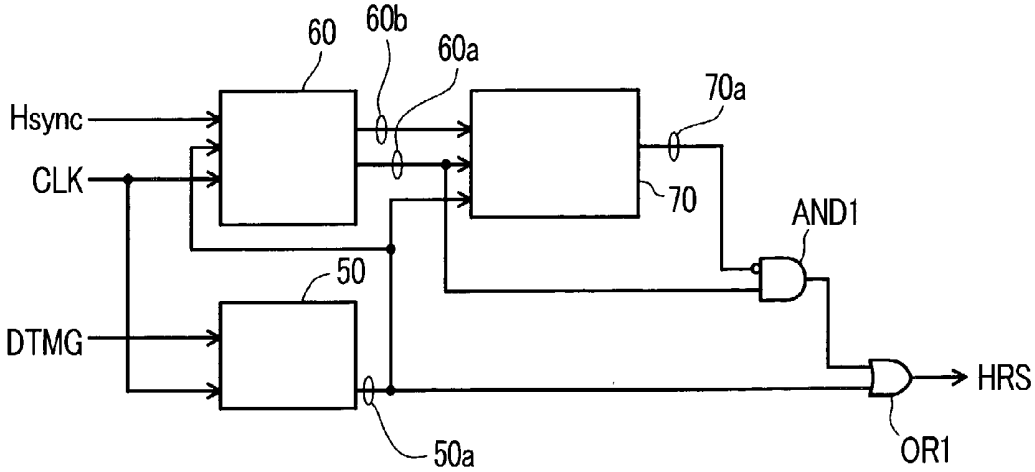

60
60b
60a
70a
Hsync
CLK
70
AND1
50
DTMG
HRS
50a
OR1

FIG. 21

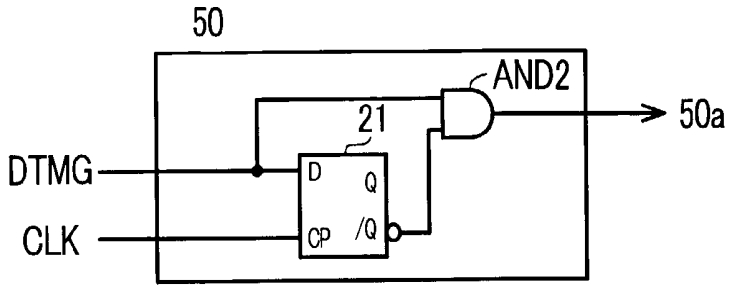

50
AND2
21
50a
DTMG
D
Q
CLK
CP
/Q

FIG. 22

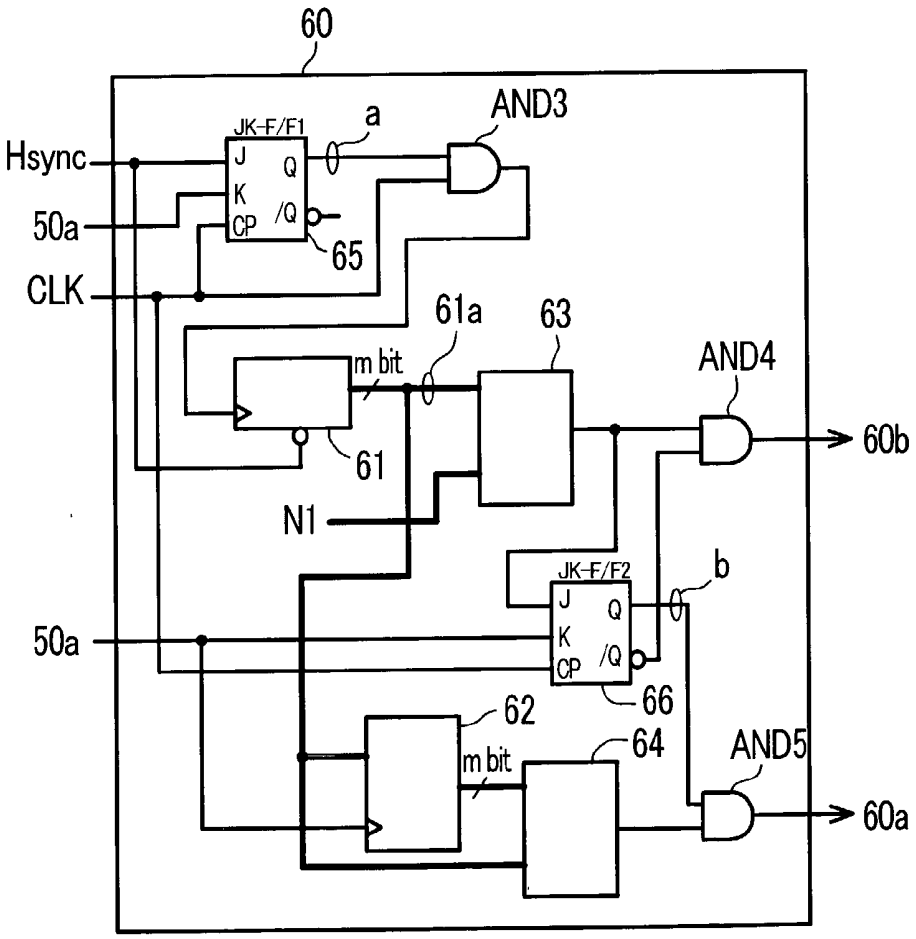

60
JK-F/F1
a
AND3
Hsync
J
Q
50a
K
CP
/Q
65
CLK
61a
63
m bit
AND4
60b
61
N1
JK-F/F2
b
50a
J
Q
K
CP
/Q
66
62
64
AND5
m bit
60a

FIG. 23

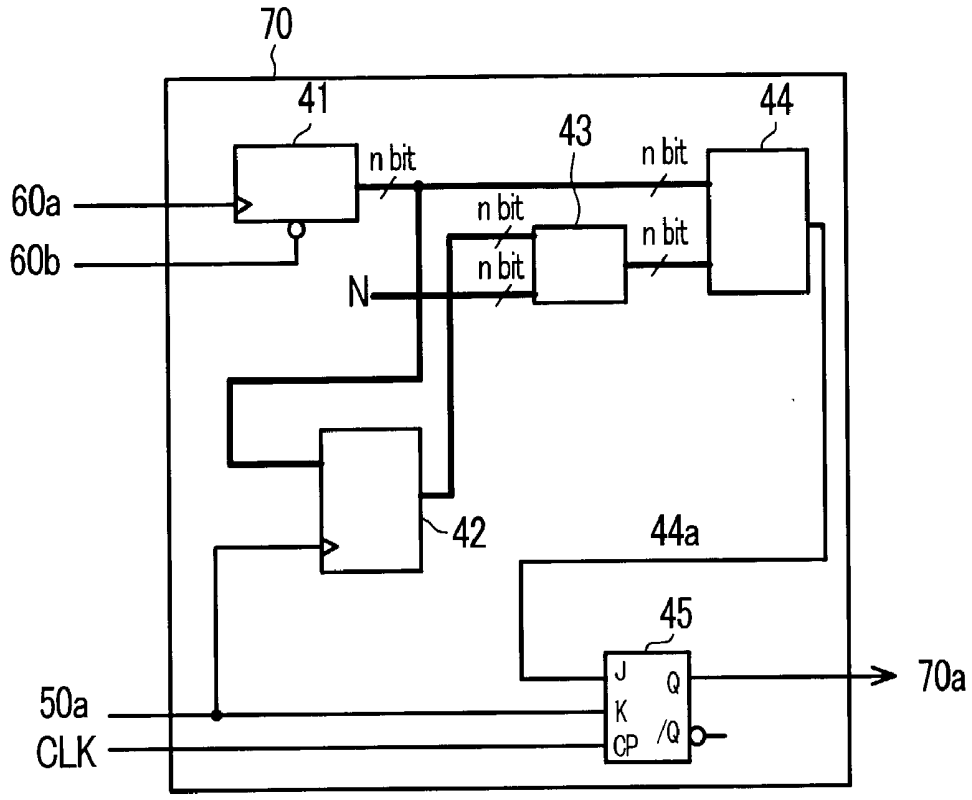

70
41
44
43
n bit
n bit
n bit
n bit
n bit
60a
60b
N
42
44a
45
J
K
CP
Q
/Q
70a
50a
CLK

FIG. 24

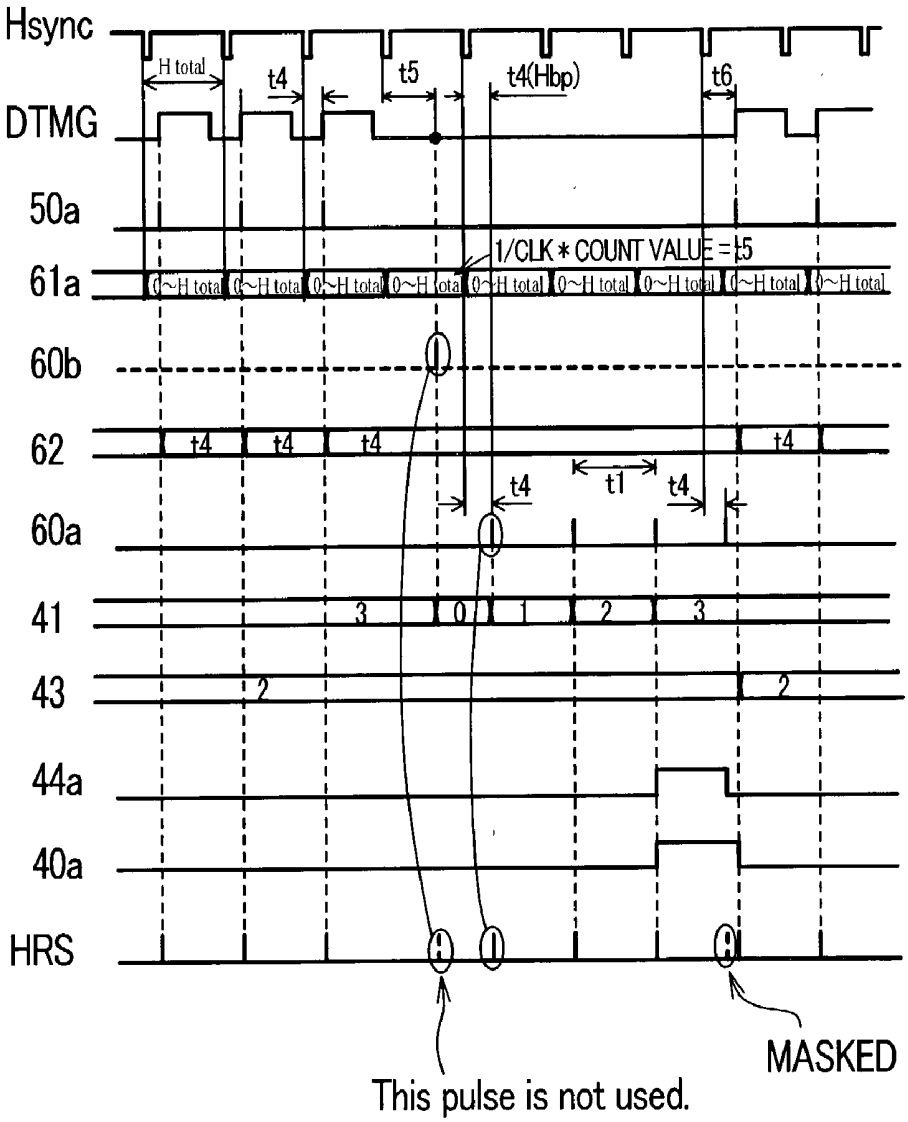
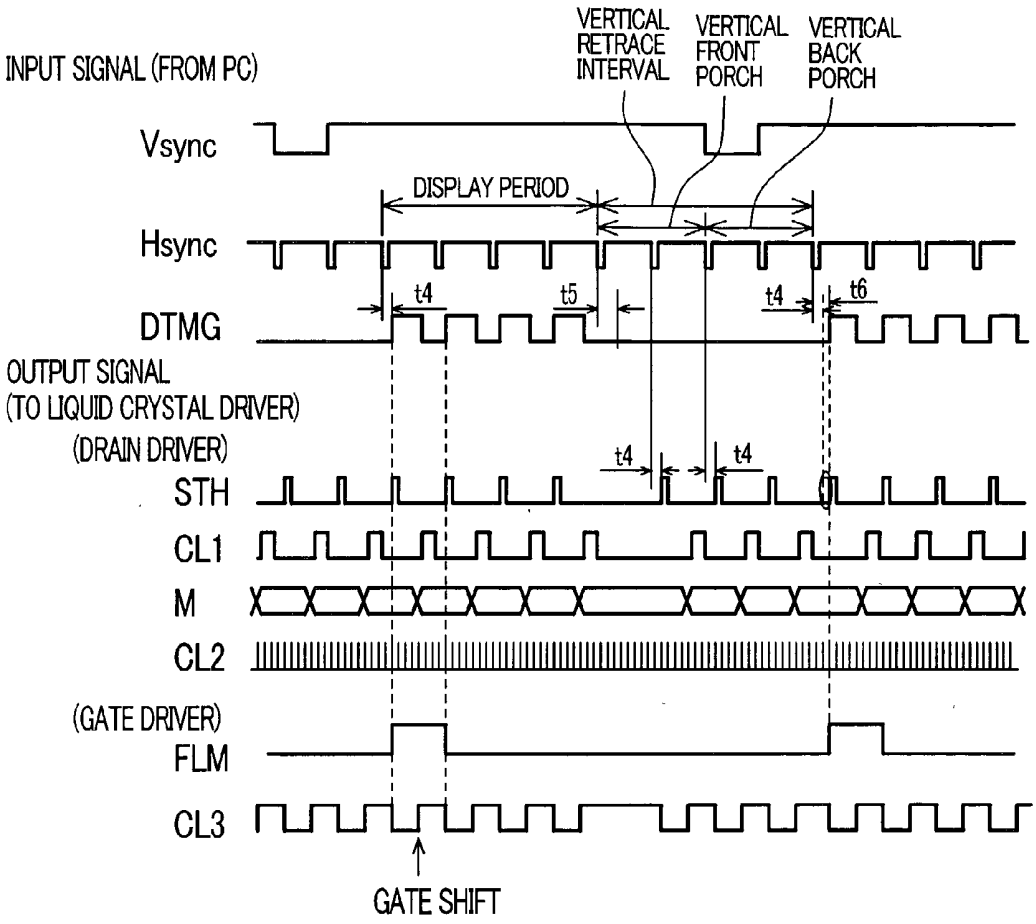

Hsync
DTMG
50a
61a
60b
62
60a
41
43
44a
40a
HRS
H total
t4
t5
t4(Hbp)
t6
1/CLK * COUNT VALUE = t5
0~H total
t1
3
0
1
2
This pulse is not used.
MASKED

FIG. 25


INPUT SIGNAL (FROM PC)
VERTICAL RETRACE INTERVAL
VERTICAL FRONT PORCH
VERTICAL BACK PORCH
Vsync
DISPLAY PERIOD
Hsync
t4
t5
t4
t6
DTMG
OUTPUT SIGNAL
(TO LIQUID CRYSTAL DRIVER)
(DRAIN DRIVER)
t4
t4
STH
CL1
M
CL2
(GATE DRIVER)
FLM
CL3
GATE SHIFT

# LIQUID CRYSTAL DISPLAY DEVICE AND DRIVING METHOD OF THE SAME

## BACKGROUND OF THE INVENTION

[0001] The present invention relates to a liquid crystal display device and a driving method of the same, and more particularly, to an art usefully applicable to a driving method which applies a gray scale voltage to video signal lines within a vertical retrace interval.

[0002] Active matrix liquid crystal display devices which have active elements (for example, thin film transistors) for individual pixels and drive the active elements in a switching manner are widely used as display devices for notebook types of personal computers (hereinafter referred to simply as personal computer(s)).

[0003] A TFT type of liquid crystal display module is known as one kind of active matrix liquid crystal display device. The TFT type of liquid crystal display module includes a TFT (Thin Film Transistor) type of liquid crystal display panel (TFT-LCD), drain drivers disposed on a longer side of the liquid crystal display panel, and gate drivers and an interface part each of which is disposed on a shorter side of the liquid crystal display panel.

[0004] In general, the drain drivers are driven on the basis of driving signals from a display control device (or timing controller) provided in the interface part.

[0005] In the above-described type of liquid crystal display module, the interval from the completion of line scanning in the n-th frame until the start of line scanning in the next (n+1)-th frame is called a vertical retrace interval, and a line scanning period in each frame is called a display period.

[0006] A related art liquid crystal display module is constructed to output a gray scale voltage for displaying white or black from its drain drivers to its drain signal lines at intervals of one line scanning period within the vertical retrace interval so that voltages written in its pixels are prevented from being varied and causing lateral stripes on its display screen owing to leak currents from the thin film transistors of the pixels within the vertical retrace interval.

[0007] Namely, in the related art liquid crystal display module, even within the vertical retrace interval, a driving signal is transmitted from a display control device provided in its interface part to the drain drivers to drive the drain drivers.

[0008] However, if synchronizing signals inputted from the outside (for example, a computer host) vary and the vertical retrace interval varies, contention occurs between a driving signal transmitted from the display control circuit to the drain drivers within the vertical retrace interval and a driving signal transmitted from the display control circuit to the drain drivers within the display period of the next frame after the completion of the vertical retrace interval. This leads to the problem that the drain drivers malfunction and in the worst case, the drain drivers are destroyed.

[0009] The invention has been made to solve the problem of the related art, and provides an art which, even when a vertical retrace interval varies in a liquid crystal display device and a driving method thereof, makes it possible to prevent contention from occurring between a driving signal transmitted from a display control circuit to a driving circuit within the vertical retrace interval and a driving signal transmitted from the display control circuit to the driving circuit within the display period of the next frame after the completion of the vertical retrace interval.

[0010] The invention also provides an art which, in the liquid crystal display device and the driving method thereof, makes it possible to prevent the voltages written in pixels from being varied and causing lateral stripes on its display screen, thereby improving the display quality of the display screen.

[0011] The above and novel features of the invention will become apparent from the following description of the invention when taken in conjunction with the accompanying drawings.

## SUMMARY OF THE INVENTION

[0012] Representative aspects of the invention disclosed in the present application will be described below in brief.

[0013] Namely, the invention provides a liquid crystal display device having a plurality of pixels, a plurality of signal lines which apply a gray scale voltage to each of the pixels, and a driving circuit which outputs the gray scale voltage to each of the signal lines, as well as a driving method of the liquid crystal display device. In the liquid crystal display device and the driving method thereof, the gray scale voltage is outputted from the driving circuit to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within a vertical retrace interval, where M represents a value obtained by dividing the vertical retrace interval by a regular horizontal scanning time and rounding up fractions to the nearest whole number, and N represents an integer not smaller than one.

[0014] According to the invention, the gray scale voltage is outputted from the driving circuit to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within a vertical retrace interval, where M represents a value obtained by adding together the number of lines each having a period scanned entirely and the number of lines each having a period scanned at least partly, when scanning is performed with the regular horizontal scanning time within the vertical retrace interval, and N represents an integer not smaller than one.

[0015] Particularly in the invention, it is preferable that the gray scale voltage be outputted from the driving circuit to each of the signal lines by a number of times not smaller than M/2 times and not greater than (M−N) times within the vertical retrace interval.

[0016] In this case, it is preferable that the gray scale voltage be outputted from the driving circuit to each of the signal lines within the vertical retrace interval in synchronism with a regular horizontal synchronizing signal or an internally generated horizontal reference signal.

[0017] In addition, in the invention, it is preferable that when the gray scale voltage is to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval, the polarity of the gray scale voltage to be outputted be inverted at least once.

[0018] In addition, in the invention, it is preferable that the gray scale voltage to be outputted from the driving circuit to

each of the signal lines within the vertical retrace interval be a gray scale voltage for displaying white or black.

[0019] The invention also provides a liquid crystal display device having a plurality of pixels, a plurality of signal lines which apply a gray scale voltage to each of the pixels, a driving circuit which outputs the gray scale voltage to a plurality of pixels, and a display control circuit which controls the driving circuit, as well as a driving method of the liquid crystal display device. The display control circuit includes a first circuit which detects a vertical retrace interval on the basis of an externally inputted horizontal synchronizing signal and generates a first to an M-th within-retrace-interval horizontal reference signals within the vertical retrace interval, a second circuit which generates a horizontal reference signal by masking the (M−N)-th and the following within-retrace-interval horizontal reference signals among the within-retrace-interval horizontal reference signals generated by the first circuit, where N represents an integer not smaller than one and (M−N) represents an integer not smaller than two, and a third circuit which generates a driving signal for driving the driving circuit, within the vertical retrace interval on the basis of the horizontal reference signal outputted from the second circuit. The driving circuit outputs the gray scale voltage to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within the vertical retrace interval on the basis of the driving signal.

[0020] The invention also provides a liquid crystal display device having a plurality of pixels, a plurality of signal lines which apply a gray scale voltage to each of the pixels, a driving circuit which outputs the gray scale voltage to a plurality of pixels, and a display control circuit which controls the driving circuit, as well as a driving method of the liquid crystal display device. The display control circuit includes a first circuit which detects a vertical retrace interval on the basis of an externally inputted display timing signal and generates a first to an M-th within-retrace-interval horizontal reference signals within the vertical retrace interval, a second circuit which generates a horizontal reference signal by masking the (M−N)-th and the following within-retrace-interval horizontal reference signals among the within-retrace-interval horizontal reference signals generated by the first circuit, where N represents an integer not smaller than one and (M−N) represents an integer not smaller than two, and a third circuit which generates a driving signal for driving the driving circuit, within the vertical retrace interval on the basis of the horizontal reference signal outputted from the second circuit. The driving circuit outputs the gray scale voltage to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within the vertical retrace interval on the basis of the driving signal.

[0021] In addition, in the invention, it is preferable that the horizontal reference signal outputted from the second circuit within the vertical retrace interval be not smaller than M/2 in number.

[0022] Furthermore, in the invention, it is preferable that the display control circuit also includes a fourth circuit which generates a within-display-period horizontal reference signal on the basis of an externally inputted display timing signal.

[0023] According to the invention, within a vertical retrace interval, the transmission of the driving signal from the display control device to the driving circuit is stopped one or more lines before line scanning for the next frame is started after the completion of the vertical retrace interval, whereby it is possible to prevent contention from occurring between a driving signal transmitted from the display control circuit to drain drivers within the vertical retrace interval and a driving signal transmitted from the display control circuit to the drain drivers within the display period of the next frame after the completion of the vertical retrace interval. Accordingly, it is possible to prevent the drain drivers from malfunctioning or being destroyed.

[0024] In addition, the drain drivers are driven by transmitting the driving signal from the display control device to the drain drivers within the vertical retrace interval without any contention between the driving signal transmitted from the display control circuit to the drain drivers within the vertical retrace interval and the driving signal transmitted from the display control circuit to the drain drivers within the display period of the next frame after the completion of the vertical retrace interval. Accordingly, it is possible to prevent the voltages written in pixels from being varied and causing lateral stripes on the display screen of the liquid crystal display device, thereby improving the display quality of the display screen.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0025] **FIG. 1** is a block diagram showing the schematic construction of a TFT type of liquid crystal display module to which the invention is applied;

[0026] **FIG. 2** is a view showing the equivalent circuit of one example of the liquid crystal display panel shown in **FIG. 1**;

[0027] **FIG. 3** is a view showing the equivalent circuit of another example of the liquid crystal display panel shown in **FIG. 1**;

[0028] **FIG. 4** is a block diagram showing a schematic construction of one example of the drain drivers shown in **FIG. 1**;

[0029] **FIG. 5** is a view showing a case where a dot inversion method is used as a method of driving a liquid crystal display module, and aiding in explaining the polarities of gray scale voltages to be outputted from drain drivers to drain signal lines D;

[0030] **FIG. 6** is a view showing one example of a timing chart in which vertical retrace intervals do not vary at all or only slightly vary in the liquid crystal display module shown in **FIG. 1**;

[0031] **FIG. 7** is a view showing a timing chart in which a vertical retrace interval becomes short in the liquid crystal display module shown in **FIG. 1**;

[0032] **FIG. 8** is a view showing a timing chart in which a vertical retrace interval becomes long in the liquid crystal display module shown in **FIG. 1**;

[0033] **FIG. 9** is a view showing one example of a timing chart of a liquid crystal display module according to Embodiment 1 of the invention;

[0034] **FIG. 10** is a view showing a timing chart in which, during a vertical retrace interval, liquid crystal driving for only one line is performed and AC driving is stopped until the input of the next frame;

[0035] **FIG. 11** is a view aiding in explaining the reason why defective visual display occurs in the timing chart shown in **FIG. 10**;

[0036] **FIG. 12** is a view aiding in explaining the reason why defective visual display occurs in the timing chart shown in **FIG. 10**;

[0037] **FIG. 13** is a view showing the charge-holding characteristics of pixels in the case where liquid crystal driving is performed on a plurality of lines during a vertical retrace interval;

[0038] **FIG. 14** is a view showing the charge-holding characteristics of pixels in the case where liquid crystal driving is performed on a plurality of lines during a vertical retrace interval;

[0039] **FIG. 15** is a block diagram showing the construction of a horizontal reference signal generation part of Embodiment 2 of the invention;

[0040] **FIG. 16** is a circuit diagram showing the circuit construction of the within-display-period horizontal reference signal generation circuit shown in **FIG. 15**;

[0041] **FIG. 17** is a circuit diagram showing the circuit construction of the within-retrace-interval horizontal reference signal generation circuit shown in **FIG. 15**;

[0042] **FIG. 18** is a circuit diagram showing the circuit construction of the horizontal-reference-signal masking signal generation circuit shown in **FIG. 15**;

[0043] **FIG. 19** is a view showing a timing chart of main signals generated by the circuits shown in FIGS. **16** to **18**;

[0044] **FIG. 20** is a block diagram showing the construction of a horizontal reference signal generation part of Embodiment 3 of the invention;

[0045] **FIG. 21** is a circuit diagram showing the circuit construction of the within-display-period horizontal reference signal generation circuit shown in **FIG. 20**;

[0046] **FIG. 22** is a circuit diagram showing the circuit construction of the within-retrace-interval horizontal reference signal generation circuit shown in **FIG. 20**;

[0047] **FIG. 23** is a circuit diagram showing the circuit construction of the horizontal-reference-signal masking signal generation circuit shown in **FIG. 20**;

[0048] **FIG. 24** is a view showing a timing chart of main signals generated by the circuits shown in FIGS. **21** to **23**; and

[0049] **FIG. 25** is a view showing one example of a timing chart of a liquid crystal display module of Embodiment 3 of the invention.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0050] Preferred embodiments of the present invention will be described below in detail with reference to the accompanying drawings.

[0051] In all the drawings to be used for explaining preferred embodiments, parts having the same functions are denoted by the same reference numerals, and the repetitive descriptions of the same parts are omitted.

[0052] [Embodiment 1]

[0053] <Basic Construction of TFT Type of Liquid Crystal Display Module to which the Invention is Applied>

[0054] **FIG. 1** is a block diagram showing the schematic construction of a TFT type of liquid crystal display module to which the invention is applied.

[0055] In the liquid crystal display module (LCM) shown in **FIG. 1**, drain drivers **130** are disposed along one longer side of a liquid crystal display panel (TFT-LCD) **10**, while gate drivers **140** are disposed along one shorter side of the liquid crystal display panel **10**.

[0056] The drain drivers **130** and the gate drivers **140** are directly mounted on a peripheral portion of one glass substrate (for example, a TFT substrate) of the liquid crystal display panel **10**.

[0057] An interface part **100** is mounted on an interface board, and this interface board is mounted on the reverse side of the liquid crystal display panel **10**.

[0058] <Construction of Liquid Crystal Display Panel **10** Shown in **FIG. 1**>

[0059] **FIG. 2** is a view showing the equivalent circuit of one example of the liquid crystal display panel **10** shown in **FIG. 1**. As shown in **FIG. 2**, the liquid crystal display panel **10** has a plurality pixels formed in matrix form.

[0060] Each of the pixels is disposed in the area of intersection of two adjacent signal lines (drain signal lines D or gate signal lines G) and two adjacent signal lines (gate signal lines G or drain signal lines D).

[0061] Each of the pixels has thin film transistors TFT**1** and TFT**2** and the source electrodes of the thin film transistors TFT**1** and TFT**2** of each of the pixels are connected to a pixel electrode ITO**1**.

[0062] Since a liquid crystal layer is disposed between the pixel electrode ITO**1** and a common electrode IT**02**, a liquid crystal capacitance CLC is equivalently connected between the pixel electrode ITO**1** and the common electrode IT**02**.

[0063] An added capacitance CADD is connected between the source electrodes of the thin film transistors TFT**1** and TFT**2** and the front-stage one of the two adjacent gate signal lines G.

[0064] **FIG. 3** is a view showing the equivalent circuit of another example of the liquid crystal display panel **10** shown in **FIG. 1**.

[0065] In the example shown in **FIG. 2**, the added capacitance CADD is formed between the front-stage gate signal line G and the source electrodes, whereas in the equivalent circuit of the example shown in **FIG. 3, a** charge-holding capacitance CSTG is formed between the source electrodes and a common signal line CN to which to apply a common voltage Vcom. The invention is applicable to either of the examples.

[0066] Incidentally, **FIGS. 2 and 3** show the equivalent circuits of a vertical electric field type of liquid crystal display panel, and in each of **FIGS. 2 and 3**, symbol AR denotes a display area. **FIGS. 2 and 3** are also circuit diagrams which are drawn to correspond to actual geometric arrangements.

[0067] In each of the liquid crystal display panels **10** shown in **FIGS. 2 and 3**, the drain electrodes of the respective thin film transistors TFT**1** and TFT**2** of each of the pixels which are disposed in the column direction are connected to the adjacent one of the drain signal lines D, and each of the drain signal lines D is connected to the corresponding one of the drain drivers **130** which apply gray scale voltages to the liquid crystals of the corresponding ones of the pixels disposed in the column direction.

[0068] The gate electrodes of the respective thin film transistors TFT**1** and TFT**2** of each of the pixels which are disposed in the row direction are connected to the adjacent one of the gate signal lines G, and each of the gate signal lines G is connected to the corresponding one of the gate drivers **140** which supplies, for one horizontal scanning period, scanning driving voltages (positive bias voltages or negative bias voltages) to the gate electrodes of the thin film transistors TFT**1** and TFT**2** of the corresponding ones of the pixels disposed in the row direction.

[0069] <Construction and Outline of Operation of Interface Part **100** Shown in **FIG. 1**>

[0070] The interface part **100** shown in **FIG. 1** includes a display control device **110** and a power source circuit **120**.

[0071] The display control device **110** is made of one semiconductor integrated circuit (LSI), and controls and drives the drain drivers **130** and the gate drivers **140** on the basis of display control signals such as dot clock CLK, data enable signals (or display timing signals) DTMG, horizontal synchronizing signals Hsync and vertical synchronizing signals Vsync as well as display data (R, G and B) all of which are to be transmitted from a computer host.

[0072] When the display control device **110** receives a data enable signal DTMG, the display control device **110** determines that this signal indicates a display start position, and outputs a data latching start pulse (or display data latching start signal) STH (hereinafter referred to as the start pulse STH) to the first one of the drain drivers **130** via a signal line **135**, and in addition, outputs received display data for a single line to the drain drivers **130** via a bus line **133** for display data.

[0073] At this time, the display control device **110** outputs a data latching clock CL**2** (hereinafter referred to as the clock CL**2**) for latching display data, to the data latching circuit of each of the drain drivers **130** via a signal line **131**.

[0074] The display data from the host computer is transmitted as, for example, 6-bit data in units of one pixel, i.e., one set of red (R), green (G) and blue (B) data, at intervals of a unit time period.

[0075] In addition, the latching operation of the data latching circuit in the first drain driver **130** is controlled by the start pulse STH inputted to the first drain driver **130**.

[0076] When the latching operation of the data latching circuit in the first drain driver **130** is completed, the start pulse STH is inputted to the second drain driver **130** from the first drain driver **130**, and the latching operation of the data latching circuit in the second drain driver **130** is controlled by the start pulse STH.

[0077] Similarly, the latching operation of the data latching circuit in each of the following drain drivers **130** is controlled, whereby erroneous display data is prevented from being written into the data latching circuit.

[0078] When the inputting of the data enable signal DTMG is completed or a predetermined time period passes after the data enable signal DTMG has been inputted, the display control device **110** determines that one horizontal line of display data has been completed, and outputs, to each of the drain drivers **130** via a signal line **132**, an output timing control clock CL**1** (hereinafter referred to simply as the drain output pulse CL**1**) which is a display control signal for outputting the display data stored in the data latching circuit of each of the drain drivers **130** to each of the drain signal lines D of the liquid crystal display panel **100**.

[0079] When the first data enable signal DTMG is inputted to the display control device **110** after the inputting of a vertical synchronizing signal, the display control device **110** determines that this signal DTMG indicates the first display line, and outputs a frame start pulse (or frame start indication signal) FLM to the gate drivers **140** via a signal line **142**.

[0080] In addition, the display control device **110** outputs a data shift clock CL**3** which is a shift clock having the cycle of one horizontal scanning period (hereinafter referred to as the clock CL**3**) to the gate drivers **140** via a signal line **141** so that a positive bias voltage is sequentially applied to each of the gate signal lines G of the liquid crystal display panel **10** at intervals of one horizontal scanning period on the basis of the horizontal synchronizing signal.

[0081] In this manner, a plurality of thin film transistors TFT which are connected to each of the gate signal lines G of the liquid crystal display panel **10** are held in their closed states for one horizontal synchronizing period.

[0082] By the above-described operation, an image is displayed on the liquid crystal display panel **10**.

[0083] <Construction of Power Source Circuit **120** Shown in **FIG. 1**>

[0084] The power source circuit **120** shown in **FIG. 1** is made of a gray scale reference voltage generation circuit **121**, a common electrode (counter electrode) voltage generation circuit **123** and a gate electrode voltage generation circuit **124**.

[0085] The gray scale reference voltage generation circuit **121** is made of a series resistance voltage dividing circuit, and outputs a ten-level gray scale reference voltage (VO to V**9**).

[0086] The gray scale reference voltage (VO to V**9**) is supplied to each of the drain drivers **130**.

[0087] In addition, an AC driving signal (AC driving timing signal; M) from the display control device **110** is supplied to each of the drain drivers **130** via the signal line **134**.

[0088] The common electrode voltage generation circuit **123** generates a driving voltage to be applied to the common electrode IT**02**, while the gate electrode voltage generation circuit **124** generates a driving voltage (a positive bias voltage and a negative bias voltage) to be applied to the gate electrodes of the thin film transistors TFT**1** and TFT**2**.

[0089] <Construction of Drain Driver **130** Shown in **FIG. 1**>

[0090] **FIG. 4** is a block diagram showing a schematic construction of one example of the drain drivers **130** shown in **FIG. 1**.

[0091] The shown drain driver **130** is made of one semiconductor integrated circuit (LSI).

[0092] In **FIG. 4, a** positive gray scale voltage generation circuit **151***a* generates a 64-level gray scale voltage of positive polarity on the basis of the five-level gray scale reference voltage (**V0** to **V4**) supplied from the gray scale reference voltage generation circuit **121**, and outputs the 64-level gray scale voltage to an output circuit **157** via a voltage bus line **158***a*.

[0093] A negative gray scale voltage generation circuit **151***b* generates a 64-level gray scale voltage of negative polarity on the basis of the five-level gray scale reference voltage (**V5** to **V9**) of negative polarity supplied from the gray scale reference voltage generation circuit **121**, and outputs the 64-level gray scale voltage to the output circuit **157** via a voltage bus line **158***b*.

[0094] A shift register circuit **153** in a control circuit **152** of the drain driver **130** generates a data latching signal for an input register circuit **154** and outputs the data latching signal to the input register circuit **154**, on the basis of the clock signal CL2 inputted from the display control device **110**.

[0095] The input register circuit **154** latches display data of 6 bits for each color by the number of output lines in synchronism with the clock signal CL2 inputted from the display control device **110**, on the basis of the data latching signal outputted from the shift register circuit **153**.

[0096] A storage register circuit **155** latches the display data stored in the input register circuit **154**, according to the clock CL1 inputted from the display control device **110**.

[0097] The display data latched in the storage register circuit **155** is inputted to the output circuit **157** via a level shift circuit **156**.

[0098] The output circuit **157** selects one gray scale voltage level corresponding to the display data from the 64-level gray scale voltage of positive polarity or the 64-level gray scale voltage of negative polarity, and outputs the selected one gray scale voltage level to each of the drain signal lines D.

[0099] <AC Driving Method of Liquid Crystal Display Module Shown in **FIG. 1**>

[0100] In general, if the same voltage (DC voltage) is continuously applied to a liquid crystal layer for a long time, the inclination of the liquid crystal layer is fixed, so that an image-retention phenomenon is caused to reduce the life of the liquid crystal layer.

[0101] To prevent this problem, in a liquid crystal display module, a voltage to be applied to its liquid crystal layer is made to alternate at intervals of a constant time period, i.e., a gray scale voltage to be applied to each of its pixel electrodes is made to vary between its positive voltage side and its negative voltage side at intervals of a constant time period on the basis of a common voltage to be applied to its common electrodes (or counter electrodes).

[0102] As a driving method for applying AC voltage to this liquid crystal layer, a common symmetry method and a common inversion method are known.

[0103] The common inversion method is a method of alternately inverting both the common voltage to be applied to the common electrodes and the gray scale voltage to be applied to the pixel electrodes between their positive voltage sides and their negative voltage sides.

[0104] The common symmetry method is a method of keeping constant the common voltage to be applied to the common electrodes and alternately inverting the gray scale voltage to be applied to the pixel electrodes between the positive voltage sided and the negative voltage side on the basis of the common voltage to be applied to the common electrodes.

[0105] **FIG. 5** is a view showing a case where a dot inversion method is used as a method of driving a liquid crystal display module, and aiding in explaining the polarities of gray scale voltages to be outputted from its drain drivers to its drain signal lines (i.e., gray scale voltages to be applied to its pixel electrodes).

[0106] In the dot inversion method, as shown in **FIG. 5** by way of example, in the odd lines of each odd frame, gray scale voltages of negative polarity (represented by "•" in **FIG. 5**) relative to a common voltage Vcom applied to the common electrodes are applied to the odd-numbered ones of the drain signal lines from the drain drivers, while gray scale voltages of positive polarity (represented by "o" in **FIG. 5**) relative to the common voltage Vcom applied to the common electrodes are applied to the even-numbered ones of the drain signal lines from the drain drivers.

[0107] Furthermore, in the even lines of each odd frame, gray scale voltages of positive polarity are applied to the odd-numbered drain signal lines from the drain drivers, while gray scale voltages of negative polarity are applied to the even-numbered drain signal lines from the drain drivers.

[0108] In addition, the polarity of each of the lines is inverted from frame to frame, and as shown in **FIG. 5**, in the odd lines of each even frame, gray scale voltages of positive polarity are applied to the odd-numbered drain signal lines from the drain drivers, while gray scale voltages of negative polarity are applied to the even-numbered drain signal lines from the drain drivers.

[0109] Furthermore, in the even lines of each even frame, gray scale voltages of negative polarity are applied to the odd-numbered drain signal lines from the drain drivers, while gray scale voltages of positive polarity are applied to the even-numbered drain signal lines from the drain drivers.

[0110] By using the above-described dot inversion method, the gray scale voltages applied to any adjacent ones of the drain signal lines become opposite to each other in polarity, and currents which flow through the common electrodes and the gate electrodes of the thin film transistors TFT cancel each other between mutually adjacent pixels, whereby power consumption can be reduced.

[0111] In addition, since currents flowing through the common electrodes are small and voltage drops are not large, the voltage levels of the common electrodes are stable, whereby a decrease in display quality can be minimized.

[0112] <Timing Chart of Liquid Crystal Display Module Shown in **FIG. 1**>

[0113] As described above, the drain drivers **130** are controlled and driven by driving signals such as the start

pulse STH, the clock CL2, the drain output pulse CL1 and the AC driving signal M all of which are transmitted from the display control device **110**, and the gate drivers **140** are controlled and driven by the frame start pulse FLM and the clock CL3 which are transmitted from the display control device **110**.

[0114] **FIG. 6** is a view showing one example of a timing chart in which vertical retrace intervals do not vary at all or only slightly vary in the liquid crystal display module shown in **FIG. 1**.

[0115] The time t1 shown in **FIG. 6** is one horizontal cycle time (i.e., one horizontal scanning period), and when an image is to be displayed on the liquid crystal display panel **10**, it is in general necessary to control the drain drivers **130** and the gate drivers **140** on the basis of a predetermined sequence within the period of the time t1 which starts in synchronism with the leading edge of the data enable signal DTMG, although control methods differ according to the specifications of drivers.

[0116] One example of this sequence is shown in **FIG. 6**.

[0117] In the sequence shown in **FIG. 6**, after the data enable signal DTMG has been inputted to the display control device **110**, the display control device **110** transmits the start pulse STH, and starts latching data in the drain drivers **130**.

[0118] Then, the display control device **110** sets the clock CL3 to a high level (hereinafter referred to simply as an H level), thereby shifting a horizontal line to be scanned to the next line of the gate signal line G and turning on the gate electrodes of the thin film transistors TFT1 and TFT2 along a horizontal line to be scanned.

[0119] After data have been latched in the drain drivers **130**, the display control device **110** inverts the AC driving signal M, and sets the drain output pulse CL1 to an H level.

[0120] After that, the display control device **110** sets the drain output pulse CL1 to a low level (hereinafter referred to simply as an L level), and causes gray scale voltages of positive or negative polarity corresponding to display data to be outputted from the drain drivers **130** to the drain signal lines D.

[0121] In this sequence, as a matter of course, the pulse width, the period and the like of each of the signals must satisfy the specifications of liquid crystal drivers.

[0122] If the above-described sequence is not satisfied, expected visual display may not be obtained, or there is also a possibility that liquid crystal drivers are destroyed.

[0123] The time t2 shown in **FIG. 6** indicates the time (vertical retrace interval detection time) required to determine the vertical retrace interval.

[0124] Although there are various methods for determining the vertical retrace interval, **FIG. 6** shows an example in which at the point of time when the input of a data enable signal DTMG is not accepted during the elapse of the time t2 after the rise of the previous data enable signal DTMG, it is determined that a vertical retrace interval has started.

[0125] Within the vertical retrace interval, the output of gray scale voltages from the drain drivers **130** to the drain signal lines D is performed at a cycle of the time t1 after the elapse of the time t2.

[0126] Incidentally, the above-described operation of outputting gray scale voltages from the drain drivers **130** to the drain signal lines D is hereinafter referred to as "liquid crystal driving within a(the) vertical retrace interval".

[0127] Before this liquid crystal driving within the vertical retrace interval, gray scale voltages corresponding to display data are written into the respective pixels along all the lines of the liquid crystal display panel **10**; for example, in the case of driving with a dot inversion method, the gray scale voltages of positive polarity or negative polarity shown in **FIG. 5** are written.

[0128] Accordingly, during this liquid crystal driving within the vertical retrace interval, no gray scale voltages are written into the pixels, but for a reason which will be described later, gray scale voltages of arbitrary level (generally, gray scale voltages for displaying white or black) are outputted from the drain drivers **130** to the drain signal lines D.

[0129] Therefore, in the liquid crystal display module shown in **FIG. 1**, data for the liquid crystal driving within the vertical retrace interval is transmitted from the display control device **110** to the drain drivers **130** at least once.

[0130] In the sequence shown in **FIG. 6**, there is no contention between an output sequence for the last line during the liquid crystal driving within the vertical retrace interval and an output sequence activated by the input of a data enable signal DTMG for the next frame, so that the drain drivers **130** are prevented from malfunctioning or being destroyed.

[0131] However, if the vertical retrace interval varies, contention occurs between the output sequence for the last line during the liquid crystal driving within the vertical retrace interval and the output sequence activated by the input of the data enable signal DTMG for the next frame.

[0132] For example, the periods of the synchronizing signals received by the liquid crystal display module are not always constant owing to enlargement/reduction processing for S.S. (Spread Spectrum), display data and the like in a host computer which serves a signal source. In such a case, the vertical retrace interval varies.

[0133] **FIG. 7** is a view showing a timing chart in which a vertical retrace interval becomes short in the liquid crystal display module shown in **FIG. 1**.

[0134] In **FIG. 7**, as a first example of a timing chart containing variations, there is shown a case where, within the vertical retrace interval, the length of one horizontal synchronizing signal Hsync becomes a time t3 shorter than the time t1 which is one regular horizontal scanning cycle time.

[0135] Referring to a cross-hatched portion in **FIG. 7** (which represents that contention occurs between the output sequences), a drain output pulse CL1 is not outputted within the time t3 with respect to a start pulse STH outputted immediately before the data enable signal DTMG for the next frame, but with respect to a start pulse STH synchronized with the data enable signal DTMG for the next frame, two drain output pulses CL1 are outputted within the time t1 and the pulse width of the clock CL3 becomes narrow.

[0136] Accordingly, the sequence shown in **FIG. 7** does not satisfy the sequence shown in **FIG. 6** (the case where vertical retrace intervals do not vary at all or only slightly vary).

[0137] **FIG. 8** is a view showing a timing chart in which a vertical retrace interval becomes long in the liquid crystal display module shown in **FIG. 1**.

[0138] In **FIG. 8**, as a second example of a timing chart containing variations, there is shown a case where, within the vertical retrace interval, the length of one horizontal synchronizing signal Hsync becomes a time t**3** longer than the time t**1** which is one regular horizontal scanning cycle time.

[0139] Referring to a cross-hatched portion in **FIG. 8** (which represents that contention occurs between the output sequences), similarly to the case of **FIG. 7, a** drain output pulse CL**1** is not outputted within a time (t**3**−t**1**) with respect to a start pulse STH outputted immediately before the data enable signal DTMG for the next frame, but with respect to a start pulse STH synchronized with the data enable signal DTMG for the next frame, two drain output pulses CL**1** are outputted within the time t**1**.

[0140] The sequence shown in **FIG. 8** does not satisfy the sequence shown in **FIG. 6**, either.

[0141] In the case where the externally inputted signals follow a timing chart such as that shown in **FIG. 7** or **8**, even if the output sequences are generated in accordance with one horizontal scanning cycle of a display period after it has been determined that a vertical retrace interval has started, expected visual display may not be obtained, or there is a possibility that liquid crystal drivers are destroyed.

[0142] <Timing Chart of Liquid Crystal Display Module According to Embodiment 1 of the Invention>

[0143] **FIG. 9** is a view showing one example of a timing chart of a liquid crystal display module according to Embodiment 1 of the invention.

[0144] In Embodiment 1, after a vertical retrace interval has started, the liquid crystal driving within the vertical retrace interval is stopped one or more lines before a data enable signal DTMG for the next frame is inputted.

[0145] **FIG. 9** shows a timing chart in which a vertical retrace interval becomes short similarly to the case of the timing chart shown in **FIG. 7**. In **FIG. 9**, the liquid crystal driving within the vertical retrace interval is stopped one line before a data enable signal DTMG for the next frame is inputted.

[0146] To this end, in Embodiment 1, within a vertical retrace interval, the display control device **110** stops transmitting pulses circled with "o" in **FIG. 9** to the drain drivers **130** and the gate drivers **140**, thereby stopping the liquid crystal driving within the vertical retrace interval.

[0147] Accordingly, in Embodiment 1, it is possible to perform the liquid crystal driving within the vertical retrace interval without any contention between the output sequence within the vertical retrace interval and the output sequence within the display period of the next frame after the completion of the vertical retrace interval.

[0148] The reason why the liquid crystal driving within the vertical retrace interval is performed will be described below.

[0149] **FIG. 10** is a view showing a timing chart in which, during a vertical retrace interval, liquid crystal driving for only one line is performed and AC driving is stopped until the input of the next frame.

[0150] In **FIG. 10**, symbol t**7** denotes an interval during which AC driving is not being performed.

[0151] In the driving according to the timing chart shown in **FIG. 10**, there is a possibility that defective visual display occurs due to the length of a vertical retrace interval, the leak characteristics of the thin film transistors TFT**1** and TFT**2** of each pixel, and display data.

[0152] **FIGS. 11 and 12** are views aiding in explaining the reason why defective visual display occurs in the timing chart shown in **FIG. 10**.

[0153] **FIG. 11** is a view aiding in explaining the case where display data represent a raster display whose amplitude is between a gray scale voltage a and a gray scale voltage a', and shows the charge-holding characteristics of pixels with a gray scale voltage a applied to stop AC driving during the driving of the first line within a vertical retrace interval.

[0154] In this case, if the leak characteristics of the thin film transistors TFT**1** and TFT**2** of the pixels are inferior, leak currents occur in the pixels along the last line written (charged) with the gray scale voltage a', so that the voltage written in the pixels varies.

[0155] In this case, since the gray scale voltage a is written in the pixels along the second line from the last during the vertical retrace interval, even if the gray scale voltage a is applied to stop AC driving during the driving of the first line within the vertical retrace interval, the potential of the pixels and the potential of the drain signal lines D coincide with each other, and no leak currents flow in the pixels along the last line.

[0156] Accordingly, a luminance difference occurs between lines on the display screen, so that a lateral stripe occurs.

[0157] **FIG. 12** is a view aiding in explaining the case where display data represent a raster display whose amplitude is between the gray scale voltage a and the gray scale voltage a', and shows the charge-holding characteristics of the pixels with a gray scale voltage b applied to stop AC driving during the driving of the first line within a vertical retrace interval.

[0158] In this case, when the gray scale voltage b is finally applied, leak currents occur in the pixels along the last line written with the gray scale voltage a' and the pixels along the second last line written with the gray scale voltage a, so that lateral stripes occur.

[0159] However, in the case shown in **FIG. 12**, the voltages written in the pixels on the adjacent lines vary owing to the leak currents, and the potential difference between the voltage written in the pixels on one of the adjacent lines and the voltage written in the pixels on the other is smaller than the potential difference shown in **FIG. 11**, so that lateral stripes are not very outstanding.

[0160] **FIGS. 13 and 14** are views showing the charge-holding characteristics of the pixels in the case where liquid crystal driving is performed on a plurality of lines within a vertical retrace interval.

[0161] Similarly to **FIG. 11**, **FIG. 13** shows the case where display data represent a raster display whose amplitude is between the gray scale voltage a and the gray scale

voltage a', and the gray scale voltage a and the gray scale voltage a' are alternately applied to the first and following lines within a vertical retrace interval to effect liquid crystal driving.

[0162] In this case, on the first line during the vertical retrace interval, similarly to the case of **FIG. 11**, leak currents to the pixels along the last line written with the gray scale voltage a' occur and the voltage written in the pixels vary, and no leak currents flow to the pixels along the second last line written with the gray scale voltage a.

[0163] However, on the second line during the vertical retrace interval, leak currents to the pixels along the second last line written with the gray scale voltage a occur and the voltage written in the pixels vary.

[0164] In addition, in the pixels along the last line written with the gray scale voltage a', the amount of voltage variation on the first line is cancelled by the leak currents, and the pixel voltages are written with the gray scale voltage a'.

[0165] On the third line, for the above-described reason, the pixel voltage on the second last line written with the gray scale voltage a becomes the gray scale voltage a.

[0166] Accordingly, no luminance difference occurs between lines on the display screen, whereby it is possible to prevent the occurrence of lateral strips.

[0167] **FIG. 14** shows the case where display data represent a raster display whose amplitude is between the gray scale voltage a and the gray scale voltage a' similarly to the display data shown in **FIG. 12**, and the gray scale voltage b and the gray scale voltage b' are alternately applied to the first and following lines within a vertical retrace interval to effect liquid crystal driving.

[0168] In this case, the pixel voltages of the pixels along the last line and the pixel voltages of the pixels along the second line from the last vary owing to line scanning during the vertical retrace interval, but the amounts of voltage variations on both lines are approximately the same.

[0169] Accordingly, in the case of **FIG. 14**, the pixels along the last line and the pixels along the second line from the last vary similarly in luminance, whereby it is possible to prevent lateral stripes from occurring on the display screen.

[0170] As described above, in Embodiment 1, the voltages written in the pixels are prevented from being varied and causing lateral stripes on the display screen, whereby it is possible to improve the display quality of the display screen.

[0171] Incidentally, in Embodiment 1, letting M be a value obtained by dividing the vertical retrace interval by a regular horizontal scanning time and rounding up fractions to the nearest whole number, and letting N be an integer not smaller than one, the liquid crystal driving within the vertical retrace interval is preferably performed on not smaller than two lines and not greater than (M−N) times, more preferably on not smaller than M/2 times and not greater than (M−N) times.

[0172] Incidentally, the value M is also a value obtained by adding together the number of lines scanned during the whole of the vertical retrace interval and the number of lines scanned during at least a part of the vertical retrace interval, in the case where scanning is performed with the regular horizontal scanning time within the vertical retrace interval.

[0173] The value of N is preferably N=1 or N=2 in view of the necessity to drive as many lines as possible, but is not limited to such a value. AC driving is desirably performed at least once, preferably by a predetermined number of times so that the period of AC driving becomes approximately the same the display period.

[0174] In addition, the gray scale voltage applied during the liquid crystal driving within the vertical retrace interval is preferably a gray scale voltage corresponding to white or black.

[0175] [Embodiment 2]

[0176] <Unique Construction of Liquid Crystal Display Module According to Embodiment 2>

[0177] In Embodiment 2, to realize a timing chart such as that shown in **FIG. 9**, the display control device **110** generates a horizontal reference signal and generates driving signals for liquid crystal drivers on the basis of the horizontal reference signal, and masks in advance a horizontal reference signal between which and the driving signals for liquid crystal drivers contention may occur.

[0178] **FIG. 15** is a block diagram showing the construction of a horizontal reference signal generation part of Embodiment 2 of the invention.

[0179] The horizontal reference signal generation part of Embodiment 2 is made of a within-display-period horizontal reference signal generation circuit **20**, a within-retrace-interval horizontal reference signal generation circuit **30**, and a horizontal-reference-signal masking signal generation circuit **40**.

[0180] The horizontal reference signal generation part also has an AND circuit AND**1** and OR circuit OR**1**.

[0181] The within-display-period horizontal reference signal generation circuit **20** generates, by using a data enable signal DTMG, a horizontal reference signal for generating driving signals for driving liquid crystal drivers within a display period (a within-display-period horizontal reference signal **20***a*).

[0182] The within-retrace-interval horizontal reference signal generation circuit **30** detects a vertical retrace interval and subsequently generates a horizontal reference signal for generating driving signals for driving liquid crystal drivers within the vertical retrace interval (a within-retrace-interval horizontal reference signal **30***a*). The within-retrace-interval horizontal reference signal generation circuit **30** also generates a vertical retrace interval indication signal **30***b*.

[0183] The horizontal-reference-signal masking signal generation circuit **40** counts the number of lines within a vertical retrace interval and generates a signal for masking horizontal reference signals within the vertical retrace interval for an arbitrary number of lines (a within-retrace-interval horizontal reference masking signal **40***a*).

[0184] The horizontal reference signal generation part finally generates a horizontal reference signal HR on the basis of these signals.

[0185] As described above, the driving signals for liquid crystal drivers are the start pulse STH, the clock CL**2**, the

drain output pulse CL1 and the AC driving signal M all of which are transmitted from the display control device **110** to the drain drivers **130**, as well as the frame start pulse FLM and the clock CL3 which are transmitted from the display control device **110** to the gate drivers **140**.

[0186] **FIG. 16** is a circuit diagram showing the circuit construction of the within-display-period horizontal reference signal generation circuit **20** shown in **FIG. 15**.

[0187] **FIG. 17** is a circuit diagram showing the circuit construction of the within-retrace-interval horizontal reference signal generation circuit **30** shown in **FIG. 15**.

[0188] **FIG. 18** is a circuit diagram showing the circuit construction of the horizontal-reference-signal masking signal generation circuit **40** shown in **FIG. 15**.

[0189] **FIG. 19** is a view showing a timing chart of main signals generated by the circuits shown in FIGS. **16** to **18**.

[0190] The circuits shown in FIGS. **16** to **18** will be described below.

[0191] The within-display-period horizontal reference signal generation circuit **20** shown in **FIG. 16** has a D flip-flop circuit **21** having an input terminal D to which to input the data enable signal DTMG and a clock input terminal CP to which to input the clock signal CLK.

[0192] An AND circuit AND2 carries out the logical AND between the output from an output terminal/Q of the D flip-flop circuit **21** and the data enable signal DTMG, and generates the within-display-period horizontal reference signal **20***a* which is synchronized with the rise of the data enable signal DTMG and has one dot clock width of the clock signal CLK as shown in **FIG. 19**.

[0193] In the within-retrace-interval horizontal reference signal generation circuit **30** shown in **FIG. 17**, an Htotal counter_1 (hereinafter referred to simply as the counter_1) **31** counts dot clocks CLK, and is reset by the within-display-period horizontal reference signal **20***a*. A count value **31***a* of the counter_131 is stored in an Htotal hold register (hereinafter referred to simply as the register) **35** by the within-display-period horizontal reference signal **20***a*.

[0194] Namely, the count value **31***a* stored in the register **35** is the number of dot clocks CLK per period of the within-display-period horizontal reference signal **20***a*, and indicates one horizontal scanning time within a display period.

[0195] As shown in **FIG. 19**, when the data enable signal DTMG is not inputted, the within-display-period horizontal reference signal **20***a* is not generated, whereby the counter_131 counts the dot clocks CLK without being reset by the within-display-period horizontal reference signal **20***a*.

[0196] The count value of the counter_131 is inputted into a comparator_133, and when the count value reaches a count value of NO, the comparator_133 outputs the vertical retrace interval indication signal **30***b* shown in **FIG. 19**.

[0197] As shown in **FIG. 15**, the vertical retrace interval indication signal **30***b* is inputted into the OR circuit OR1, and the OR circuit OR1 outputs a first within-vertical-retrace-interval horizontal reference signal HRS as shown in **FIG. 19**.

[0198] Incidentally, letting 1/CLK be one period of the dot clock CLK, N0 is selected to satisfy (1/CLK)×N0=t2.

[0199] Namely, even if the count value of the counter_131 exceeds a predetermined time (t2 in **FIG. 19**), the comparator_133 detects that the inputting of the data enable signal DTMG is not being performed, and detects a vertical retrace interval.

[0200] In this case, since the within-display-period horizontal reference signal **20***a* is not inputted into the register **35**, the count value stored in the register **35** becomes a count value latched by the previous within-display-period horizontal reference signal **20***a* (i.e., a count value indicative of one horizontal scanning time within a display period).

[0201] The vertical retrace interval indication signal **30***b* outputted from the comparator_133 is also inputted into the OR circuit OR2, and the OR circuit OR2 goes to its H level.

[0202] At this time, an Htotal counter_2 (hereinafter referred to simply as the counter_2) **32** is reset, and the counter_232 counts the dot clocks CLK.

[0203] A count value **32***a* of the counter_232 is inputted into a comparator_234, and when the count value of the counter_232 coincides with the count value stored in the register **35**, the comparator_234 outputs the within-retrace-interval horizontal reference signal **30***a*.

[0204] Since the within-retrace-interval horizontal reference signal **30***a* outputted from the comparator_234 is inputted into the OR circuit OR2, the counter_232 is reset, and the counter_232 again starts to count the dot clocks CLK.

[0205] Accordingly, as shown in **FIG. 19**, the comparator_234 outputs the within-retrace-interval horizontal reference signal **30***a* at intervals of the time t1.

[0206] In the horizontal-reference-signal masking signal generation circuit **40** shown in **FIG. 18, a** retrace line counter **41** is reset by the vertical retrace interval indication signal **30***b* outputted from the comparator_133 shown in **FIG. 17**, and counts the within-retrace-interval horizontal reference signal **30***a* outputted from the comparator_234 shown in **FIG. 17**.

[0207] Namely, the retrace line counter **41** counts the total number of lines within a vertical retrace interval. Incidentally, the total number of lines is the number of lines obtained when each line whose scanning time is less than one horizontal scanning time is also counted as one line. In Embodiment 2, since the value of the retrace line counter **41** starts with "0", a value smaller by one than an actual total number of lines is displayed.

[0208] A retrace line hold register (hereinafter referred to simply as the line register) **42** stores the count value of the retrace line counter **41** in response to the within-display-period horizontal reference signal **20***a*. Namely, the total number of lines within the vertical retrace interval of the previous frame is stored in the line register **42**.

[0209] The count value stored in the line register **42** is inputted into a subtracter **43**, and in the subtracter **43**, the number of lines to be masked, N, is subtracted from the count value.

[0210] The output from the subtracter **43** is inputted into a comparator_**344**, and is compared with the count value outputted from the retrace line counter **41**.

[0211] For example, if the number of lines stored in the line register **42** is three and the number of lines to be masked, N, is one as shown in **FIG. 19**, when the count value outputted from the retrace line counter **41** becomes 2 (=3−1), the comparator_**344** outputs a masking start signal as shown in **FIG. 19**.

[0212] This masking start signal is inputted into a terminal j of a J-K flip-flop circuit **45**, and at this time, since the within-display-period horizontal reference signal **20***a* is not inputted into a terminal K, the J-K flip-flop circuit **45** outputs the within-retrace-interval horizontal reference masking signal **40***a* from a terminal Q as shown in **FIG. 19**.

[0213] The within-retrace-interval horizontal reference masking signal **40***a* goes to its L level when the within-display-period horizontal reference signal **20***a* for the next frame is inputted into the terminal K of the J-K flip-flop circuit **45** as shown in **FIG. 19**.

[0214] The inverted signal of the within-retrace-interval horizontal reference masking signal **40***a* is inputted to the AND circuit AND1 shown in **FIG. 15**, so that the within-retrace-interval horizontal reference signal **30***a* within the H-level period of the within-retrace-interval horizontal reference masking signal **40***a* is masked by the AND circuit AND1 as shown in **FIG. 19**.

[0215] As shown in **FIG. 15**, the within-display-period horizontal reference signal **20***a* outputted from the within-display-period horizontal reference signal generation circuit **20**, the vertical retrace interval indication signal **30***b* outputted from the within-retrace-interval horizontal reference signal generation circuit **30** (this signal is also used as one kind of within-retrace-interval horizontal reference signal), and the within-retrace-interval horizontal reference signal **30***a* outputted through the AND circuit AND1 after having been outputted from the within-retrace-interval horizontal reference signal generation circuit **30** are inputted into the OR circuit OR1, and the OR circuit OR1 outputs the horizontal reference signal HRS for generating driving signals for liquid crystal drivers which do not come into contention.

[0216] Accordingly, in Embodiment 2, it is possible to perform the liquid crystal driving within the vertical retrace interval without any contention between the output sequence within the vertical retrace interval and the output sequence within the display period of the next frame after the completion of the vertical retrace interval.

[0217] Incidentally, the horizontal reference signal generation part shown in **FIG. 15** is provided in the display control device **110**, and this horizontal reference signal generation part uses only the data enable signal DTMG and the dot clock CLK.

[0218] For this reason, in Embodiment 2, the vertical synchronizing signal Vsync and the horizontal synchronizing signal Hsync are not needed as the display control signals to be inputted externally.

[0219] [Embodiment 3]

[0220] <Unique Construction of Liquid Crystal Display Module According to Embodiment 3>

[0221] In Embodiment 3 as well, to realize a timing chart such as that shown in **FIG. 9**, the display control device **110** generates a horizontal reference signal and generates driving signals for liquid crystal drivers on the basis of the horizontal reference signal, and masks in advance a horizontal reference signal between which and the driving signals for liquid crystal drivers contention may occur. However, in Embodiment 3, the data enable signal DTMG, the dot clock CLK and the horizontal synchronizing signal Hsync are used.

[0222] **FIG. 20** is a block diagram showing the construction of a horizontal reference signal generation part of Embodiment 3 of the invention.

[0223] The horizontal reference signal generation part of Embodiment 3 is made of a within-display-period horizontal reference signal generation circuit **50**, a within-retrace-interval horizontal reference signal generation circuit **60**, and a horizontal-reference-signal masking signal generation circuit **70**.

[0224] The horizontal reference signal generation part also has an AND circuit AND1 and OR circuit OR1.

[0225] However, the horizontal reference signal generation part of Embodiment 3 differs from the horizontal reference signal generation part of Embodiment 2 in that a vertical retrace interval indication signal **60***b* outputted from the within-retrace-interval horizontal reference signal generation circuit **60** is not inputted into the OR circuit OR1.

[0226] **FIG. 21** is a circuit diagram showing the circuit construction of the within-display-period horizontal reference signal generation circuit **50** shown in **FIG. 20**.

[0227] **FIG. 22** is a circuit diagram showing the circuit construction of the within-retrace-interval horizontal reference signal generation circuit **60** shown in **FIG. 20**.

[0228] **FIG. 23** is a circuit diagram showing the circuit construction of the horizontal-reference-signal masking signal generation circuit **70** shown in **FIG. 20**.

[0229] **FIG. 24** is a view showing a timing chart of main signals generated by the circuits shown in FIGS. **21** to **23**.

[0230] **FIG. 25** is a view showing one example of a timing chart of the liquid crystal display module of Embodiment 3.

[0231] The reason why the vertical retrace interval indication signal **60***b* is not inputted into the OR circuit OR1 is as follows: As described above in connection with **FIG. 24**, there is a likelihood that if the vertical retrace interval indication signal **60***b* is used as a within-retrace-interval horizontal reference signal **60***a*, the vertical retrace interval indication signal **60***b* comes into contention for the next within-retrace-interval horizontal reference signal **60***a* generated by the within-retrace-interval horizontal reference signal generation circuit **60**.

[0232] The within-display-period horizontal reference signal generation circuit **50** shown in **FIG. 21** is the same as the within-display-period horizontal reference signal generation circuit **20** shown in **FIG. 16**, and the detailed description of the within-display-period horizontal reference signal generation circuit **50** is omitted.

[0233] Similarly, the horizontal-reference-signal masking signal generation circuit **70** shown in **FIG. 23** is the same as

the horizontal-reference-signal masking signal generation circuit **40** shown in **FIG. 18**, and the detailed description of the horizontal-reference-signal masking signal generation circuit **70** is omitted.

[**0234**] The within-retrace-interval horizontal reference signal generation circuit **60** shown in **FIG. 22** will be described below.

[**0235**] A horizontal synchronizing signal Hsync is inputted into a terminal j of a J-K flip-flop circuit **65**, while a within-display-period horizontal reference signal **50***a* is inputted into a terminal K of the J-K flip-flop circuit **65**. Accordingly, if the horizontal synchronizing signal Hsync is inputted, an output terminal Q (denoted by a in **FIG. 22**) goes to its H level in synchronism with the fall of the dot clock CLK, while if the within-display-period horizontal reference signal **20***a* is inputted, the output terminal Q goes to its L level in synchronism with the fall of the dot clock CLK.

[**0236**] Accordingly, while the output terminal Q of the J-K flip-flop circuit **65** is at the H level, the dot clock CLK is inputted into a back porch (Hbp) counter (hereinafter referred to simply as the counter) **61**.

[**0237**] A count value **61***a* of the counter **61** is stored in a back porch (Hbp) hold register (hereinafter referred to simply as the register) **62** by the within-display-period horizontal reference signal **50***a*.

[**0238**] Since this counter **61** is reset by the horizontal synchronizing signal Hsync, the count value stored in the register **62** is the number of dot clocks CLK within the horizontal back porch time t**4** shown in **FIG. 25**, and indicates the horizontal back porch time t**4**.

[**0239**] Since the within-display-period horizontal reference signal **50***a* is inputted into the terminal K of the J-K flip-flop circuit **66**, the output terminal Q is at the L level within the display period. Since the output from the output terminal Q is inputted into an AND circuit AND**5**, the comparison result outputted from a comparator_**264** is masked.

[**0240**] In addition, within the display period, an output terminal /Q of the J-K flip-flop circuit **66** is at its H level, and the H-level output is inputted into an AND circuit AND**4**. However, within the display period, since the comparison result is not outputted from a comparator_**163**, there is no output from the AND circuit AND**4**.

[**0241**] As shown in **FIG. 24**, when the data enable signal DTMG is not inputted, the within-display-period horizontal reference signal **50***a* is not generated, and the output terminal Q of the J-K flip-flop circuit **65** is maintained at the H level until the within-display-period horizontal reference signal **50***a* for the next frame is inputted.

[**0242**] Accordingly, when the counter **61** counts up and the count value in the comparator_**163** reaches a count value of N**1**, the comparator_**163** outputs the comparison result.

[**0243**] Incidentally, letting 1/CLK be one period of the dot clock CLK, N**1** is selected to satisfy (1/CLK)×N**1**=t**5**.

[**0244**] The comparison result output from the comparator_**163** is inputted into the AND circuit AND**4**, while the output from the output terminal /Q of the J-K flip-flop circuit **66** is inputted into the AND circuit AND**4**. However, since the output terminal /Q is at the H level, the vertical retrace interval indication signal **60***b* is outputted from the AND circuit AND**4** as shown in **FIG. 24**.

[**0245**] The comparison result output from the comparator_**163** is inputted into a terminal j of the J-K flip-flop circuit **66**.

[**0246**] When the comparison result output from the comparator_**163** is inputted into the terminal j of the J-K flip-flop circuit **66**, the output terminal Q goes to the H level and the output terminal /Q goes to its L level in synchronism with the fall of the dot clock CLK.

[**0247**] Accordingly, the output of the AND circuit AND**4** is maintained at the L level until the within-display-period horizontal reference signal **50***a* for the next frame is inputted into the terminal j of the J-K flip-flop circuit **66**. Accordingly, after the vertical retrace interval indication signal **60***b* has been outputted from the AND circuit AND**4**, the comparison result output from the comparator_**163** is kept from passing through the AND circuit AND**4**.

[**0248**] In the meantime, the count value **61***a* of the counter **61** is also inputted into the comparator_**264**, and when the count value of the counter **61** coincides with the count value stored in the register **62**, the comparator_**264** outputs the comparison result.

[**0249**] In this case, since the within-display-period horizontal reference signal **50***a* is not inputted into the register **62**, the count value stored in the register **62** becomes a count value latched by the previous within-display-period horizontal reference signal **50***a* (i.e., a count value indicative of one horizontal back porch time t**4**).

[**0250**] The comparison result output from the comparator_**264** is inputted into the AND circuit AND**5**, while the output from the output terminal Q of the J-K flip-flop circuit **66** is inputted into the AND circuit AND**5**. Since the output terminal Q is at the H level, the AND circuit AND**5** outputs the within-retrace-interval horizontal reference signal **60***a* at intervals of the time t**1** as shown in **FIG. 24**.

[**0251**] The comparator_**264** also outputs the comparison result within the display period, but the output terminal Q of the J-K flip-flop circuit **66** is at the L level within the display period, whereby the AND circuit AND**5** is maintained at the L level. Accordingly, the comparison result output from the comparator_**264** does not at all pass through the AND circuit AND**5**.

[**0252**] In Embodiment 3, since the number of signals to be masked, N, is N=1 as shown in **FIG. 24**, the last within-retrace-interval horizontal reference signal **60***a* is finally masked and the horizontal reference signal HRS is obtained. In addition, the data start latch pulse STH does not appear at a position circled with "o" in **FIG. 25**. In this manner, liquid crystal driving is stopped N lines before the data enable signal DTMG for the next frame is inputted.

[**0253**] Accordingly, even if the horizontal back porch time varies to a time t**6** different from the time t**4** in the next frame, contention does not occur.

[**0254**] Incidentally, in Embodiment 3, the number of signals to be masked, N, is not limited to one, and may be one or more.

[0255] Accordingly, in Embodiment 3 as well, it is possible to perform the liquid crystal driving within the vertical retrace interval without any contention between the output sequence within the vertical retrace interval and the output sequence within the display period of the next frame after the completion of the vertical retrace interval.

[0256] Incidentally, the horizontal reference signal generation part shown in **FIG. 20** is provided in the display control device **110**, and this horizontal reference signal generation part uses only the data enable signal DTMG, the dot clock CLK, and the horizontal synchronizing signal Hsync. For this reason, in Embodiment 3, the vertical synchronizing signal Vsync is not needed as the display control signals to be inputted externally.

[0257] As is apparent from the foregoing description, in the liquid crystal display module according to each of the above-described embodiments, it is possible to set a wide variety of input modes. Accordingly, the invention can be usefully applied to, for example, liquid crystal display modules for monitors which need various input modes.

[0258] Incidentally, in the description of each of the embodiments, reference has been made to a vertical electric field type of liquid crystal display panel to which the invention is applied, but the invention is not limited to only this type and may also be applied to an in-plane switching type of liquid crystal display panel.

[0259] In the vertical electric field type of liquid crystal display panel shown in each of **FIGS. 2 and 3**, a common electrode ITO**2** is provided on a substrate opposed to a TFT substrate, whereas in the in-plane switching type of liquid crystal display panel, counter electrodes CT and counter electrode signal lines CL for applying a common voltage Vcom to the counter electrodes CT.

[0260] Accordingly, each liquid crystal capacitance Cpix is equivalently connected between a pixel electrode PX and a counter electrode CT. A storage capacitance Cstg is also formed between the pixel electrode PX and the counter electrode CT.

[0261] In the description of the embodiments, reference has been made to an embodiment which adopts a dot inversion method as a driving method, but the invention is not limited to the dot inversion method. The invention can also be applied to a plural-line inversion method or a common inversion method in which the polarity of driving voltages to be applied to pixel electrodes ITO**1** and common electrodes ITO**2** is inverted at intervals of one line or a plurality of lines.

[0262] Although the invention made by the present inventor has been specifically described with reference to the embodiments, it is a matter of course that the invention is not limited to any of the above-described embodiments and various modifications can be made without departing from the gist of the invention.

[0263] The representative advantages of the invention disclosed in the present application will be described below in brief.

[0264] (1) According to the invention, it is possible to prevent contention from occurring between a driving signal transmitted from a display control circuit to a driving circuit within a vertical retrace interval and a driving signal transmitted from the display control circuit to the driving circuit within the display period of the next frame after the completion of the vertical retrace interval. Accordingly, it is possible to prevent the driving circuit from malfunctioning or being destroyed.

[0265] (2) According to the invention, a gray scale voltage is outputted to each signal line from the driving circuit within a vertical retrace interval by a number of times not smaller than twice and not greater than (the number of vertical lines−N (N is arbitrary)) times. Accordingly, the voltages written in pixels are prevented from being varied and causing lateral stripes on the display screen, whereby it is possible to improve the display quality of the display screen.

What is claimed is:

**1**. A driving method of a liquid crystal display device having a plurality of pixels, a plurality of signal lines which apply a gray scale voltage to each of the pixels, and a driving circuit which outputs the gray scale voltage to each of the signal lines, comprising the step of:

outputting the gray scale voltage from the driving circuit to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within a vertical retrace interval, where M represents a value obtained by dividing the vertical retrace interval by a regular horizontal scanning time and rounding up fractions to the nearest whole number, and N represents an integer not smaller than one.

**2**. A driving method of a liquid crystal display device according to claim 1, wherein the gray scale voltage is outputted from the driving circuit to each of the signal lines by a number of times not smaller than M/2 times and not greater than (M−N) times within the vertical retrace interval.

**3**. A driving method of a liquid crystal display device according to claim 1, wherein the gray scale voltage is outputted from the driving circuit to each of the signal lines within the vertical retrace interval in synchronism with a regular horizontal synchronizing signal.

**4**. A driving method of a liquid crystal display device according to claim 1, wherein the gray scale voltage is outputted from the driving circuit to each of the signal lines within the vertical retrace interval in synchronism with an internally generated horizontal synchronizing signal.

**5**. A driving method of a liquid crystal display device according to claim 1, wherein when the gray scale voltage is to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval, the polarity of the gray scale voltage to be outputted is inverted at least once.

**6**. A driving method of a liquid crystal display device according to claim 1, wherein the gray scale voltage to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval is a gray scale voltage for displaying white or black.

**7**. A driving method of a liquid crystal display device having a plurality of pixels, a plurality of signal lines which apply a gray scale voltage to each of the pixels, and a driving circuit which outputs the gray scale voltage to each of the signal lines, comprising the step of:

outputting the gray scale voltage from the driving circuit to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within a vertical retrace interval, where M represents a value obtained by adding together the number of lines each having a period scanned entirely and the number of lines each having a period scanned at least partly, when scanning is performed with the regular horizontal scanning time within the vertical retrace interval, and N represents an integer not smaller than one.

**8**. A driving method of a liquid crystal display device according to claim 7, wherein the gray scale voltage is outputted from the driving circuit to each of the signal lines by a number of times not smaller than M/2 times and not greater than (M−N) times within the vertical retrace interval.

**9**. A driving method of a liquid crystal display device according to claim 7, wherein the gray scale voltage is outputted from the driving circuit to each of the signal lines within the vertical retrace interval in synchronism with a regular horizontal synchronizing signal.

**10**. A driving method of a liquid crystal display device according to claim 7, wherein the gray scale voltage is outputted from the driving circuit to each of the signal lines within the vertical retrace interval in synchronism with an internally generated horizontal synchronizing signal.

**11**. A driving method of a liquid crystal display device according to claim 7, wherein when the gray scale voltage is to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval, the polarity of the gray scale voltage to be outputted is inverted at least once.

**12**. A driving method of a liquid crystal display device according to claim 7, wherein the gray scale voltage to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval is a gray scale voltage for displaying white or black.

**13**. A liquid crystal display device comprising:

a plurality of pixels;

a plurality of signal lines which apply a gray scale voltage to each of the pixels; and

a driving circuit which outputs the gray scale voltage to a plurality of pixels,

the driving circuit outputting the gray scale voltage to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within a vertical retrace interval, where M represents a value obtained by dividing the vertical retrace interval by a regular horizontal scanning time and rounding up fractions to the nearest whole number, and N represents an integer not smaller than one.

**14**. A liquid crystal display device according to claim 13, wherein the driving circuit outputs the gray scale voltage to each of the signal lines by a number of times not smaller than M/2 times and not greater than (M−N) times within the vertical retrace interval.

**15**. A liquid crystal display device according to claim 13, wherein when the gray scale voltage is to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval, the driving circuit inverts the polarity of the gray scale voltage to be outputted, at least once.

**16**. A liquid crystal display device according to claim 13, wherein the driving circuit outputs a gray scale voltage for displaying white or black to each of the signal lines within the vertical retrace interval.

**17**. A liquid crystal display device comprising:

a plurality of pixels;

a plurality of signal lines which apply a gray scale voltage to each of the pixels; and

a driving circuit which outputs the gray scale voltage to each of the signal lines,

the driving circuit outputting the gray scale voltage to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within a vertical retrace interval, where M represents a value obtained by adding together the number of lines each having a period scanned entirely and the number of lines each having a period scanned at least partly, when scanning is performed with the regular horizontal scanning time within the vertical retrace interval, and N represents an integer not smaller than one.

**18**. A liquid crystal display device according to claim 17, wherein the driving circuit outputs the gray scale voltage to each of the signal lines by a number of times not smaller than M/2 times and not greater than (M−N) times within the vertical retrace interval.

**19**. A liquid crystal display device according to claim 17, wherein when the gray scale voltage is to be outputted from the driving circuit to each of the signal lines within the vertical retrace interval, the driving circuit inverts the polarity of the gray scale voltage to be outputted, at least once.

**20**. A liquid crystal display device according to claim 17, wherein the driving circuit outputs a gray scale voltage for displaying white or black to each of the signal lines within the vertical retrace interval.

**21**. A liquid crystal display device comprising:

a plurality of pixels;

a plurality of signal lines which apply a gray scale voltage to each of the pixels;

a driving circuit which outputs the gray scale voltage to a plurality of pixels; and

a display control circuit which controls the driving circuit,

the display control circuit including:

a first circuit which detects a vertical retrace interval on the basis of an externally inputted horizontal synchronizing signal and generates a first to an M-th within-retrace-interval horizontal reference signals within the vertical retrace interval;

a second circuit which generates a horizontal reference signal by masking the (M−N)-th and the following within-retrace-interval horizontal reference signals among the within-retrace-interval horizontal reference signals generated by the first circuit, where N represents an integer not smaller than one and (M−N) represents an integer not smaller than two; and

a third circuit which generates a driving signal for driving the driving circuit, within the vertical retrace

interval on the basis of the horizontal reference signal outputted from the second circuit,

the driving circuit outputting the gray scale voltage to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within the vertical retrace interval on the basis of the driving signal.

**22**. A liquid crystal display device according to claim 21, wherein the horizontal reference signal outputted from the second circuit within the vertical retrace interval is not smaller than M/2 in number.

**23**. A liquid crystal display device according to claim 21, wherein the display control circuit also includes a fourth circuit which generates a within-display-period horizontal reference signal on the basis of an externally inputted display timing signal.

**24**. A liquid crystal display device comprising:

a plurality of pixels;

a plurality of signal lines which apply a gray scale voltage to each of the pixels;

a driving circuit which outputs the gray scale voltage to a plurality of pixels; and

a display control circuit which controls the driving circuit,

the display control circuit including:

a first circuit which detects a vertical retrace interval on the basis of an externally inputted display timing signal and generates a first to an M-th within-retrace-interval horizontal reference signals within the vertical retrace interval;

a second circuit which generates a horizontal reference signal by masking the (M−N)-th and the following within-retrace-interval horizontal reference signals among the within-retrace-interval horizontal reference signals generated by the first circuit, where N represents an integer not smaller than one and (M−N) represents an integer not smaller than two; and

a third circuit which generates a driving signal for driving the driving circuit, within the vertical retrace interval on the basis of the horizontal reference signal outputted from the second circuit,

the driving circuit outputting the gray scale voltage to each of the signal lines by a number of times not smaller than twice and not greater than (M−N) times within the vertical retrace interval on the basis of the driving signal.

**25**. A liquid crystal display device according to claim 24, wherein the horizontal reference signal outputted from the second circuit within the vertical retrace interval is not smaller than M/2 in number.

**26**. A liquid crystal display device according to claim 24, wherein the display control circuit also includes a fourth circuit which generates a within-display-period horizontal reference signal on the basis of an externally inputted display timing signal.

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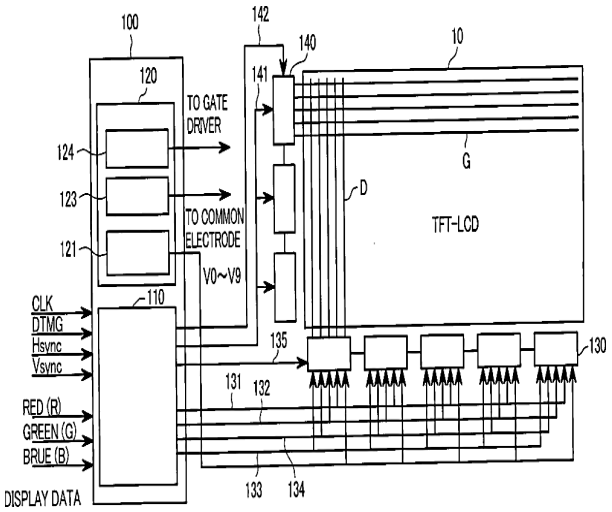
摘要(译)

即使当垂直回扫间隔变化时，液晶显示装置的驱动方法也可以防止在垂直回扫间隔内传输到驱动电路的驱动信号与在显示周期内传输到驱动电路的驱动信号之间的争用。垂直回扫间隔后的下一帧。该装置具有像素，信号线和将灰度电压输出到信号线的驱动电路。在该方法中，使M是通过将垂直回扫间隔除以规则的水平扫描时间并将小数点后的分数四舍五入并且使N为1或更大的整数而获得的值，从中输出灰度电压在垂直回扫间隔内，驱动电路到信号线的次数在两次和（MN）次之间。