



US 20020131004A1

(19) **United States**(12) **Patent Application Publication**
Watanabe et al.(10) **Pub. No.: US 2002/0131004 A1**(43) **Pub. Date: Sep. 19, 2002**(54) **LIQUID CRYSTAL DISPLAY APPARATUS
WITH ADDRESS MARKS CONNECTED TO
CONNECTIONS****Publication Classification**(51) **Int. Cl.⁷** **G02F 1/1343**(52) **U.S. Cl.** **349/139**(76) Inventors: **Makoto Watanabe**, Tokyo (JP);
Syunsuke Shiga, Tokyo (JP)

Correspondence Address:

**DICKSTEIN SHAPIRO MORIN & OSHINSKY
LLP****Steven I. Weisburd****41st Floor****1177 Avenue of the Americas****New York, NY 10036-2714 (US)**

(57)

ABSTRACT

In a liquid crystal display apparatus including a transparent substrate, a plurality of first bus lines formed on the transparent substrate, a plurality of second bus lines formed on the transparent substrate substantially perpendicular to the first bus lines, a plurality of common electrode lines formed on the transparent substrate in parallel with the first bus lines, and a plurality of pixels each connected to one of the first bus lines, one of the second bus lines and one of the common electrode lines, a plurality of address marks are formed on the transparent substrate and each of the address marks is connected to one of the first bus lines, the second bus lines and the common electrode lines.

(21) Appl. No.: **10/098,681**(22) Filed: **Mar. 14, 2002**(30) **Foreign Application Priority Data**

Mar. 14, 2001 (JP) 2001-072536

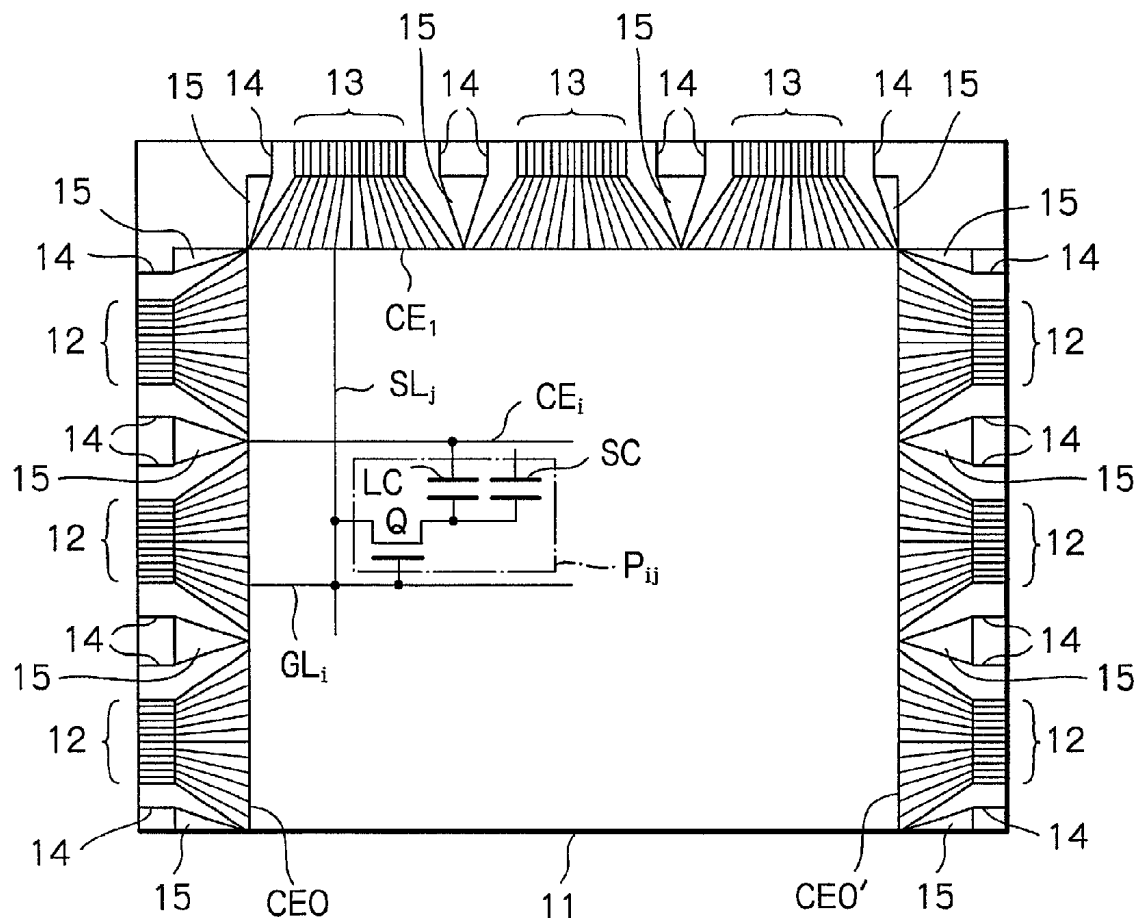


Fig. 2 PRIOR ART

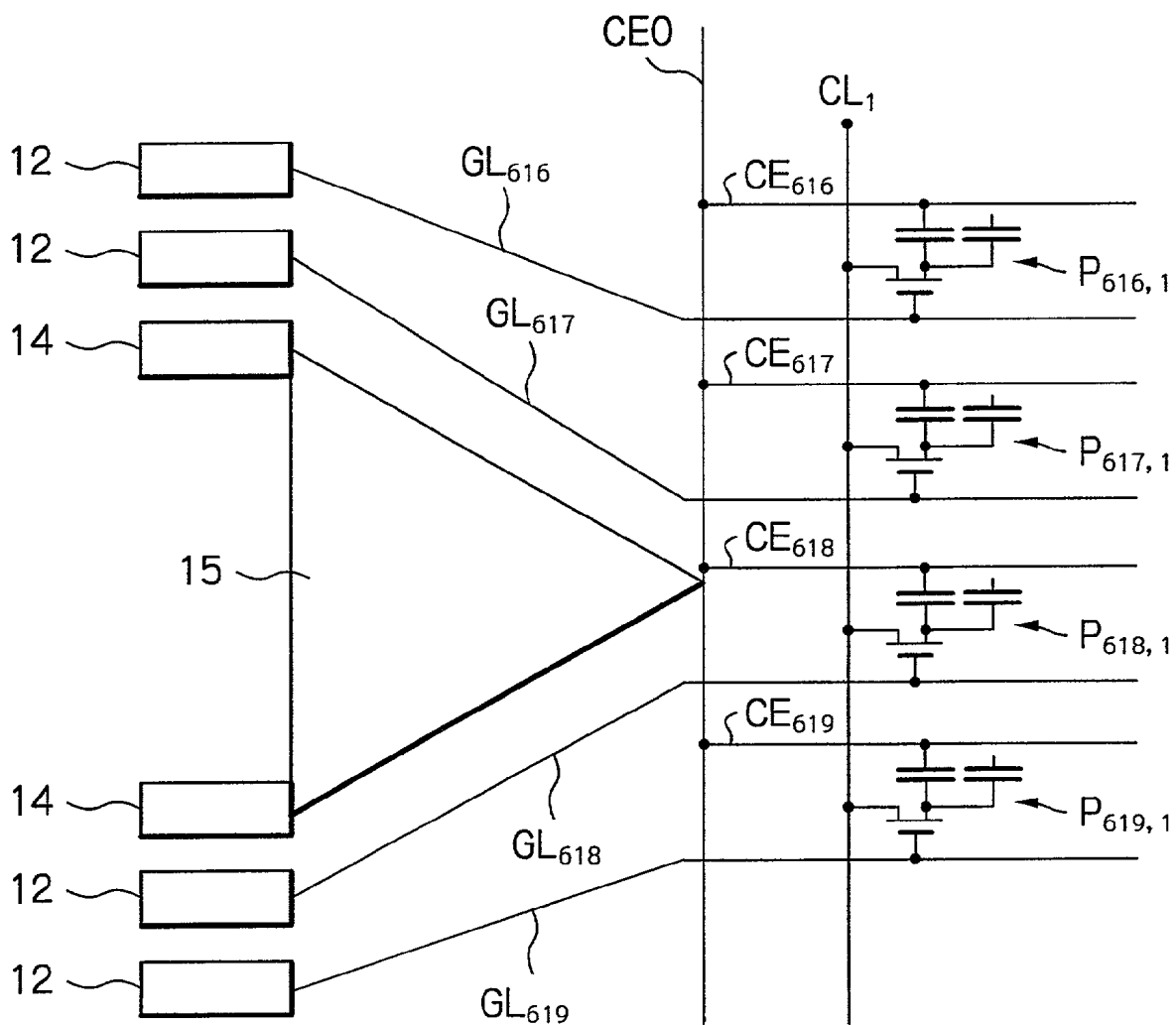


Fig. 3 PRIOR ART

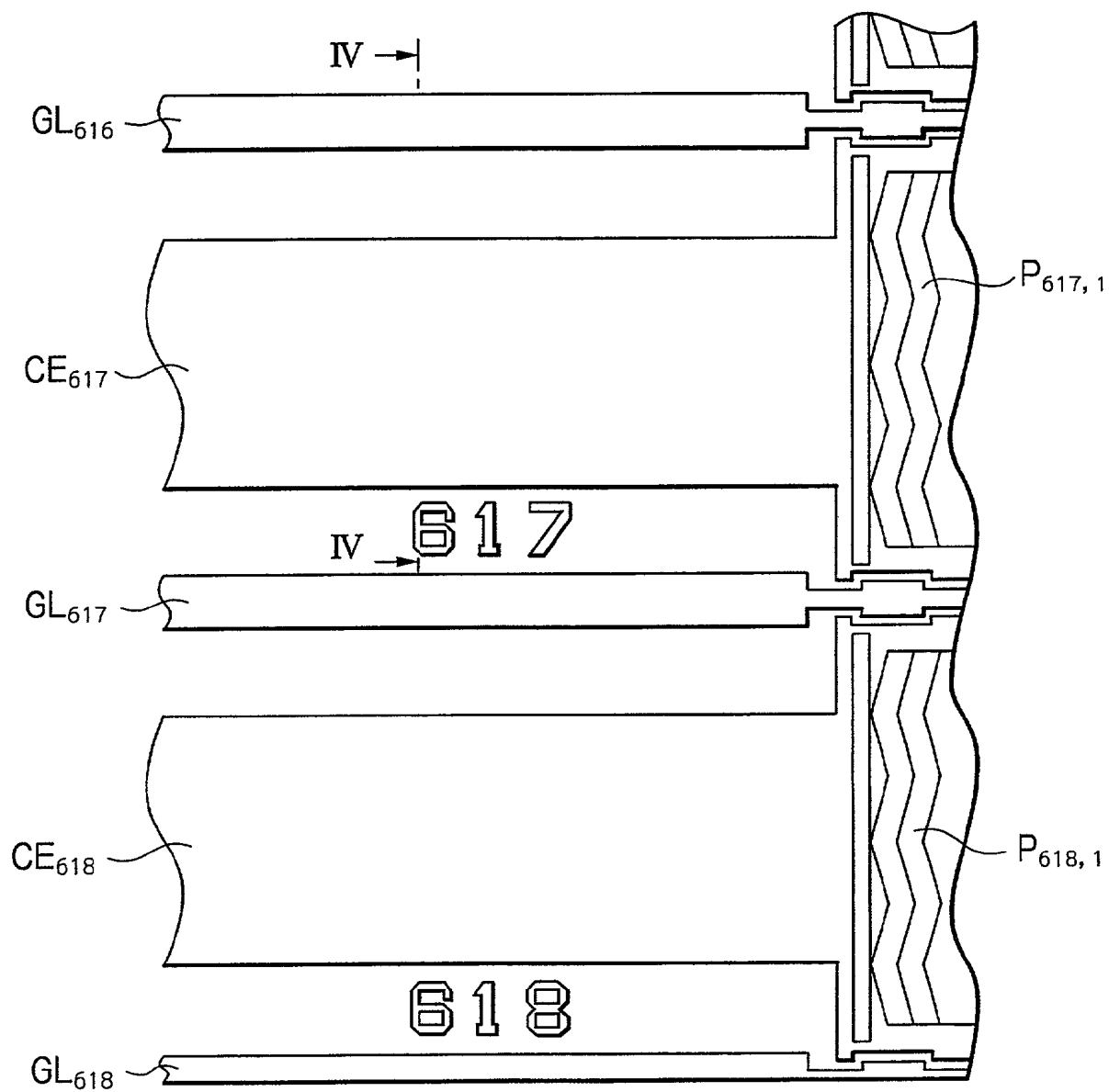


Fig. 4 PRIOR ART

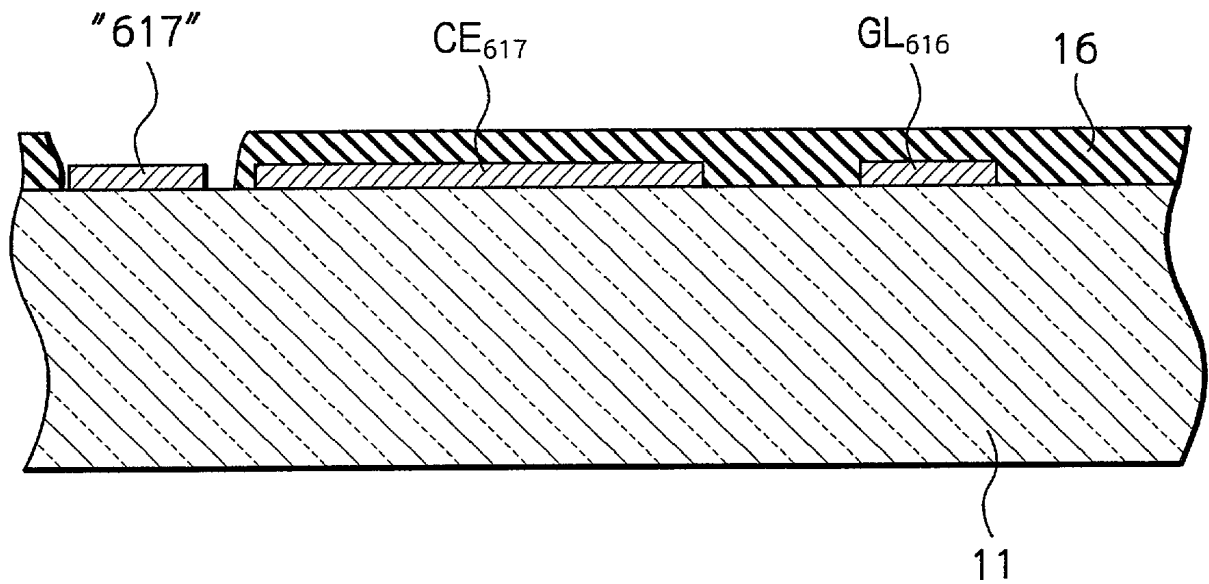


Fig. 5 PRIOR ART

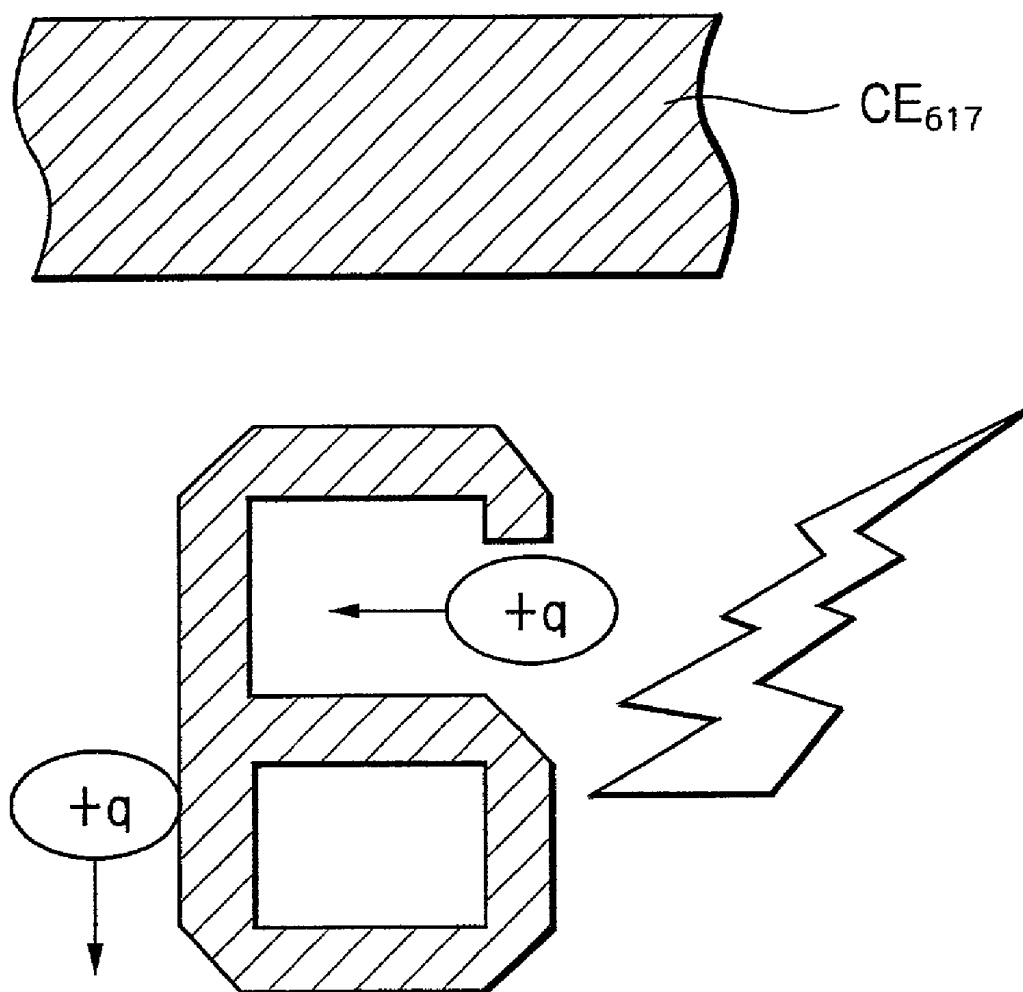


Fig. 6 PRIOR ART

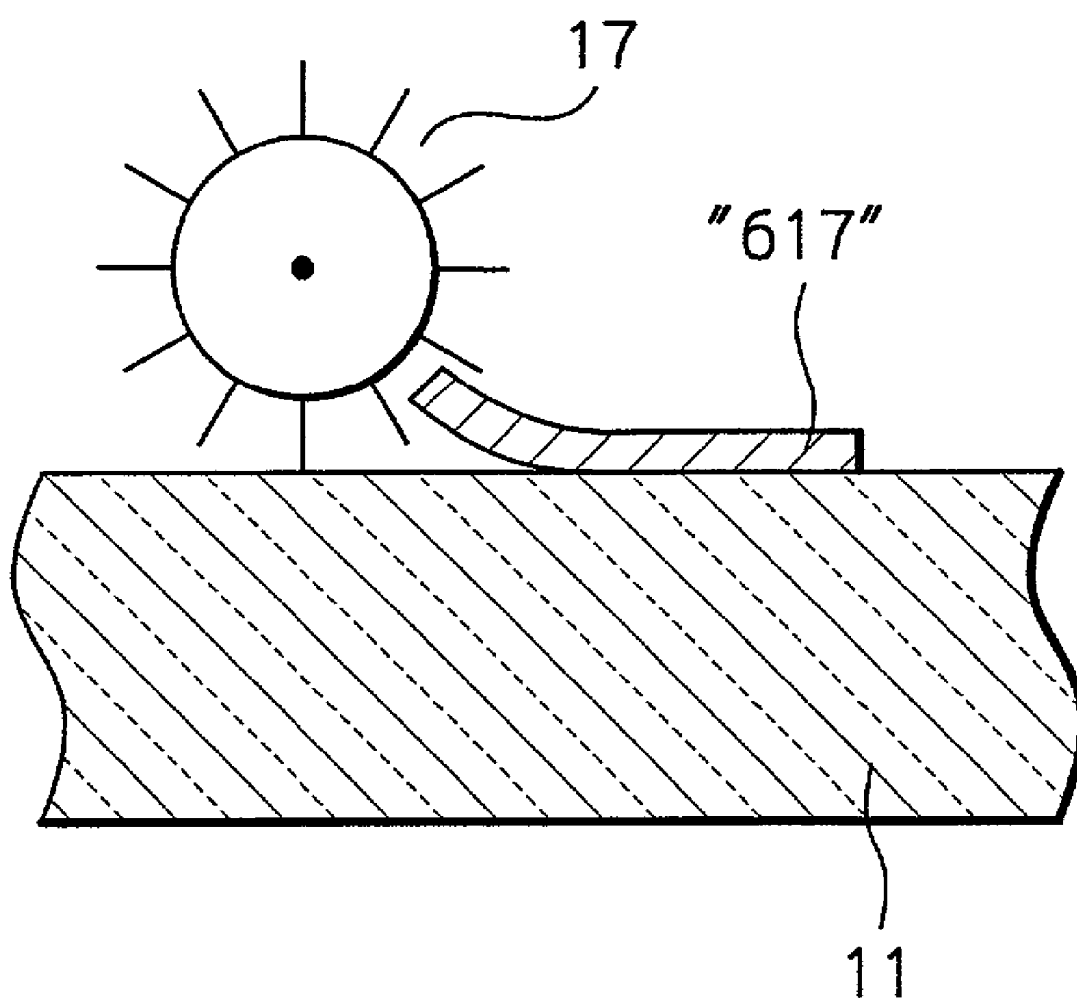


Fig. 7

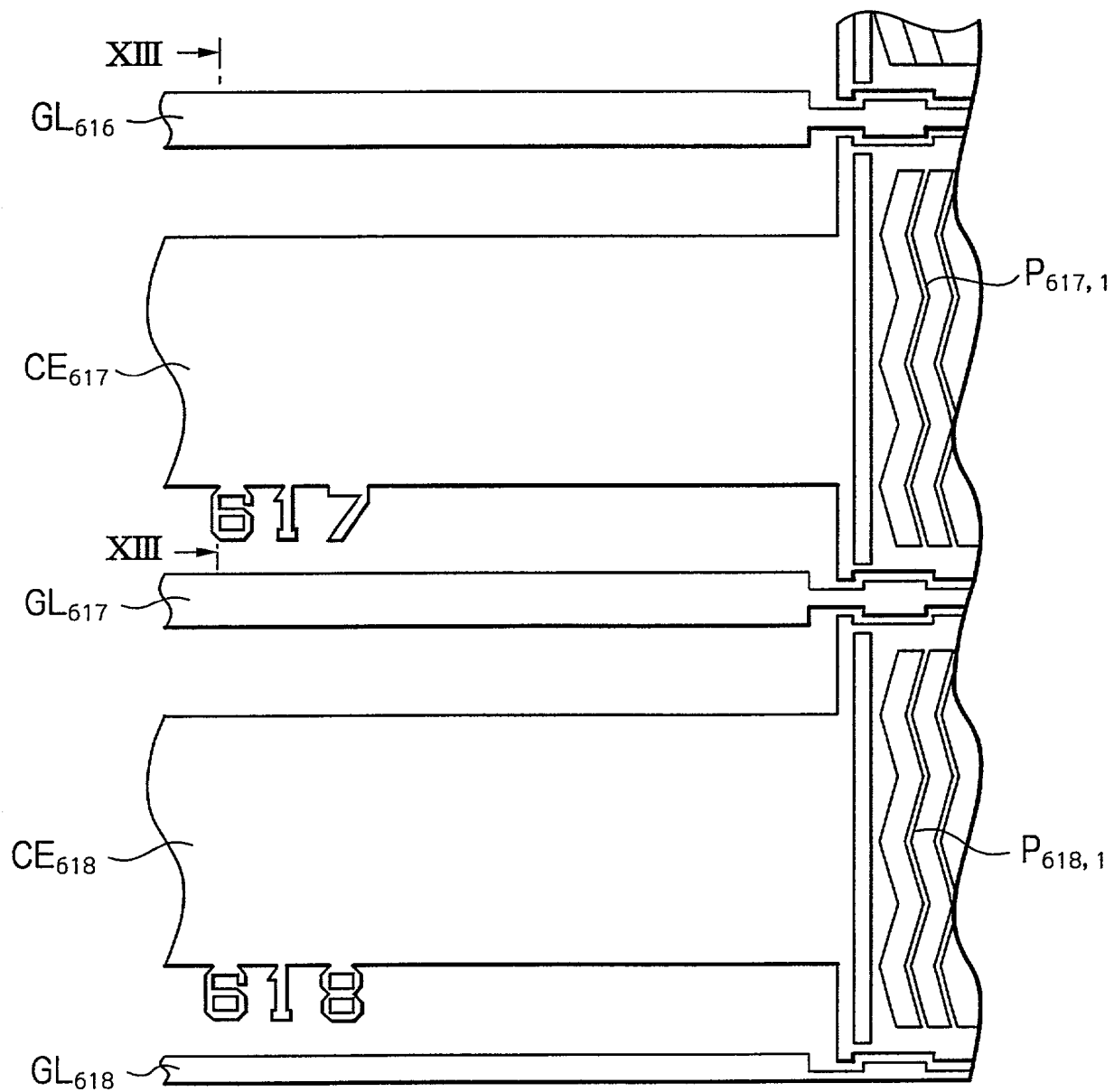


Fig. 8

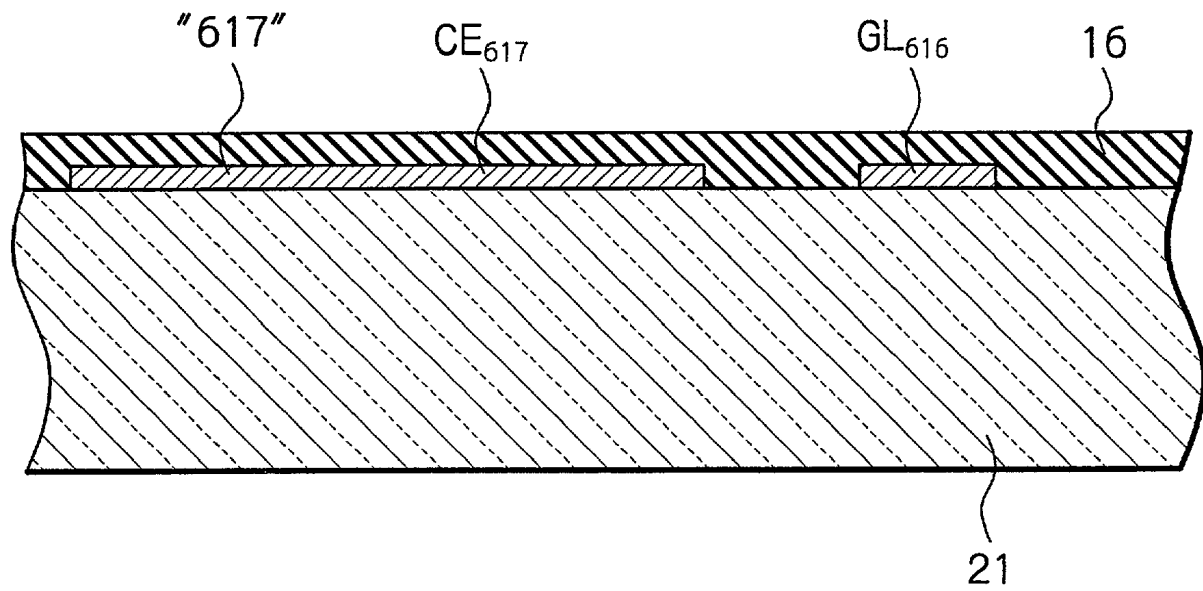


Fig. 9

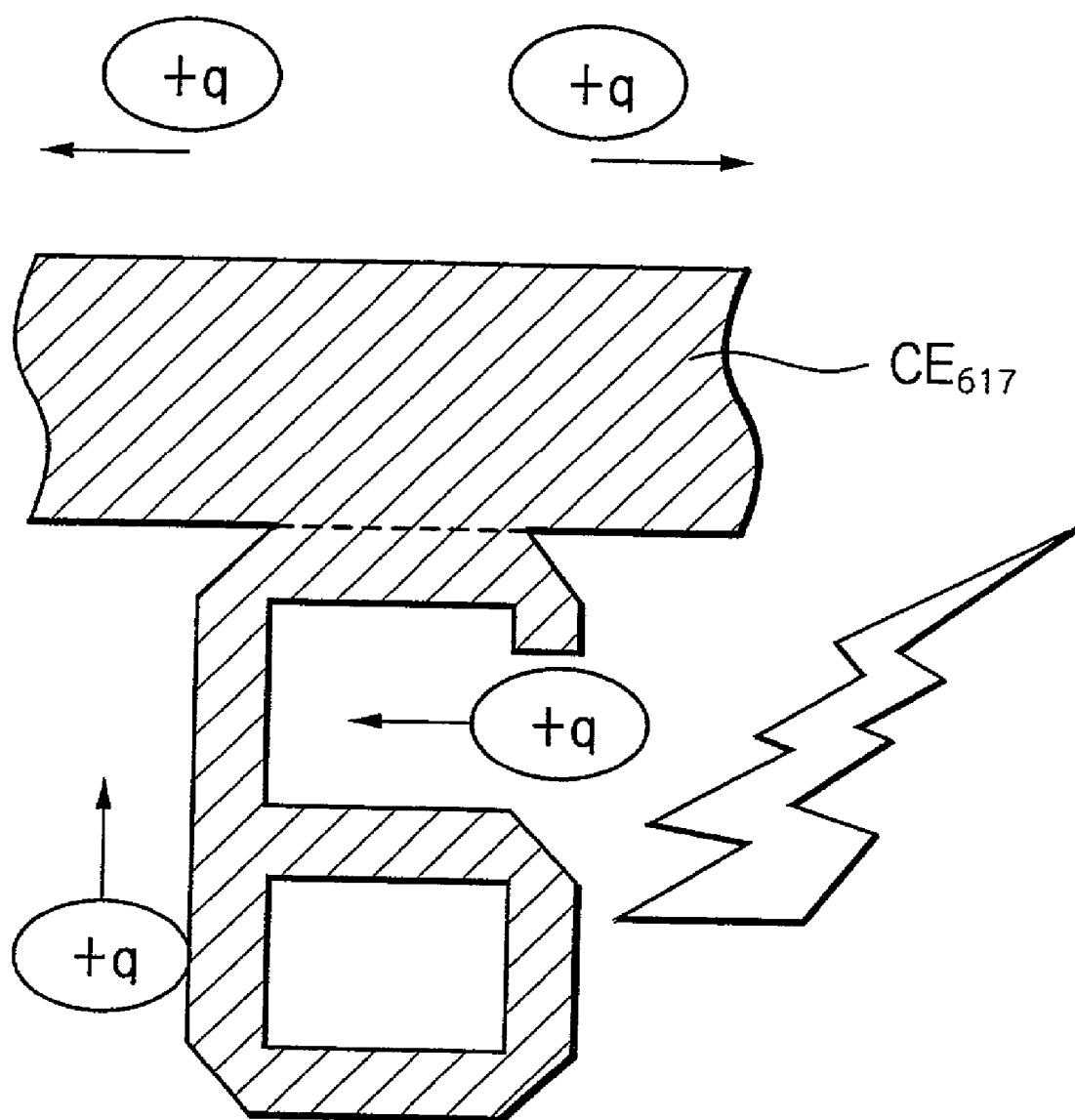


Fig. 10

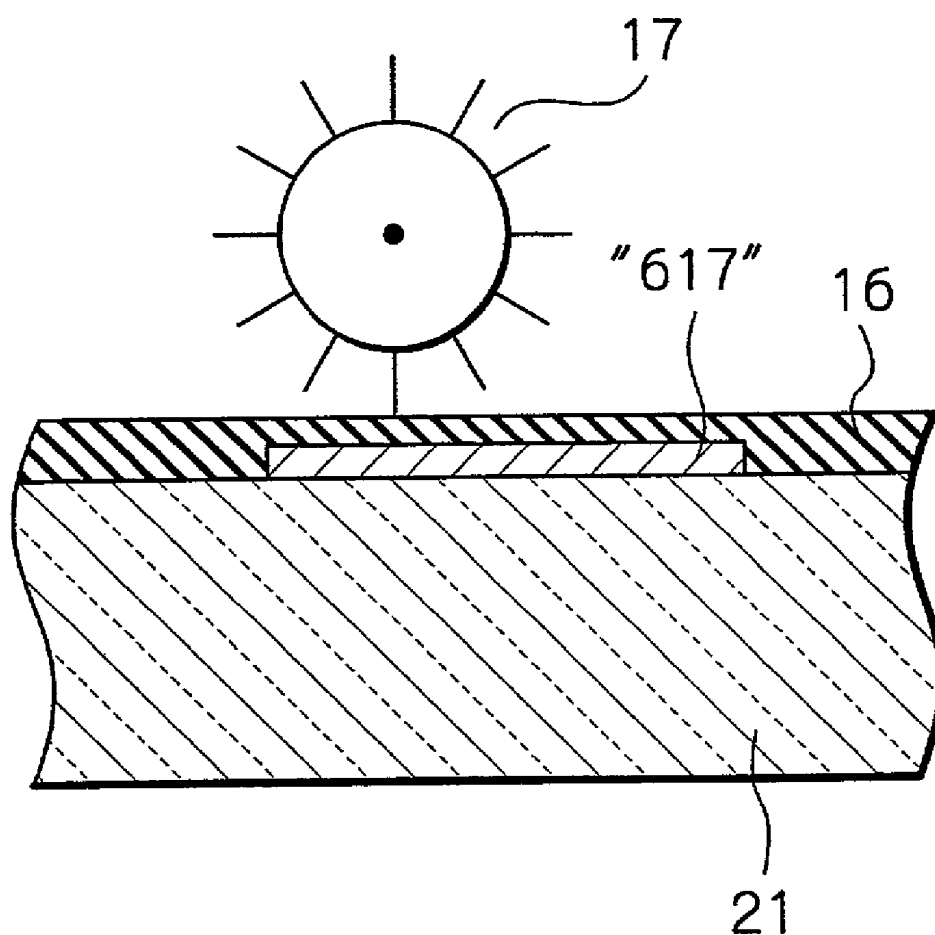
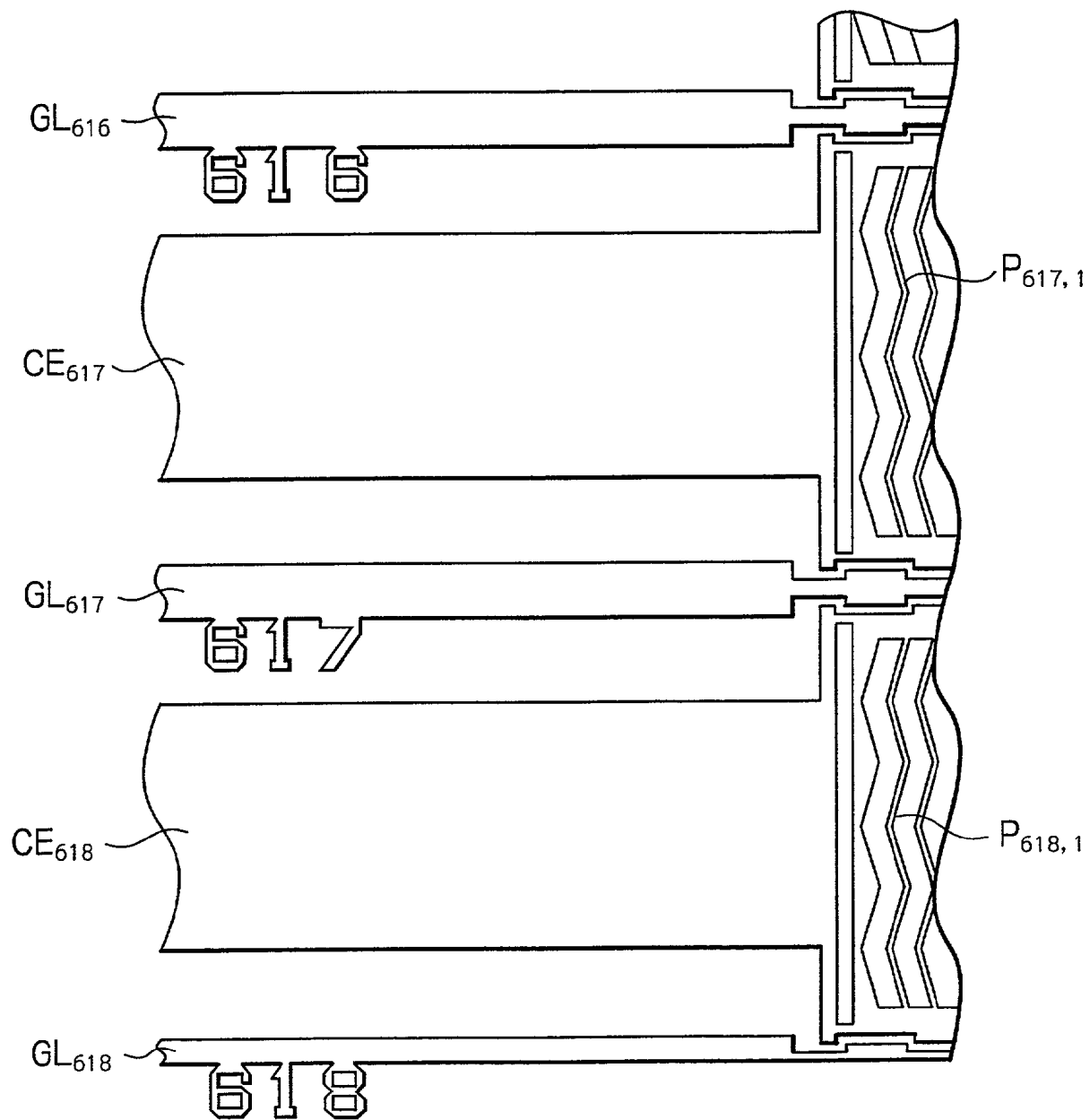


Fig. 11



LIQUID CRYSTAL DISPLAY APPARATUS WITH ADDRESS MARKS CONNECTED TO CONNECTIONS

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal display (LCD) apparatus, and more particularly, to the improvement of address marks for easily specifying a defective location in the LCD apparatus.

[0003] 2. Description of the Related Art

[0004] Generally, a prior art LCD apparatus is constructed by a transparent substrate, a plurality of gate bus lines formed on the transparent substrate, a plurality of signal bus lines formed on the transparent substrate substantially perpendicular to the gate bus lines, a plurality of common electrode lines formed on the transparent substrate in parallel with the gate bus lines, and a plurality of pixels connected to one of the gate bus lines, one of the signal bus lines and one of the common electrode lines.

[0005] During an inspection mode, in order to easily specify a defective location, a plurality of address marks are provided for the gate bus lines (the common electrode lines) and the signal bus lines (see JP-A-2000-147549). This will be explained later in detail.

[0006] In the above-described prior art LCD apparatus, however, there are the following problems. First, when a static charge is transferred by means of a spark or the like to one address mark, since the address mark is electrically isolated, the static charge is consumed as Joule heat therein, so that the address mark is melted, which would generate defects by dust. Second, if each of the address marks serves as a test pad so that the address marks are exposed to the air, when a rubbing process using a rubbing roller is performed upon the address marks, the address marks are peeled off, which also would generate defects by dust.

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide an LCD apparatus with address marks capable of avoiding defects by dust.

[0008] According to the present invention, in an LCD apparatus including a transparent substrate, a plurality of first bus lines formed on the transparent substrate, a plurality of second bus lines formed on the transparent substrate substantially perpendicular to the first bus lines, a plurality of common electrode lines formed on the transparent substrate in parallel with the first bus lines, and a plurality of pixels each connected to one of the first bus lines, one of the second bus lines and one of the common electrode lines, a plurality of address marks are formed on the transparent substrate and each of the address marks is connected to one of the first bus lines, the second bus lines and the common electrode lines. Thus, since each of the address marks is connected to one of the bus lines and the common electrode lines, even if a static charge is transferred to one of the address marks, the static charge is transferred to the bus lines or the common electrode lines, which would avoid defects by dust.

[0009] Also, the address marks are covered by an insulating layer. Thus, even if a rubbing process is performed upon the address marks, the address marks are hardly peeled off, which also would avoid defects by dust.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The present invention will be more clearly understood from the description set forth below, as compared with the prior art, with reference to the accompanying drawings, wherein:

[0011] FIG. 1 is a plan view illustrating a prior art LCD apparatus;

[0012] FIG. 2 is a partial circuit diagram of the LCD apparatus of FIG. 1;

[0013] FIG. 3 is a plan view of the address marks of FIG. 2;

[0014] FIG. 4 is a cross-sectional view taken along the line IV-IV of FIG. 3;

[0015] FIG. 5 is a plan view for explaining a problem in the address marks of FIG. 3;

[0016] FIG. 6 is a cross-sectional view for explaining another problem in the address marks of FIG. 3;

[0017] FIG. 7 is a plan view illustrating a first embodiment of the LCD apparatus according to the present invention;

[0018] FIG. 8 is a cross-sectional view taken along the line VIII-VIII of FIG. 7;

[0019] FIG. 9 is a plan view for explaining an effect in the address marks of FIG. 7;

[0020] FIG. 10 is a cross-sectional view for explaining another effect in the address marks of FIG. 7; and

[0021] FIG. 11 is a plan view illustrating a second embodiment of the LCD apparatus according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] Before the description of the preferred embodiments, a prior art LCD apparatus will be explained with reference to FIGS. 1, 2, 3, 4, 5 and 6.

[0023] In FIG. 1, which is a plan view illustrating a prior art LCD apparatus, a gate bus line GL_i ($i=1, 2, \dots, m$) and a signal bus lines SL_j ($j=1, 2, \dots, n$) are provided on a transparent substrate 17, and a pixel P_{ij} is provided at an intersection between the gate bus line GL_i and the signal bus line SL_j . Also, the pixel P_{ij} is constructed by a thin film transistor (TFT) Q, a liquid crystal cell LC and a storage capacitor SC. In this case, the liquid crystal cell LC is connected to a common electrode line CE_j arranged in parallel with the gate bus line GL_i . Also, the storage capacitor SC is connected to an adjacent gate line in a gate storage type or a storage line (not shown) in a storage capacitor type, thereby substantially increasing the capacitance of the liquid crystal cell LC.

[0024] Also, gate (scan) terminals 12 are provided on the transparent substrate 11 and one of the scan terminals 12 is connected to the gate bus line GL_i . Similarly, signal termi-

nals 13 are provided on the transparent substrate 11 and one of the signal terminals 13 is connected to the signal bus line SL_j .

[0025] Further, common terminals 14 and terminal blocks 15 are provided and are connected to the common electrode line CE_i . The common electrode line CE_i is connected to two main common electrode lines CE_0 and CE_0' which are connected via the terminal blocks 15 to the common terminals 14. Note that FIG. 2 illustrates a partial circuit diagram of the LCD apparatus of FIG. 1 around the main common electrode line CE_0 .

[0026] In the LCD apparatus of FIG. 1 and 2, in order to easily specify a defective location, an address mark is provided for the gate bus line GL_i and the common electrode line CE_i ($i=1, 2, \dots, m$) as illustrated in FIG. 3 (see FIG. 3 of JP-A-2000-147549). For example, a scan address mark "617" is provided for the gate bus line GL_{617} and the common electrode line CE_{617} , and a scan address mark "618" is provided for the gate bus line GL_{618} and the common electrode line CE_{618} .

[0027] As illustrated in FIG. 4, the address marks "617", "618", . . . are made of the same material of the common electrode lines CE_i ($i=1, 2, \dots, m$). For example, this material is Cr, Al or Mo. In this case, if each of the address marks serves as a test pad, although the gate bus line GL_i and the common electrode line CE_i are covered by an insulating layer 16 made of silicon oxide or silicon nitride, the address marks are exposed to the air.

[0028] The address marks of FIGS. 3 and 4 have the following problems. First, as illustrated in FIG. 5, when a static charge +q is transferred by means of a spark or the like to one address mark, the static charge +q is consumed as Joule heat therein, so that the address mark is melted, which would generate defects by dust. Second, if each of the address marks serves as a test pad so that the address marks are exposed to the air, as illustrated in FIG. 6, when a rubbing process using a rubbing roller 17 is performed upon the address marks, the address marks are peeled off, which also would generate defects by dust.

[0029] In FIG. 7, which illustrates a first embodiment of the LCD apparatus according to the present invention, an address marks provided for the gate bus line GL_i and the common electrode line CE_i ($i=1, 2, \dots, m$) is connected to the common electrode line CE_i ($i=1, 2, \dots, m$). For example, a scan address mark "617" is connected to the common electrode line CE_{617} , and a scan address mark "618" is connected to the common electrode line CE_{618} .

[0030] As illustrated in FIG. 8, the address marks "617", "618", . . . are made of the same material as the common electrode lines CE_i ($i=1, 2, \dots, m$). For example, this material is Cr, Al or Mo. In this case, the address marks as well as the gate bus line GL_i and the common electrode line CE_i are covered by an insulating layer 16 made of silicon oxide or silicon nitride, so that the address marks are not exposed to the air.

[0031] The address marks of FIGS. 7 and 8 have the following effects. First, as illustrated in FIG. 9, when a static charge +q is transferred by means of a spark or the like to one address mark, the static charge +q is transferred to the common electrode line CE_{617} , so that the address mark is not melted, which would not generate defects by dust. Second,

since the address marks are not exposed to the air, as illustrated in FIG. 10, when a rubbing process using a rubbing roller 17 is carried out, the address marks are hardly peeled off due to the presence of the insulating layer 17, which would not generate defects by dust.

[0032] In FIG. 11, which illustrates a second embodiment of the LCD apparatus according to the present invention, an address mark provided for the gate bus line GL_i and the common electrode line CE_i ($i=1, 2, \dots, m$) is connected to the gate bus line GL_i ($i=1, 2, \dots, m$). For example, a scan address mark "617" is connected to the gate bus line GL_{617} , and a scan address mark "618" is connected to the gate bus line GL_{618} .

[0033] In the second embodiment, the same effects as in the first embodiment can be expected.

[0034] In the above-described embodiments, although one address mark is provided for the gate bus line GL_i and the common electrode line CE_i , one address mark can be provided for the signal bus line SL_j .

[0035] Also in the above-described embodiments, although the address marks are constructed by numerals, the address marks can be constructed by letters or combinations of numerals and letters.

[0036] As explained hereinabove, according to the present invention, defects by dust can be avoided.

1. A liquid crystal display apparatus comprising:

- a transparent substrate;
- a plurality of first bus lines formed on said transparent substrate;
- a plurality of second bus lines formed on said transparent substrate substantially perpendicular to said first bus lines;
- a plurality of common electrode lines formed on said transparent substrate in parallel with said first bus lines;
- a plurality of pixels each connected to one of said first bus lines, one of said second bus lines and one of said common electrode lines; and
- a plurality of address marks formed on said transparent substrate, each of said address marks being connected to one of said first bus lines, said second bus lines and said common electrode lines.

2. The apparatus as set forth in claim 1, wherein each of said address marks is provided at an end of said one of said first bus lines, said second bus lines and said common electrode lines.

3. The apparatus as set forth in claim 1, further comprising an insulating layer for covering said address marks.

4. The apparatus as set forth in claim 1, wherein said address marks comprise the same material as said one of said first bus lines, said second bus lines and said common electrode lines.

5. A liquid crystal display apparatus comprising:

- a transparent substrate;
- a plurality of gate bus lines formed on said transparent substrate;

- a plurality of signal bus lines formed on said transparent substrate substantially perpendicular to said gate bus lines;
 - a plurality of common electrode lines formed on said transparent substrate in parallel with said gate bus lines;
 - a plurality of pixels each connected to one of said gate bus lines, one of said signal bus lines and one of said common electrode lines; and
 - a plurality of address marks formed on said transparent substrate, each of said address marks being connected to one of said gate bus lines.
6. The apparatus as set forth in claim 5, wherein each of said address marks is provided at an end of said one of said gate bus lines.
7. The apparatus as set forth in claim 5, further comprising an insulating layer for covering said address marks.
8. The apparatus as set forth in claim 5, wherein said address marks comprise the same material as said gate bus lines.
9. A liquid crystal display apparatus comprising:
- a transparent substrate;
 - a plurality of gate bus lines formed on said transparent substrate;
 - a plurality of signal bus lines formed on said transparent substrate substantially perpendicular to said gate bus lines;
 - a plurality of common electrode lines formed on said transparent substrate in parallel with said gate bus lines;
 - a plurality of pixels each connected to one of said gate bus lines, one of said signal bus lines and one of said common electrode lines; and
 - a plurality of address marks formed on said transparent substrate, each of said address marks being connected to one of said signal bus lines.

10. The apparatus as set forth in claim 9, wherein each of said address marks is provided at an end of said one of said signal bus lines.

11. The apparatus as set forth in claim 9, further comprising an insulating layer for covering said address marks.

12. The apparatus as set forth in claim 9, wherein said address marks comprise the same material as said signal bus lines.

13. A liquid crystal display apparatus comprising:

- a transparent substrate;
- a plurality of gate bus lines formed on said transparent substrate;
- a plurality of signal bus lines formed on said transparent substrate substantially perpendicular to said gate bus lines;
- a plurality of common electrode lines formed on said transparent substrate in parallel with said gate bus lines;
- a plurality of pixels each connected to one of said gate bus lines, one of said signal bus lines and one of said common electrode lines; and
- a plurality of address marks formed on said transparent substrate, each of said address marks being connected to one of said common electrode lines.

14. The apparatus as set forth in claim 13, wherein each of said address marks is provided at an end of said one of said common electrode lines.

15. The apparatus as set forth in claim 13, further comprising an insulating layer for covering said address marks.

16. The apparatus as set forth in claim 13, wherein said address marks comprise the same material as said common electrode lines.

* * * * *

专利名称(译)	具有连接到连接的地址标记的液晶显示装置		
公开(公告)号	US20020131004A1	公开(公告)日	2002-09-19
申请号	US10/098681	申请日	2002-03-14
[标]申请(专利权)人(译)	滋贺县SYUNSUKE		
申请(专利权)人(译)	WATANABE MAKOTO 滋贺县SYUNSUKE		
当前申请(专利权)人(译)	WATANABE MAKOTO 滋贺县SYUNSUKE		
[标]发明人	WATANABE MAKOTO SHIGA SYUNSUKE		
发明人	WATANABE, MAKOTO SHIGA, SYUNSUKE		
IPC分类号	G02F1/136 G02F1/13 G02F1/1333 G02F1/1345 G02F1/1343		
CPC分类号	G02F1/1345 G02F1/13452 G02F2001/133354		
优先权	2001072536 2001-03-14 JP		
其他公开文献	US6812984		
外部链接	Espacenet USPTO		

摘要(译)

在液晶显示装置中，包括透明基板，形成在透明基板上的多条第一总线，形成在基本垂直于第一总线的透明基板上的多条第二总线，形成多条公共电极线所述透明基板与所述第一总线并列，所述多个像素均连接至所述第一总线之一，所述第二总线之一和所述公共电极线之一，所述透明基板上形成有多个地址标记基板和每个地址标记连接到第一总线，第二总线和公共电极线之一。

