



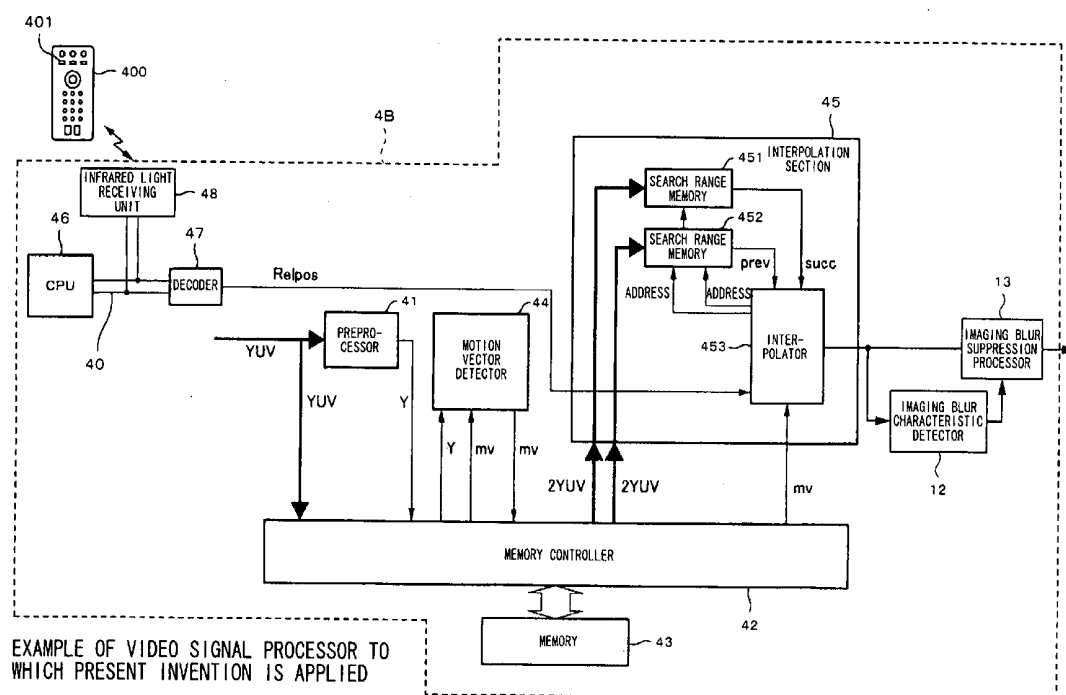
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(19) **United States**(12) **Patent Application Publication**
Miyazaki et al.(10) **Pub. No.: US 2009/0184916 A1**(43) **Pub. Date: Jul. 23, 2009**(54) **IMAGE DISPLAY APPARATUS****Publication Classification**(75) Inventors: **Shinichiro Miyazaki**, Kanagawa (JP); **Ichiro Murakami**, Tokyo (JP); **Toru Nishi**, Kanagawa (JP)(51) **Int. Cl.**
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WESTFIELD, NJ 07090 (US)(52) **U.S. Cl. 345/102; 386/126; 386/E05.001**(73) Assignee: **Sony Corporation**, Tokyo (JP)(21) Appl. No.: **12/226,595**(22) PCT Filed: **Feb. 20, 2008**(86) PCT No.: **PCT/JP2008/052903**§ 371 (c)(1),
(2), (4) Date: **Oct. 20, 2008**(30) **Foreign Application Priority Data**

Feb. 20, 2007 (JP) 2007-039559

(57) **ABSTRACT**

The present invention provides an image display apparatus capable of reducing a hold blur in accordance with circumstances. A black inserting process for inserting a black display area into a display screen in a liquid crystal display panel 2 according to at least one of substance of a video signal in an original frame and brightness of viewing environment for user is performed. Concretely, for example, when a video signal in the original frame is a cinema signal (film signal), the black inserting process of inserting a black display area into the display screen in the liquid crystal display panel 2 is performed. More concretely, for example, a backlight driving unit 71 performs switching drive between turn-on and turn-off of a backlight 72 so that the black inserting process is performed on the display screen in the liquid crystal display panel 2.



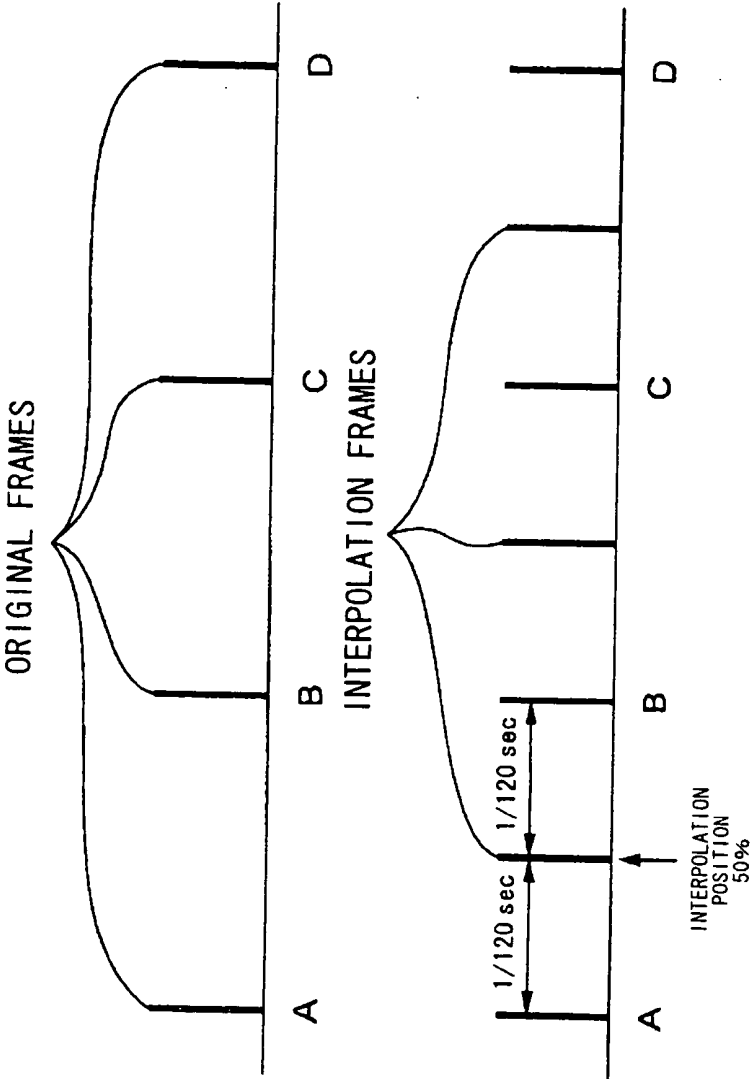
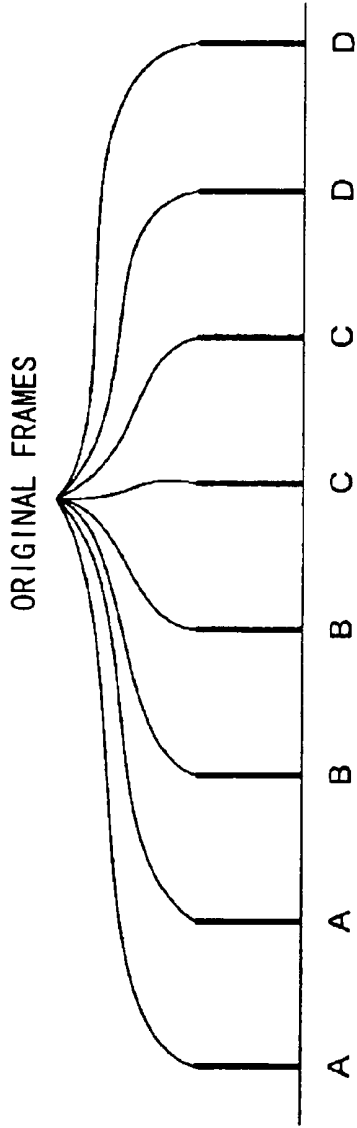


FIG. 1 (a)

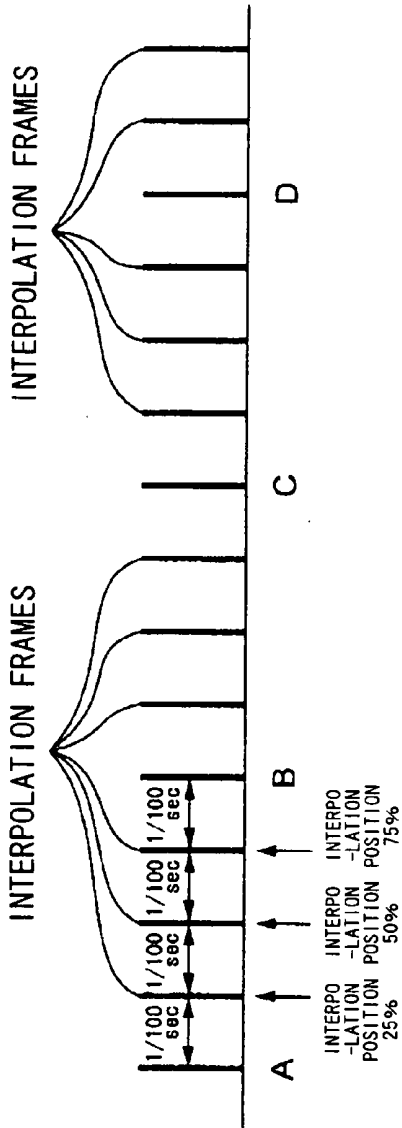
FIG. 1 (b)

FRAME RATE CONVERSION OF CAMERA SIGNAL



50Hz

FIG. 2 (a)

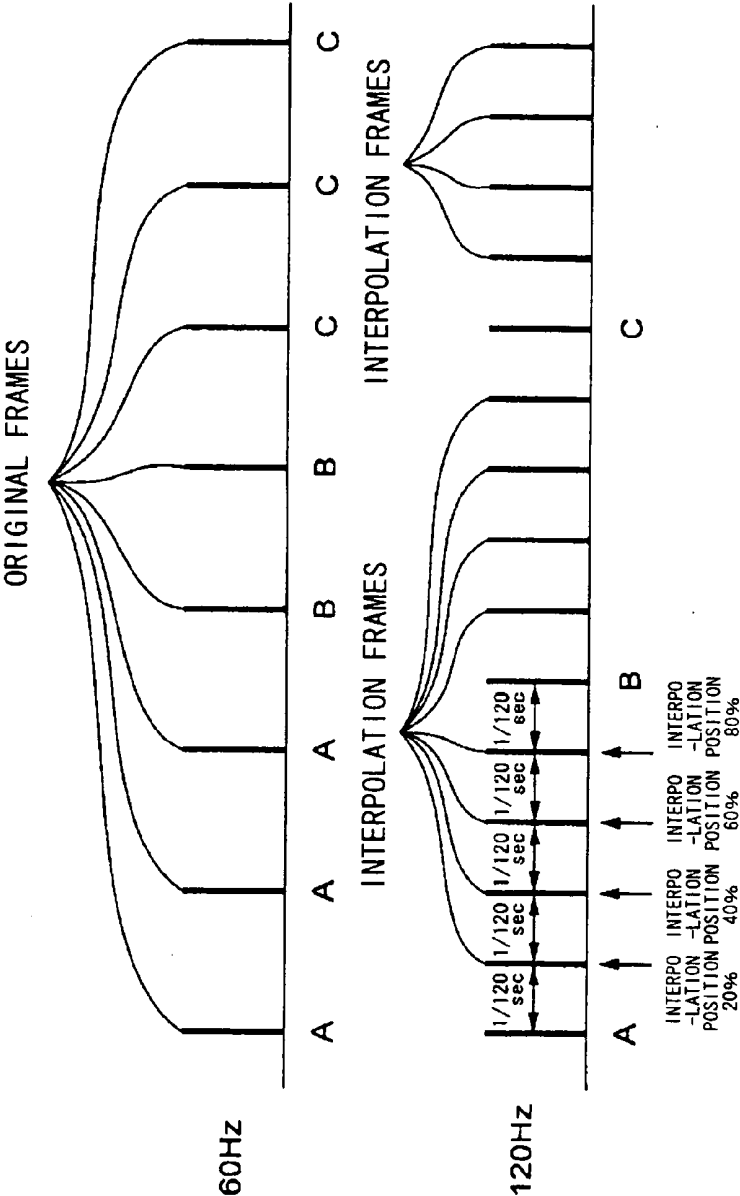


100Hz

FIG. 2 (b)

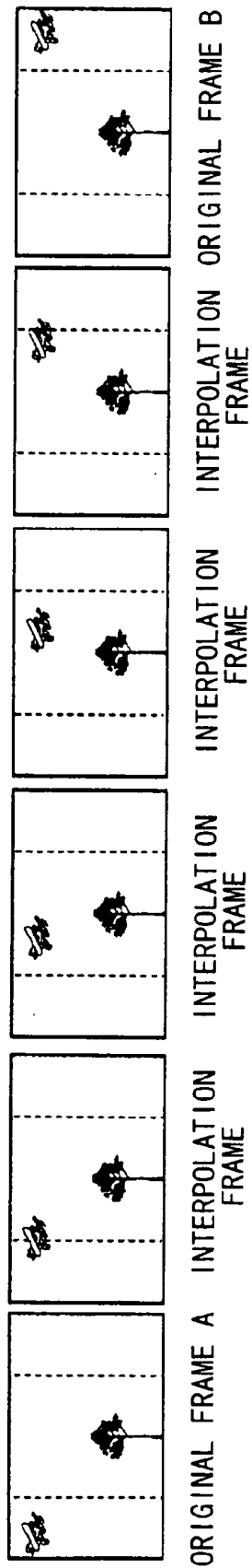
1:4 FRAME RATE CONVERSION

(2:2 PULLDOWN)



FRAME RATE CONVERSION OF FILM SIGNAL (3:2 PULLDOWN)

FIG. 3



EXAPMLE OF FRAME-RATE-CONVERTED VIDEO IMAGES OF RELATED ART

FIG. 4

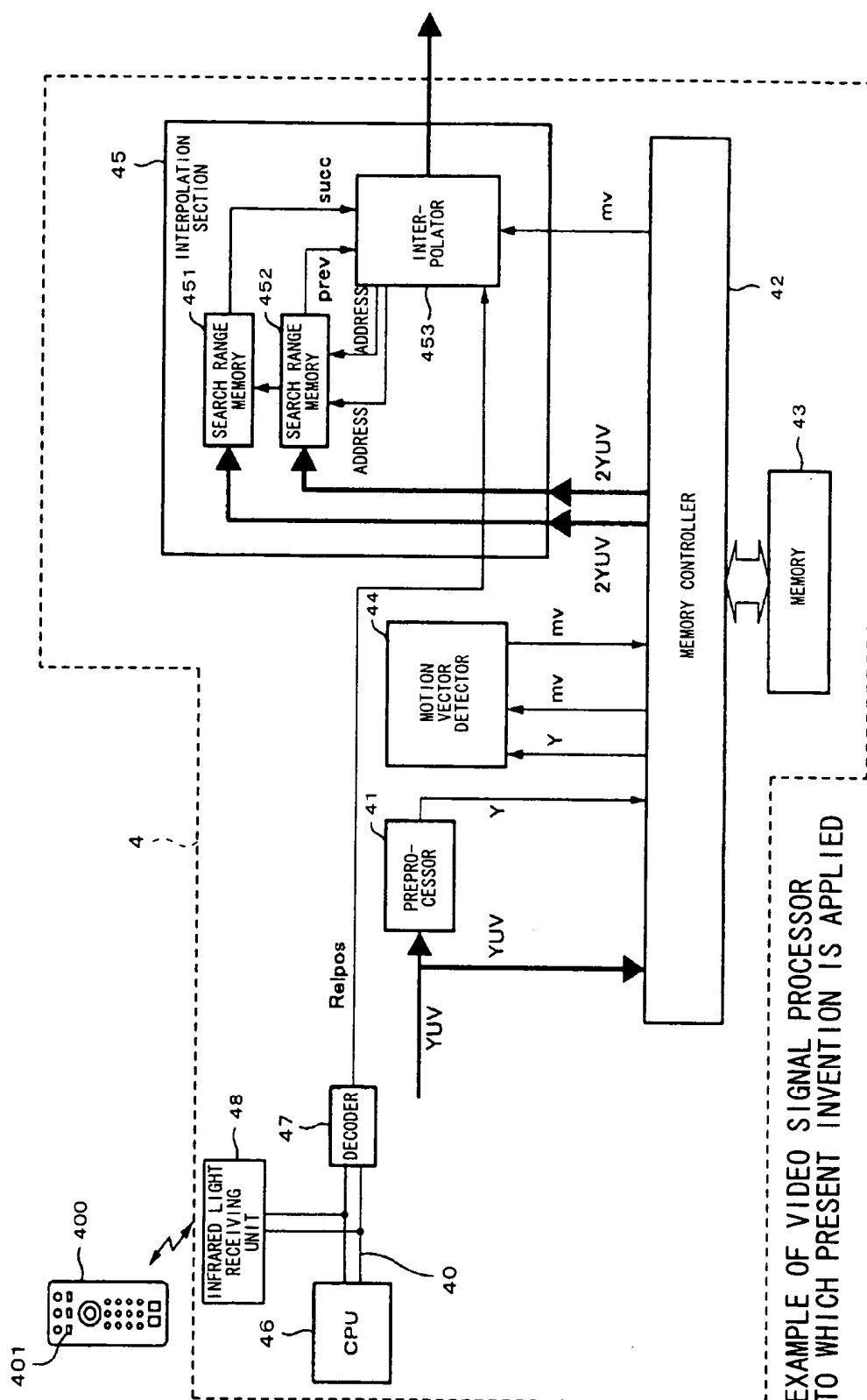
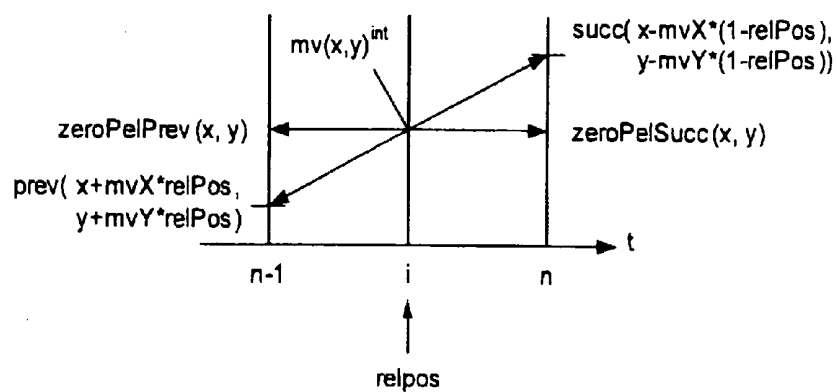


FIG. 5



PRINCIPLE OF ADDRESS CALCULATIN IN INTERPOLATOR

FIG. 6

Out_phase	0	1	2	3	4
2:2 PULLDOWN	Relpos_22_0 [5:0]	Relpos_22_1 [5:0]	Relpos_22_2 [5:0]	Relpos_22_3 [5:0]	
3:2 PULLDOWN	Relpos_32_0 [5:0]	Relpos_32_1 [5:0]	Relpos_32_2 [5:0]	Relpos_32_3 [5:0]	Relpos_32_4 [5:0]

PARAMETERS OF INTERPOLATION POSITION OF EACH FRAME

FIG. 7

3:2 PULLDOWN	Relpos_32_0 [5:0]	Relpos_32_1 [5:0]	Relpos_32_2 [5:0]	Relpos_32_3 [5:0]	Relpos_32_4 [5:0]
STRONG	0.	0.2.	0.4.	0.6.	0.8.
INTERMEDIATE	0.	0.15.	0.3.	0.7	0.85.
WEAK	0.	0.1.	0.2.	0.8	0.9.

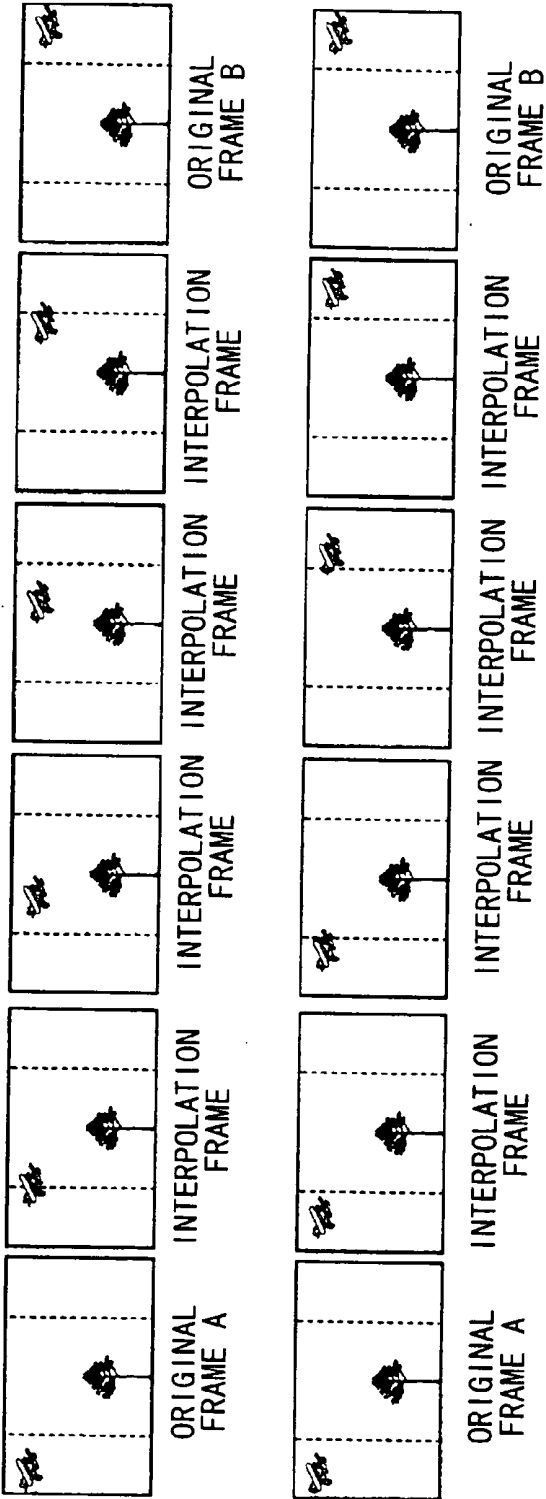
EXAMPLE OF PARAMETERS OF INTERPOLATION POSITION
IN THE CASE OF 3:2 PULLDOWN FILM SIGNAL

FIG. 8

2:2 PULLDOWN	Relpos_22_0 [5:0]	Relpos_22_1 [5:0]	Relpos_22_2 [5:0]	Relpos_22_3 [5:0]
STRONG	0.	0.25.	0.5.	0.75.
INTERMEDIATE	0.	0.15.	0.3.	0.85
WEAK	0.	0.1.	0.2.	0.9

EXAMPLE OF PARAMETERS OF INTERPOLATION POSITION
IN THE CASE OF 2:2 PULLDOWN FILM SIGNAL

FIG. 9



EXAMPLE OF FRAME-RATE-CONVERTED VIDEO IMAGE

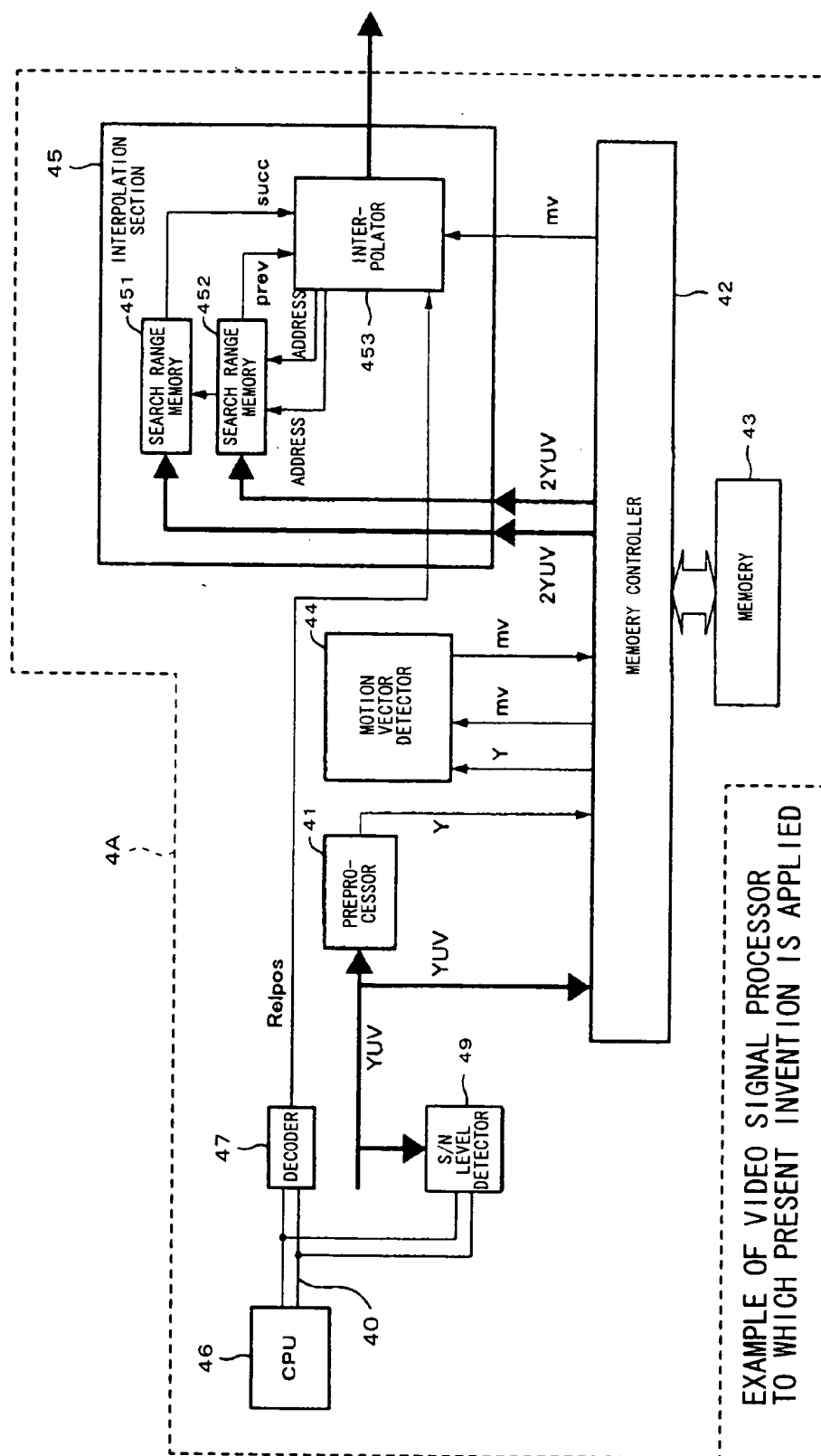


FIG. 11

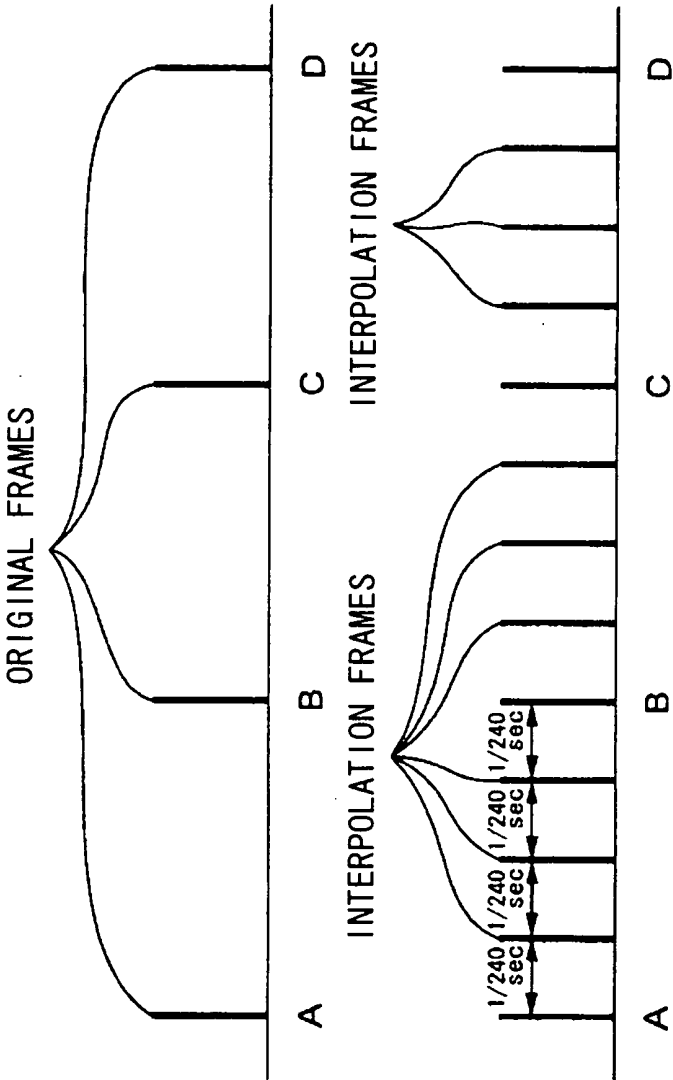


FIG. 12 (a)

FIG. 12 (b) 1:4 FRAME RATE CONVERSION

FRAME RATE CONVERSION TO 240 Hz OF CAMERA SIGNAL

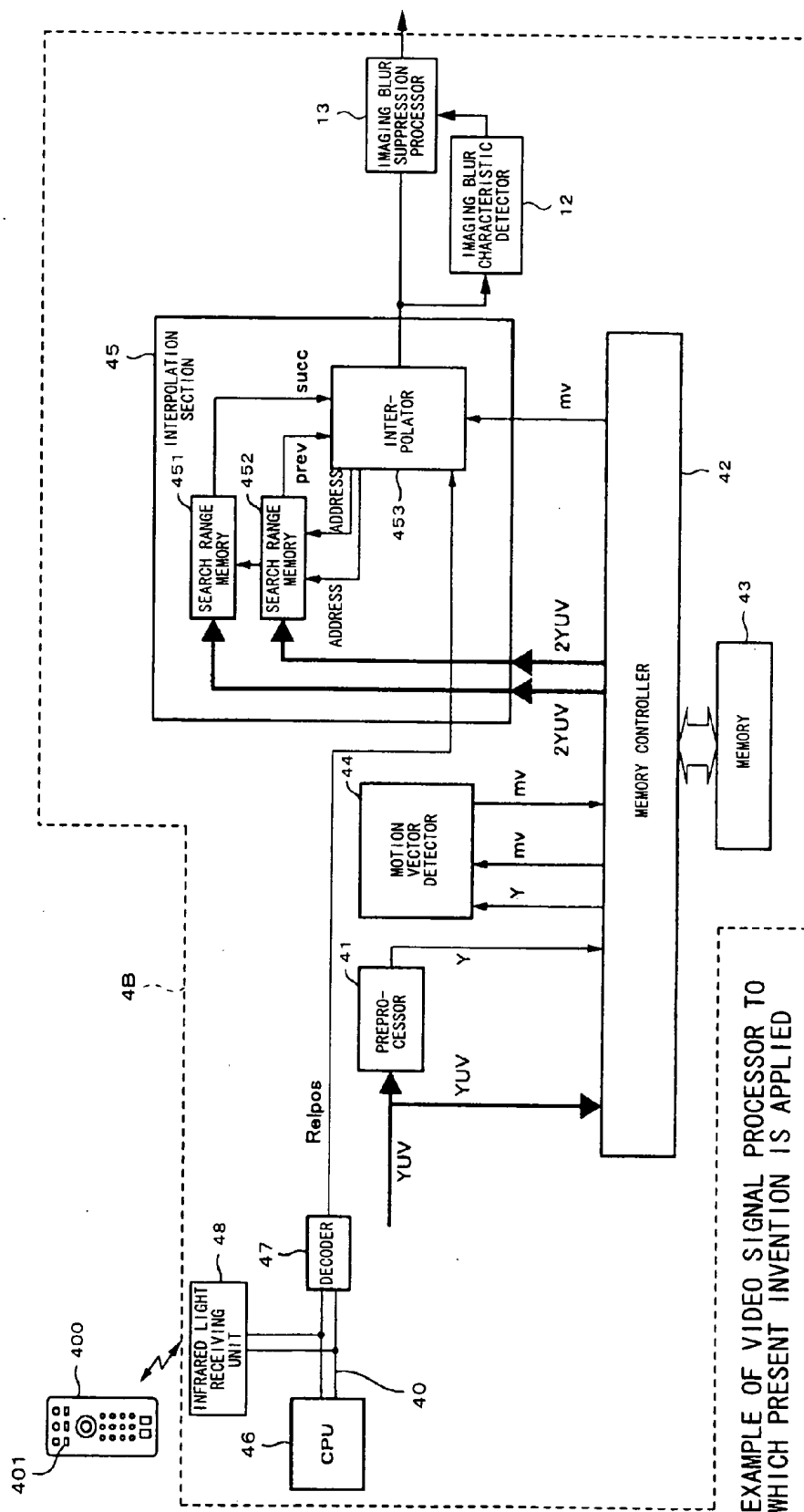


FIG. 13

EXAMPLE OF VIDEO SIGNAL PROCESSOR TO WHICH PRESENT INVENTION IS APPLIED

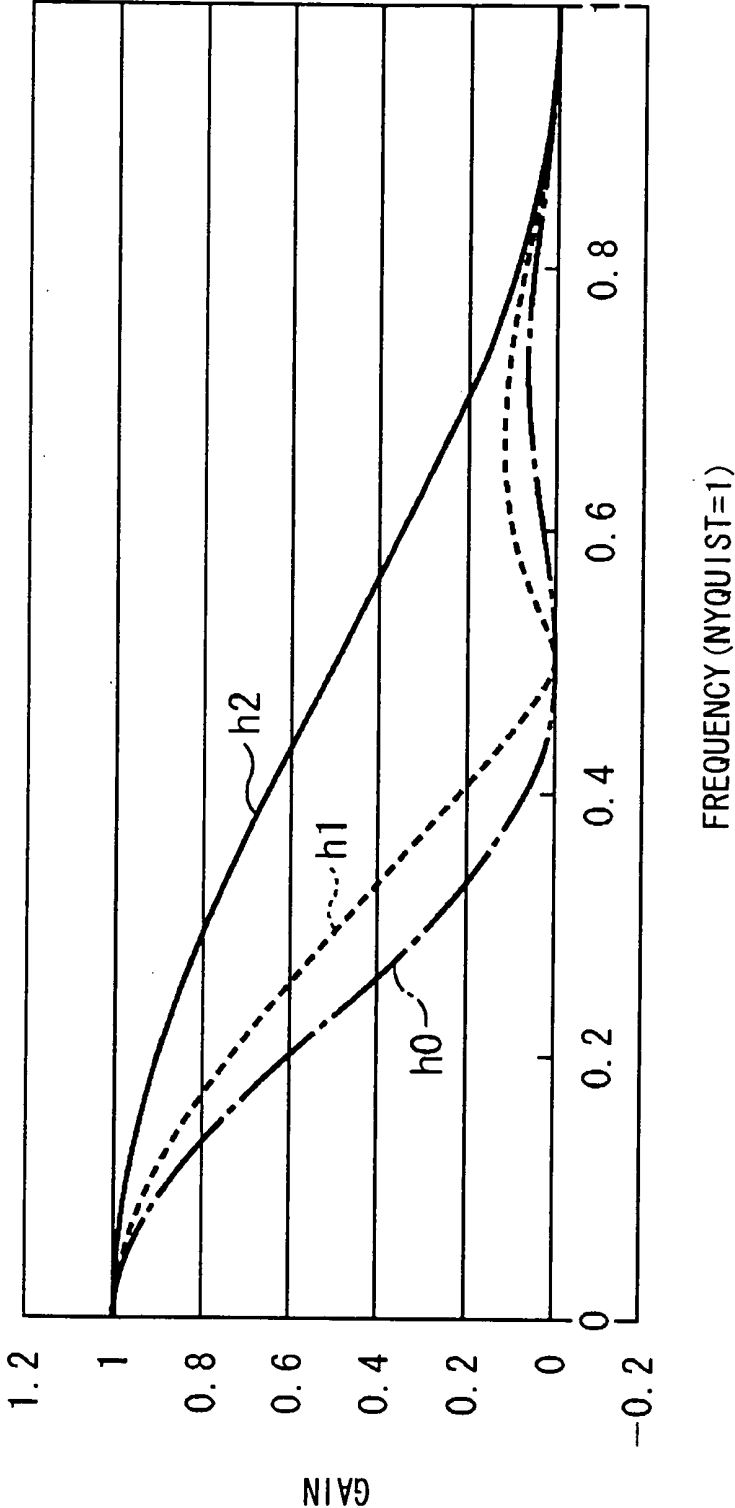


FIG. 14

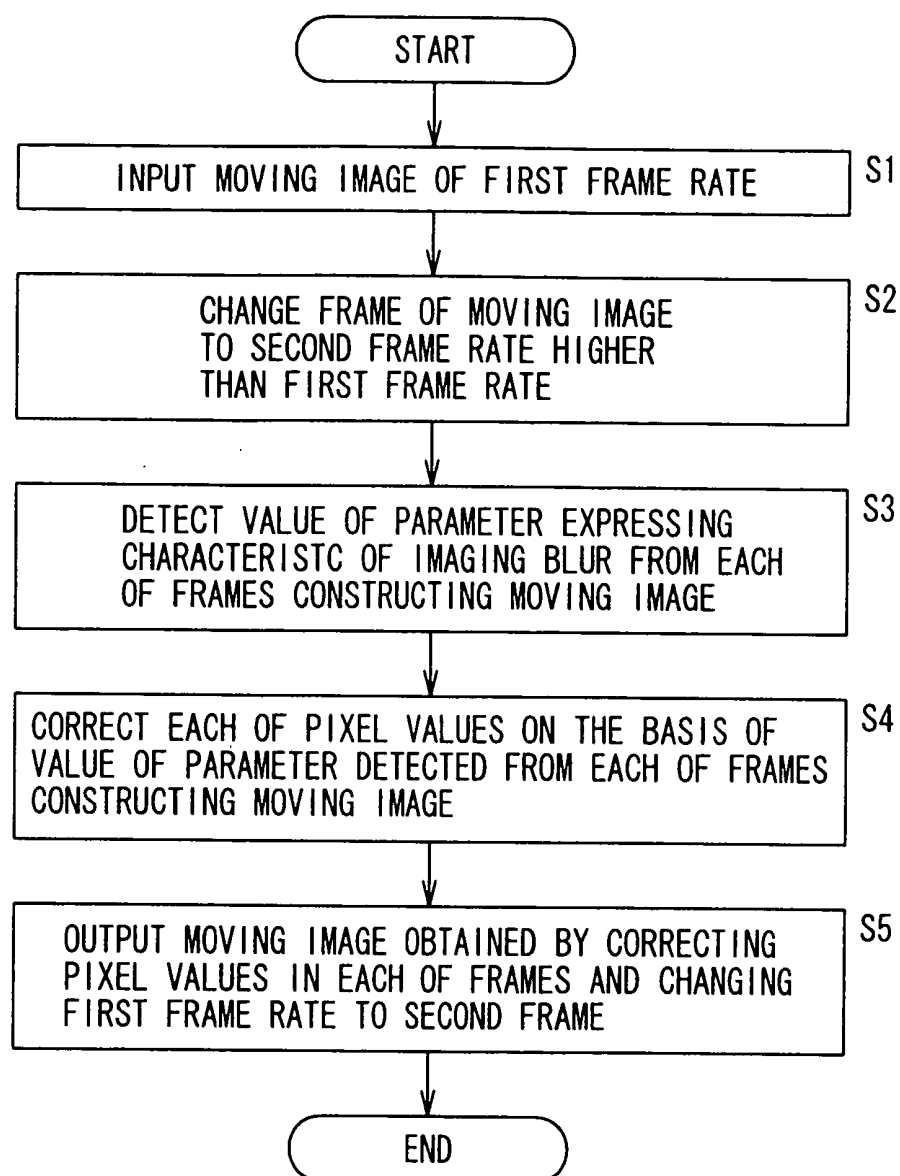


FIG. 15

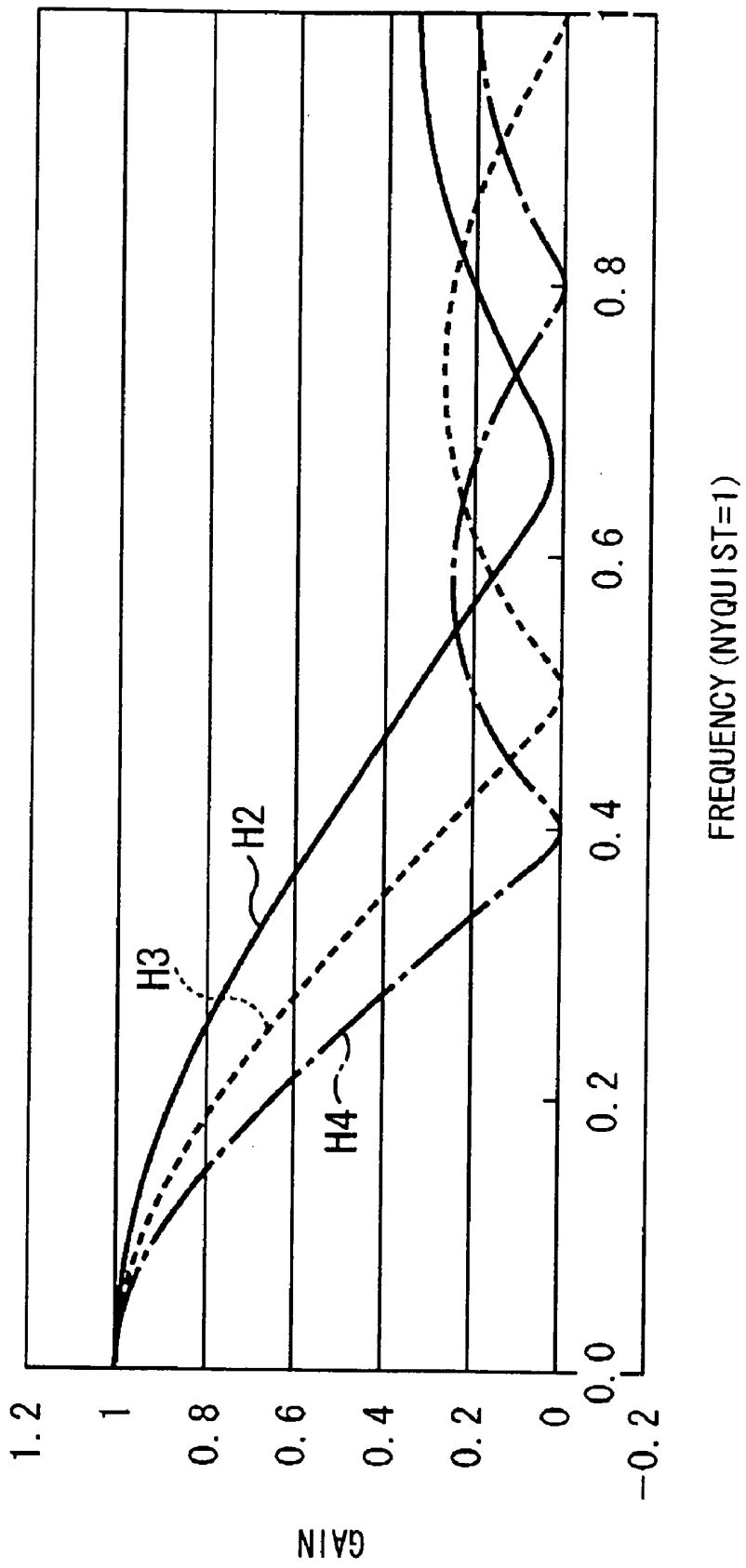


FIG. 16

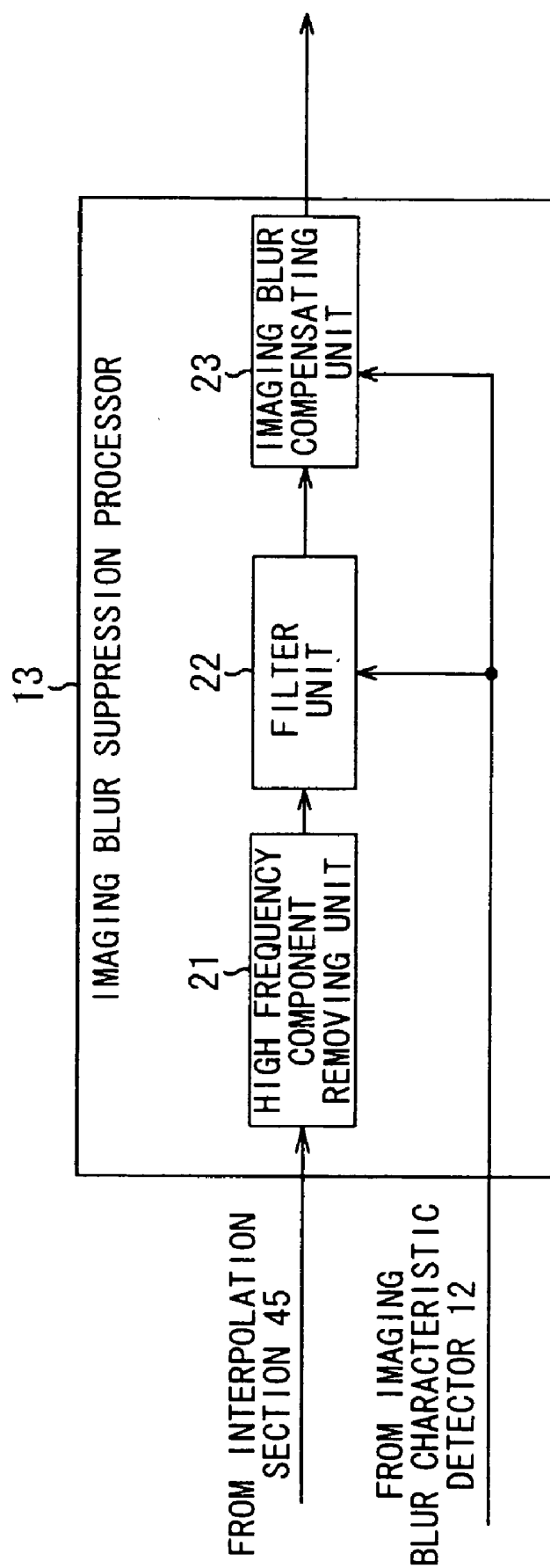


FIG. 17

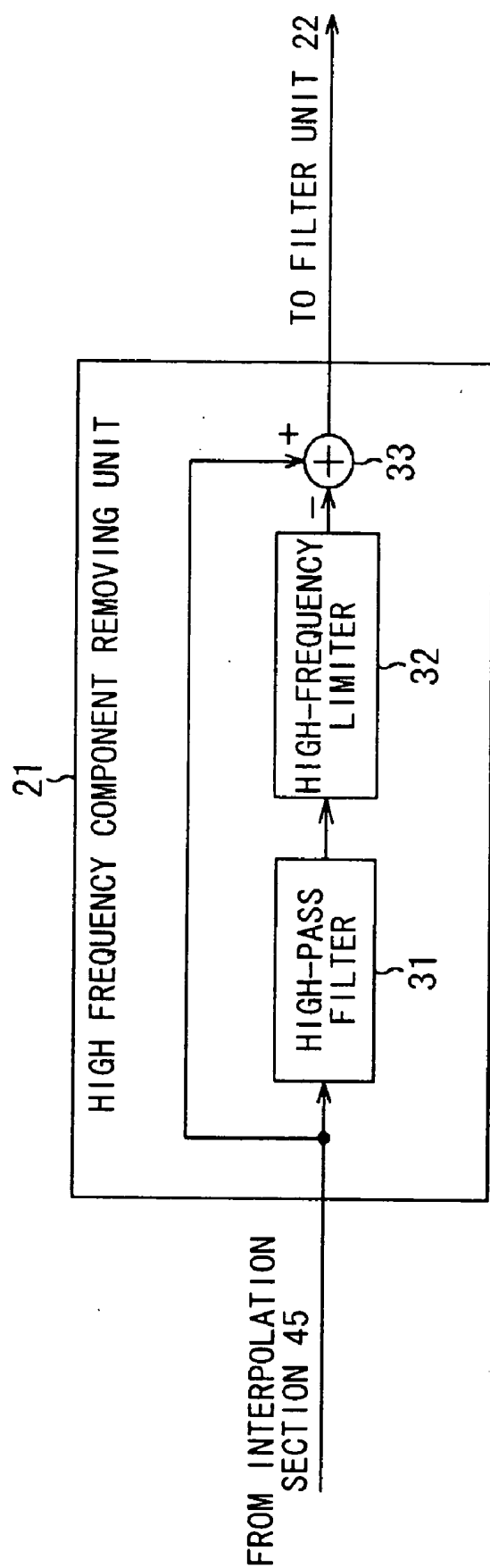


FIG. 18

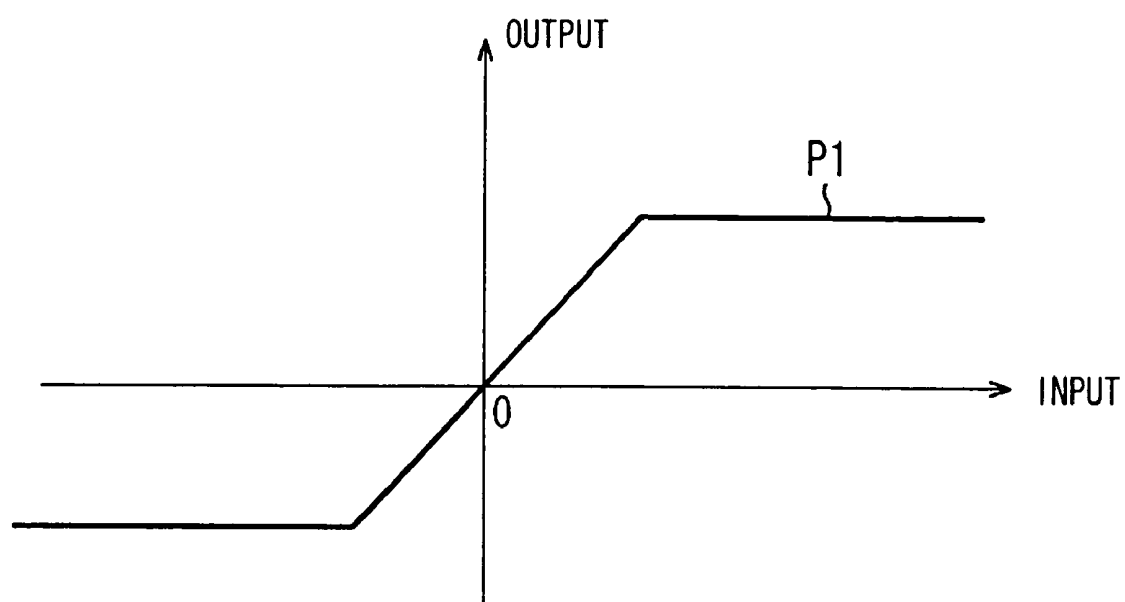


FIG. 19

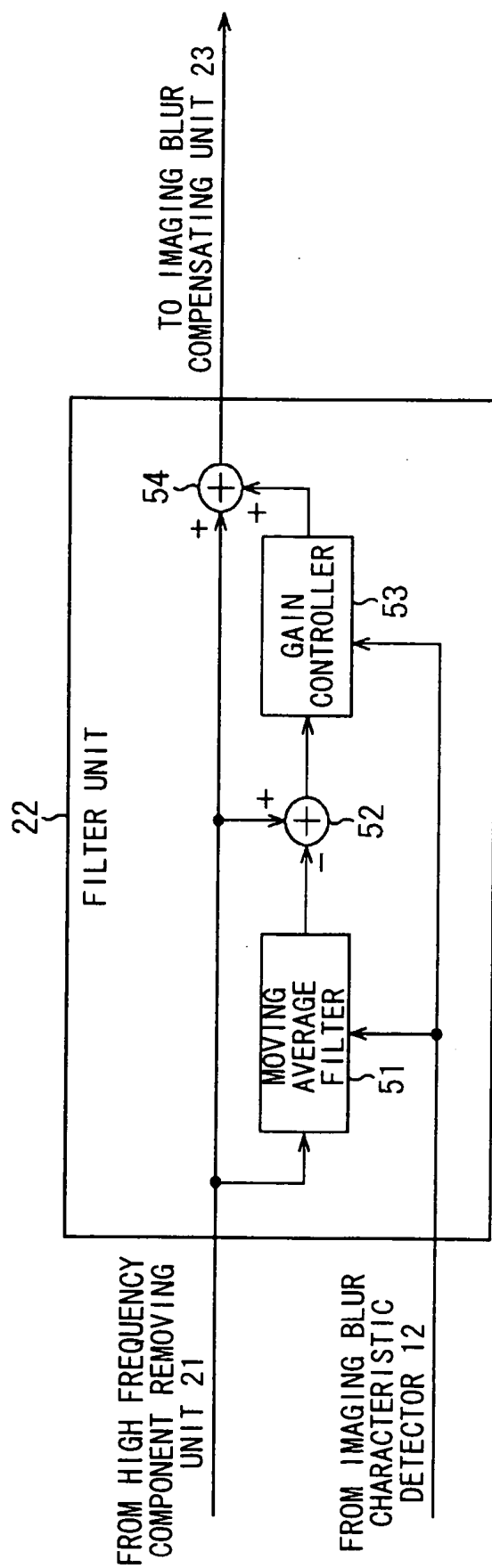


FIG. 20

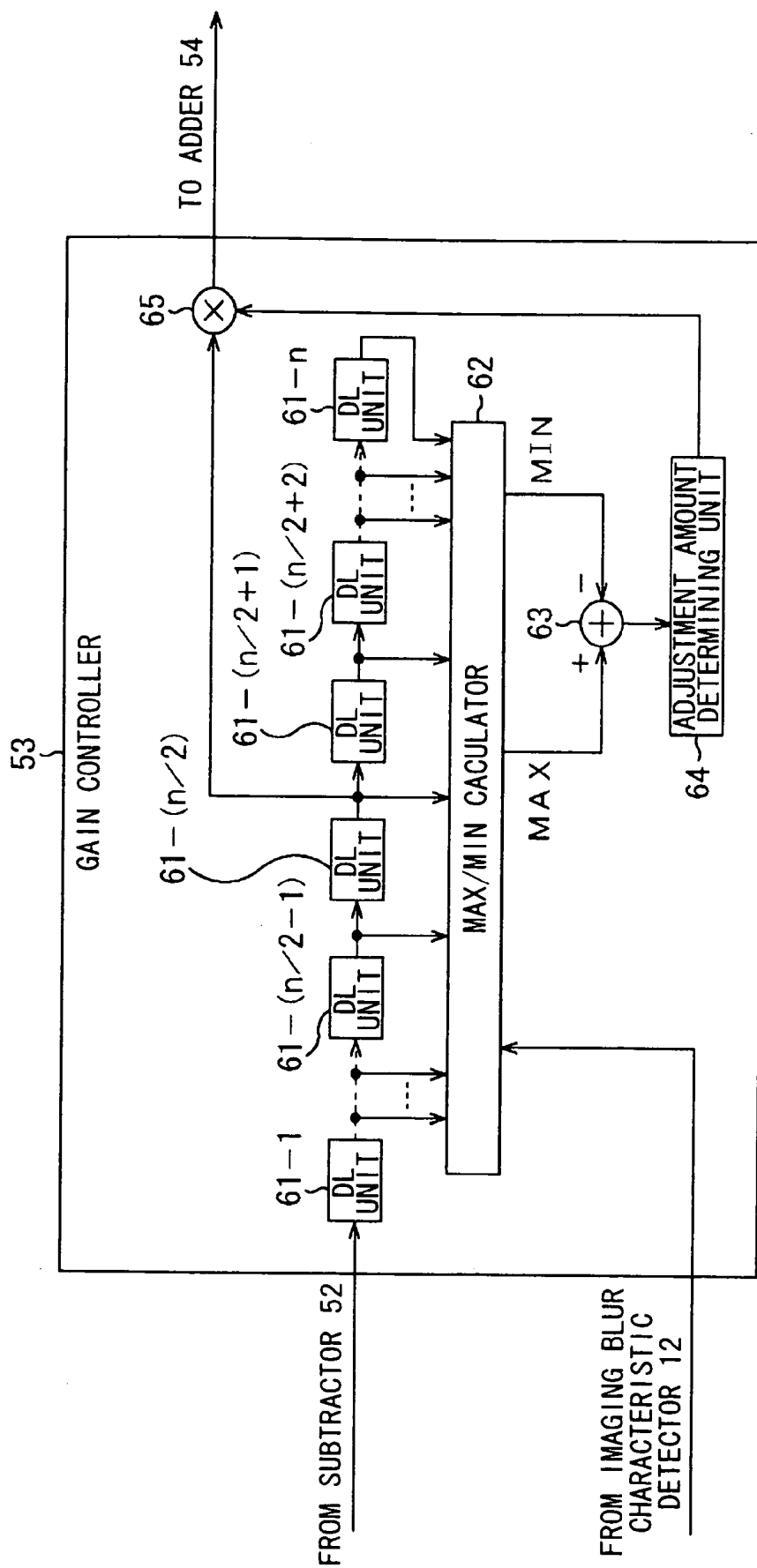


FIG. 21

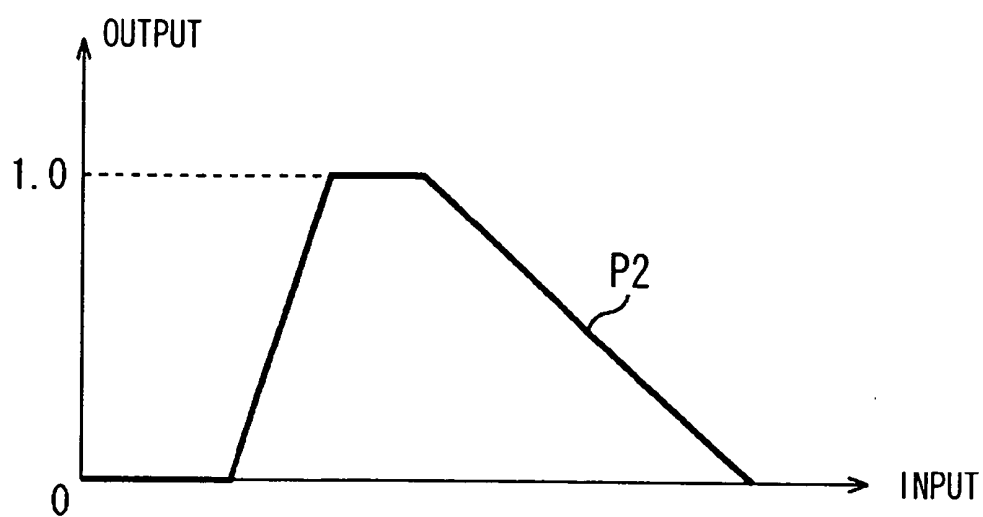


FIG. 22

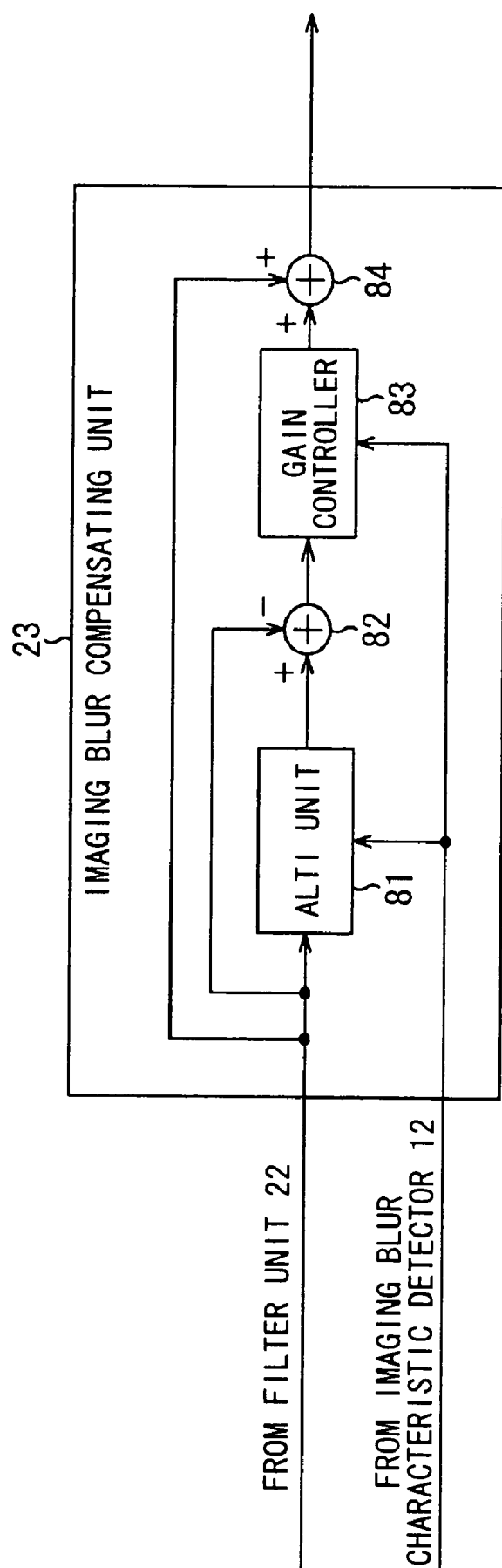


FIG. 23

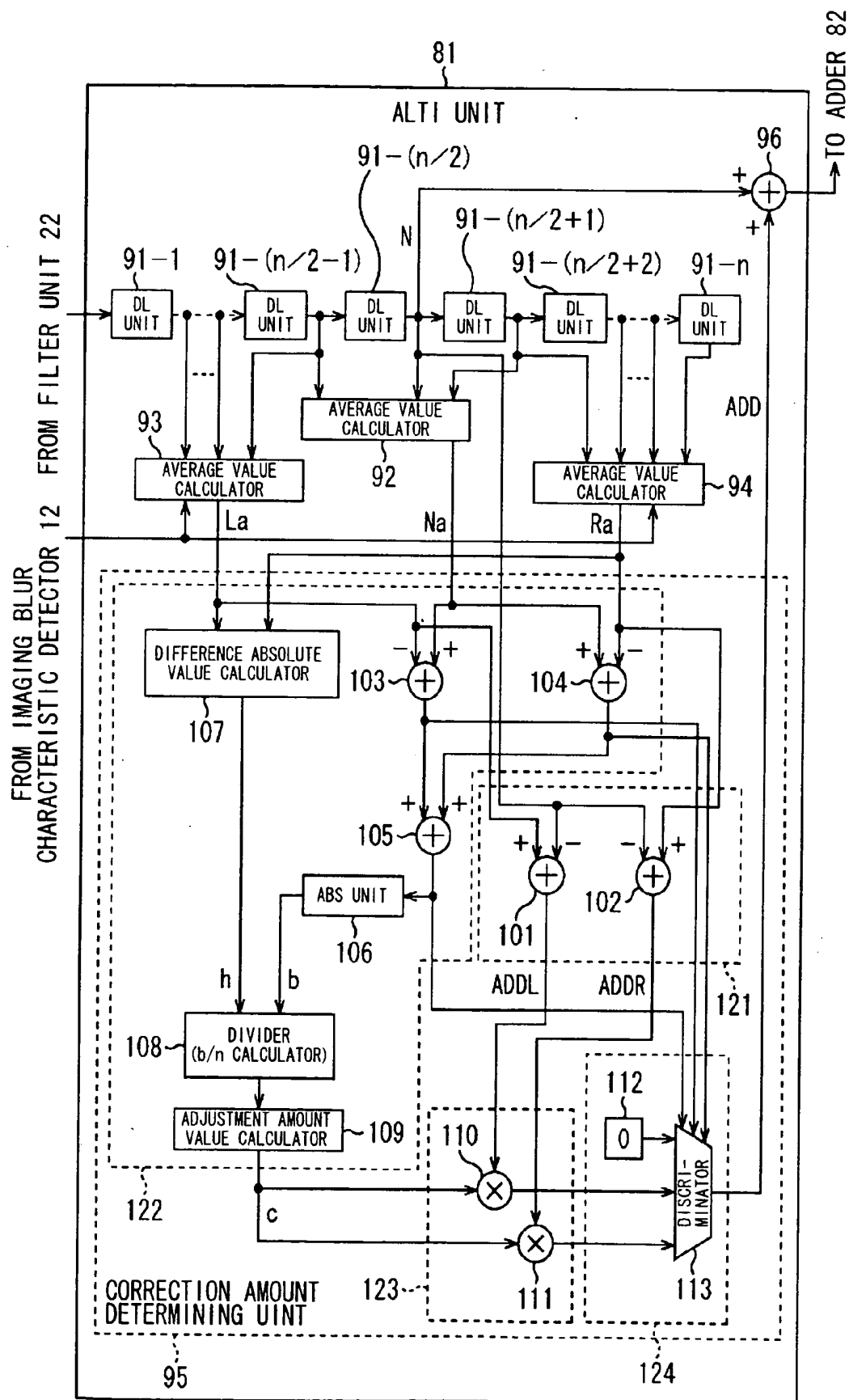


FIG. 24

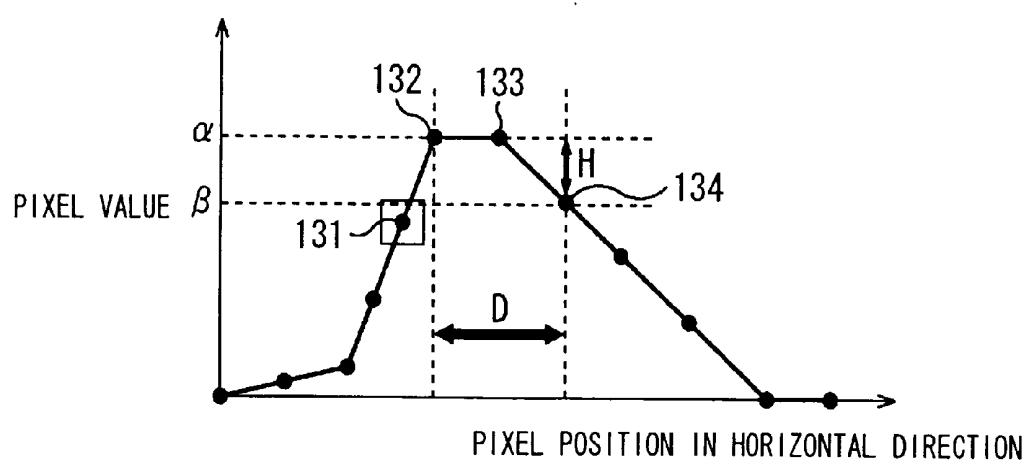


FIG. 25

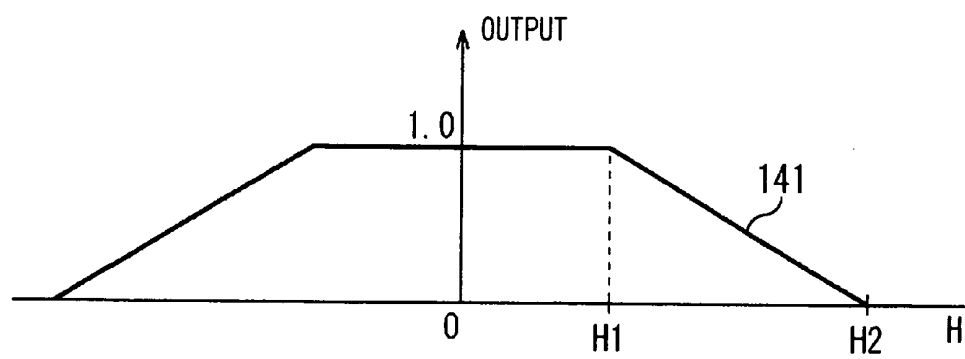


FIG. 26

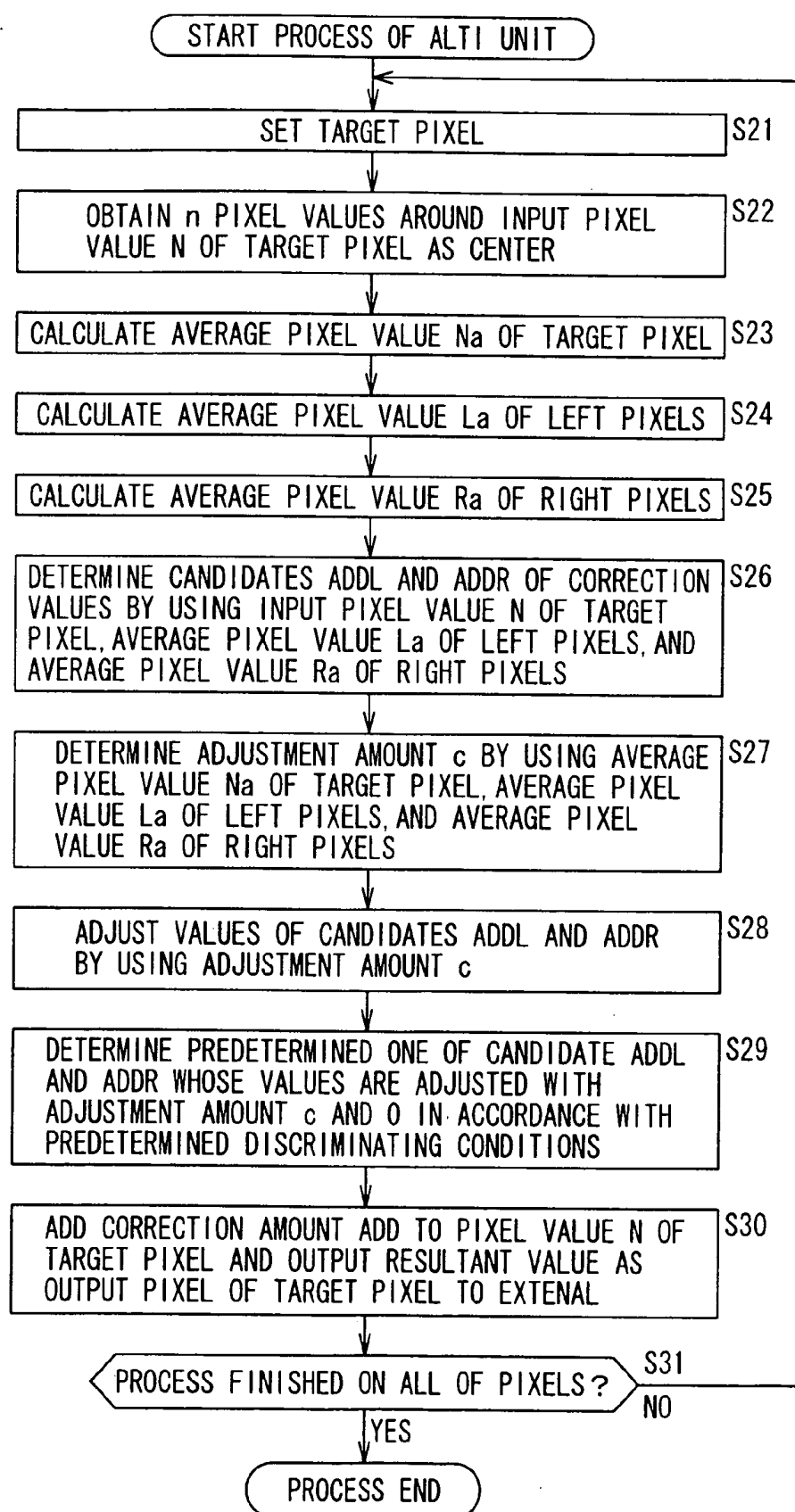


FIG. 27

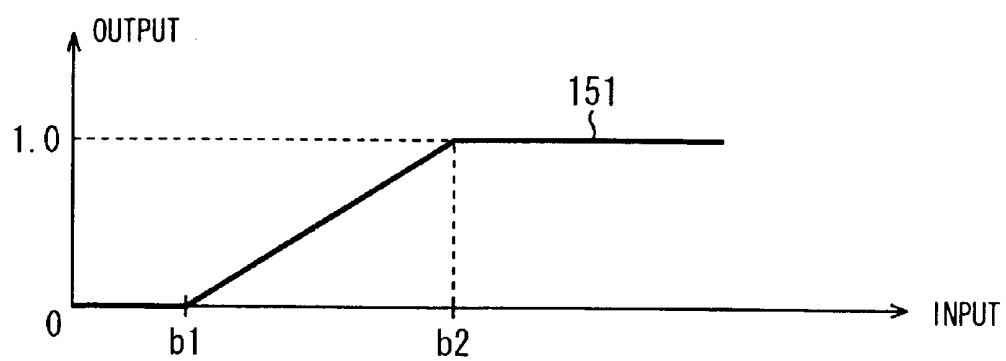


FIG. 28

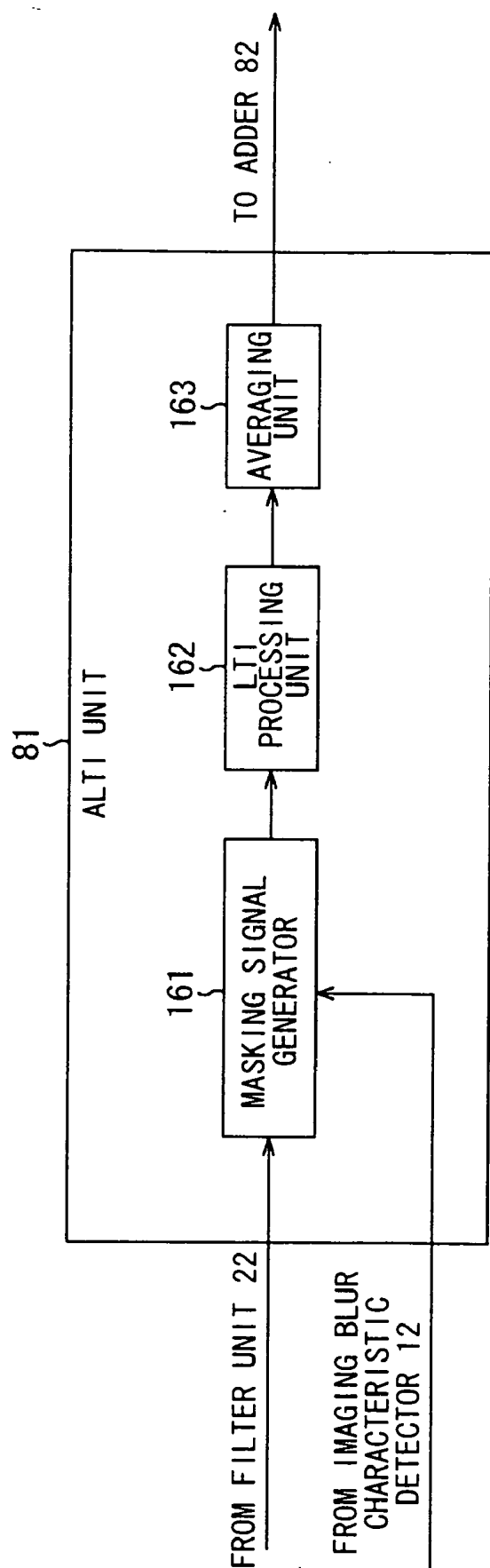


FIG. 29

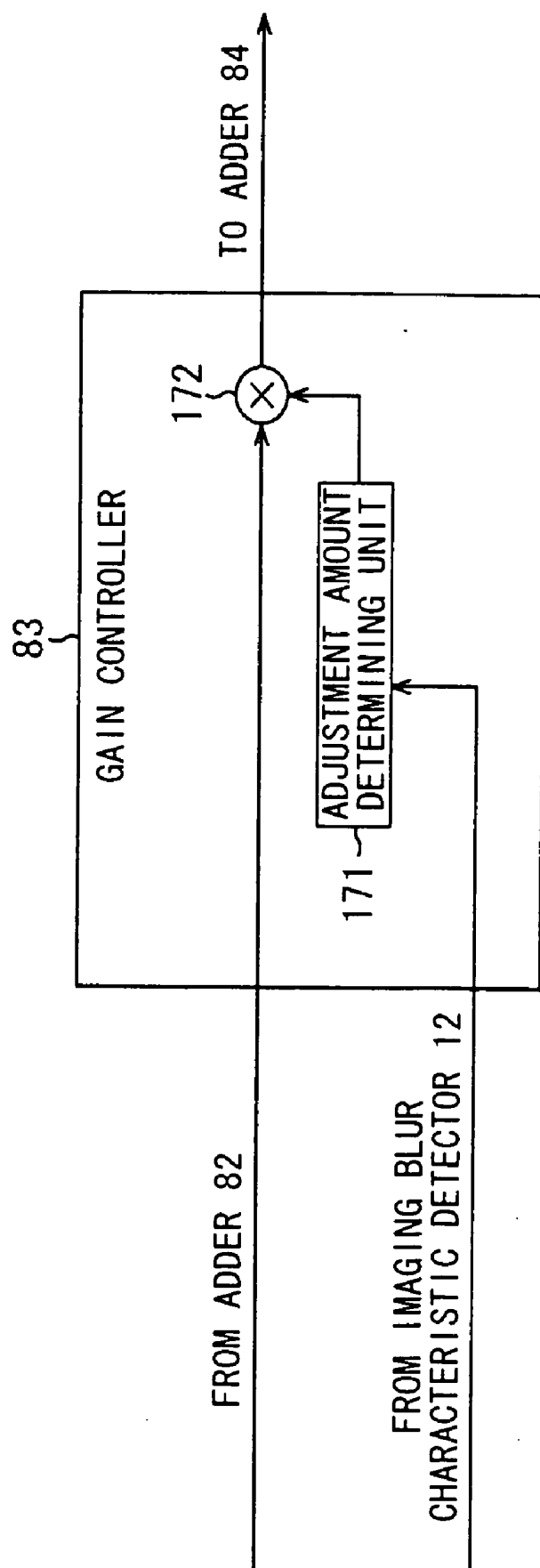


FIG. 30

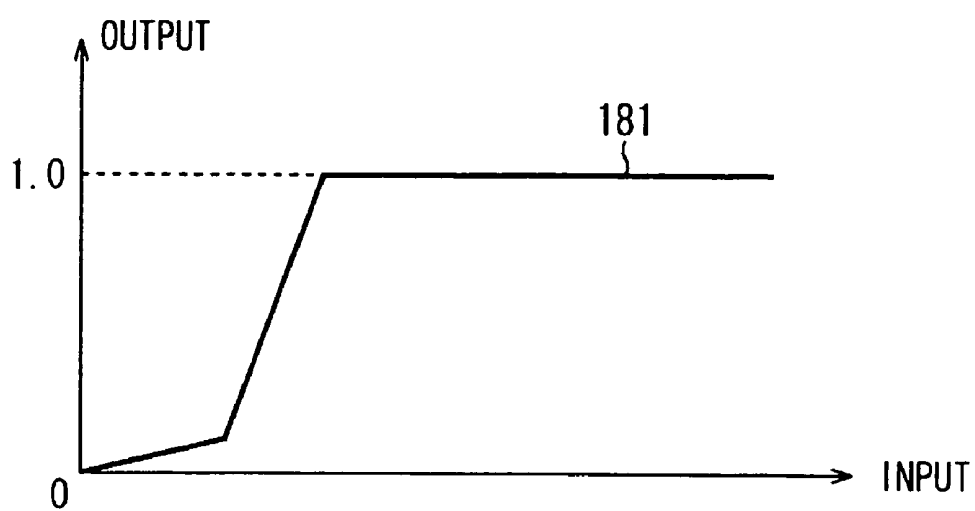


FIG. 31

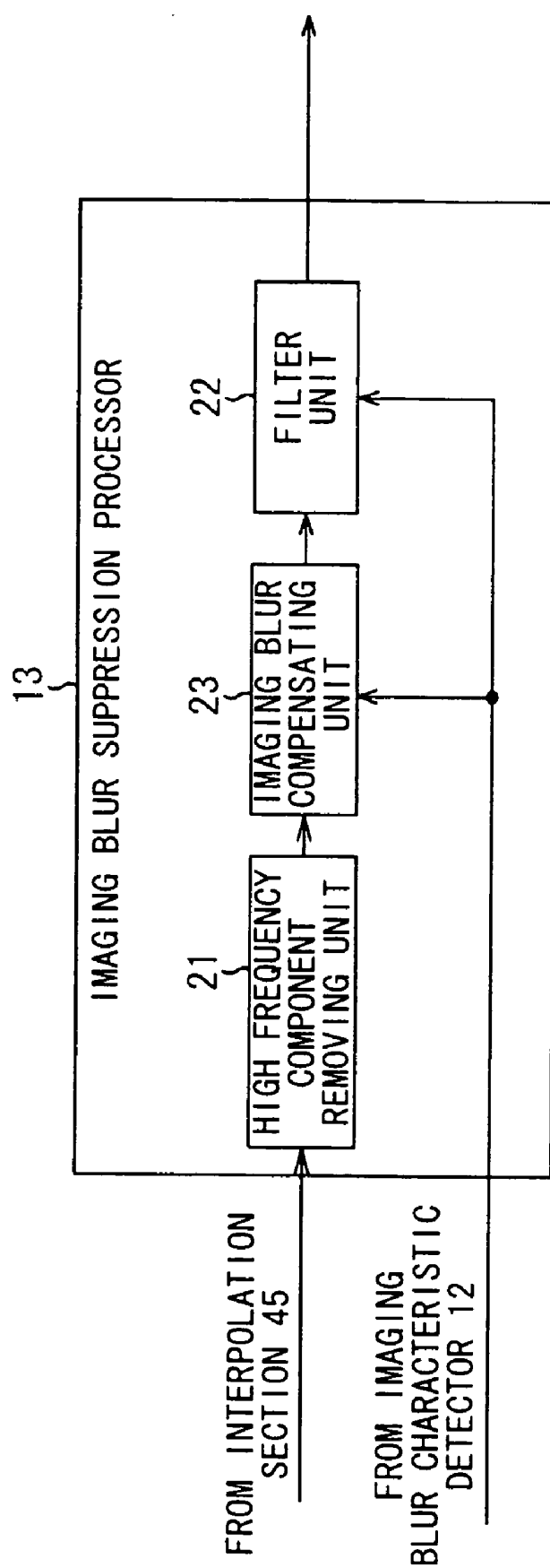


FIG. 32

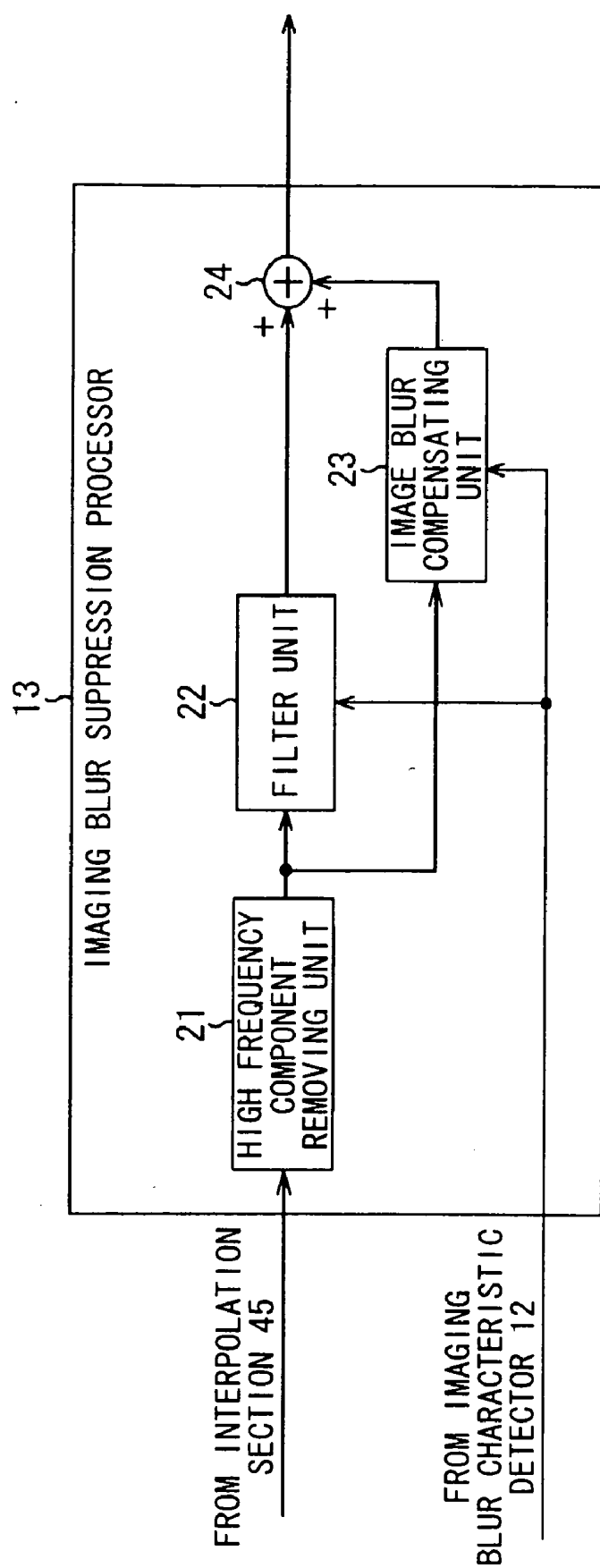


FIG. 33

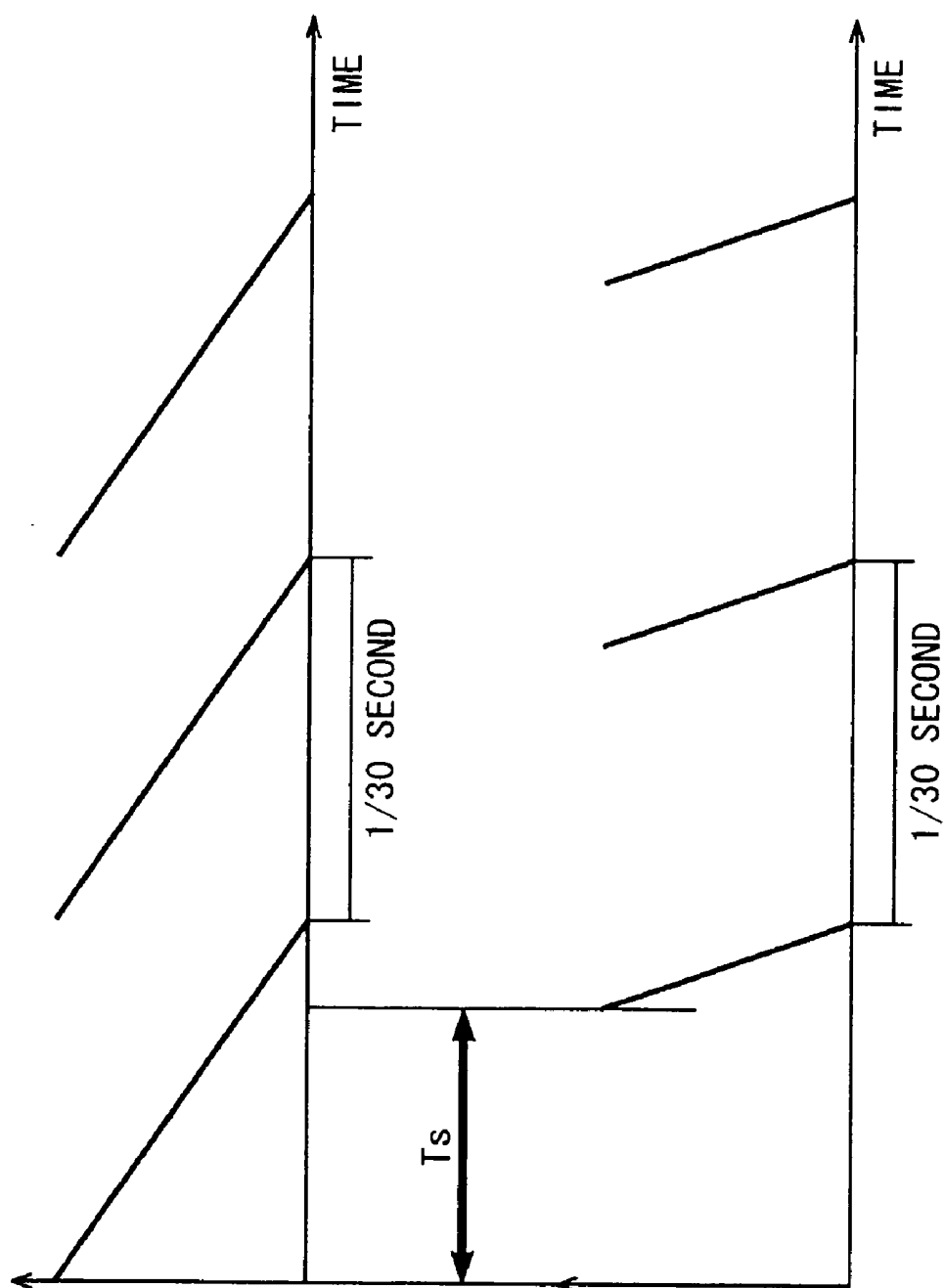


FIG. 34

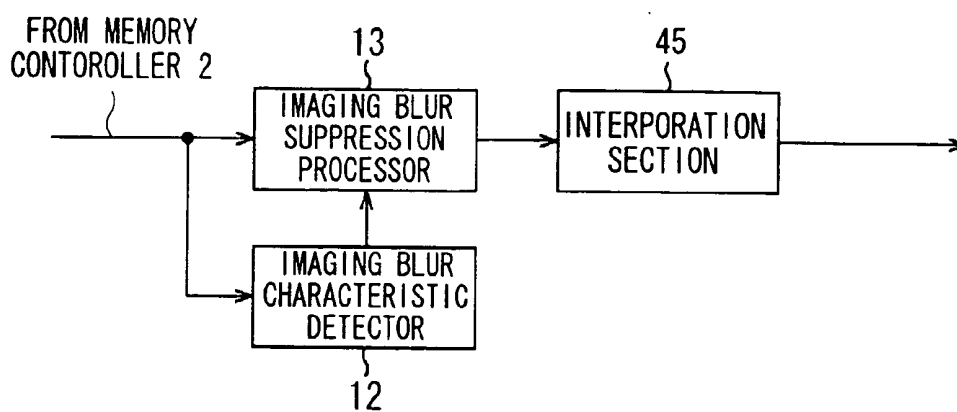


FIG. 35

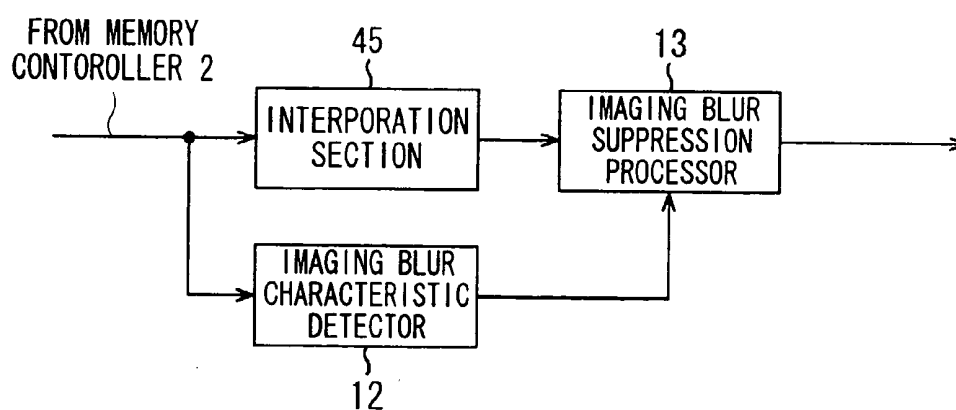


FIG. 36

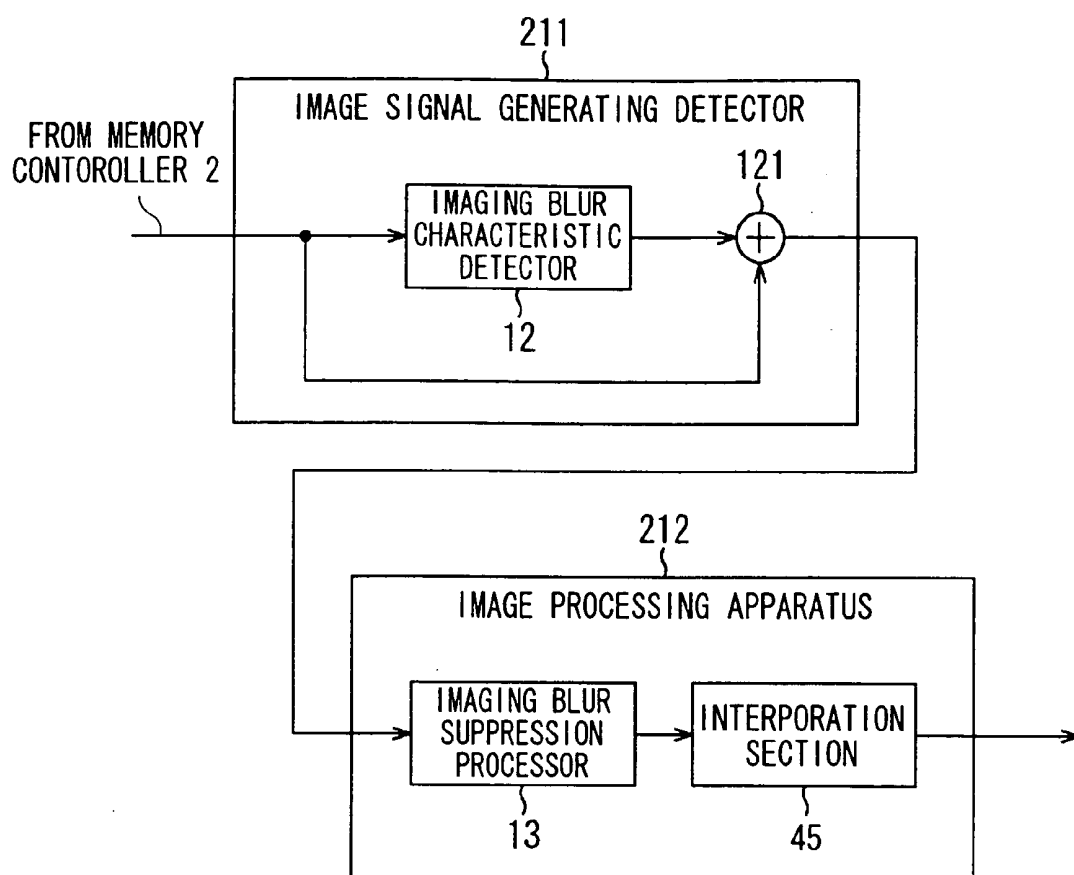


FIG. 37

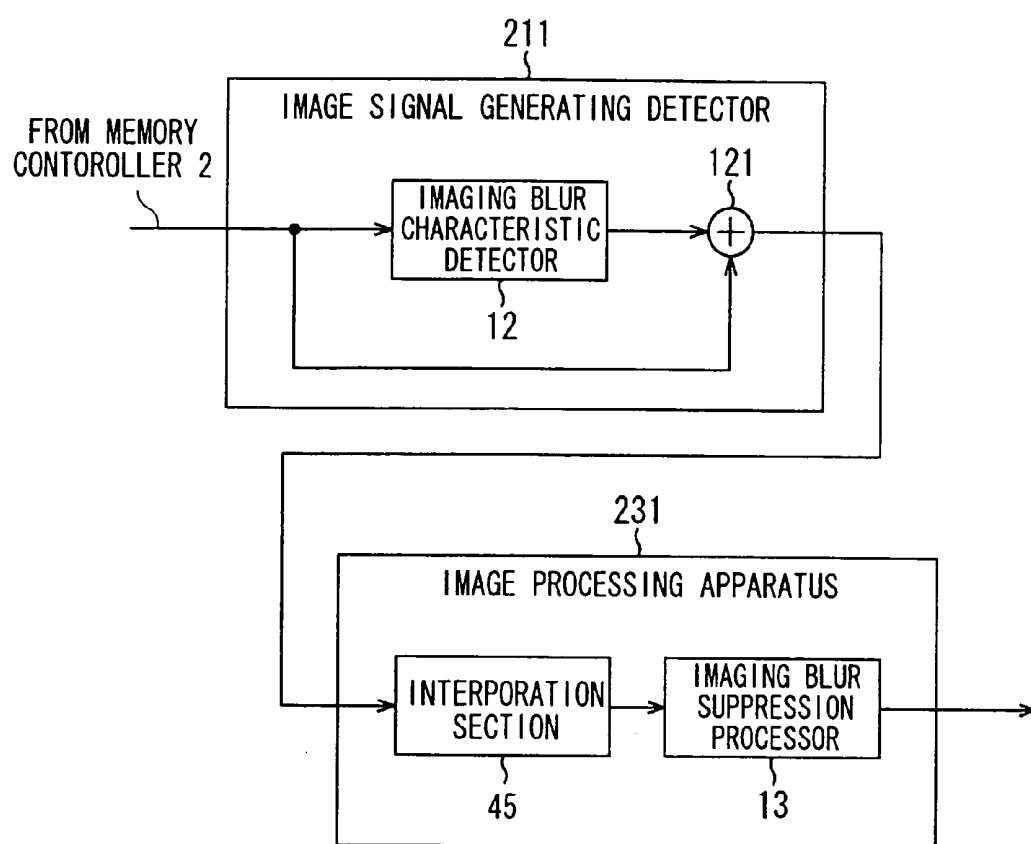


FIG. 38

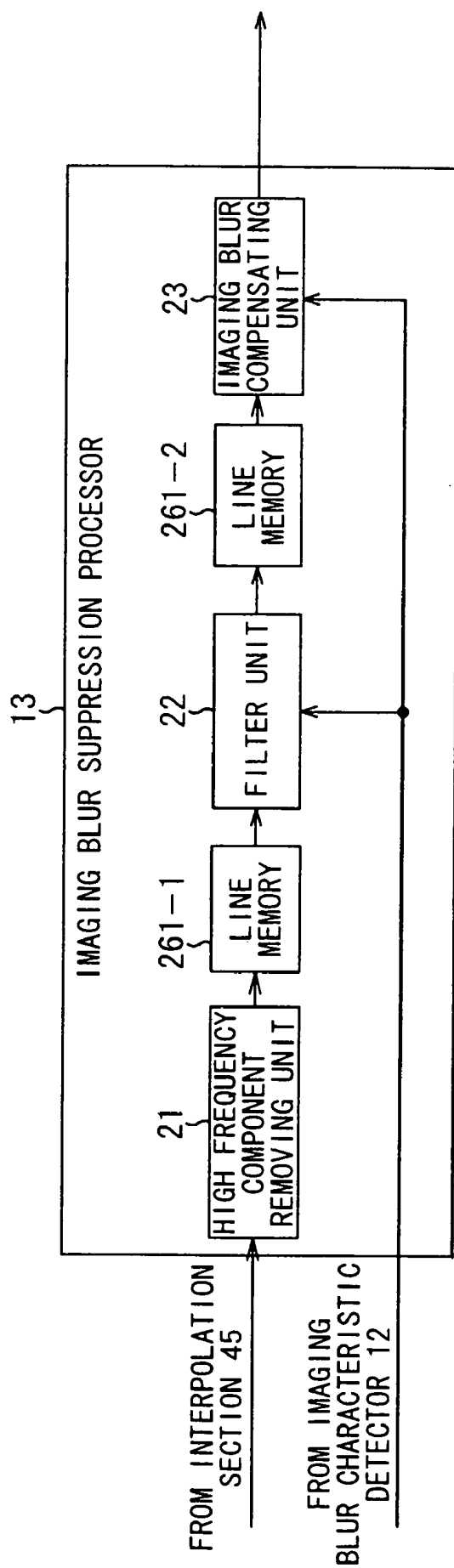


FIG. 39

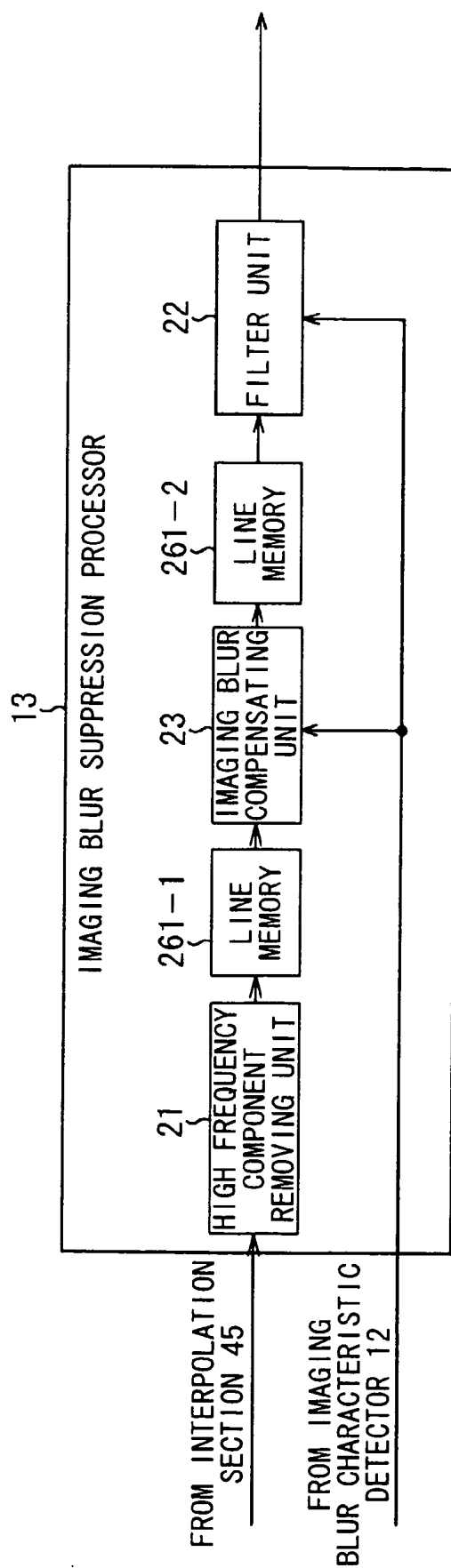


FIG. 40

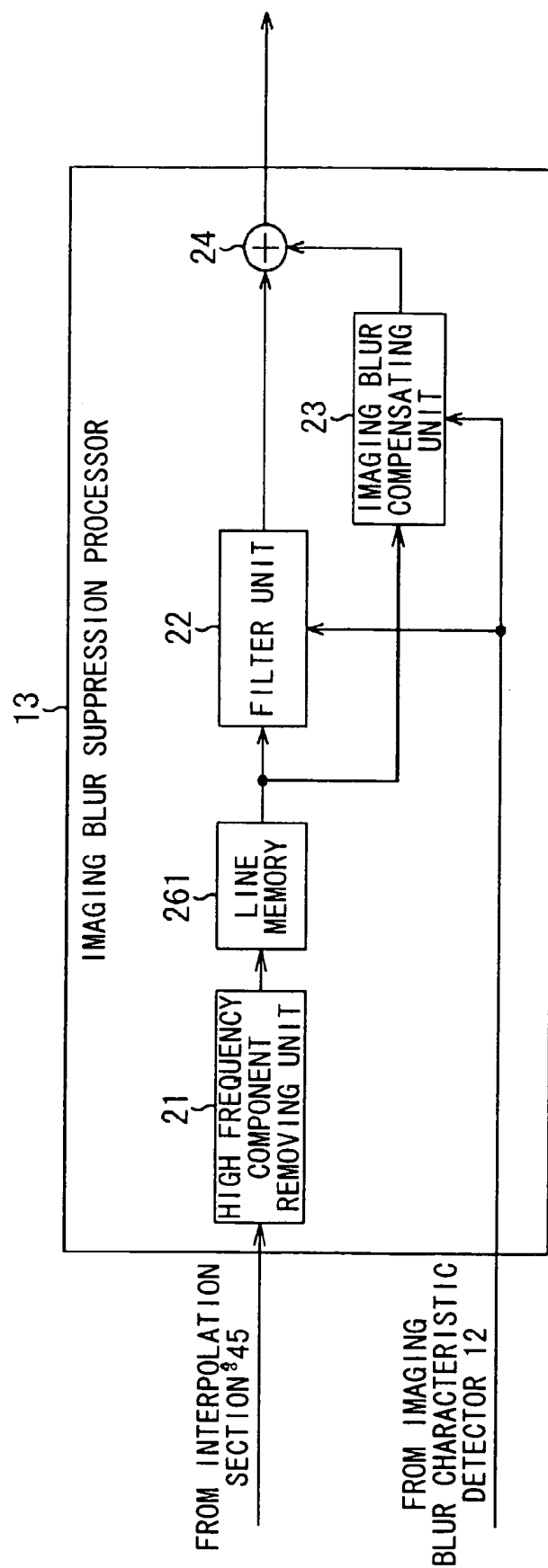


FIG. 41

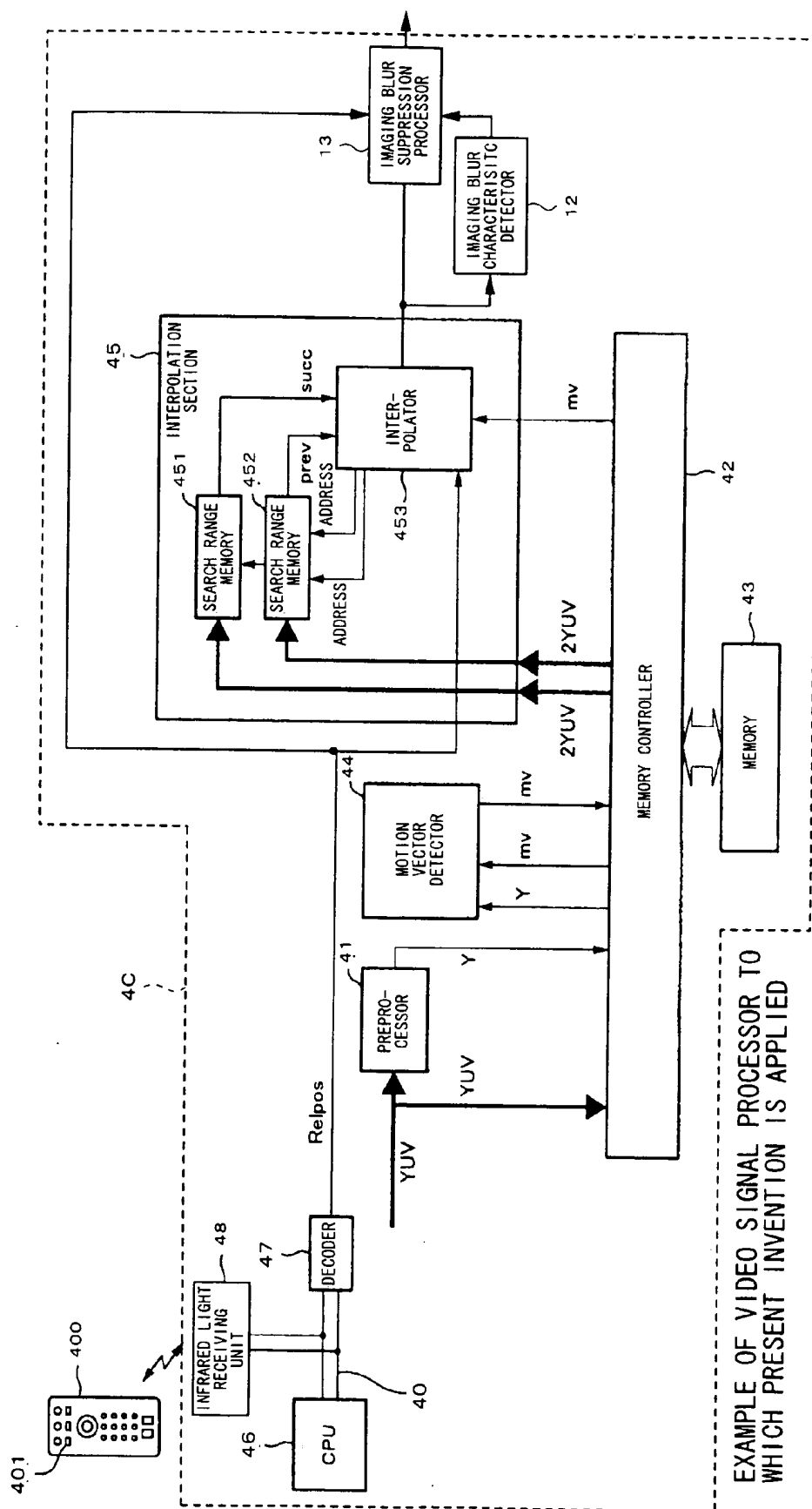


FIG. 42

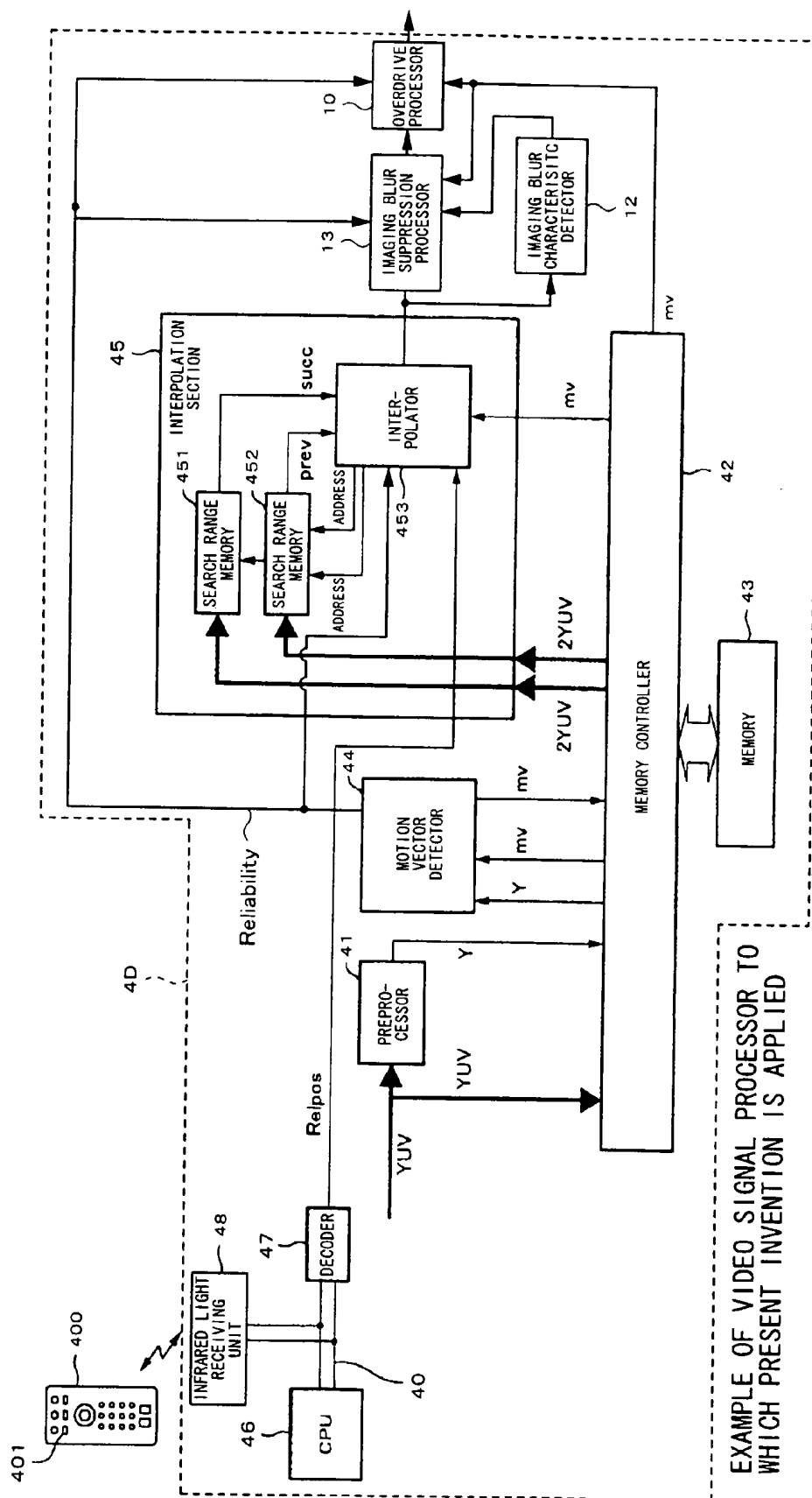


FIG. 43

EXAMPLE OF VIDEO SIGNAL PROCESSOR TO WHICH PRESENT INVENTION IS APPLIED

SIGNAL	CHANGE IN VALUE			
MC ON/OFF (PRESENCE/ABSENCE OF DETECTION OF MOTION VECTOR)	0⇒1	1⇒0	0⇒0	1⇒1
Reliability(RELIABILITY)	P-Y	P+Y	P+Y	P-Y

FIG. 44

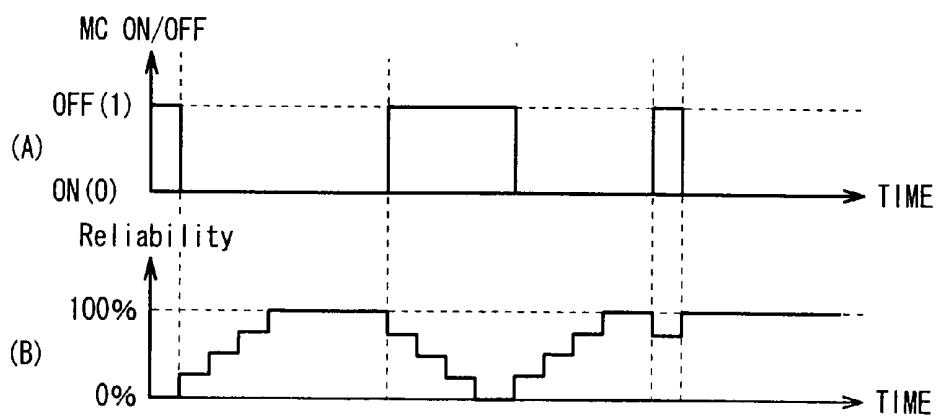


FIG. 45

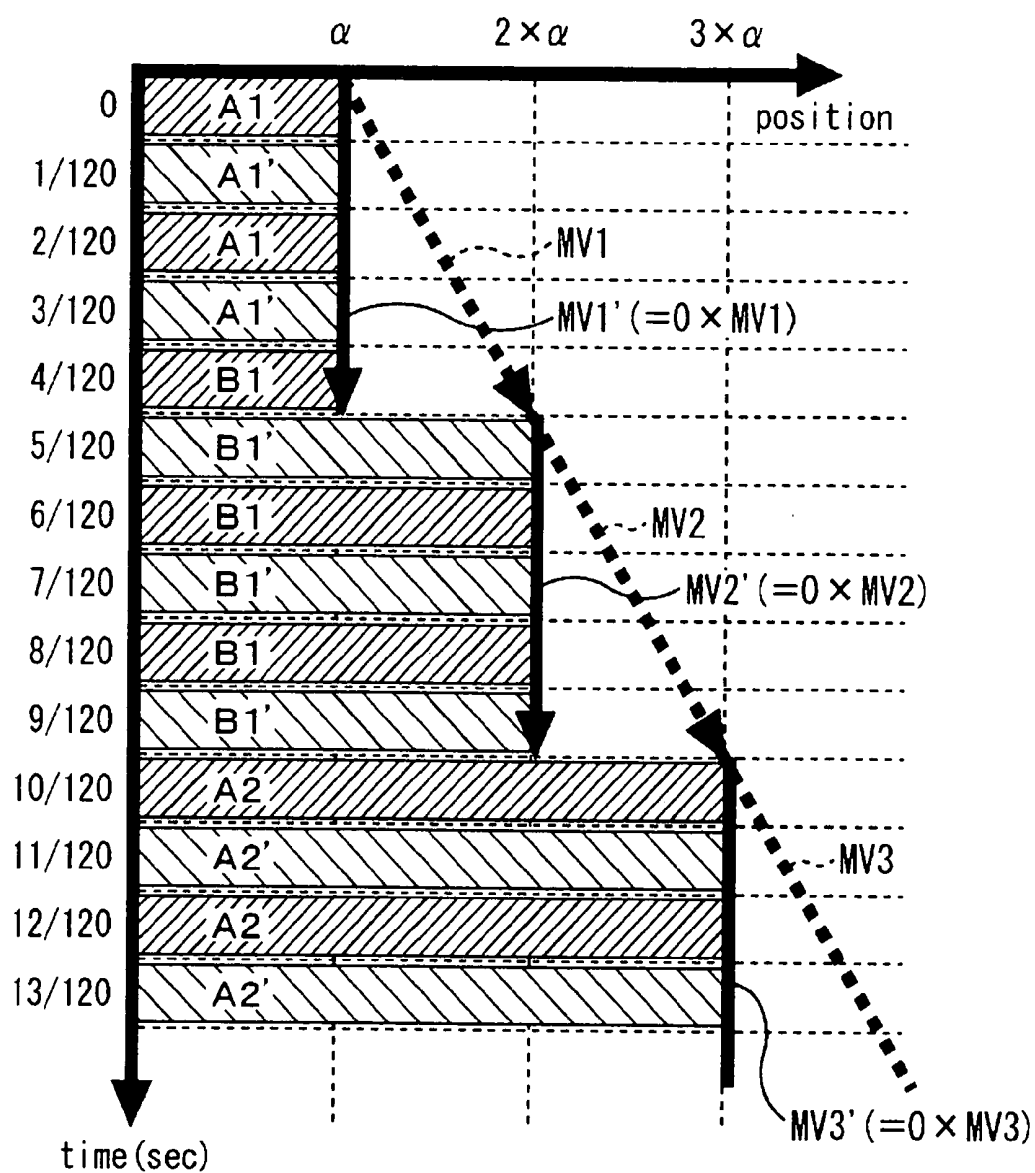


FIG. 46

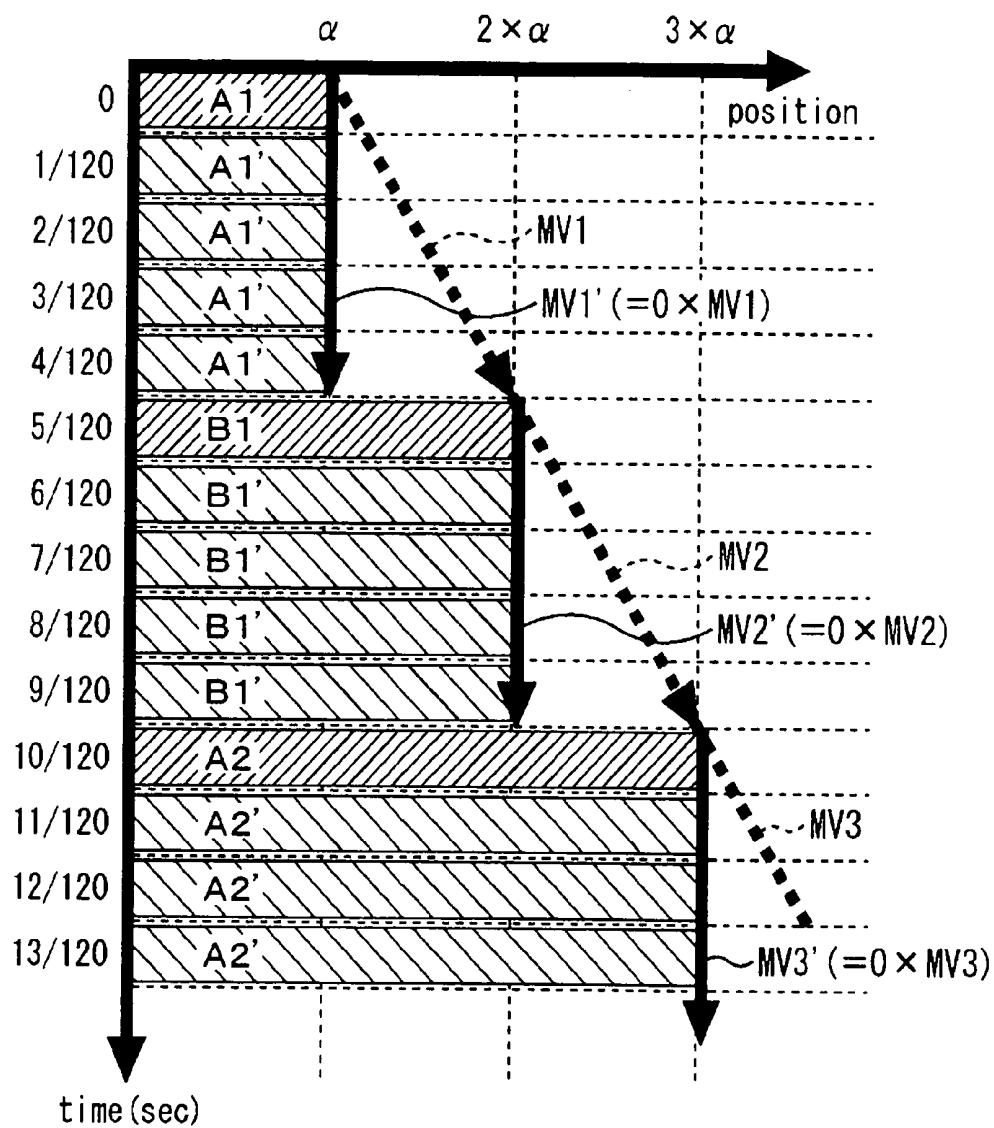


FIG. 47

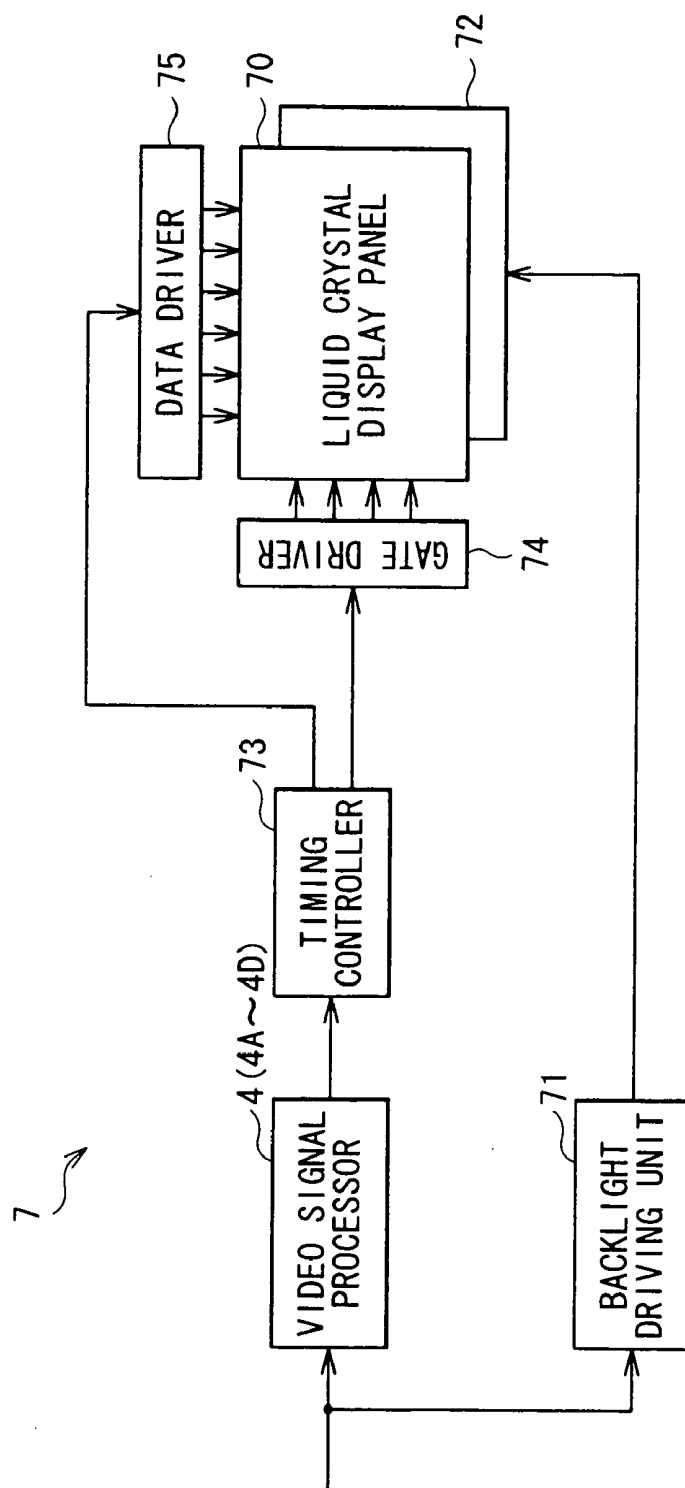


FIG. 48

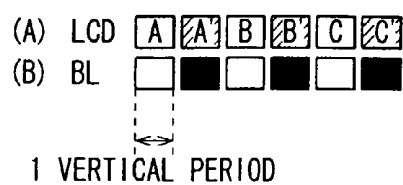


FIG. 49

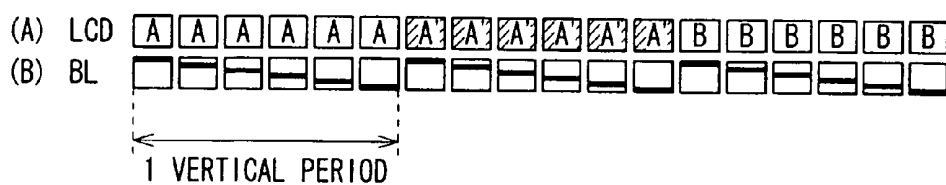


FIG. 50

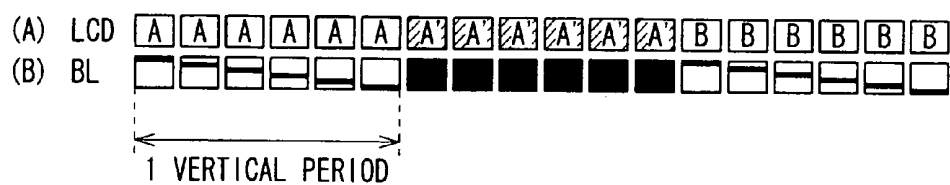


FIG. 51



FIG. 52

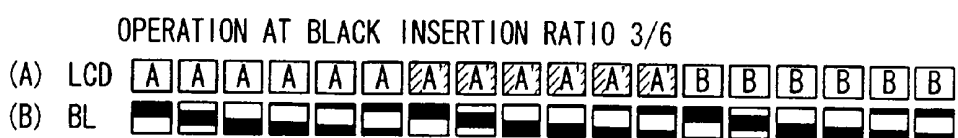


FIG. 53

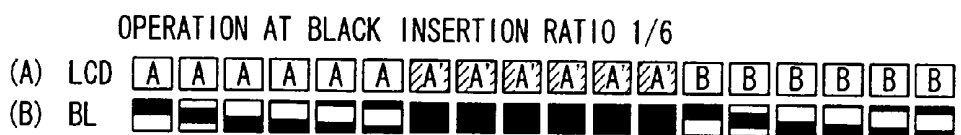


FIG. 54

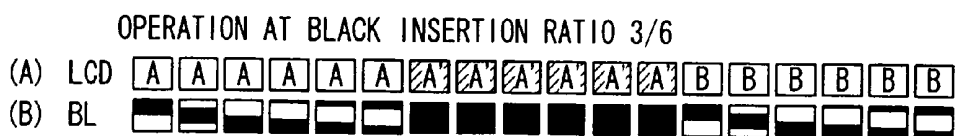


FIG. 55

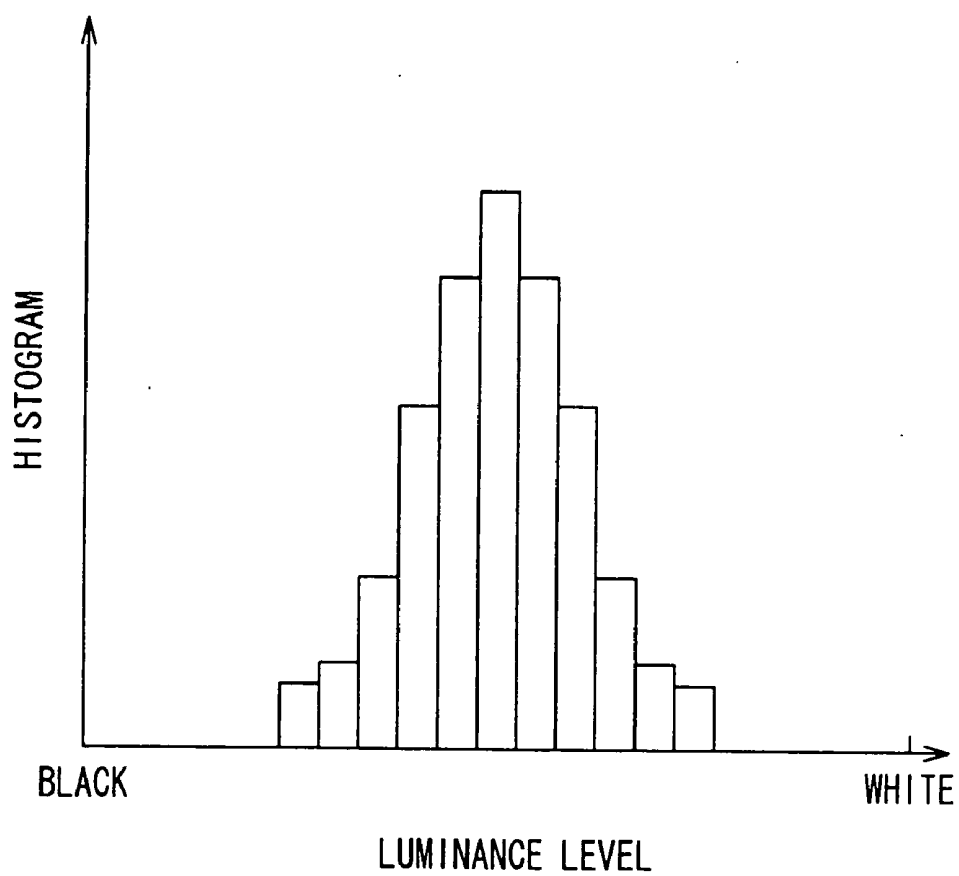


FIG. 56

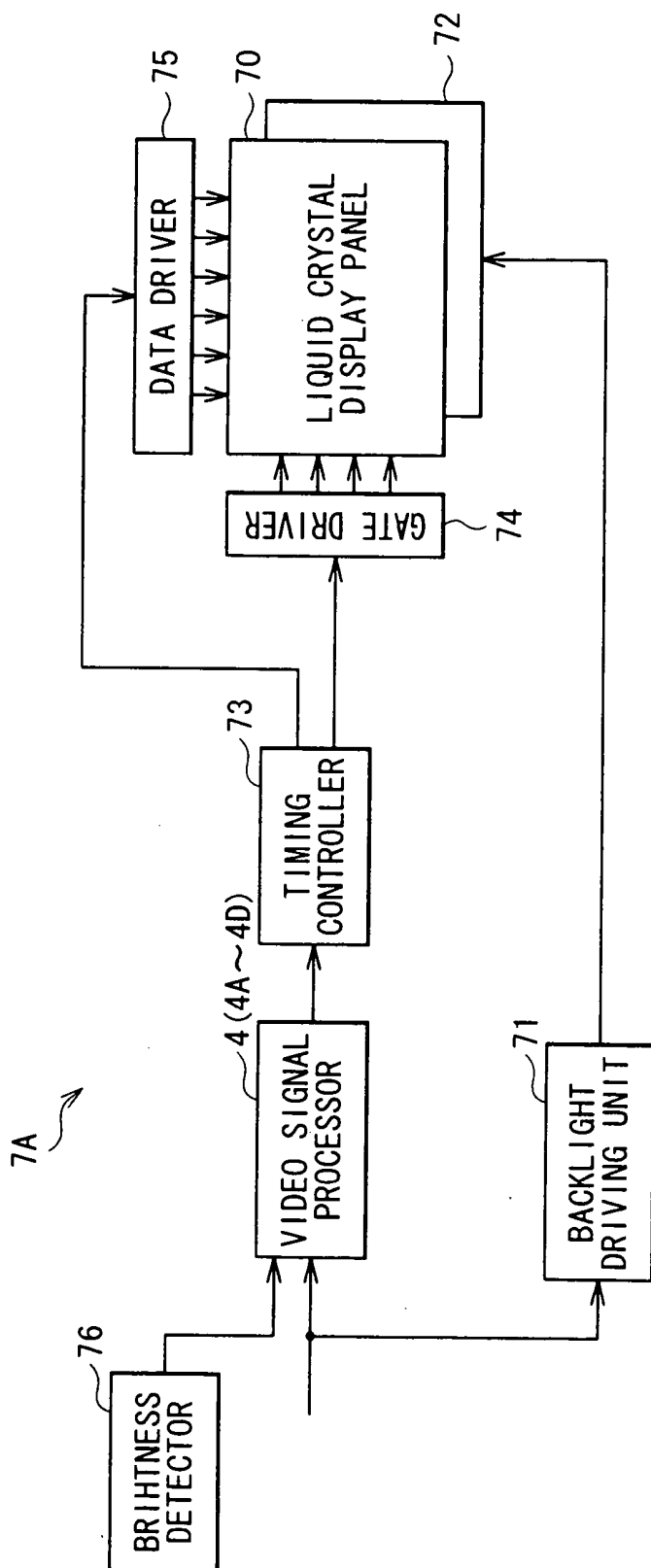


FIG. 57

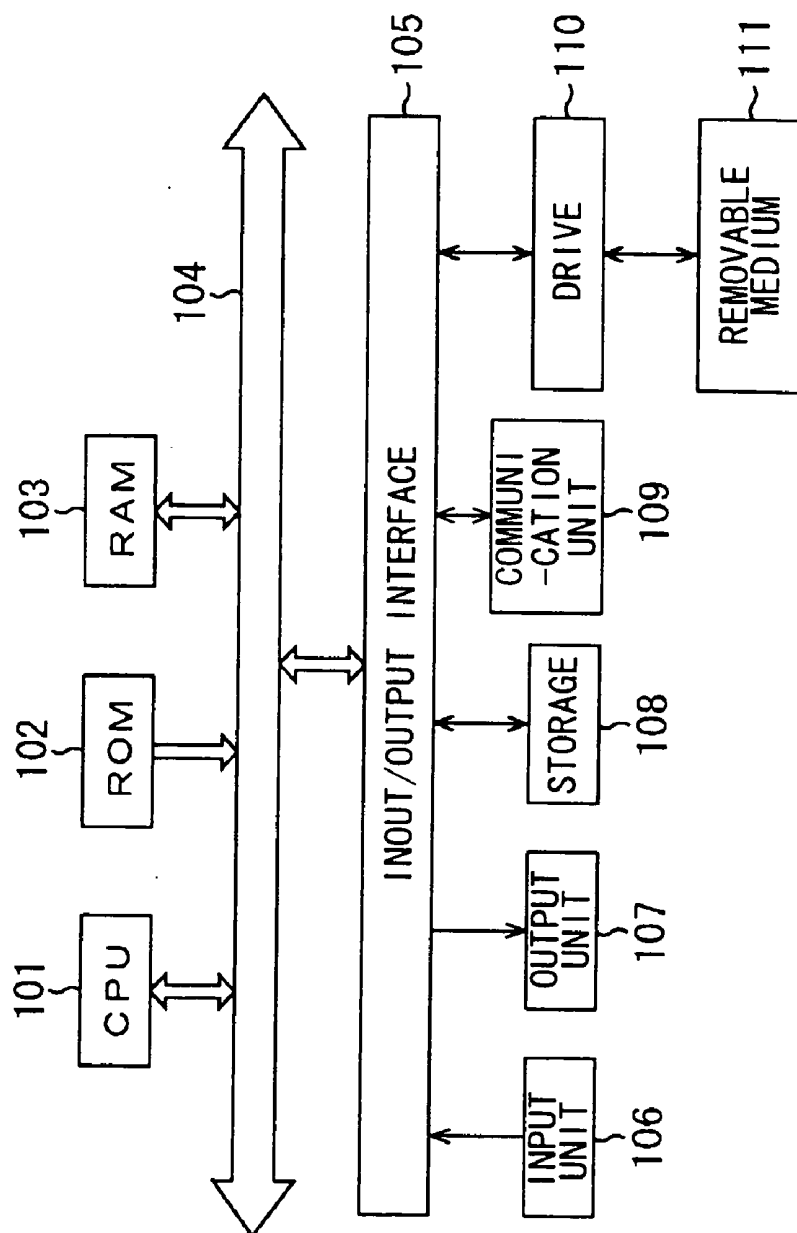


FIG. 58

IMAGE DISPLAY APPARATUS

TECHNICAL FIELD

[0001] The present invention relates to a hold-type image display apparatus having a video signal processor for performing a predetermined video signal process.

BACKGROUND ART

[0002] As one of video signal processes for improving picture quality in a television receiver, a DVD player, and the like there is frame rate conversion using motion compensation.

[0003] The principle of frame rate conversion will be described using FIGS. 1 to 3 with respect to a video signal captured by a camera for television broadcast (hereinafter, referred to as a camera signal) and a video signal obtained by telecine converting a film to a television system (hereinafter, called film signal or cinema signal).

[0004] FIG. 1(a) shows original frames A, B, C, and D of a camera signal of an NTSC system. In the case of converting the frame rate of the camera signal to 120 Hz, as shown in FIG. 1(b), an interpolation frame is added at a timing of every $\frac{1}{120}$ sec between neighboring original frames (between the frames A and B, between the frames B and C, and between the frames C and D).

[0005] FIG. 2(a) shows original frames A, B, C, and D of a film signal which is telecine converted (2:2 pulldown) to the PAL system. Each of the original frames is repeated twice. In the case of converting the frame rate of the 2:2 pulldown film signal to 100 Hz, as shown in FIG. 2(b), three interpolation frames are added at $\frac{1}{100}$ sec intervals between original frames neighboring at 25 Hz cycles (between the frames A and B, between frames B and C, and between frames C and D).

[0006] FIG. 3(a) shows original frames A, B, and C of a film signal which is telecine converted (3:2 pulldown) to the NTSC system. The odd-numbered original frames A and C are repeated three times, and the even-numbered original frame B is repeated twice. In the case of converting the frame rate of the 3:2 pulldown film signal to 120 Hz, as shown in FIG. 3(b), four interpolation frames are added at $\frac{1}{120}$ sec intervals between original frames neighboring at 24 Hz cycles (between the frames A and B and between the frames B and C).

[0007] Each of the interpolation frames is generated by interpolating video images of an earlier original frame and a following original frame. The interpolation is performed by a method of calculating addresses of pixels of the earlier original frame and the following original frame used for calculating pixel values of an interpolation frame on the basis of parameters of an interpolation position of a video image in each interpolation frame and motion vectors between the earlier original frame and the following original frame, and then placing weights to the pixel values of the addresses in accordance with interpolation positions.

[0008] The frame rate conversion produces an effect of eliminating a motion blur in a camera signal and an effect of reducing a judder (unsmoothness of motion in a video image) in a film signal.

[0009] FIGS. 1 to 3 also show interpolation positions of video images in the interpolation frames in the conventional frame rate conversion. As shown in FIG. 1(b), the interpolation position of a video image in the interpolation frames, at the time of converting the frame rate of the NTSC camera signal to 120 Hz, is conventionally set to a position obtained

by equally dividing the magnitude of the motion of a video image between the earlier original frame and the following original frame (the size determined by motion vector detection) to two portions, that is, a position of 50% of the magnitude of the motion.

[0010] As shown in FIG. 2(b), the interpolation positions of video images in three interpolation frames at the time of converting the frame rate of the 2:2 pulldown film signal to 100 Hz are conventionally set to positions obtained by equally dividing the magnitude of video image motion between the earlier original frame and the following original frame to four portions, that is, positions of 25%, 50%, and 75% of the magnitude of the motion.

[0011] As shown in FIG. 3(b), the interpolation positions of video images in four interpolation frames at the time of converting the frame rate of the 3:2 pulldown film signal to 120 Hz are conventionally set to positions obtained by equally dividing the magnitude of the motion of a video image between the earlier original frame and the following original frame to five portions, that is, positions of 20%, 40%, 60%, and 80% of the magnitude of the motion.

[0012] FIG. 4 is a diagram showing examples of video images of the 3:2 pulldown film signal subjected to the frame rate conversion in the interpolation positions in the related art. The video image of an airplane moves between neighboring original frames A and B. In four interpolation frames, video images of the airplane are interpolated in positions obtained by equally dividing the magnitude of the motion into five portions.

[0013] In addition, for example, a technique related to such frame rate conversion is proposed in Patent document 1.

[0014] Patent document 1: Japanese Unexamined Patent Application Publication No. 2003-189257

DISCLOSURE OF INVENTION

[0015] As described above, in the frame rate conversion using motion compensation, conventionally, interpolation positions of a video image in interpolation frames are set to positions obtained by evenly dividing the magnitude of a motion of the video image between the earlier original frame and the following original frame.

[0016] However, in the case of a film signal, when interpolation is performed in the interpolation positions obtained by evenly dividing the magnitude of the motion of the video image between original frames as exemplified in FIG. 4, a judder is largely reduced, and the motion of the video image becomes very smooth. As a result, a person accustomed to a judder in a film signal gets an impression that the taste of the film signal is lost.

[0017] Further, in the frame rate conversion using motion compensation, in the case where the motion of a video image between neighboring original frames becomes very fast, the motion vector lies out of a motion vector search range (block matching range), and a large judder occurs. In such a case, there is a problem that since a large judder suddenly occurs while the user is watching a video image in which motion is very smooth, the user feels discomfort.

[0018] In addition, hitherto, to make motion of a video image at the time of converting the frame rate of a film signal (cinema signal) smoother, a technique of shifting a pixel position of a field after the frame conversion in the direction of a motion vector has been proposed (refer to Patent Document 1). However, a technique of weakening the degree of

reduction of a judder while reducing the judder at the time of converting the frame rate of a film signal is not proposed.

[0019] By the way, in the case of performing a video signal process for improving the picture quality such as the frame rate conversion by using a motion vector, when the motion vector lies out of the motion vector search range (block matching range) as above, the motion vector may not be able to be detected well. In such a case, if the motion vector is used as it is, the video signal process is not performed well. Another issue arises such that picture quality deteriorates.

[0020] Further, in the case of displaying the video signal subjected to the video signal process on a fixed pixel (hold) type display apparatus such as a liquid crystal display, another issue occurs such that a so-called hold blur occurs due to its configuration. It is demanded to reduce the hold blur as much as possible. Since viewability of such a hold blur varies according to circumstances, an improvement method according to circumstances is desired.

[0021] The present invention has been achieved in view of such issues, and its first object is to provide an image display apparatus, a video signal processor, and a video signal processing method capable of weakening the degree of reduction of a judder while reducing the judder at the time of converting frame rate of a film signal (cinema signal) using motion compensation.

[0022] A second object of the present invention is to provide an image display apparatus, a video signal processor, and a video signal processing method capable of suppressing deterioration in picture quality due to detection precision of a motion vector at the time of performing a predetermined video signal process for improving picture quality.

[0023] Further, a third object of the present invention is to provide an image display apparatus capable of reducing a hold blur in accordance with circumstances.

[0024] An image display apparatus of the present invention has video signal processing means for performing a predetermined video signal process on a plurality of original frames along time base, and display means for displaying a video image on the basis of a video signal subjected to the video signal process. In this case, the display means is hold-type display means. In addition, the image display apparatus is configured to perform a black inserting process of inserting a black display area into a display screen in the display means according to at least one of the substance of the video signal in the original frame and luminance of a user's viewing environment.

[0025] In the image display apparatus of the present invention, the predetermined video signal process is performed on the plurality of original frames along the time base, and a video image is displayed on the basis of the video signal subjected to such a video signal process. In addition, the black inserting process of inserting a black display area into a display screen of the display means is performed according to at least one of the substance of a video signal in the original frame and the luminance of the user's viewing environment.

[0026] In the image display apparatus of the invention, the black inserting process of inserting a black display area into a display screen of the display means is performed according to at least one of the substance of a video signal in the original frame and the luminance of the user's viewing environment. Thus, a hold blur is able to be reduced in accordance with circumstances.

BRIEF DESCRIPTION OF DRAWINGS

[0027] FIG. 1 Diagrams showing the principle of frame rate conversion of a camera signal and interpolation positions in related art.

[0028] FIG. 2 Diagrams showing the principle of frame rate conversion of a film signal and interpolation positions in related art.

[0029] FIG. 3 Diagrams showing the principle of frame rate conversion of a film signal and interpolation positions in related art.

[0030] FIG. 4 A diagram exemplifying video images of the film signal subjected to frame rate conversion in the interpolation positions in related art.

[0031] FIG. 5 A block diagram showing an example of a circuit configuration of a video signal processor according to a first embodiment of the invention.

[0032] FIG. 6 A diagram showing the principle of address calculation by interpolator.

[0033] FIG. 7 A diagram showing interpolation position parameters supplied from a CPU.

[0034] FIG. 8 A diagram showing values of the interpolation position parameters in the case of a 3:2 pulldown film signal.

[0035] FIG. 9 A diagram showing values of the interpolation position parameters in the case of a 2:2 pulldown film signal.

[0036] FIG. 10 Diagrams showing video images of film signals subjected to the frame rate conversion using the apparatus of FIG. 5.

[0037] FIG. 11 A block diagram showing an example of the circuit configuration of a video signal processor according to a modified example of the first embodiment.

[0038] FIG. 12 Diagrams showing frame rate conversion to 240 Hz of a camera signal.

[0039] FIG. 13 A block diagram showing an example of the configuration of a video signal processor according to a second embodiment of the present invention.

[0040] FIG. 14 A diagram showing an example of a frequency characteristic of a blur in an image formed on the retina of a human.

[0041] FIG. 15 A flowchart explaining an example of image process executed by the video signal processor of FIG. 13.

[0042] FIG. 16 A diagram showing an example of the frequency characteristic of an imaging blur according to a travel vector (travel speed, motion vector).

[0043] FIG. 17 A block diagram showing an example of a functional configuration of an imaging blur suppression processor in the video signal processor of FIG. 13.

[0044] FIG. 18 A block diagram showing an example of the functional configuration of a high frequency component removing unit in the imaging blur suppression processor of FIG. 17.

[0045] FIG. 19 A diagram showing an example of the characteristic of a high-frequency limiter in the high frequency component removing unit of FIG. 18.

[0046] FIG. 20 A block diagram showing an example of the functional configuration of a filter unit in the imaging blur suppression processor of FIG. 17.

[0047] FIG. 21 A block diagram showing an example of the functional configuration of a gain controller in the filter unit in FIG. 20.

[0048] FIG. 22 A diagram showing an example of the characteristic of an adjustment amount determining unit in the gain controller in FIG. 21.

[0049] FIG. 23 A block diagram showing an example of the functional configuration of an imaging blur compensating unit in the imaging blur suppression processor of FIG. 17.

[0050] FIG. 24 A block diagram showing an example of the functional configuration of an ALTI unit in the imaging blur compensating unit in FIG. 23.

[0051] FIG. 25 A diagram illustrating an example of an object to be processed of the ALTI unit of FIG. 24 to explain a method of correcting a pixel value in the case of computing average of pixel values of a group of pixels arranged successively on the right side of a target pixel.

[0052] FIG. 26 A diagram for supplementarily explaining the pixel value correcting method in the case of computing average of pixel values of a group of pixels arranged successively on the right side of the target pixel.

[0053] FIG. 27 A flowchart explaining an example of processes of the ALTI unit of FIG. 24.

[0054] FIG. 28 A diagram showing an example of the characteristic of an adjustment amount value calculator in the ALTI unit of FIG. 24.

[0055] FIG. 29 A block diagram showing another example different from FIG. 12 of the functional configuration of the ALTI unit in the imaging blur compensating unit of FIG. 23.

[0056] FIG. 30 A block diagram showing an example of the functional configuration of the gain controller in the imaging blur compensating unit in FIG. 23.

[0057] FIG. 31 A diagram showing an example of the characteristic of the adjustment amount determining unit in the gain adjusting unit in FIG. 30.

[0058] FIG. 32 A block diagram showing an example different from FIG. 17 of the functional configuration of the imaging blur suppression processor in the video signal processor of FIG. 13.

[0059] FIG. 33 A block diagram showing an example different from FIGS. 17 and 32 of the functional configuration of the imaging blur suppression processor in the video signal processor of FIG. 13.

[0060] FIG. 34 A diagram illustrating shutter speed of a camera and the characteristic of an imaging blur.

[0061] FIG. 35 A block diagram showing an example different from FIG. 13 of the configuration of a part of a video signal processor according to the second embodiment.

[0062] FIG. 36 A block diagram showing an example different from FIGS. 13 and 35 of the configuration of a part of the video signal processor of the second embodiment.

[0063] FIG. 37 A block diagram showing an example different from FIGS. 13, 35, and 36 of the configuration of a part of the video signal processor of the second embodiment.

[0064] FIG. 38 A block diagram showing an example different from FIGS. 13, 35, 36, and 37 of the configuration of a part of the video signal processor of the second embodiment.

[0065] FIG. 39 A block diagram showing an example different from FIGS. 17, 32, and 33, of the functional configuration of the imaging blur suppression processor in the video signal processor of FIG. 13.

[0066] FIG. 40 A block diagram showing an example different from FIGS. 17, 32, 33, and 39, of the functional configuration of the imaging blur suppression processor in the video signal processor of FIG. 13.

[0067] FIG. 41 A block diagram showing an example different from FIGS. 17, 32, 33, 39, and 40, of the functional configuration of the imaging blur suppression processor in the video signal processor of FIG. 13.

[0068] FIG. 42 A block diagram showing the configuration of a video signal processor according to a modified example of the second embodiment.

[0069] FIG. 43 A block diagram showing an example of the configuration of a video signal processor according to a modified example of a third embodiment of the invention.

[0070] FIG. 44 A diagram showing an example of the relation between the presence/absence of detection of a motion vector and reliability.

[0071] FIG. 45 A timing waveform chart showing an example of the relation between the presence/absence of detection of a motion vector and reliability.

[0072] FIG. 46 A timing chart showing an example of a change in a gain multiplied with a motion vector according to reliability.

[0073] FIG. 47 A timing chart showing another example of a change in a gain multiplied with a motion vector according to reliability.

[0074] FIG. 48 A block diagram showing an example of the configuration of an image display apparatus according to a fourth embodiment of the present invention.

[0075] FIG. 49 A timing chart showing an example of a black inserting process (blinking process) on the frame unit basis by a backlight driving unit illustrated in FIG. 48.

[0076] FIG. 50 A timing chart showing an example of the black inserting process (blinking process) on the black insertion line unit basis by the backlight driving unit illustrated in FIG. 48.

[0077] FIG. 51 A timing chart showing an example of the black inserting process (blinking process) in combination of the black insertion line unit basis and the frame unit basis by the backlight driving unit illustrated in FIG. 48.

[0078] FIG. 52 A timing chart showing an example of a black insertion ratio in the black inserting process on the frame unit basis.

[0079] FIG. 53 A timing chart showing another example of the black insertion ratio in the black inserting process on the frame unit basis.

[0080] FIG. 54 A timing chart showing an example of the black insertion ratio in the black inserting process in combination of the black insertion line unit basis and the frame unit basis.

[0081] FIG. 55 A timing chart showing another example of the black insertion ratio in the black inserting process in combination of the black insertion line unit basis and the frame unit basis.

[0082] FIG. 56 A characteristic diagram showing an example of a luminance histogram distribution of an entire screen.

[0083] FIG. 57 A block diagram showing an example of the configuration of an image display apparatus according to a modified example of the fourth embodiment.

[0084] FIG. 58 A block diagram showing an example of a hardware configuration of all or part of a video signal processor to which the present invention is applied.

BEST MODE(S) FOR CARRYING OUT THE INVENTION

[0085] Embodiments of the present invention will be described in detail hereinbelow with reference to the drawings.

First Embodiment

[0086] FIG. 5 is a block diagram showing an example of the circuit configuration of a video signal processor (video signal processor 4) according to a first embodiment of the present

invention. The video signal processor 4 is built in a television receiver. A digital component signal YUV subjected to processes such as tuning and decoding by a tuner, a decoder, and the like which are not shown is supplied to the video signal processor 4.

[0087] The digital component signal YUV supplied to the video signal processor 4 is input to a preprocessor 41 and sequentially written to a memory 43 via a memory controller 42.

[0088] The preprocessor 41 performs a process of separating a luminance signal Y from the digital component signal YUV. The luminance signal Y separated by the preprocessor 41 is also sequentially written in the memory 43 via the memory controller 42.

[0089] The luminance signal Y written in the memory 43 is sequentially read by the memory controller 42 (as shown in FIGS. 2 and 3, in the case of a film signal in which the same original frame is repeated twice or three times, the same original frame is read only once) and is sent to a motion vector detector 44. The motion vector detector 44 performs a motion vector detecting process by block matching using the luminance signal Y of the present frame and the luminance signals Y of the immediately preceding and subsequent frames.

[0090] A motion vector mv of each of the frames detected by the motion vector detector 44 is written in the memory 43 via the memory controller 42. After that, the motion vector mv is read from the memory 43 and sent again to the motion vector detector 44 so as to be referred to in motion vector detection of the following frame.

[0091] Further, the memory controller 42 reads the digital component signals YUV written in the memory 43 at double speed, in two series while deviating the signals from each other by one frame (in the case of a film signal in which the same original frame is repeated twice or three times as shown in FIGS. 2 and 3, the same original frame is read only once). Further, the memory controller 42 reads the motion vector mv indicative of motion between the two frames at double speed. The two series of digital component signals 2YUV and the motion vector mv read in such a manner are transmitted to an interpolation section 45.

[0092] The interpolation section 45 is provided with two series of search range memories 451 and 452 and an interpolator 453. One of the two series of digital component signals 2YUV from the memory controller 42 is written to the search range memory 451 and the other is written to the search range memory 452. The motion vector mv from the memory controller 42 is input to the interpolator 453.

[0093] Further, from a CPU 46 in the television receiver, an interpolation position parameter Relpos indicative of the interpolation position of a video image in an interpolation frame is supplied to the interpolation section 45 via an I²C bus 40 as a serial bus and a decoder 47 for parallel converting the serial signal (the details of the interpolation position parameter Relpos will be described later). The interpolation position parameter Relpos is also input to the interpolator 453.

[0094] On the basis of the motion vector mv and the interpolation position parameter Relpos, the interpolator 453 calculates addresses of pixels in original frames in the search range memories 451 and 452 used for calculating pixel values of an interpolation frame.

[0095] FIG. 6 is a diagram conceptually showing the principle of the address calculation. n-1 indicates, in the vertical axis direction, an address (the position in the x direction and the y direction on the screen) of each of pixels of an original

frame which comes fast out of the two original frames deviated by one frame which are written in the search range memories 451 and 452. n indicates, in the vertical axis direction, an address of each of pixels of the later original frame out of the two original frames.

[0096] i indicates the address of each of pixels in the interpolation frame in the vertical axis direction. The horizontal axis indicates time and shows timing of the interpolation frame i between the original frames n-1 and n (herein as an example, the timing corresponding to the interpolation frame in the center out of the three interpolation frames in FIG. 2(b)). Relpos indicates an interpolation position parameter supplied for generation of the interpolation frame i.

[0097] mv(x,y)int shows the motion vector mv between the original frames n-1 and n with respect to the address (x, y) of a pixel which is being generated at present (called reference pixel) in each of pixels of the interpolation frame i. zeroPelPrev(x,y) indicates the value of a pixel in the reference address (x, y) in the original frame n-1. zeroPelSucc(x, y) indicates the value of a pixel in the reference address (x, y) in the original frame n.

[0098] The interpolator 453 obtains the addresses of the pixels in the original frames n-1 and n used for calculating the pixel value of the reference address (x, y) by the following formula (1) on the basis of the reference address (x, y), a component mvX in the x direction of the motion vector mv(x, y)int, a component mvY in the y direction of the motion vector mv(x,y)int, and the interpolation position parameter Relpos.

[0099] [Mathematical Formula 1]

Address of pixel in original frame n-1=(x+mvX·Relpos, y+mvY·Relpos)

Address of pixel in original frame n=(x-mvX·(1-Relpos), y-mvY·(1-Relpos)) (1)

[0100] The interpolator 453 sends the addresses obtained as described above to the search range memories 451 and 452 and reads pixel values prev and succ of the addresses. Then using the pixel values prev and succ and the interpolation position parameter Relpos, a pixel value Out of the reference address (x, y) of the interpolation frame i is calculated by the following formula (2).

[0101] [Mathematical Formula 2]

Out=prev·(1-Relpos)+succ·Relpos (2)

[0102] By executing such calculation sequentially on each of pixels of the interpolation frame i (sequentially updating the value (x, y) of the reference address), the interpolation frame i is generated.

[0103] Next, the interpolation position parameter Relpos supplied from the CPU 46 to the interpolation section 45 will now be described. FIG. 7 is a diagram showing the interpolation position parameter Relpos supplied from the CPU 46. In the case where a 2:2 pulldown film signal (refer to FIG. 2(a)) is supplied as the digital component signal YUV to the video signal processor 4 of FIG. 5, the CPU 46 supplies parameters of four phases Relpos_22_0, Relpos_22_1, Relpos_22_2, and Relpos_22_3 every 1/100 sec (that is, at 1/2 sec cycles). Each of the parameters of the phases is made of six bits ([5:0] in the diagram expresses six bits).

[0104] Relpos_22_0 is a parameter for outputting the preceding one of the two original frames deviated from each other by one frame in the search range memories 451 and 452 from the interpolator 453. Relpos_22_1 to Relpos_22_3 are

parameters for generating three interpolation frames at $\frac{1}{100}$ sec intervals as shown in FIG. 2(b) between the two original frames.

[0105] In the case where the 2:2 pulldown film signal is supplied, the same original frame is held for $\frac{1}{25}$ sec in the search range memories 451 and 452 (FIG. 5). Then, during $\frac{1}{25}$ sec, the interpolator 453 calculates an interpolation frame by the formulae (1) and (2) on each of the parameters of respective phases Relpos_22_0, Relpos_22_1, Relpose_22_2, and Relpos_22_3. By repeating the process at $\frac{1}{25}$ sec cycles, the 2:2 pulldown film signal is frame-rate-converted.

[0106] On the other hand, in the case where a 3:2 pulldown film signal (refer to FIG. 3(a)) is supplied as the digital component signal YUV to the video signal processor 4 of FIG. 5, the CPU 46 supplies interpolation position parameters of five phases Relpos_32_0, Relpos_32_1, Relpos_32_2, Relpos_32_3, and Relpos_32_4 every $\frac{1}{120}$ sec (that is, at $\frac{1}{24}$ sec cycles).

[0107] Relpos_32_0 is a parameter for outputting the preceding one of the two original frames deviated from each other by one frame in the search range memories 451 and 452 from the interpolator 453. Relpos_32_1 to Relpos_32_4 are parameters for generating four interpolation frames at $\frac{1}{120}$ sec intervals as shown in FIG. 3(b) between the two original frames.

[0108] In the case where the 3:2 pulldown film signal is supplied, the same original frame is held for $\frac{1}{24}$ sec in the search range memories 451 and 452. Then, during $\frac{1}{24}$ sec, the interpolator 453 calculates an interpolation frame by the formulae (1) and (2) on each of the parameters of respective phases Relpos_32_0, Relpos_32_1, Relpose_32_2, Relpos_32_3, and Relpos_32_4. By repeating the process at $\frac{1}{24}$ sec cycles, the 3:2 pulldown film signal is frame-rate-converted.

[0109] The value of the interpolation position parameter Relpos is selected by the user. Specifically, as shown in FIG. 5, a remote controller 400 attached to the television receiver is provided with an interpolation position adjustment button 401 for switching and selecting the value of the interpolation position parameter Relpos in three levels of "strong, medium, and weak".

[0110] A signal indicative of the selection result by the interpolation position adjustment button 401 is received from the remote controller 400 by an infrared light receiving unit 48 in the television receiver. When the signal is transmitted to the CPU 46 via the I²C bus 40, the CPU 46 sets the value of the interpolation position parameter Relpos according to the selection result.

[0111] FIG. 8 is a diagram showing the values of the interpolation position parameters Relpos set by the CPU 46 in accordance with the selection result of the interpolation position adjustment button 401 in the case where the 3:2 pulldown film signal is supplied. In the case where "strong" is selected by the interpolation position adjustment button 401, the values of Relpos_32_0, Relpos_32_1, Relpos_32_2, Relpos_32_3, and Relpos_32_4 are set to 0, 0.2, 0.4, 0.6, and 0.8, respectively.

[0112] Since the value of the parameter Relpos_32_0 of the first phase is 0, the preceding one of the two original frames in the search range memories 451 and 452 is output as it is from the interpolator 453 by the formulae (1) and (2).

[0113] Further, since the values of the parameters Relpos_32_1, Relpos_32_2, Relpos_32_3, and Relpos_32_4 of the second, third, fourth, and fifth phases change uniformly by 0.2 like 0.2, 0.4, 0.6 and 0.8, from the formulae (1) and (2), the

interpolation positions of video images in the four interpolation frames generated between the two original frames in the search range memories 451 and 452 are the same as the interpolation positions in related art shown in FIG. 3(b). The positions are obtained by uniformly dividing the magnitude of a motion of a video image between the two original frames into five portions, that is, positions of 20%, 40%, 60%, and 80% according to the magnitude of the motion.

[0114] In the case where "medium" is selected by the interpolation position adjustment button 401, the values of Relpos_32_0, Relpos_32_1, Relpos_32_2, Relpos_32_3, and Relpos_32_4 are set to 0, 0.15, 0.3, 0.7, and 0.85, respectively. Since the value of the parameter Relpos_32_0 of the first phase is 0, like in the case of "strong", the preceding one of the two original frames in the search range memories 451 and 452 is output as it is from the interpolator 453.

[0115] On the other hand, the values 0.15 and 0.3 of the parameters Relpos_32_1 and Relpos_32_2 of the second and third phases as shown in FIG. 3(b), these are parameters for generating an interpolation frame closer to the preceding original frame of the four interpolation frames between the neighboring original frames smaller than the values 0.2 and 0.4 in the case of "strong".

[0116] The values 0.7 and 0.85 of the parameters Relpos_32_3 and Relpos_32_4 of the fourth and fifth phases as shown in FIG. 3(b), these are parameters for generating an interpolation frame closer to the subsequent one of the four interpolation frames between the neighboring original frames larger than the values 0.6 and 0.8 in the case of "strong".

[0117] By the values of the parameters Relpos_32_1 to Relpos_32_4, in the case of "medium", the interpolation positions of the video image in the four interpolation frames generated between the two original frames in the search range memories 451 and 452 are positions of 15%, 30%, 70%, and 85% according to the magnitude of the motion of the video image between the two original frames. That is, the interpolation positions of the video images in the four interpolation frames are not positions (the same interpolation positions as those in related art) obtained by evenly dividing the magnitude of the motion of the video image between the two original frames like in the case of "strong" but are positions closer to the video images in the original frames close to the interpolation frames than the evenly divided positions.

[0118] In the case where "weak" is selected by the interpolation position adjustment button 401, the values of Relpos_32_0, Relpos_32_1, Relpos_32_2, Relpos_32_3, and Relpos_32_4 are set to 0, 0.1, 0.2, 0.8, and 0.9, respectively. The values 0.1 and 0.2 of the parameters of the second and third phases (parameters for generating interpolation frames closer to the front original frame, in the four interpolation frames between the neighboring original frames) are further smaller than the values 0.15 and 0.3 in the case of "medium".

[0119] Further, the values 0.8 and 0.9 of the parameters of the fourth and fifth phases (parameters for generating interpolation frames closer to the rear original frame, in the four interpolation frames between the neighboring original frames) are larger than the values 0.7 and 0.85 in the case of "medium".

[0120] By the values of the parameters Relpos_32_1 to Relpos_32_4, in the case of "weak", the interpolation positions of the video image in the four interpolation frames generated between the two original frames in the search range memories 451 and 452 are positions of 10%, 20%, 80%, and 90% according to the magnitude of the motion of the video

image between the two original frames. That is, the interpolation positions of the video images in the four interpolation frames are positions nearer to the video image in the original frame closer to the interpolation frames as compared with the case of “medium”.

[0121] FIG. 9 is a diagram showing the values of the interpolation position parameters Relpos set by the CPU 46 in accordance with the selection result of the interpolation position adjustment button 401 in the case where the 2:2 pulldown film signal is supplied. In the case where “strong” is selected by the interpolation position adjustment button 401, the values of Relpos_22_0, Relpos_22_1, Relpos_22_2, and Relpos_22_3 are set to 0, 0.25, 0.5, and 0.75, respectively.

[0122] Since the value of the parameter Relpos_22_0 of the first phase is 0, the preceding original frame of the two original frames in the search range memories 451 and 452 is output as it is from the interpolator 453.

[0123] Further, since the values of the parameters Relpos_22_1, Relpos_22_2, and Relpos_22_3 of the second, third, and fourth phases change uniformly by 0.25 like 0.25, 0.5, and 0.75, from the formulae (1) and (2), the interpolation positions of video images in the three interpolation frames generated between the two original frames in the search range memories 451 and 452 are the same as the interpolation positions in related art shown in FIG. 2(b). The positions are obtained by uniformly dividing the magnitude of a motion of a video image between the two original frames into four portions, that is, positions of 25%, 50%, and 75% according to the magnitude of the motion.

[0124] In the case where “medium” is selected by the interpolation position adjustment button 401, the values of Relpos_22_0, Relpos_22_1, Relpos_22_2, and Relpos_22_3 are set to 0, 0.15, 0.3, and 0.85, respectively. Since the value of the parameter Relpos_22_0 of the first phase is 0, like in the case of “strong”, the preceding one of the two original frames in the search range memories 451 and 452 is output as it is from the interpolator 453.

[0125] On the other hand, the value 0.15 of the parameter Relpos_22_1 of the second phase (as shown in FIG. 2(b), this is a parameter for generating an interpolation frame closer to the preceding original frame in the three interpolation frames between the neighboring original frames) smaller than the value 0.25 in the case of “strong”.

[0126] Further, as shown in FIG. 2(b), the parameter Relpos_22_2 of the third phase is a parameter for generating an interpolation frame right in the middle of the front original frame and the rear original frame in the three interpolation frames between the neighboring original frames. Herein, by classifying the middle interpolation frame as an interpolation frame nearer to the front original frame, the value of the parameter Relpos_22_2 becomes the value 0.3 smaller than the value 0.5 in the case of “strong”.

[0127] The value 0.85 of the parameter Relpos_22_3 of the fourth phase (as shown in FIG. 2(b), this is a parameter for generating an interpolation frame nearer to the rear original frame in the three interpolation frames between the neighboring original frames) is larger than the value 0.75 in the case of “strong”.

[0128] By the values of the parameters Relpos_22_1 to Relpos_22_3, in the case of “medium”, the interpolation positions of the video image in the three interpolation frames generated between the two original frames in the search range memories 451 and 452 are positions of 15%, 30%, and 85% according to the magnitude of the motion of the video image

between the two original frames. That is, the interpolation positions of the video images in the three interpolation frames are not positions (the same interpolation positions as those in related art) obtained by evenly dividing the magnitude of the motion of the video image between the two original frames like in the case of “strong” but are positions closer to the video images in the original frame nearer to the interpolation frames than the evenly divided positions.

[0129] In the case where “weak” is selected by the interpolation position adjustment button 401, the values of Relpos_22_0, Relpos_22_1, Relpos_22_2, and Relpos_22_3 are set to 0, 0.1, 0.2, and 0.9, respectively. The values 0.1 and 0.2 of the parameters of the second and third phases (parameters for generating interpolation frames nearer to the front original frame, in the three interpolation frames between the neighboring original frames) are further smaller than the values 0.15 and 0.3 in the case of “medium”.

[0130] Further, the value 0.9 of the parameter of the fourth phase (parameter for generating an interpolation frame nearer to the rear original frame, in the three interpolation frames between the neighboring original frames) is larger than the value 0.85 in the case of “medium”.

[0131] By the values of the parameters Relpos_22_1 to Relpos_22_3, in the case of “weak”, the interpolation positions of the video image in the three interpolation frames generated between the two original frames in the search range memories 451 and 452 are positions of 10%, 20%, and 90% according to the magnitude of the motion of the video image between the two original frames. That is, the interpolation positions of the video images in the three interpolation frames are positions nearer to the video image in the original frame closer to the interpolation frames as compared with the case of “medium”.

[0132] FIG. 10 are diagrams showing, using the video images of the same original frame as that of FIG. 4 as an example, video images (FIG. 10(b)) subjected to the frame rate conversion in the case where the 3:2 pulldown film signal is supplied to the video signal processor 4 of FIG. 5 and “weak” is selected by the interpolation position adjustment button 401 in comparison with video images (FIG. 10(a)) in interpolation positions in related art.

[0133] As shown in FIG. 10(b), in two interpolation frames closer to the front original frame A, the image of an airplane is positioned nearer to the original frame A as compared with that in the case of the related art. On the other hand, in two interpolation frames closer to the rear original frame B, the image of the airplane is positioned nearer to the original frame B as compare with that in the case of the related art. Therefore, the interval between the positions of the images of the airplane of the second and third interpolation frames is larger than that of the related art.

[0134] As described above, in the video signal processor 4, when “weak” or “medium” is selected by the interpolation position adjustment button 401, the interpolation position in an interpolation frame nearer to the earlier original frame in the earlier original frame and the following original frame is shifted toward the video image of the front original frame. The interpolation position in an interpolation frame nearer to the rear original frame is shifted toward the video image of the rear original frame.

[0135] Consequently, as also shown in FIG. 10, between the interpolation frames nearer to the front original frame and the interpolation frames nearer to the rear original frame, the

interval of positions of vide images interpolated is larger than that in the case of the related art.

[0136] As described above, the interpolation frames whose interpolation positions of the video images are apart from each other more than the case of the related art. Consequently, unsmoothness of the motion of the video image between the interpolation frames is more conspicuous than the case of the related art. Therefore, at the time of performing the frame rate conversion of the film signal, while reducing a judder by the frame rate conversion, the degree of reduction is able to be lowered more than the case of the related art.

[0137] In addition, in the case where the user watches a video image of a film signal by the television receiver, some users prefer the case where the judder is reduced largely to make the motion of the video image smoother, and some users prefer the case where judder remains to some extent for the reason that they like an image of a film signal. Consequently, a user who prefers smoother motion of a video image selects "strong" with the interpolation position adjustment button **401**. A user who prefers an image where judder remains to some extent selects "weak" or "medium" with the interpolation position adjustment button **401**. Thus, the degree of reduction of judder can be selected according to the preference of each user.

[0138] As described above in "Background Art", in the frame rate conversion using motion compensation, in the case where motion of a video image between neighboring original frames becomes very quick, the motion vector lies out of the motion vector search range, so that a large judder occurs. In such a case as well, by decreasing the degree of reducing a judder by selecting "weak" or "medium" with the interpolation position adjustment button **401**, even when a large judder occurs while the user watches a video image including some judders, the user feels less strange than the conventional case where a large judder suddenly occurs in a video image in which the motion is very smooth.

[0139] In addition, in the frame rate conversion using motion compensation, it is known that, as a side effect, a phenomenon (called Halo) occurs such that noise like shimmer is seen in the contour of a video image of a moving human or the like. The Halo becomes more conspicuous as the position of the video image to be interpolated is apart from the position of the video image in the original frame. On the contrary, when "weak" or "medium" is selected with the interpolation position adjustment button **401**, the position of a video image to be interpolated becomes nearer to the video image in the original frame, so that the Halo is able to be suppressed.

[0140] In the example of FIG. 5, the remote controller **400** is provided with the interpolation position adjustment button **401** for switching and selecting the value of the interpolation position parameter Relpos in three levels of "strong, medium, and weak". However, as another example, operating means such as a volume switch for selecting the value of the interpolation position parameter Relpos while continuously (steplessly) changing the value within the range of "strong" to "weak" in FIGS. 8 and 9 may be provided for the remote controller **400** or the television receiver body. In this case, to further decrease the minimum change amount of the value of the interpolation position parameter Relpos, the number of bits of the interpolation position parameter Relpos supplied from the CPU **46** may be set to be larger than six bits (for example, about eight bits).

[0141] Next, FIG. 11 is a block diagram showing an example of the circuit configuration of a video signal processor (video signal processor **4A**) according to a modified example of the embodiment. The same reference numerals are designated to the same components as those of the video signal processor **4** shown in FIG. 5, and their description will not be repeated.

[0142] In the video signal processor **4A**, the S/N level of the digital component signal YUV supplied to the video signal processor **4A** is detected by an S/N level detector **49**. Then, a signal indicative of the detection result is sent to the CPU **46** via the I²C bus **40**.

[0143] In the frame rate conversion using the motion compensation, as described above, the phenomenon (Halo) occurs such that noise like shimmer appears in the contour of a video image of a moving human or the like. The Halo becomes more conspicuous as an interpolation position of a video image is apart from the position of the video image in the original frame. In addition, the Halo occurs more as the S/N level of a video signal decreases (the noise level increases).

[0144] In a memory in the CPU **46**, information indicative of an S/N level of a predetermined value which is preset as a border of whether a Halo occurs easily or not is pre-stored. In the case where the detection result of the S/N level detector **49** is higher than the predetermined level, the CPU **46** sets the interpolation position parameter Relpos supplied to the interpolation section **45** to the value of "strong" in FIGS. 8 and 9. On the other hand, when the detection result of the S/N level detector **49** is equal to or less than the predetermined level, the CPU **46** sets the interpolation position parameter Relpos supplied to the interpolation section **45** to the value of "weak" (or "medium") in FIGS. 8 and 9.

[0145] Thereby, in the case where the S/N level of the digital component signal YUV to be supplied is high (in the case where Halo does not easily occur), the motion of a video image is able to be made smooth. In the case where the S/N level is low (in the case where Halo easily occurs), by setting the interpolation position of the video image nearer to the video image of the original frame, the Halo is able to be suppressed.

[0146] In addition, the case of frame-rate converting the film signal is exemplified in the embodiment. However, for example, in the case of converting the frame rate of a camera signal of the NTSC system to 240 Hz as shown in FIG. 12, three interpolation frames are added at 1/240 sec intervals between neighboring original frames (between the frames A and B, between the frames B and C, and between the frames C and D). Although not shown, in the case of converting the frame rate of a camera signal in the PAL system to 200 Hz, three interpolation frames are added at 1/200 sec intervals between neighboring original frames. The present invention may be applied also to the case of converting a camera signal to a high frame rate as described above.

[0147] In the embodiment, the example of setting the value of the interpolation position parameter Relpos by selecting operation of the user and the example of setting the value of the interpolation position parameter Relpos in accordance with the S/N level of a video signal have been described. However, as further another method of setting the value of the interpolation position parameter Relpos, for example, information of genres of television broadcast programs received at present is obtained from an EPG (Electronic Program Guide) and the value of the interpolation position parameter Relpos

may be set according to the genre (for example, the value of “strong” in FIGS. 8 and 9 is set in a genre in which motion of a video image is slow, and the value of “weak” or “medium” in FIGS. 8 and 9 is set in a genre in which motion of a video image is fast).

[0148] Alternatively, the value of the interpolation position parameter Relpos may be set to the value of “weak” or “medium” in FIGS. 8 and 9 by fact reset.

[0149] Further, the values of “weak” and “medium” shown in FIGS. 8 and 9 are just an example. Obviously, by another value, the interpolation position of a video image in each interpolation frame may be set to a position nearer to the video image of the original frame closer to the interpolation frame.

[0150] Furthermore, in the embodiment, the example of applying the present invention to the video signal processor in the television receiver has been described. However, the invention is also applicable to any video signal processor for converting the frame rate of a video signal by using motion compensation such as a video signal processor in a DVD player.

Second Embodiment

[0151] A second embodiment of the present invention will now be described.

[0152] FIG. 13 shows an example of the configuration of a video signal processor (video signal processor 4B) of the second embodiment. The same reference numerals are designated to the same components as those of the foregoing embodiment, and their description will not be repeated.

[0153] The video signal processor 4B executes various image processes on moving image data on an access unit basis. The access unit is a unit of a moving image such as a frame or a field and, concretely, refers to, for example, an entire frame or a part of a frame constituting a moving image. In this case, the frame denotes here a single stationary image. Therefore, the entire frame corresponds to a frame. However, hereinafter, for simplicity of explanation, it is assumed that the video signal processor 4B executes various image processes on moving image data on the frame unit basis.

[0154] As shown in FIG. 13, the video signal processor 4B is obtained by further providing the video signal processor 4A (including the interpolation section 45 (high frame rate converting unit)) described in the first embodiment with an imaging blur characteristic detector 12 and an imaging blur suppression processor 13.

[0155] To the interpolation section 45, as described in the first embodiment, for example, a moving image signal such as a television broadcast signal is input as moving image data in the frame unit.

[0156] In the following, in the case where the moving image and moving image data corresponding to the moving image do not have to be discriminated from each other, the moving image and moving image data corresponding to the moving image will be simply called a moving image collectively. Similarly, in the case where a frame and frame data corresponding to the frame do not have to be discriminated from each other, they will be simply called a frame.

[0157] In the case where a moving image at a first frame rate is input, the interpolation section 45 performs high frame rate converting process on the moving image and supplies a moving image of a second frame rate higher than the first

frame rate, obtained as a result of the process, to the imaging blur characteristic detector 12 and the imaging blur suppression processor 13.

[0158] The high frame rate converting process is a process executed in the case where the first frame rate at the time of input is lower than the second frame rate at the time of output (display). It is a process of converting the first frame rate to the second frame rate higher than the first frame rate by creating a new frame and inserting it between each of frames constructing a moving image at the time of input.

[0159] In this case, the first frame rate refers to a frame rate of a moving image at the time point when the moving image is input to the interpolation section 45. Therefore, the first frame rate can be an arbitrary frame rate. In this case, for example, it is a frame rate when a moving image is captured by a not-shown imaging apparatus, that is, an imaging frame rate.

[0160] Further, in the embodiment, as an example of the high frame rate converter for performing such high frame rate converting process, the interpolation section 45 described in the first embodiment will be described (in the case of adding N pieces of interpolation frames between neighboring original frames, as the interpolation positions of the video image in the interpolation frames, not positions obtained by equally dividing the magnitude of the motion of the video image between the earlier original frame and the following original frame, positions closer to the video images of original frames nearer to the interpolation frames than the evenly divided positions are set). In place of the interpolation section 45, a normal high frame rate converter (which sets, as video image interpolation positions in interpolation frames, positions obtained by evenly dividing the magnitude of the motion of the video image between the earlier original frame and the following original frame) may be provided.

[0161] The imaging blur characteristic detector 12 detects the value of a parameter indicative of the characteristic of an imaging blur with respect to each of the frames constructing a moving image supplied from the interpolation section 45. The detection result of the imaging blur characteristic detector 12, that is, the value of the parameter indicative of the characteristic of the imaging blur is supplied to the imaging blur suppression processor 13.

[0162] In addition, the parameter indicative of the characteristic of the imaging blur is not limited but various parameters are able to be employed. Concrete examples of the parameter indicative of the characteristic of such an imaging blur will be described later. For example, in the case of using the absolute value of a travel vector (motion vector) as the parameter indicative of the characteristic of the imaging blur, the imaging blur characteristic detector 12 may include the motion vector detector 44 described in the first embodiment.

[0163] The number of detected values of the parameter indicative of the characteristic of the imaging blur in one frame is not particularly limited. For example, only one value of the parameter indicative of the characteristic of an imaging blur may be detected per frame. The value of the parameter indicative of the characteristic of the imaging blur may be detected for each of the pixels constructing the frame. It is also possible to divide the one frame into some blocks and detect the value of the parameter indicative of the characteristic of the imaging blur for each of the divided blocks.

[0164] The imaging blur suppression processor 13 corrects the value of each of pixels constructing a frame to be processed on the basis of a value corresponding to the frame to be

processed in the values of the parameter detected by the imaging blur characteristic detector 12 with respect to each of the frames constructing a moving image supplied from the interpolation section 45. Namely, according to the characteristic (the value of the parameter) of the imaging blur in the frame to be processed, the imaging blur suppression processor 13 corrects each of the pixel values of the frame to be processed so as to suppress the imaging blur. That is, using the detected value of the parameter, the imaging blur suppressing process of suppressing deterioration in picture quality caused by the imaging blur included in each of the frames supplied from the interpolation section 45 is performed.

[0165] Thereby, a moving image in which the imaging blur is suppressed by correcting each of the pixel values of each of the frames and which is converted to the second frame rate higher than the first frame rate at the time of input is output from the imaging blur suppression processor 13 to the outside of the video signal processor 4B.

[0166] In the example of FIG. 13, the set of the imaging blur characteristic detector 12 and the imaging blur suppression processor 13 is used in combination with the interpolation section 45. However, naturally, the set may be used by itself, or can be used in combination with a not-shown another function block (another video image signal processor for performing a predetermined image process).

[0167] That is, only by the set of the imaging blur characteristic detector 12 and the imaging blur suppression processor 13, the effect of suppressing the imaging blur can be produced. However, to make the effect more conspicuous, it is preferable to combine the set of the imaging blur characteristic detector 12 and the imaging blur suppression processor 13 with the interpolation section 45 as described above. The reason will be described below.

[0168] A blur recognized by a human when a moving image displayed on a not-shown display apparatus is formed as an image on the retina of the human is a combination of a hold blur which occurs when the human follows and sees a moving object included in the moving image and an imaging blur added at the time of capture of the moving image.

[0169] The characteristic of the imaging blur is expressed as a low-pass filter as will be described later with reference to FIG. 16 and the like. Specifically, an image signal after the imaging blur is a signal equivalent to a signal obtained by passing an image signal before an imaging blur (ideal image signal) through the low-pass filter. Therefore, the frequency characteristic of the image signal with the imaging blur is worse than that of the image signal without the imaging blur. That is, generally, the higher the frequency is, the lower the gain of the image signal with the imaging blur is as compared with that of the image signal without the imaging blur.

[0170] The characteristic of the hold blur is also expressed as the low-pass filter like the characteristic of the imaging blur. That is, an image signal with the hold blur is a signal equivalent to a signal obtained by passing an image signal without a hold blur (the image signal with the imaging blur) through the low-pass filter. Therefore, the frequency characteristic of the image signal with the hold blur is worse than that of the image signal without the hold blur. That is, generally, the higher the frequency is, the lower the gain of the image signal with the hold blur is as compared with that of the image signal without the hold blur. However, the hold blur occurs only in the case where the display apparatus is a fixed-pixel (hold) display apparatus.

[0171] Therefore, by performing the high frame rate converting process on the image signal with the imaging blur whose frequency characteristic has already deteriorated due to the imaging blur, the hold blur is able to be suppressed. However, even if the high frame rate converting process is performed, the deterioration of the imaging blur is unchanged and, finally, the effect of suppressing the blur on the retina of a human is halved. This will be described with reference to FIG. 14.

[0172] FIG. 14 shows a frequency characteristic of a blur in an image formed on the retina of a human in the case where an image of a real object moving at a travel speed 4 [pixel/frame] is captured in an image capture range of an image capturing apparatus (hereinbelow, called a camera). In FIG. 14, the horizontal axis denotes frequency, and the vertical axis indicates gain. However, each value on the horizontal axis denotes relative values in the case where the Nyquist frequency is 1.

[0173] In FIG. 14, a curve h0 indicated by an alternate long and short dash line shows the frequency characteristic of a blur in an image formed on the retina of a human, in the case where a process for reducing blurs (including the imaging blur and the hold blur) is not performed. Specifically, in the case where a moving image, which is input to the video signal processor 4B in the example of FIG. 13, is directly supplied to the display apparatus and displayed without being input to the video signal processor 4B (without being processed), the frequency characteristic of a blur in an image formed on the retina of a human who sees the moving image is the curve h0.

[0174] In contrast, for example, when the display speed is doubled by the high frame rate converting process, only the hold blur is reduced. As a result, the frequency characteristic of a blur in an image formed on the retina of a human becomes a curve h1 shown by a dotted line in the diagram. Specifically, in the case where a moving image which is input to the video signal processor 4B in FIG. 13 is subjected to the high frame rate converting process in the interpolation section 45 and then is supplied to the display apparatus and displayed without being input to the imaging blur suppression processor 13 (without reducing the imaging blur), the frequency characteristic of a blur in an image formed on the retina of a human who sees the moving image is the curve h1.

[0175] For example, when the display speed is doubled by the high frame rate converting process (the hold blur is reduced), and the degree of the imaging blur is improved by applying the present invention, the frequency characteristic of a blur in an image formed on the retina of a human becomes a curve h2 indicated by the solid line in the diagram. Specifically, in the case where a moving image which is input to the video signal processor 4B in FIG. 13 is subjected to the high frame rate converting process in the interpolation section 45, subject to imaging blur suppression by the imaging blur suppression processor 13, and then is supplied to the display apparatus and displayed, the frequency characteristic of a blur in an image formed on the retina of a human who sees the moving image is the curve h2.

[0176] It is understood from comparison between the curves h1 and h2 that reduction only in the hold blur by the high frame rate converting process is insufficient for reduction in the characteristic of the blur on the retina of a human, and further reduction in the imaging blur is necessary. However, as described above, in the technique of the related art, the

high frame rate converting process is simply performed without particularly considering necessity of reduction in the imaging blur.

[0177] Therefore, the video signal processors of the present invention, in the embodiment of FIG. 13 and embodiments of FIGS. 35 and 36 and the like which will be described later is provided with not only the interpolation section 45 but also the imaging blur characteristic detector 12 and the imaging blur suppression processor 13 in order to reduce the imaging blur, that is, to improve the characteristic of the blur on the retina of a human from the curve h0 to curve h2 in FIG. 14. However, as described in the embodiment of FIGS. 37 and 38, the imaging blur characteristic detector 12 is not an essential component for the video signal processor of the present invention.

[0178] That is, the imaging blur suppression processor 13 corrects each of the pixel values of each of frames to be processed on the basis of the value corresponding to the frames to be processed in the values of parameters indicative of characteristics of the imaging blur detected by the imaging blur characteristic detector 12, thereby suppressing deterioration in the image caused by the imaging blur in the frames subjected to the high frame rate conversion. In other words, by supplying an image signal output from the video signal processor of the present invention such as the video signal processor 4B to the not-shown display apparatus, the display apparatus is able to display a clear image in which the image deterioration (blur image) is suppressed as an image corresponding to the image signal.

[0179] As described above, it is preferable to combine the set of the imaging blur characteristic detector 12 and the imaging blur suppression processor 13 with the interpolation section 45.

[0180] Next, with reference to the flowchart of FIG. 15, the image process of the video signal processor 4B having the functional configuration of FIG. 13 will be described.

[0181] In step S1, the interpolation section 45 inputs a moving image of the first frame rate.

[0182] In step S2, the interpolation section 45 converts the frame rate of the moving image to the second frame rate higher than the first frame rate.

[0183] When the moving image converted from the first frame rate to the second frame rate is supplied from the interpolation section 45 to the imaging blur detector 12 and the imaging blur suppression processor 13, the process advances to step S3.

[0184] In step S3, the imaging blur characteristic detector 12 detects one or more values of parameters indicative of the characteristics of the imaging blur in each of the frames constructing the moving image.

[0185] When the one or more values of parameters indicative of the characteristics of the imaging blur in each of the frames constructing the moving image are supplied from the imaging blur characteristic detector 12 to the imaging blur suppression processor 13, the process advances to step S4.

[0186] In step S4, with respect to each of the frames constructing the moving image supplied from the interpolation section 45, the imaging blur suppression processor 13 corrects each of the pixel values of the frame to be processed on the basis of one or more values corresponding to the frame to be processed among the values of the parameter detected by the imaging blur detector 12.

[0187] In step S5, the imaging blur suppression processor 13 outputs the moving image obtained by correcting the pixel values of each of the frames and changing the first frame rate to the second frame rate.

[0188] After that, the image process of FIG. 15 is finished.

[0189] In the above description, for simplicity of the explanation, the processes in each of steps S1 to S5 are performed on the moving image unit basis. In reality, however, the frame is often the process unit.

[0190] In the image process of FIG. 15, the fact that the process unit of each step is a moving image is equivalent to the fact that the condition of moving the step to be processed in the steps S1 to S5 to the next step is a condition that the process of the step to be processed is performed on an entire moving image.

[0191] On the other hand, in the image process of FIG. 15, the fact that the process unit in each of the steps is a frame is equivalent to the fact that the condition of moving the step to be processed in the steps S1 to S5 to the next step is a condition of performing the process of the step to be processed on an entire frame. In other words, the state where the process unit in each of the steps is a frame is equivalent to the state where the continuous processes in the steps S1 to S5 on each of the frames are executed independently from (in parallel with) another frame. In this case, for example, when the process in the step S3 is executed on the first frame, the process in the step S2 on the second frame different from the above may be executed in parallel.

[0192] Further, in reality, it often happens that each of pixels constructing a frame to be processed is sequentially set as a pixel to be noted as an object of the process (hereinbelow, called a target pixel) and, at least, the processes in the steps S3 and S4 are sequentially and individually performed on the target pixel. That is, the process unit in the steps S3 and S4 is often a pixel.

[0193] In the following description, therefore, it will be also assumed that the processes in the steps S3 and S4 are performed on the pixel unit basis. Specifically, the process in the step S3 is a process of the imaging blur characteristic detector 12. The process in the step S4 is a process of the imaging blur suppression processor 13. Therefore, the following description will be given on assumption that the process unit of the imaging blur characteristic detector 12 and the imaging blur suppression processor 13 is a pixel.

[0194] Next, the details of the imaging blur suppression processor 13 in the video signal processor 4B in FIG. 13 will now be described. Concretely, for example, an embodiment of the imaging blur suppression processor 13 in the case of using the absolute value of a travel vector (motion vector) as a parameter indicative of the characteristic of the imaging blur will be described.

[0195] In the following, the absolute value of the travel vector (motion vector) will be called travel speed, and the direction of the travel vector (motion vector) will be called a travel direction. The travel direction can be any direction on a two-dimensional plane. Naturally, in the case where any direction on a two-dimensional plane becomes the travel direction, the video signal processor 4B of FIG. 13 can similarly execute various processes which will be described later. However, in the following, for simplicity of explanation, it is assumed that the travel direction is the lateral direction.

[0196] In the case where the travel speed is used as a parameter indicative of the characteristic of the imaging blur, for example, for each of the frames constructing a moving image,

the imaging blur characteristic detector **12** sequentially sets each of the pixels constructing the frame to be processed as a target pixel, sequentially detects a travel vector in the target pixel, and sequentially supplies the travel vector as a value of the parameter indicative of the characteristic of the imaging blur in the target pixel to the imaging blur suppression processor **13**.

[0197] Therefore, for example, for each of the frames constructing a moving image, the imaging blur suppression processor **13** sequentially sets each of the pixels constructing the frame to be processed as a target pixel, and sequentially corrects the pixel value of the target pixel on the basis of the travel speed in the target pixel supplied from the imaging blur characteristic detector **12**.

[0198] Here, the reason why the travel speed can be employed as a parameter indicative of the characteristic of the imaging blur will be described.

[0199] The characteristic of the imaging blur can be generally expressed in the form that it depends on the travel speed of a subject.

[0200] In addition, in the case where a subject itself moves in a real space and a camera is fixed, the travel speed of the subject naturally includes the travel speed of a subject (image) in a frame when the subject is captured by the camera. Further, the travel speed of the subject here includes travel speed relative to the subject (image) in the frame when the subject is captured by the camera in the case where the subject is fixed in the real space and the camera is moved by a hand shake or the like or in the case where both the subject and the camera move in the real space.

[0201] Therefore, the characteristic of the imaging blur can be expressed in the form that it depends on the travel speed in each of pixels constructing an image of a subject.

[0202] The travel speed in a pixel refers to a spatial distance between a pixel in a frame to be processed and a corresponding pixel (correspondence point) in the preceding frame. For example, in the case where a spatial distance between a pixel in a frame to be processed and a corresponding pixel (correspondence point) in the immediately preceding frame (temporally one before) is v pixels (v denotes an arbitrary integer value equal to or larger than 0), the travel speed in the pixel is v [pixels/frame].

[0203] In this case, if predetermined one of each pixel constructing an image of a subject is set as a target pixel, the characteristic of the imaging blur in the target pixel can be expressed in the form that it depends on the travel speed v [pixels/frame] in the target pixel.

[0204] More concretely, for example, in the case where the travel speed of the target pixel is 2, 3, and 4 [pixels/frame], the frequency characteristics of the imaging blur in the target pixel can be expressed by curves H2, H3, and H4, respectively, in FIG. 16.

[0205] That is, FIG. 16 shows the frequency characteristics of the imaging blur in the target pixel in the case where the travel speed in the target pixel is 2, 3, and 4 [pixels/frame]. In FIG. 16, the horizontal axis shows frequency, and the vertical axis shows gain. However, each value on the horizontal axis show relative values in the case where the Nyquist frequency is 1.

[0206] The reason why the travel speed can be employed as a parameter indicative of the characteristic of the imaging blur has been described above.

[0207] By the way, as understood from the frequency characteristics H2 to H4 in FIG. 16, when the characteristic of an

imaging blur in a target pixel is expressed in a space region, it can be expressed by a moving average filter (low-pass filter).

[0208] Specifically, when a transfer function indicative of the moving average filter (low-pass filter) (hereinbelow, called transfer function of the imaging blur) is written as H , an ideal image signal in the case where no imaging blur supposedly occurs (hereinbelow, called a signal without an imaging blur) is expressed as F in a frequency area, and an actual image signal output from a camera, that is, an image signal in which an imaging blur occurs (hereinbelow, called a signal with an imaging blur) is expressed as G in the frequency area, a signal G with the imaging blur is expressed as the following equation (3).

$$G = H \times F \quad (3)$$

[0209] An object of the invention is to remove (suppress) the imaging blur. To achieve the object, it is sufficient to forecasting calculation the signal F without the imaging blur from the signal G with the imaging blur which is known and the transfer function H of the imaging blur which is known. That is, it is sufficient to execute the following equation (4) of forecasting calculation.

$$F = \text{inv}(H) \times G \quad (4)$$

[0210] In the equation (4), $\text{inv}(H)$ indicates inverse function of the transfer function H of the imaging blur. Since the transfer function H of the imaging blur has the characteristic of a low-pass filter as described above, the inverse function $\text{inv}(H)$ of the transfer function H naturally has the characteristic of a high-pass filter.

[0211] As described above, the characteristic of the transfer function H of the imaging blur varies according to the travel speed. Concretely, for example, when the travel speed in the target pixel is 2, 3, and 4 [pixels/frame], the frequency characteristic of the transfer function H of the imaging blur in the target pixel becomes different characteristics as shown by curves H2, H3, and H4, respectively, in FIG. 16.

[0212] Thereby, the imaging blur suppression processor **13** can achieve the object of the present invention, that is, the object of removing (suppressing) the imaging blur by changing the characteristic of the transfer function H of the imaging blur in accordance with the travel speed, obtains the inverse function $\text{inv}(H)$ of the transfer function H whose characteristic was changed, and executes the computing process of the equation (4) using the inverse function $\text{inv}(H)$.

[0213] Alternately, since the computation of the equation (4) is computation of a frequency region, to achieve the object of the present invention, the imaging blur suppression processor **13** may execute a process in a space region equivalent to the computing process of the equation (4). Concretely, for example, the imaging blur suppression processor **13** may execute the following first to third processes.

[0214] In the first process, according to the travel speed in a target pixel supplied from the imaging blur characteristic detector **12**, the characteristic of the moving average filter (low-pass filter) expressing the imaging blur in the target pixel is converted. Concretely, for example, moving average filters are prepared for plural travel speeds in a one-to-one corresponding manner. A process of selecting one filter corresponding to the travel speed in the target pixel among a plurality of moving average filters is an example of the first process.

[0215] The second process is a process made of the following processes 2-1 to 2-3.

[0216] The process 2-1 is a process of displaying the moving average filter in frequency by performing Fourier transform on the moving average filter whose characteristic is converted by the first process. Concretely, for example, in the case where the transfer speed in the target pixel is 2, 3, and 4 [pixels/frame], the process of obtaining the curves H2, H3, and H4 in FIG. 16 is the process 2-1. Namely, from the viewpoint of the frequency region, the process of obtaining the transfer function H of the imaging blur in the target pixel is the process 2-1.

[0217] The process 2-2 is a process of calculating the inverse of the moving average filter which is frequency indicated by the process 2-1. That is, from the viewpoint of the frequency region, the process of generating the inverse function $\text{inv}(H)$ of the transfer function H of the imaging blur expressed by the above-mentioned equation (4) is the process 2-2.

[0218] The process 2-3 is a process of performing the inverse Fourier transform on the inverse of the moving average filter which is calculated by the process 2-2 and is frequency indicated. That is, a process of generating a high-pass filter (Wiener filter or the like) corresponding to the inverse function $\text{inv}(H)$ is the process 2-3. In other words, the process of generating an inverse filter of the moving average filter is the process 2-3. In the following, the high-pass filter generated by the process 2-3 will be called an inverse moving average filter.

[0219] The third process is a process of inputting, as an input image, an image signal g in the space region corresponding to the signal G in the equation (4) in the frequency range with the imaging blur, and applying the inverse moving average filter generated by the process 2-3 on the image signal g. By the third process, an image signal f in the space region corresponding to the signal F in the equation (4) in the frequency region without the imaging blur is reconstructed (forecasting-calculated). Concretely, for example, a process of correcting the pixel value of the target pixel by applying the inverse moving average filter on a predetermined block including the target pixel in the frame to be processed is the third process.

[0220] An embodiment of the functional configuration of the imaging blur suppression processor 13 capable of executing the first to third processes has been already invented by the inventors of the present invention and is disclosed in FIG. 17 submitted together with the application of Japanese Patent Application No. 2004-234051.

[0221] However, in the case where the imaging blur suppression processor 13 has the configuration of FIG. 17 presented together with the application of Japanese Patent Application No. 2004-234051, a first issue as described below newly occurs. That is, as also shown by the frequency characteristics H2 to H4 in FIG. 16, the moving average filter (its frequency characteristic) indicative of the imaging blur includes the frequency at which the gain becomes zero. Consequently, it is difficult for the imaging blur suppression processor 13 to generate a complete inverse filter of the moving average filter (complete inverse moving average filter). As a result, the first issue that noise increases newly occurs.

[0222] Further, the process of applying the high-pass filter (inverse moving average filter) on the image signal like the third process can be also said a process of making an edge sharp. As an image forming technique in the meaning of

“making an edge sharp”, in the past, techniques such as LTI and sharpness exist. Obviously, such a conventional technique can be applied to the imaging blur suppression processor 13.

[0223] However, in the case of applying such a conventional technique to the imaging blur suppression processor 13, the following second to fifth issues newly occur.

[0224] That is, the LTI is a technique of the related art disclosed in Japanese Unexamined Patent Application Publication No. 2000-324364 and the like. In the Japanese Unexamined Patent Application Publication No. 2000-324364, a technique of replacing the luminance (pixel value) of the target pixel with the luminance (pixel value) of a pixel neighboring the target pixel by a hard switch to correct the luminance of the target pixel, thereby sharpening an edge is the LTI. Therefore, due to the characteristic, the LTI has a second issue such that durability against noise is low, and a process image may be damaged by noise. There is also a third issue that all of edges are sharpened regardless of image data prior to the LTI.

[0225] In addition, since the techniques of the related art (LTI and sharpness) are used for image formation, the techniques have a fourth issue that the process is similarly performed also on a still picture in which no imaging blur occurs and a fifth issue that the process is uniformly performed irrespective of the amount of an imaging blur.

[0226] Accordingly, the inventors of the present invention have invented the imaging blur suppression processor 13 having, for example, the functional configuration shown in FIG. 17 of the present invention to solve the issues described above in “Problems to be solved by the Invention” along with the first to fifth issues. That is, FIG. 17 shows an example of the functional configuration of the imaging blur suppression processor 13 to which the present invention is applied.

[0227] In the example of FIG. 17, the imaging blur suppression processor 13 is configured to have a high frequency component removing unit 21, a filter unit 22, and an imaging blur compensating unit 23.

[0228] At least in the description of the imaging blur suppression processor 13, signals input to each functional block (including computing units such as an adder) constructing the imaging blur suppression processor 13 is hereinafter referred to as input signals collectively irrespective of an input unit such as a moving image, each of frames constructing a moving image, and a pixel value of each of pixels constructing each frame. Similarly, signals output from each functional block is hereinafter referred to as output signals collectively regardless of an output unit. In other words, in the case where an input unit and an output unit have to be discriminated from each other, description will be given using the unit (mainly, the pixel value). In the other case, description will be given simply using an input signal or an output signal.

[0229] As shown in FIG. 17, an output signal of the interpolation section 45 is supplied to the high frequency component removing unit 21 as an input signal to the imaging blur suppression processor 13. An output signal of the imaging blur characteristic detector 12 is supplied to the filter unit 22 and the imaging blur compensating unit 23. An output signal of the high frequency component removing unit 21 is supplied to the filter unit 22. An output signal of the filter unit 22 is supplied to the imaging blur compensating unit 23. An output signal of the imaging blur compensating unit 23 is output to the outside as an output signal indicative of the final process result of the imaging blur suppression processor 13.

[0230] In the following, the details of the high frequency component removing unit 21, the filter unit 22, and the imaging blur compensating unit 23 will be described in that order.

[0231] First, with reference to FIGS. 18 and 19, the details of the high frequency component removing unit 21 will be described.

[0232] FIG. 18 shows an example of a detailed functional configuration of the high frequency component removing unit 21. FIG. 19 shows the characteristic of after-mentioned high-frequency limiter 32 in the high frequency component removing unit 21 in FIG. 18.

[0233] In the example of FIG. 18, the high frequency component removing unit 21 is configured to have a high-pass filter 31, the high-frequency limiter 32, and a subtractor 33.

[0234] As shown in FIG. 18, an output signal of the interpolation section 45 is supplied as an input signal to the high frequency component removing unit 21 to the high-pass filter 31 and the subtractor 33.

[0235] The high-pass filter 31 has the function of an HPF (High-Pass Filter). Therefore, the high-pass filter 31 extracts a high frequency component from an input signal of the high frequency component removing unit 21 and supplies it to the high-frequency limiter 32.

[0236] The high-frequency limiter 32 has a function shown by a curve P1 in FIG. 19, assigns the high frequency component supplied from the high-pass filter 31 as an input parameter to the function, and supplies an output of the function (output of FIG. 19) to the subtractor 33. That is, as easily understood from the shape of the curve P1 in FIG. 19, the high-frequency limiter 32 limits the value of the high frequency component (input) supplied from the high-pass filter 31 in the case where the value is a predetermined value or larger, or a predetermined value or less. In other words, the high-frequency limiter 32 has a characteristic shown by the curve P1 in FIG. 19.

[0237] Referring again to FIG. 18, the subtractor 33 calculates the difference between the input signal of the high frequency component removing unit 21 and the high frequency component limited by the high-frequency limiter 32, and supplies a derived differential signal as an output signal of the high frequency component removing unit 21 to the filter unit 22.

[0238] In such a manner, high frequency components such as noise are removed from the input signal in the high-frequency component removing unit 21, and a signal obtained as a result is supplied as an output signal to the filter unit 22.

[0239] Next, referring to FIGS. 20 to 22, the details of the filter unit 22 will be described.

[0240] FIG. 20 shows an example of a detailed functional configuration of the filter unit 22. FIG. 21 shows an example of a detailed functional configuration of a gain controller 53 which will be described later, in the filter unit 22 in FIG. 20. FIG. 22 shows the characteristic of an adjustment amount determining unit 64 which will be described later, in the gain controller 53 in FIG. 21.

[0241] In the example of FIG. 20, the filter unit 22 includes a moving average filter 51 to an adder 54.

[0242] As shown in FIG. 20, an output signal of the high frequency component removing unit 21 is supplied as an input signal of the filter unit 22 to each of the moving average filter 51, a subtractor 52, and the adder 54. Further, an output signal of the imaging blur characteristic detector 12 is supplied to each of the moving average filter 51 and the gain controller 53.

[0243] The moving average filter 51 applies moving average filtering to the input signal of the filter unit 22. More specifically, the moving average filter 51 applies the moving average filter on each of pixel values of a predetermined block including the target pixel in a frame to be processed in an input signal of the filter unit 22, thereby correcting the pixel value of a target pixel. At this time, the moving average filter 51 converts the characteristic of the moving average filter in accordance with the travel speed in the target pixel in the output signal of the imaging blur characteristic detector 12. Concretely, for example, in the case where the travel speed in the target pixel is 2, 3, and 4 [pixels/frame], in view of the frequency region, the moving average filter 51 converts the characteristic of the moving average filter to those shown by the curves H2, H3, and H4, respectively, in FIG. 16. The pixel value of the target pixel corrected by the moving average filter 51 is supplied to the subtractor 52.

[0244] At this time, the moving average filter 51 can also change the number of taps (the target pixel and predetermined pixels neighboring the target pixel) used in the case of applying the moving average filter on the target pixel in accordance with the travel speed in the target pixel in the output signal of the imaging blur characteristic detector 12. Concretely, for example, the moving average filter 51 should vary the number of taps so as to be increased (that is, so as to increase width to be averaged) as the travel speed increases. The imaging blur compensating unit 23 uses the result of the moving average filter using taps of the number according to the travel speed, thereby enabling correction of higher precision, that is, correction capable of suppressing the imaging blur more to be performed.

[0245] The subtractor 52 obtains the difference between a pixel value before correction of the target pixel in the input signal of the filter unit 22 and the pixel value of the target pixel corrected by the moving average filter 51, and supplies the difference value to the gain controller 53. Hereinafter, the output signal of the subtractor 52 is called the difference between signals before and after the moving average filter.

[0246] The gain controller 53 adjusts the value of the difference between signals before and after the moving average filter, and supplies, as an output signal, the adjusted difference between signals before and after the moving average filter to the adder 54. The details of the gain controller 53 will be described later with reference to FIG. 21.

[0247] The adder 54 adds the input signal of the filter unit 22 and the output signal of the gain controller 53, and supplies the addition signal as an output signal to the imaging blur compensating unit 23. Specifically, when attention is paid to the target pixel, the adder 54 adds, as a correction amount, the adjusted value of the difference between the signals before and after the moving average filter of the target pixel to the pixel value of the target pixel prior to the correction, and supplies the addition value as the pixel value of the corrected target pixel to the imaging blur compensating unit 23 on the outside.

[0248] The process in the space region in the filter unit 22 as described above will be performed as follows in view of the frequency region.

[0249] That is, in the case where the difference between the signals before and after the moving average filter as the output signal of the subtractor 52 is considered in the frequency region, when attention is paid to a predetermined frequency, the gain of the output signal of the subtractor 52 becomes as follows. Specifically, at the noted frequency, the differential

gain between the gain of the input signal of the filter unit 22 and the gain of the input signal passed through the moving average filter becomes the gain of the output signal of the subtractor 52. The gain of the output signal of the subtractor 52 is hereinafter referred to as the differential gain between gains before and after the moving average filter.

[0250] Further, the differential gain between gains before and after the moving average filter is adjusted by the gain controller 53. The gain adjustment will be described later.

[0251] Therefore, in the case where the output signal of the filter unit 22 (adder 54) in the example of FIG. 20 is considered in the frequency region, when attention is paid to a predetermined frequency, the gain of the output signal is an addition gain obtained by adding the gain of the input signal and the differential gain between gains before and after the moving average filter after the gain adjustment. That is, at each of the frequencies, the gain of the output signal is higher than that of the input signal only by the amount of the differential gain of signals before and after the moving average filter after the gain adjustment.

[0252] In other words, the filter unit 22 as a whole executes a process basically equivalent to a process of applying a high-pass filter.

[0253] Referring to FIG. 21, the details of the gain adjuster 53 will be described.

[0254] In an example of FIG. 21, the gain controller 53 has delay units 61-1 to 61-n (hereinbelow, called DL units 61-1 to 61-n corresponding to FIG. 21), a MAX/MIN calculator 62, a subtractor 63, the adjustment amount determining unit 64, and a multiplier 65.

[0255] As shown in FIG. 21, the difference between signals before and after the moving average filter as an output signal of the subtractor 52 is supplied as an input signal to the gain controller 53 to the DL unit 61-1. The output signal of the imaging blur characteristic detector 12 is supplied to the MAX/MIN calculator 62.

[0256] With such a configuration, the gain adjuster 53 can suppress ringing which occurs in a place where the level of a signal is high.

[0257] The detailed functional configuration (connection mode of each functional block) of the gain controller 53 and its operation will be described below.

[0258] The DL units 61-1 to 61-n are connected in order. When an output signal of a preceding DL unit is supplied as an input signal to a DL unit, the DL unit delays the input signal by predetermined delay time, and supplies the resultant signal as an output signal to a subsequent DL unit. Each of output signals of the DL units 61-1 to 61-n is supplied also to the MAX/MIN calculator 62. Further, an output of the DL unit 61-(n/2) is also supplied to the multiplexer 65.

[0259] Values corresponding to n pixels arranged successively in the travel direction (in this case, the lateral direction) using the target pixel as a center in the difference between signals before and after the moving average filter as an input signal of the gain controller 53 (hereinafter referred to as the differential values of neighboring pixels) are sequentially input to the DL unit 61-1 in the arrangement order of the pixels from right to left. Therefore, after time n times as long as delay time elapses since then, one differential value between neighboring pixels in the n pixels arranged successively in the lateral direction using the target pixel as a center is output one by one from each of the DL units 61-1 to 61-n and supplied to the MAX/MIN calculator 62. Further, the differential value between neighboring pixels of the target

value is output from the DL unit 61-(n/2) and is supplied to the MAX/MIN calculator 62 as described above and is also supplied to the multiplier 65.

[0260] In addition, the number n of DL units 61-1 to 61-n is, though not particularly limited, the highest value [pixels/frame] of the travel speed in this case. It is also assumed that the travel speed in the target pixel supplied from the imaging blur characteristic detector 12 is v [pixels/frame]. However, v is an arbitrary integer value of 0 or larger.

[0261] The MAX/MIN calculator 62 determines, as a calculation range, a range including the target pixel as a center and including differential values of neighboring pixels in the v pixels of the amount corresponding to the travel speed. The MAX/MIN calculator 62 obtains a maximum value MAX and a minimum value MIN from v differential values of neighboring pixels included in the calculation range from the n differential values of neighboring supplied from the DL units 61-1 to 61-n, and supplies them to the subtractor 63.

[0262] In addition, the range including the target pixel as a center and including differential values of neighboring pixel in the v pixels of the amount corresponding to the travel speed is set as the calculation range for the following reason. That is, ringing exerts an influence only by the number of taps of the high-pass filter, in other words, only by the amount corresponding to the travel speed.

[0263] The subtractor 63 obtains the difference between a maximum value MAX and a minimum value MIN supplied from the MAX/MIN calculator 62 and supplies the differential value (=MAX-MIN) to the adjustment amount determining unit 64.

[0264] It is known that the larger the differential value (=MAX-MIN) becomes, the larger ringing around the target pixel becomes. That is, the difference (=MAX-MIN) is a value as the index of magnitude of the ringing around the target pixel.

[0265] Then, the adjustment amount determining unit 64 determines the adjustment amount on the differential values of the pixels neighboring the target pixel on the basis of the differential value (=MAX-MIN) supplied from the subtractor 63, and supplies it to the multiplier 65.

[0266] Specifically, for example, the adjustment amount determining unit 64 holds a function indicated by the curve P2 in FIG. 22, assigns the differential value (=MAX-MIN) supplied from the subtractor 63 as an input parameter to the function, and supplies an output of the function (the output of FIG. 22) as the adjustment amount on the differential values of pixels neighboring the target pixel to the multiplier 65. That is, as easily understood from the shape of the curve P2 in FIG. 22, after the differential value (=MAX-MIN) supplied from the subtractor 63 exceeds a predetermined value, the adjustment amount (output) decreases in order to suppress occurrence of ringing. In other words, the adjustment amount determining unit 64 has the characteristic shown by the curve P2 in FIG. 22.

[0267] Referring again to FIG. 21, the multiplier 65 multiplies the differential value of pixels neighboring the target pixel supplied from the DL unit 61-(n/2) with the adjustment amount supplied from the adjustment amount determining unit 64 (in the example of FIG. 22, the value in the range of 0 to 1), and supplies the resultant value as the differential value between the adjusted signals neighboring the target pixel. That is, the difference values between the neighboring pixels adjusted are sequentially supplied as output signals of the gain controller 53 to the adder 54.

[0268] As described above, when the differential value ($=\text{MAX}-\text{MIN}$) as an output signal of the subtractor 63 exceeds a predetermined value, as the differential value ($=\text{MAX}-\text{MIN}$) increases, the adjustment amount (output) also gradually decreases toward 1 to 0. Therefore, in the case where the differential value ($=\text{MAX}-\text{MIN}$) as an output signal of the subtractor 63 is equal to or larger than a predetermined value, an adjustment value which is less than 1 is multiplied to the differential amount of pixels neighboring the target pixel. Thus, the difference of the pixels neighboring the target pixel is adjusted so as to be decreased. As a result, ringing around the target pixel is suppressed.

[0269] In view of the frequency region, it can be said, as a result, that the process in the space region in the gain controller 53 as described above is a process of adjusting the differential gain between gains before and after the moving average filter in order to suppress ringing.

[0270] Next, referring to FIGS. 23 to 31, the details of the imaging blur compensating unit 23 will be described.

[0271] FIG. 23 shows an example of a detailed functional configuration of the imaging blur compensating unit 23.

[0272] In the example of FIG. 23, the imaging blur compensating unit 23 is configured to have an ALTI unit 81, a subtractor 82, a gain controller 83, and an adder 84.

[0273] As shown in FIG. 23, an output signal of the filter unit 22 is input, as an input signal of the imaging blur compensating unit 23, to the ALTI unit 81, the subtractor 82, and the adder 84. An output signal of the imaging blur characteristic detector 12 is supplied to the ALTI unit 81 and the gain controller 83.

[0274] Paying attention to the pixel value of a target pixel in an input signal of the imaging blur compensating unit 23, each of the ALTI 81 to the adder 84 will be hereinafter described.

[0275] As described above, the pixel value of a target pixel at the stage when it is supplied to the imaging blur compensating unit 23 is often different from that at the stage when it is input to the imaging blur suppression processor 13 in FIG. 17 since it is already corrected by the high frequency component removing unit 21 and the filter unit 22. Further, as will be described later, the pixel value of the target pixel is properly corrected also in the imaging blur compensating unit 23. Then, to avoid confusion, during explanation of the imaging blur compensating unit 23, each pixel value at the stage when it is input to each functional block will be called an input pixel value, and a pixel value at the stage when it is output from each functional block will be called an output pixel value. Further, there is a case that, with respect to the same pixel, a plurality of different pixel values are input from a plurality of preceding functional blocks to a certain function block. In such a case, the pixel value closer to an original (mainly, a pixel value before correction) will be called an input pixel value, and the other pixel values will be called output pixel values of a subsequent functional block. For example, although the details will be described later, different values are supplied as pixel values of the target pixel from the ALTI unit 81 and the external filter unit 22 to the subtractor 82. Therefore, the pixel value supplied from the external filter unit 22 will be called an input pixel value, and the pixel value supplied from the ALTI unit 81 will be called an output pixel value of the ALTI unit 81.

[0276] The ALTI unit 81 determines a correction amount according to the travel speed in the target pixel supplied from the imaging blur characteristic detector 12, adds the correc-

tion amount to the input pixel value of the target pixel, and supplies the added value as an output pixel value of the target pixel to the subtractor 82. The more details of the ALTI unit 81 will be described later with reference to FIG. 24.

[0277] The subtractor 82 calculates the difference between the output pixel value of the target pixel of the ALTI unit 81 and the input pixel value of the target pixel, and supplies the differential value (hereinbelow, called a target pixel differential value) to the gain controller 83.

[0278] The gain controller 83 adjusts the target pixel differential value supplied from the subtractor 82 in accordance with the travel speed in the target pixel supplied from the imaging blur characteristic detector 12, and supplies the adjusted target pixel differential value as a final correction amount for the target pixel to the adder 84.

[0279] The adder 84 adds the final correction amount from the gain controller 83 to the input pixel value of the target pixel, and outputs the added value as an output pixel value of the target pixel to the outside. That is, the output pixel value of the target pixel of the adder 84 is output as the pixel addition value of the target pixel finally corrected by the imaging blur suppression compensating unit 23 to the outside.

[0280] The details of each of the ALTI unit 81 and the gain controller 83 in the imaging blur compensating unit 23 will be described in order below.

[0281] First, referring to FIGS. 24 to 29, the details of the ALTI unit 81 will be described.

[0282] FIG. 24 shows an example of a detailed functional configuration of the ALTI unit 81.

[0283] In an example of FIG. 24, the ALTI unit 81 is configured to have delay units 91-1 to 91-n (hereinbelow, called DL units 91-1 to 91-n as shown in FIG. 24), average value calculators 92 to 94, a correction amount determining unit 95, and an adder 96.

[0284] The detailed functional configuration (connection mode of each functional block) of the ALTI unit 81 and its operation will be described below.

[0285] The DL units 91-1 to 91-n are connected in order. Each of the DL units 91-1 to 91-n delays each of the pixel values output from a preceding DL unit only by predetermined delay time, and outputs the resultant signal to a subsequent DL unit. Each of the pixel values output from the DL units 91-1 to 91-(n/2-1) is supplied to an average value calculator 93. The pixel values output from the DL units 91-(n/2-1), 91-(n/2), and 91-(n/2+1) are supplied to the average value calculator 92. The pixel values output from the DL units 91-(n/2+1) to 91-n are supplied to the average value calculator 94. The pixel value output from the DL unit 91-(n/2) is also supplied to the correction amount determining unit 95 and the adder 96.

[0286] Each pixel value of n pixels arranged successively in the travel direction (in this case, the lateral direction) using the target pixel as a center are sequentially input to the DL unit 91-1 in the arrangement order of the pixels from right to left. Therefore, after time n times as long as delay time nearly elapses since then, the pixel value of each of the n pixels arranged successively in the lateral direction using the target pixel as a center is output one by one from each of the DL units 91-1 to 91-n.

[0287] In addition, description will be given on assumption that each of pixel values at the stage when they are output from each of DL units 91-1 to 91-n is input pixel values to the ALTI unit 81.

[0288] Concretely, an input pixel value N of the target pixel is output from the DL unit $91-(n/2)$. The input pixel value of each of the $n/2-1$ pixels arranged successively on the left side of the target pixel is output from each of the DL units $91-1$ to $91-(n/2-1)$. On the other hand, the input pixel value of each of the $n/2-1$ pixels arranged successively on the right side of the target pixel is output from each of the DL units $91-(n/2+1)$ to $91-n$.

[0289] In addition, the number n of DL units $91-1$ to $91-n$ is, though not particularly limited, the highest value [pixels/frame] of the travel speed in this case. It is also assumed that the travel speed in the target pixel supplied from the imaging blur characteristic detector 12 is v [pixels/frame] in a manner similar to the above example.

[0290] Therefore, to the average value calculator 92 , the input pixel value N of the target pixel, the input pixel value of the pixel on the left side of the target pixel, and the input pixel value of the pixel on the right side of the target pixel are input. Then, the average value calculator 92 calculates an average value N_a of the input pixel value N of the target pixel, the input pixel value of the pixel on the left side of the target pixel, and the input pixel value of the pixel on the right side of the target pixel (hereinbelow, called an average pixel value N_a of the target pixel), and supplies the average value N_a to the correction amount determining unit 95 .

[0291] As the details will be described later, a correction amount ADD of the target pixel determined by the correction amount determining unit 95 is adjusted by a predetermined adjustment amount c . The adjustment value c is not a fixed value but a variable value determined by a predetermined process (hereinbelow, called an adjustment amount determining process). In the embodiment, in the adjustment amount determining process, the average pixel value N_a of the target pixel is used for the following reason. Although the input pixel value N of the target pixel can be used as it is in the adjustment amount determining process, in this case, if noise is included in the target pixel, an image to be processed may be broken. That is, the reason is to prevent breakage of an image to be processed.

[0292] To the average value calculator 93 , the input pixel values of $n/2-1$ pixels successively arranged on the left side of the target pixel are supplied. Then, the average value calculator 93 selects k pixels (where k is about $v/2$) which is about the half of the travel speed in order in the left direction of the pixel on the left side of the target pixel, and determines a range including the input pixel values of the selected k pixels as a calculation range. Then, the average value calculator 93 calculates an average value L_a of the k input pixel values included in the calculation range (hereinbelow, called the average pixel value L_a of the left pixels) in the supplied $n/2-1$ input pixel values, and supplies it to the correction amount determining unit 95 .

[0293] On the other hand, to the average value calculator 94 , the input pixel values of the $n/2-1$ pixels arranged successively on the right side of the target pixel are supplied. Then, the average value calculator 94 selects k pixels in order in the right direction of the pixel on the right side of the target pixel, and determines a range including the input pixel values of the selected k pixels as a calculation range. Then, the average value calculator 94 calculates an average value R_a of the k input pixel values included in the calculation range (hereinbelow, called the average pixel value R_a of the right pixels) in the supplied $n/2-1$ input pixel values, and supplies it to the correction amount determining unit 95 .

[0294] As the details will be described later, the average pixel value L_a of the left pixels and the average pixel value R_a of the right pixels are used for the adjustment amount determining process and a process for determining a candidate of the correction amount (hereinbelow, called candidate determining process).

[0295] That is, in the LTI of the related art disclosed in Japanese Unexamined Patent Application Publication No. 2000-324364, the differential value between the input pixel value of one pixel (hereinbelow, called left pixel) apart from the target pixel only by a predetermined distance in the left direction and the input pixel value of the target pixel is determined as a first candidate of the correction amount. Further, the differential value between the input pixel value of one pixel (hereinbelow, called right pixel) apart from the target pixel only by a predetermined distance in the right direction and the input pixel value of the target pixel is determined as a second candidate of the correction amount. Then, one of the first and second candidates is determined as a correction amount as it is without being adjusted. Consequently, the LTI of the related art has an issue such that if noise is included in the input pixel value of the left pixel or the right pixel, the correction amount (two candidates) may not be properly determined.

[0296] Therefore, to solve the issue, that is, to properly determine candidates of the correction amount, in the candidate determining process of the embodiment, the input pixel value of one pixel such as a left pixel or right pixel is not simply used, but the average pixel value L_a of the left pixels and the average pixel value R_a of the right pixels are used.

[0297] However, there is the case that the change direction of each input pixel value included in the calculation range is not constant, that is, increases and then decreases, or decreases and then increases. In other words, there is the case that the polarity of the gradient of a line connecting points indicative of input each pixel value included in the calculation range (points 131 to 134 and the like of FIG. 25 which will be described later) is inverted on a plane using the pixel positions in the horizontal direction as the horizontal axis and using the pixel values as the vertical axis (for example, the plane of FIG. 25 which will be described later). In such a case, a new issue occurs such that even if a simple average value of input pixel values included in the calculation range is employed as the average pixel value L_a of the left pixels or the average pixel value R_a of the right pixels, a correction amount (candidate) may not be properly determined.

[0298] Therefore, to solve the new issue, in the embodiment, each of the average value calculators 93 and 94 updates an input pixel value β indicated by a first point after polarity inversion in the input pixel values included in the calculation range to a pixel value γ by computing the right side of the following equation (5) using an input pixel value α indicated by a second point before polarity inversion. Each of the average value calculators 93 and 94 regards the input pixel value of the pixel indicated by the first point as the updated pixel value γ , and calculates the average pixel value L_a of left pixels or the average pixel value R_a of right pixels.

$$\gamma = \alpha - H \times f(H) \quad (5)$$

[0299] In the equation (5), as shown in FIG. 25, H denotes the differential value ($=\alpha-\beta$) between the pixel value α of the second point (point 133 in the diagram) before polarity inversion and the pixel value β of the first point (point 134 in the diagram) after polarity inversion.

[0300] That is, FIG. 25 shows an example of pixel values of 12 pixels arranged successively in the horizontal direction including the target pixel 131. In FIG. 25, the horizontal axis indicates “pixel position in the horizontal direction”, and the vertical axis indicates “pixel values”. In the example of FIG. 25, the calculation range of the average value calculator 94, that is, the calculation range of the average pixel value R_a of right pixels is a range D including the pixel values α , α , and β indicated by the three points 132 to 133 on the right side of point 131 indicative of the target pixel.

[0301] From the example of FIG. 25, it is understood that the polarity of the gradient from point 133 to point 134 is determined. To be specific, the point 134 is the first point after the polarity inversion, and the point 133 is the second point before the polarity determination. Therefore, in the example of FIG. 25, the average value calculator 94 varies the input pixel value indicated by the point 134 from the pixel value β to the pixel value γ by assigning and calculating the difference value $H(=\alpha-\beta)$ between the input pixel value α indicated by the point 133 and the input pixel value β indicated by the input pixel value α and the point 134 to the right side of the equation (5). Then, the average value calculator 94 calculates the average pixel value R_a of right pixels using the updated pixel value γ as the input pixel value of the pixel indicated by the point 134 in the calculation range D and using the original pixel value α as it is as each of input pixel values of the other points 132 and 133. That is, $R_a=(\alpha+\alpha+\gamma)/3$ is computed.

[0302] In the embodiment, in computation of the right side of the equation (5), a function having the characteristic like line 141 of FIG. 26 is used as the function $f(H)$.

[0303] As shown in FIG. 26, in the case where the differential value H between the pixel value α before polarity inversion and the pixel value β after polarity inversion is equal to a value H_2 or larger, an output of the function $f(H)$ is zero. In addition, when the differential value H is large, it means that the gradient after polarity inversion is sharp. Therefore, in the case where the gradient after polarity inversion is sharp to certain extent or more, that is, in the case where the differential value H is the value H_2 or larger, the pixel value γ updated by the equation (5) becomes the pixel value α . That is, as shown in FIG. 25, in the case where the gradient after polarity inversion is sharp to certain extent or more, the average pixel value R_a of right pixels in the calculation range D is calculated using the pixel value α in place of the pixel value β as the input pixel value of the pixel indicated by the point 134 after polarity inversion. That is, $R_a=(\alpha+\alpha+\alpha)/3=\alpha$ is computed and the average pixel value R_a of right pixels is determined as the pixel value α .

[0304] On the other hand, as shown in FIG. 26, in the case where the differential value H between the pixel value α before polarity inversion and the pixel value β after polarity inversion is equal to the value H_1 or less, an output of the function $f(H)$ becomes 1. In addition, when the differential value H is small, it means that the gradient after polarity inversion is gentle. Therefore, in the case where the gradient after polarity inversion is gentle to certain extent or more, that is, in the case where the differential value H is the value H_1 or less, the pixel value γ updated by the equation (5) remains the pixel value β . That is, in the case where the gradient after polarity inversion is gentle to certain extent or more, although not shown, the average pixel value R_a of right pixels in the calculation range D is calculated using the pixel value β as it is as the input pixel value indicated by the point 134 after

polarity inversion. That is, $R_a=(\alpha+\alpha+\beta)/3$ is computed and the average pixel value R_a of right pixels is determined as the pixel value $\{(\alpha+\alpha+\beta)/3\}$.

[0305] In addition, when the gradient after polarity inversion is gentle to certain extent or more, the original pixel value β is used as it is without updating the pixel value indicated by the point 134 after polarity inversion for the following reason. That is, in the case where the gradient after polarity inversion is gentle to certain extent or more, the possibility that polarity inversion occurs due to noise is high for the following reason. By obtaining an average without updating the input pixel values, the appropriate average pixel value R_a of right pixels without noise can be obtained.

[0306] The case of calculating the average pixel value R_a of right pixels has been described above using the concrete example of FIG. 25. Also in the other cases, for example, in the case of calculating the average pixel value L_a of left pixels, the input pixel value of the pixel indicated by the point after polarity inversion is updated from the pixel value β to the pixel value γ similarly by the equation (5).

[0307] Referring again to FIG. 24, the number of taps (the number of pixel values) used in the case of calculating the average value in each of the above-described average value calculators 92 to 94 is fixed in the above example. However, it may be varied, for example, according to the travel speed in the target pixel in the output signal of the imaging blur characteristic detector 12. Concretely, for example, it may be varied so as to increase the number of taps (that is, to increase the width of average) as the travel speed increases. The results of the average value calculators 92 to 94 using taps of the number according to the travel speed as described above are used by the correction amount determining unit 95 which will be described later, thereby enabling a correction amount for performing higher-precision correction, that is, correction capable of further suppressing the imaging blur to be determined.

[0308] The correction amount determining unit 95 determines the correction amount ADD by using the input pixel value N of the target pixel from the DL unit 91-($n/2$), the average pixel value N_a of the target pixel from the average value calculator 92, the average pixel value L_a of left pixels from the average value calculator 93, and the average pixel value R_a of right pixels from the average value calculator 94, and supplies it to the adder 96.

[0309] Here, the adder 96 adds the correction amount ADD from the correction amount determining unit 95 to the input pixel value N of the target pixel from the DL unit 91-($n/2$), and supplies the addition result as an output pixel value of the target pixel, that is, a corrected pixel value of the target pixel to the adder 82 on the outside of the ALTI unit 82.

[0310] Before explaining an example of a detailed functional configuration of the correction amount determining unit 95, the process of the ALTI unit 81 will be described with reference to the flowchart of FIG. 27.

[0311] In step S21, the ALTI unit 81 sets a target pixel.

[0312] In step S22, the DL units 91-1 to 91- n of the ALTI unit 81 obtain n pieces of neighboring input pixel values around the input pixel value N of the target pixel as a center.

[0313] In step S23, the average value calculator 92 of the ALTI unit 81 calculates the average pixel value N_a of the target pixel and supplies it to the correction amount determining unit 95 as described above.

[0314] In step S24, the average value calculator 93 in the ALTI unit 82 calculates the average pixel value La of left pixels and supplies it to the correction amount determining unit 95 as described above.

[0315] In step S25, the average value calculator 94 in the ALTI unit 82 calculates the average pixel value Ra of right pixels and supplies it to the correction amount determining unit 95 as described above.

[0316] In addition, as obvious from FIG. 24, each of the average value calculators 92 to 94 executes the process independently of others. Therefore, the order of processes in the steps S23 to S25 is not limited to the example of FIG. 27 but may be arbitrary order. That is, in reality, the processes in the steps S23 to S25 are executed in parallel and independently of others.

[0317] In step S26, the correction amount determining unit 95 in the ALTI unit 82 determines two candidates ADDL and ADDR of the correction amount by using the input pixel value N of the target pixel from the DL unit 91-(n/2), the average pixel value La of left pixels from the average value calculator 93, and the average pixel value Ra of right pixels from the average value calculator 94. That is, the process of step S26 is the above-described candidate determining process. The candidates ADDL and ADDR of the correction amount are respective output signals from subtractors 101 and 102 which will be described later. In addition, the details of the candidate determining process in step S26 and the candidates ADDL and ADDR of the correction amount will be described later.

[0318] In step S27, the correction amount determining unit 95 determines the adjustment amount c by using the average pixel value Na of the target pixel from the average value calculator 92, the average pixel value La of the left pixels from the average value calculator 93, and the average pixel value Ra of the right pixels from the average value calculator 94. That is, the process in step S27 is the above-described adjustment amount determining process. The adjustment amount c denotes an output signal of the adjustment amount value calculator 109 which will be described later. The details of the adjustment amount determining process in step S27 and the adjustment amount c will be described later.

[0319] In addition, as the details will be described later, in reality, the processes in the steps S26 and S27 are executed in parallel and independently of each other. That is, the order of the processes in the steps S26 and S27 is not limited to the example of FIG. 27 but may be arbitrary order.

[0320] In step S28, the correction amount determining unit 95 adjusts each of the values of the candidates ADDL and ADDR by using the adjustment amount c. In the following, the process in the step S28 will be called the adjusting process. The details of the adjusting process will be described later.

[0321] In step S29, the correction amount determining unit 95 determines (selects), as the correction amount ADD, predetermined one of the candidates ADDL and ADDR whose values are adjusted by the adjustment amount c in accordance with a predetermined discrimination condition, and supplies it to the adder 96. In the following, the process in the step S29 will be called a correction amount selecting process. The details (including the discrimination condition) of the correction amount selecting process will be described later.

[0322] In step S30, the adder 96 in the ALTI unit 81 adds the correction amount ADD to the input pixel value N of the

target pixel and outputs the resultant addition value as the output pixel value of the target pixel to the adder 82 on the outside.

[0323] In step S31, the ALTI unit 81 determines whether the process has been finished on all of the pixels or not.

[0324] In the case where it is determined in the step S31 that the process has not been finished yet on all of the pixels, the process is returned to the step S21, and the following processes are repeated. Specifically, another pixel is set as the target pixel, the correction amount ADD is added to the input pixel value N of the target pixel, and the resultant addition value is output as the output pixel value of the target pixel to the adder 82 on the outside. Naturally, each of the pixel value N and the correction amount ADD often varies among the pixels.

[0325] After all of the pixels are set as the target pixels and the loop process in the steps S21 to S31 is repeatedly executed for each of the set target pixels as above, it is determined in step S31 that the process on all of the pixels is finished and the process of the ALTI unit 81 is finished.

[0326] In addition, since the ALTI unit 81 is a component of the imaging blur suppression processor 13 in FIG. 13, the process of the ALTI unit 81 in FIG. 27 is executed as a part of the process of the step S4 in FIG. 15.

[0327] As described above, the correction amount determining unit 95 executes the processes in the steps S26 to S29. In the following, referring again to FIG. 24, while describing an example of the detailed functional configuration of the correction amount determining unit 95, the details of the processes in the steps S26 to S29 will be also described.

[0328] As shown in FIG. 24, the correction amount determining unit 95 is provided with the adders 101 and 102 in order to execute the above-described candidate determining process in the step S26 in FIG. 27. In other words, a candidate determining unit 121 constructed by the subtractors 101 and 102 executes the candidate determining process in the step S26.

[0329] The subtractor 101 calculates the differential value (=La-N) between the average pixel value La of left pixels from the average value calculator 93 and the input pixel value N of the target pixel from the DL unit 91-(n/2) and supplies the differential value as the candidate ADDL of the correction amount to a multiplier 110.

[0330] In addition, as will be described later, in the case where the candidate ADDL of the correction amount is determined as the correction amount ADD without being adjusted (multiplied with the adjustment amount c=1), the adder 96 adds the correction amount ADD(=La-N) to the input pixel value N of the target pixel and the resultant addition value (=La) is output to the outside. That is, in the case where the candidate ADDL (=La-N) of the correction amount is used as it is as the correction amount ADD, the pixel value of the target pixel is corrected (replaced) from the original pixel value N to the average pixel value La of left pixels.

[0331] The subtractor 102 calculates the differential value (=Ra-N) between the average pixel value Ra of right pixels from the average value calculator 94 and the input pixel value N of the target pixel from the DL unit 91-(n/2) and supplies the differential value as the candidate ADDR of the correction amount to a multiplier 111.

[0332] In addition, as will be described later, in the case where the candidate ADDR of the correction amount is determined as the correction amount ADD without being adjusted (multiplied with the adjustment amount c=1), the adder 96 adds the correction amount ADD(=Ra-N) to the input pixel

value N of the target pixel and the resultant addition value ($=Ra$) is output to the outside. That is, in the case where the candidate ADDR ($=Ra-N$) of the correction amount is used as it is as the correction amount ADD, the pixel value of the target pixel is corrected (replaced) from the original pixel value N to the average pixel value Ra of right pixels.

[0333] In addition, as shown in FIG. 24, the correction amount determining unit 95 is provided with components from a subtractor 103 to an adjustment amount value calculator 109 in order to execute the adjustment amount determining process in the step S27 in FIG. 27. In other words, an adjustment amount determining unit 122 constructed by the subtractor 103 to the adjustment amount determining unit 109 executes the adjustment amount determining process in the step S27.

[0334] The subtractor 103 calculates the differential value ($=Na-La$) between the average pixel value Na of the target pixel from the average value calculator 92 and the average pixel value La of left pixels from the average value calculator 93 and supplies the differential value to an adder 105.

[0335] A subtractor 104 calculates the differential value ($=Na-Ra$) between the average pixel value Na of the target pixel from the average value calculator 92 and the average pixel value Ra of right pixels from the average value calculator 94 and supplies the differential value to the adder 105.

[0336] The adder 105 calculates the sum of output signals of the subtractors 103 and 104 and outputs the calculation result to an ABS unit 106.

[0337] The ABS unit 106 calculates an absolute value b of the output signal of the adder 105 and supplies the absolute value b to a divider 108.

[0338] In other words, in a plane using the pixel values as the vertical axis and using pixel positions in the horizontal direction as the horizontal axis, a quadratic differential value at a second point on a line sequentially connecting a first point indicative of the average pixel value La of left pixels, the second point indicative of the average pixel value Na of the target pixel, and a third point indicative of the average pixel value Ra of right pixels is computed by the subtractors 103 and 104 and the adder 105. The absolute value b of the quadratic differential value is computed by the ABS unit 106, and supplied to the divider 108. Therefore, the absolute value b output from the ABS unit 106 will be called the quadratic differential absolute value b below.

[0339] In the plane, in the case where a straight line connecting the first point indicative of the average pixel value La of left pixels and the third point indicative of the average pixel value Ra of right pixels is used as a boundary line, the quadratic differential absolute value b is a value indicative of the distance of the second point indicative of the average pixel value Na of the target pixel from the boundary line in the vertical axis direction.

[0340] Consequently, the correction amount determining unit 95 adjusts each of the values of the candidates ADDL and ADDR of the correction amount in accordance with the magnitude of the quadratic difference absolute value b , and determines one of the adjusted candidates ADDL and ADDR as the correction amount ADD. That is, the adder 96 outputs, as the output pixel value of the target pixel, the addition value between the input pixel value N of the target pixel and the correction amount ADD adjusted according to the magnitude of the quadratic differential absolute value b . As a result, an edge portion in the output signal (the frame to be processed) of the adder 96 can be made gentle.

[0341] However, even if the quadratic differential absolute values b are the same, when the absolute value h of the difference between the average pixel value La of left pixels and the average pixel value Ra of right pixels, that is, the distance h between the first and third points in the vertical axis direction in the above-described plane (hereinbelow, called height h) varies, the meaning of the magnitude of the quadratic differential absolute value b varies. Specifically, even if the quadratic differential absolute value b is the same, in the case where the magnitude is much smaller than the height h , in other words, in the case where a division value ($=b/h$) obtained by dividing the quadratic differential value b by the height h is small, it can be determined that the possibility of occurrence of noise around the target pixel is high. On the other hand, even if the quadratic differential absolute values b are the same, in the case where the magnitude is not so small as compared with the height h , in other words, in the case where the division value ($=b/h$) has certain magnitude or more, it can be determined that the possibility of occurrence of noise around the target pixel is low.

[0342] Therefore, if the values of the candidates ADDL and ADDR are adjusted simply according to the magnitude of the quadratic differential absolute value b , the correction amount ADD of the input pixel value N of the target pixel becomes the same value irrespective of whether noise occurs or not. A new issue occurs such that the input pixel value N of the target pixel may not be properly corrected.

[0343] Then, to solve the new issue, the adjustment amount determining unit 122 of the correction amount determining unit 95 of the embodiment is provided with the components from the subtractor 103 to the ABS unit 106 and, in addition, a difference absolute value calculator 107, the divider (b/h calculator) 108, and the adjustment amount value calculator 109.

[0344] The differential absolute value calculator 107 calculates the difference value between the average pixel value La of left pixels from the average value calculator 93 and the average pixel value Ra of right pixels from the average value calculator 94, further calculates the absolute value h ($h=|La-Na|$) of the difference value, that is, the height h , and supplies the height h to the divider 108.

[0345] The divider 108 divides the quadratic differential absolute value b from the ABS unit 106 by the height h from the difference absolute value calculator 107 and provides the division value ($=b/h$) to the adjustment amount value calculator 109. That is, the division value ($=b/h$) can be said as a value obtained by normalizing the quadratic differential absolute value b by the height h . Therefore, the division value ($=b/h$) will be called a normalized quadratic differential value ($=b/h$).

[0346] The adjustment amount value calculator 109 calculates the adjustment amount c for the candidates ADDL and ADDR on the basis of the normalized quadratic differential value ($=b/h$) from the divider 108, and supplies it to the multipliers 110 and 111.

[0347] Specifically, for example, the adjustment amount value calculator 109 holds a function of the characteristic expressed by a curve 151 in FIG. 28, assigns the normalized quadratic differential value ($=b/h$) from the divider 108 as an input parameter to the function, and supplies an output of the function (output of FIG. 28) as the adjustment amount c to the multipliers 110 and 111.

[0348] That is, as easily understood from the shape of the curve 151 of FIG. 28, when the normalized quadratic differ-

ential value ($=b/h$) is smaller than a predetermined value **b1**, the possibility of noise is high, and the adjustment amount c (output) becomes zero. In this case, as will be described later, the candidates ADDL and ADDR are adjusted by being multiplied with zero as the adjustment amount c , so that each of the adjusted candidates ADDL and ADDR becomes zero. Therefore, the correction amount ADD also becomes zero, and the input pixel value N of the target pixel is not corrected.

[0349] Further, when the normalized quadratic differential value ($=b/h$) exceeds the predetermined value **b1** and increases, the adjustment amount c (output) also increases gradually. In this case, as will be described later, each of the candidates ADDL and ADDR is adjusted by being multiplied with the adjustment amount c which is less than 1, so that each of the adjusted candidates ADDL and ADDR becomes smaller than the original value. Therefore, the correction amount ADD becomes one of the candidates ADDL and ADDR which became smaller than the original values. The corrected pixel value of the target pixel becomes larger than the average pixel value L_a of left pixels or smaller than the average pixel value R_a of right pixels.

[0350] Further, when the normalized quadratic differential value ($=b/h$) becomes a predetermined value **b2** or larger after that, the adjustment amount c (output) becomes 1. In this case, as will be described later, each of the candidates ADDL and ADDR is adjusted by being multiplied with 1 as the adjustment amount c , so that each of the adjusted candidates ADDL and ADDR remains the original value (that is, not adjusted). Therefore, the correction amount ADD becomes one of the candidates ADDL and ADDR remaining as the original values. As described above, the corrected pixel value of the target pixel becomes the average pixel value L_a of left pixels or the average pixel value R_a of right pixels.

[0351] As described above, in the present embodiment, the adjustment amount c is determined using the function of the characteristic expressed by the line **151** of FIG. **28**, to which the normalized quadratic differential value ($=b/h$) is input as a parameter. Consequently, by adjusting the correction amount ADD with the adjustment amount c (to be accurate, by adjusting the candidates ADDL and ADDR of the correction amount), the edge portion in the output signal (the frame to be processed) of the adder **96** can be made gentle. Specifically, in the LTI of the related art, the pixel value of the target pixel is corrected by switching (simple replacement of the pixel value) of a hard switch. There is consequently an issue that the edge portion in the output signal may not be made gentle. However, by employing the ALTI unit **81** of the embodiment, the issue can be solved.

[0352] Referring again to FIG. **24**, the detailed description of the correction amount determining unit **95** will be continued. Specifically, the correction amount determining unit **95** is provided with the multipliers **110** and **111** in order to execute the adjusting process in the step **S28** in FIG. **27**. In other words, an adjusting unit **123** constructed by the multipliers **101** and **111** executes the adjusting process in the step **S28**.

[0353] The multiplier **110** multiplies the candidate ADDL from the subtractor **101** with the correction amount c from the adjustment amount value calculator **109**, and supplies the resultant multiplied value as the adjusted candidate ADDL to a discriminator **113**.

[0354] The multiplier **111** multiplies the candidate ADDR from the subtractor **102** with the correction amount c from the

adjustment amount value calculator **109**, and supplies the resultant multiplied value as the adjusted candidate ADDR to the discriminator **113**.

[0355] In addition, the correction amount determining unit **95** is also provided with a fixed value generator **112** and the discriminator **113** in order to execute the correction amount selecting process in the step **S29** in FIG. **27**. In other words, a correction amount selecting unit **124** constructed by the fixed value generator **112** and the discriminator **113** executes the correction amount selecting process in the step **S29**.

[0356] In the embodiment, the fixed value generator **112** usually generates "0" as shown in FIG. **24** and supplies it to the discriminator **113**.

[0357] To the discriminator **113**, output signals of the subtractors **103** and **104**, the adder **105**, the multipliers **110** and **111**, and the fixed value generator **112** are supplied. The discriminator **113** selects (determines), as the correction amount ADD, predetermined one of "0" from the fixed value generator **112**, the corrected candidate ADDL from the multiplier **110**, and the corrected candidate ADDR from the multiplier **111** on the basis of a predetermined selecting condition using output signals of the subtractors **103** and **104** and the adder **105**, and supplies it to the adder **96**.

[0358] Concretely, for example, in the above-mentioned plane using the pixel values as the vertical axis and using pixel positions in the horizontal direction as the horizontal axis, a straight line connecting a first point indicative of the average pixel value L_a of left pixels and a third point indicative of the average pixel value R_a of right pixels is set as a boundary line. The selecting condition of the embodiment is specified that the corrected candidate ADDR is selected as the correction amount ADD in the case where the change direction of the boundary line is an upward direction and a second point indicative of the average pixel value N_a of the target pixel is disposed on the upper side of the boundary line. On the contrary, the selecting condition of the embodiment is specified that the corrected candidate ADDL is selected as the correction amount ADD in the case where the change direction of the boundary line is an upward direction and the second point is disposed on the lower side of the boundary line.

[0359] In this case, the discriminator **113** can recognize the change direction of the boundary line and the positional relation between the boundary line and the second point on the basis of the output signals of the subtractors **103** and **104** and the adder **105**.

[0360] Then, for example, in the case where the discriminator **113** recognizes that the change direction of the boundary line is an upward direction and the second point is disposed on the upper side of the boundary line on the basis of the output signals of the subtractors **103** and **104** and the adder **105**, the discriminator **113** selects (determines) the corrected candidate ADDR from the multiplier **111** as the correction amount ADD and supplies it to the adder **96**.

[0361] On the other hand, for example, in the case where the discriminator **113** recognizes that the change direction of the boundary line is an upward direction and the second point is disposed on the lower side of the boundary line on the basis of the output signals of the subtractors **103** and **104** and the adder **105**, the discriminator **113** selects (determines) the corrected candidate ADDL from the multiplier **110** as the correction amount ADD and supplies it to the adder **96**.

[0362] It is also assumed that, in the case where the target pixel is positioned in a location other than an edge portion for

example, selection of 0 as the correction amount ADD is specified as a selecting condition of the embodiment. In this case, for example, when the discriminator 113 recognizes that all of the output signals of the subtractors 103 and 104 and the adder 105 are almost zero, that is, when the average pixel value La of left pixels, the input pixel value N of the target pixel, and the average pixel value Rc of right pixels are almost the same or the like, the discriminator 113 recognizes that the target pixel is positioned in a location other than the edge portion, selects (determines) "0" from the fixed value generator 112 as the correction amount ADD, and supplies it to the adder 96.

[0363] As an embodiment of the ALTI unit 81, the ALTI unit 81 having the functional configuration of FIG. 24 has been described above. As long as processes equivalent to the above-described series of processes can be executed, any functional configuration may be used as the functional configuration of the ALTI unit 81. Concretely, for example, the ALTI unit 81 may have a functional configuration shown in FIG. 29. That is, FIG. 29 shows an example of a detailed functional configuration different from FIG. 24 of the ALTI unit 81.

[0364] In the example of FIG. 29, the ALTI unit 81 is configured to have a masking signal generator 161, an LTI processing unit 162, and an averaging unit 163.

[0365] The masking signal generator 161 receives the output signal of the filter unit 22 as own input signal and sequentially sets, as the target pixel, each of the pixels constructing the frame to be processed in the input signal. The masking signal generator 161 searches pixels on the left and right sides of the target pixel by the number of pixels corresponding to the half of the travel speed from the target pixel, and performs masking process on each signal indicative of the pixel values of the number of pixels corresponding to the travel speed. The travel speed of the target pixel is supplied from the imaging blur characteristic detector 12 as described above. The masked signals are supplied from the masking signal generator 161 to the LTI processing unit 162.

[0366] The LTI processing unit 162 performs the LTI process on each of the masked signals and supplies, as an output signal, the resultant signal to the averaging unit 163.

[0367] The averaging unit 163 averages signals of the number corresponding to the number of search times in the masking signal generator 161, in the output signals of the LTI processing unit 162 and supplies the resultant signal as an output signal of the ALTI unit 81 to the adder 82 on the outside.

[0368] Referring to FIGS. 24 to 29, the details of the ALTI unit 81 in the imaging blur compensating unit 23 in FIG. 23 have been described above.

[0369] Next, referring to FIGS. 30 and 31, the details of the gain controller 83 in the imaging blur compensating unit 23 in FIG. 23 will be described.

[0370] FIG. 30 shows an example of the detailed functional configuration of the gain controller 83. FIG. 31 shows the characteristic of an adjustment amount determining unit 171 which will be described later in the gain controller 83 in FIG. 30.

[0371] In the example of FIG. 30, the gain controller 83 is configured to have the adjustment amount determining unit 171 and a multiplier 172.

[0372] The adjustment amount determining unit 171 holds a function expressed by a curve 181 in FIG. 31, assigns travel speed in the target pixel supplied from the imaging blur

characteristic detector 12 as an input parameter to the function, and supplies an output of the function (output of FIG. 31) as an adjustment amount to the multiplier 172. In other words, the adjustment amount determining unit 171 has the characteristic expressed by the curve 181 of FIG. 31.

[0373] To the multiplier 172, an adjustment amount from the adjustment amount determining unit 171 and, in addition, an output signal of the adder 82 are also supplied. As obvious from the functional configuration of FIG. 23, an output signal of the adder 82 is a candidate of a final correction amount added to an input pixel value of a target pixel for the imaging blur compensating unit 23, in the adder 84. Specifically, the multiplier 172 multiplies the candidate of the final correction amount with the adjustment amount from the adjustment amount determining unit 171 and supplies the resultant multiplied value, as the final adjustment amount, to the adder 84.

[0374] That is, as easily understood from the shape of the line 181 in FIG. 31 and the functional configuration of FIG. 23 of the imaging blur compensating unit 23, the gain controller 83 controls so that the process result (hereinafter called as ALTI) of the ALTI unit 81 does not exert much influence on the final correction amount of the pixel value of the target pixel when the travel speed is low. When the travel speed is low, deterioration in the gain due to imaging blur is small, and it is sufficient to increase the attenuated gain by the filter unit 22 in FIGS. 17 and 20. That is, it is sufficient to output the output signal of the filter unit 22 as a final output signal of the imaging blur compensating unit 23 without performing much correction on the output signal.

[0375] Referring to FIGS. 17 to 31, an example of the imaging blur suppression processor 13 in the video signal processor 4B in FIG. 13 has been described above.

[0376] However, the functional configuration of the imaging blur suppression processor 13 is not limited to the example of FIG. 17, but may be variously modified. Concretely, for example, FIGS. 32 and 33 show two examples of the functional configuration of the imaging blur suppression processor 13 to which the present invention is applied, and the two examples are different from the example of FIG. 17.

[0377] In the example of FIG. 32, in a manner similar to the example of FIG. 17, the imaging blur suppression processor 13 is configured to have the high frequency component removing unit 21, the filter unit 22, and the imaging blur compensating unit 23.

[0378] Also in the example of FIG. 32, in a manner similar to the example of FIG. 17, an output signal of the interpolation section 45 is supplied as an input signal to the imaging blur suppression processor 13 to the high frequency component removing unit 21. An output signal of the imaging blur characteristic detector 12 is supplied to the filter unit 22 and the imaging blur compensating unit 23.

[0379] However, in the example of FIG. 32, an output signal of the high frequency component removing unit 21 is supplied to the imaging blur compensating unit 23. An output signal of the imaging blur compensating unit 23 is supplied to the filter unit 22. An output signal of the filter unit 22 is output as an output signal indicative of the final process result of the imaging blur suppression processor 13 to the outside.

[0380] In other words, in the example of FIG. 32, the disposing positions of the filter unit 22 and the imaging blur compensating unit 23 are opposite to those in the example of FIG. 17. That is, the order of disposing positions of the filter

unit 22 and the imaging blur compensating unit 23 (the process order) is not particularly limited. Any of the units may be disposed first.

[0381] Further, in the example of FIG. 33, like in the examples of FIGS. 17 and 32, the imaging blur suppression processor 13 is provided with the high frequency component removing unit 21, the filter unit 22, and the imaging blur compensating unit 23 and further, in addition to the functional blocks, is also provided with an adder 24.

[0382] Also in the example of FIG. 33, like in the examples of FIGS. 17 and 32, an output signal of the interpolation section 45 is supplied as an input signal for the imaging blur suppression processor 13 to the high frequency component removing unit 21. Further, an output signal of the imaging blur characteristic detector 12 is supplied to each of the filter unit 22 and the imaging blur compensating unit 23.

[0383] However, in the example of FIG. 33, an output signal of the high frequency component removing unit 21 is supplied to each of the filter unit 22 and the imaging blur compensating unit 23. Output signals of the filter unit 22 and the imaging blur compensating unit 23 are supplied to the adder 24. The adder 24 adds the output signal of the filter unit 22 and the output signal of the imaging blur compensating unit 23, and outputs the resultant addition signal as an output signal indicative of the final process result of the imaging blur suppression processor 13 to the outside.

[0384] In other words, the filter unit 22 and the imaging blur compensating unit 23 are arranged in series in the examples of FIGS. 17 and 32 but are arranged in parallel in the example of FIG. 33. That is, the filter unit 22 and the imaging blur compensating unit 23 may be arranged in series or in parallel. However, if both of the filter unit 22 and the imaging blur compensating unit 23 use a line memory, by arranging the filter unit 22 and the imaging blur compensating unit 23 in parallel as shown in the example of FIG. 33, the line memory can be shared. As a result, an effect such that the circuit scale (by the amount of the line memory) can be reduced is produced.

[0385] As described above, at the time of reducing a blur of a moving body at the time of image capturing (imaging blur) by image process, in the conventional technique, the process is performed uniformly irrespective of the stationary state and the degree of the blur amount. In contrast, in the present invention, for example, by using the imaging blur suppression processor 13, a travel vector (travel speed) is calculated, and an enhancement amount is changed according to the state of a moving image. Thus, without making ringing occur, the blur can be reduced. Further, in the LTI of the related art, the signal was switched by the hard switch, so that a processed image is often broken. However, the imaging blur suppression processor 13 has the ALTI unit 81 as a component. Consequently, a signal can be switched by software and, as a result, breakage of the processed image can be suppressed.

[0386] In addition, in the above-described example, for simplicity of explanation, the direction of the travel vector (travel direction) is the horizontal direction. However, even when the travel direction is another direction, the imaging blur suppression processor 13 can basically perform similar processes as the series of processes described above. Specifically, regardless of the travel direction, the imaging blur suppression processor 13 can correct the pixel value of the target pixel so as to suppress the imaging blur. Concretely, for example, it is sufficient for the ALTI unit 81 in the functional configuration of FIG. 24 to enter the pixel values of n pixels

arranged successively in the travel direction (for example, the vertical direction) using the target pixel as a center in the arrangement order to the DL unit 91-1. In the other functional blocks as well, operations are similarly performed.

[0387] Incidentally, in the above-described example, at the time of correcting the pixel values, the imaging blur suppression processor 13 uses the travel speed (the absolute value of the travel vector) as a parameter. However, other than the travel speed, as long as the parameter shows the characteristic of an imaging blur, an arbitrary parameter can be used.

[0388] Concretely, for example, the imaging blur suppression processor 13 can use, as a parameter showing the characteristic of an imaging blur, shutter speed of a camera at the time of capturing a moving image to be processed. The reason is that, for example, as shown in FIG. 34, when the shutter speed varies, the degree of an imaging blur also varies only by the amount of time T_s in the diagram.

[0389] Specifically, in FIG. 34, the upper diagram shows the case where the shutter speed is $1/30$ second which is the same as the frame speed. The lower diagram shows the case where the shutter speed is $(1/30 - T_s)$ second faster than the frame speed. In both of the diagrams of FIG. 34, the horizontal axis expresses the time base, and the vertical axis expresses the ratio of shutter open time. For example, the ratio of the shutter open time is expressed as $(T_s/V_s) \times 100[\%]$ where the shutter speed is V_a [seconds] (V_a is an arbitrary value of 0 or larger), the ratio of first time when the shutter is open is set as 0%, the ratio of second time after lapse of V [seconds] from the first time and the shutter is closed is set as 100%, and time from the first time to present time is expressed as T_a [seconds] (T_a is an arbitrary positive value from 0 or more to V or less). In this case, in the vertical axis of the diagrams in FIG. 23, the value which is in contact with the time base is 100 [%], and the maximum value (the highest value on each of straight lines) is 0 [%]. That is, the ratio of the shutter open time increases toward the bottom in the vertical axis of the diagrams in FIG. 34.

[0390] It is now assumed that one detecting element in a camera corresponds to a pixel in a frame, for example. In this case, as shown in the upper diagram of FIG. 34, when the shutter speed is $1/30$ second, an integrated value of light incident in $1/30$ second in which the shutter is open is output as a pixel value of the corresponding pixel from one detecting element in the camera. On the other hand, when the shutter speed is $(1/30 - T_s)$ second, an integrated value of light incident in $(1/30 - T_s)$ second in which the shutter is open is output as a pixel value of the corresponding pixel from one detecting element in the camera.

[0391] That is, the shutter speed corresponds to light accumulation time (exposure time) in a detecting element. Therefore, for example, when a moving object crossing a predetermined detecting element exists in a real space, light different from light corresponding to the object, for example, light of the background incident on the detecting element at the shutter speed of $1/30$ second is larger than that at the shutter speed of $(1/30 - T_s)$ second only by the amount of time T_s [second]. The ratio that the light accumulation value of the background or the like different from the object mixed in the pixel value output from one detecting element at the shutter speed of $1/30$ second is higher than that at the shutter speed of $(1/30 - T_s)$ second. As a result, the degree of an imaging blur increases.

[0392] The above is summarized as follows. The lower the shutter speed becomes, the higher the degree of image blur becomes. That is, it can be therefore said that the shutter speed

expresses a characteristic of an imaging blur. Therefore, the shutter speed can be used as a parameter expressing a characteristic of an imaging blur as well as the travel speed.

[0393] In addition, in the case where the shutter speed is used as a parameter showing a characteristic of an imaging blur, for example, the imaging blur characteristic detector 12 in FIG. 13 can detect the shutter speed of each frame by analyzing header information added to a moving image (data) supplied from the interpolation section 45 and the like, and supply the shutter speed as a parameter expressing a characteristic of the imaging blur to the imaging blur suppression processor 13. The imaging blur suppression processor 13 can properly correct each pixel value by executing, for example, the series of processes using the shutter speed in place of the travel speed. The functional configuration of the imaging blur suppression processor 13 in the case of using the shutter speed can be basically the same as that in the case of using the travel speed. That is, the imaging blur suppression processor 13 described with reference to FIGS. 17 to 31 can properly correct each pixel value by executing the series of processes using the shutter speed as a parameter value.

[0394] The video signal processor 4B having the configuration shown in FIG. 13 has been described above as an example of the video signal processor of the embodiment. The video signal processor of the embodiment is not limited to the example of FIG. 13 but may have other various configurations.

[0395] Specifically, for example, each of FIGS. 35 to 38 is a block diagram of a part of a video signal processor according to a modified example of the embodiment.

[0396] For example, a video signal processor of FIG. 35 is configured to have, like the video signal processor 4B of FIG. 13, the interpolation section 45, the imaging blur characteristic detector 12, and the imaging blur suppression processor 13.

[0397] However, in the video signal processor of FIG. 35, an object of the correction process of the imaging blur suppression processor 13 is a moving image which is input to the video signal processor, that is, a moving image before it is subject to the high frame rate converting process of the interpolation section 45. Consequently, the imaging blur characteristic detector 12 detects the value of a parameter showing a characteristic of the imaging blur in the moving image prior to the high frame rate converting process of the interpolation section 45 and supplies the detection result to the imaging blur suppression processor 13.

[0398] Therefore, as the image process of the video signal processor of FIG. 35, the processes in the steps S1, S3, S4, S2, and S5 in the image processes in FIG. 15 are executed in order.

[0399] In addition, for example, a video signal processor of FIG. 36 is configured to have, like the video signal processor 4B of FIG. 13 and the video signal processor of FIG. 35, the interpolation section 45, the imaging blur characteristic detector 12, and the imaging blur suppression processor 13.

[0400] In the video signal processor of FIG. 36, an object of the correction process of the imaging blur suppression processor 13 is a moving image obtained by performing the high frame rate converting process of the interpolation section 45 on the input moving image like in the video signal processor 4B of FIG. 13. Consequently, the imaging blur suppression processor 13 performs a correcting process on the moving image subjected to the high frame rate converting process.

[0401] However, the imaging blur characteristic detector 12 in the video signal processor of FIG. 36 detects a parameter showing a characteristic of the imaging blur in the input moving image, that is, in the moving image prior to the high frame rate converting process of the interpolation section 45 and supplies the detection result to the imaging blur suppression processor 13. That is, the imaging blur suppression processor 13 of the video signal processor of FIG. 36 corrects each pixel value using the value of the parameter detected in the moving image prior to the high frame rate converting process.

[0402] Therefore, as the image process of the video signal processor of FIG. 36, the processes executed in a flow similar to that of the imaging process of FIG. 15, that is, the processes in the steps S1, S2, S3, S4, and S5 are executed in order. However, the process in the step S3 is a process of "detecting the value of a parameter showing a characteristic of the imaging blur from a moving image prior to the high frame rate converting process, that is, from each of frames constructing a moving image entered by the process in the step S1".

[0403] In contrast to the video signal processors of FIGS. 35 and 36, each of video signal processors of FIGS. 37 and 38 is configured to have the interpolation section 45 and the imaging blur suppression processor 13 and does not include the imaging blur characteristic detector 12 as a component.

[0404] Specifically, as shown in FIGS. 37 and 38, the imaging blur characteristic detector 12 is provided together with a superimposing unit 221 in another video signal processor 211 (hereinafter, called an image signal generating apparatus 211 as described in the drawing). A moving image entered to the image signal generating apparatus 211 is supplied to the imaging blur characteristic detector 12 and the superimposing unit 221. The imaging blur characteristic detector 12 detects the value of a parameter expressing a characteristic of an imaging blur from the moving image and supplies it to the superimposing unit 221. The superimposing unit 221 superimposes the value of the parameter indicative of the characteristic of the imaging blur on the moving image and outputs a resultant signal.

[0405] Therefore, to the video signal processor of FIG. 37 and the video signal processor of FIG. 38, the moving image (signal) on which the value of the parameter expressing the characteristic of the imaging blur is superimposed is supplied from the image signal generating apparatus 211.

[0406] Then, for example, in the video signal processor of FIG. 37, the imaging blur suppression processor 13 separates the value of the parameter expressing the characteristic of the imaging blur and the moving image from each other, and corrects each of the pixel values on the basis of the separated value of the parameter expressing the characteristic of the imaging blur with respect to each of the frames constructing the separated moving image.

[0407] Next, the interpolation section 45 performs the high frame rate converting process on the moving image corrected by the imaging blur suppression processor 13 and outputs the resultant moving image, that is, the moving image converted to the high frame rate and corrected.

[0408] Therefore, as the image process of the video signal processor of FIG. 37, the processes in the steps S1, S4, S2, and S5 in the image processes in FIG. 15 are executed in order.

[0409] In contrast, for example, in the video signal processor of FIG. 38, the interpolation section 45 separates the value of the parameter expressing the characteristic of the imaging blur and the moving image from each other, performs the high

frame rate converting process on the separated moving image, and supplies the resultant moving image, that is, the moving image converted to high frame rate to the imaging blur suppression processor 13. At this time, the value of the parameter showing the characteristic of the imaging blur separated by the interpolation section 45 is also supplied to the imaging blur suppression processor 13.

[0410] Next, the imaging blur suppression processor 13 corrects each of the pixel values on the basis of the value of the parameter expressing the characteristic of the imaging blur with respect to each of the frames constructing the moving image converting to high frame rate, and outputs the resultant moving image, that is, the moving image corrected and converted to high frame rate.

[0411] Incidentally, in the above description on the imaging blur suppression processor 13, for simplicity of explanation, the travel direction (the direction of the travel vector) is the horizontal direction. Consequently, as a pixel used in the case of performing the above-described various processes such as the filtering and correction on the target pixel, pixels neighboring the target pixel in the horizontal direction are used. In addition, a process using pixels neighboring the target pixel in a predetermined direction will be called a process in the predetermined direction. That is, the above-described example relates to the process in the horizontal direction.

[0412] However, as described above, any direction in a two-dimensional plane can be the travel direction. Naturally, the imaging blur suppression processor 13 can execute the various processes in the same manner in any direction in a two-dimensional plane such as the vertical direction as the travel direction. However, to perform the process in the case where the travel direction is the vertical direction (or the process in the case where the travel direction is an oblique direction, which is a combination process of the process in the vertical direction and the process in the horizontal direction), the imaging blur suppression processor 13 has to employ, for example, the configuration of FIG. 39 in place of the configuration of FIG. 17, the configuration of FIG. 40 in place of the configuration of FIG. 32, and the configuration of FIG. 41 in place of the configuration of FIG. 33.

[0413] That is, FIGS. 39 to 41 show three examples of the functional configuration of the imaging blur suppression processor 13 to which the present invention is applied, which are different from the above-described examples.

[0414] In FIGS. 39, 40, and 41, the same reference numerals as those in FIGS. 17, 32, and 33 are designated to corresponding parts (blocks). Their description will be the same so that it will not be repeated.

[0415] In the imaging blur suppression processor 13 of FIG. 39, to enable a process in the vertical direction in the configuration of the example of FIG. 17, a line memory 261-1 is further provided at the ante stage of the filter unit 22, and a line memory 261-2 is provided at the ante stage of the imaging blur compensating unit 23.

[0416] Similarly, in the imaging blur suppression processor 13 of FIG. 40, to enable a process in the vertical direction in the configuration of the example of FIG. 32, the line memory 261-1 is further provided at the ante stage of the imaging blur compensating unit 23, and the line memory 261-2 is provided at the ante stage of the filter unit 22.

[0417] On the other hand, in the imaging blur suppression processor 13 in the example of FIG. 41, to enable a process in the vertical direction in the configuration of the example of

FIG. 33, only one common line memory 261 is further provided at the ante stage of the imaging blur compensating unit 23 and the filter unit 22.

[0418] As described above, by employing the imaging blur suppression processor 13 in the example of FIG. 41, as compared with the case employing the configuration example of FIG. 39 or 40, the number of line memories can be reduced without deteriorating the effect of the image blur suppression. That is, by employing the configuration of the example of FIG. 41 as the configuration of the imaging blur suppression processor 13, as compared with the case employing the configuration of the example of FIG. 39 or 40, the circuit scale of the imaging blur suppression processor 13 can be reduced and, moreover, the circuit scale of the video signal processor 4B of FIG. 13 can be reduced.

[0419] In addition, in the embodiment, for example, like in a video signal processor 4C shown in FIG. 42, an interpolation position parameter Relpos output from the decoder 47 may be supplied not only to the interpolator 453 but also to the imaging blur suppression processor 13. In such a configuration, the imaging blur suppression processor 13 can change the process amount in the imaging blur suppression process in accordance with the distance of the interpolation position closer to a video image of an original frame in each of interpolation frames, which is set by the interpolation section 45. Therefore, the degree of reducing the imaging blur can be changed according to nonuniformity of arrangement of interpolation frames (strength of a judder). By finely adjusting the degree of suppression of a hold blur in a display image and the degree of suppression of an imaging blur, the picture quality at the time of watching a movie or the like can be improved.

[0420] In the high frame rate converting process executed in the various embodiments, the combination of the first frame rate (frame frequency) of an input video signal and the second frame rate (frame frequency) of an output video signal is not particularly limited but may be an arbitrary combination. Concretely, for example, 60 (or 30) [Hz] is employed as the first frame rate of an input video signal, and 120 [Hz] can be employed as the second frame rate of an output video signal. For example, 60 (or 30) [Hz] is employed as the first frame rate of an input video signal and 240 [Hz] can be employed as the second frame rate of an output video signal. For example, 50 [Hz] corresponding to the PAL (Phase Alternation by Line) system is employed as the first frame rate of an input video signal, and 100 [Hz] or 200 [Hz] can be employed as the second frame rate of an output video signal. For example, 48 [Hz] corresponding to the telecine is employed as the first frame rate of an input video signal, and a predetermined frequency equal to or higher than 48 [Hz] can be employed as the second frame rate of an output video signal.

[0421] In addition, by performing the high frame rate converting process in the various embodiments on the input video signal resulted from an existing television system or the like, existing contents can be displayed with high grade.

Third Embodiment

[0422] A third embodiment of the present invention will now be described.

[0423] FIG. 43 shows an example of the configuration of a video signal processor (video signal processor 4D) according to the embodiment. In addition, the same reference numerals are designated to the same components as those in the foregoing embodiments and their description will not be repeated.

[0424] The video signal processor 4D is obtained by further providing the video signal processor 4B described in the second embodiment with an overdrive processor 10 and performs video signal processes in the interpolation section 45, the imaging blur suppression processor 13, and the overdrive processor 10 in consideration of the reliability in detection of a motion vector mv in the motion vector detector 44. In addition, in the case of detecting a motion vector also in the imaging blur characteristic detector 12, reliability in detection of the motion vector may be considered. In the embodiment, the case where the imaging blur suppression processor 13 and the overdrive processor 10 perform a video signal process using the motion vector mv detected by the motion vector detector 44 will be described below.

[0425] The overdrive processor 10 performs an overdrive process on a video signal supplied from the imaging blur suppression processor 13 by using the motion vector mv detected by the motion vector detector 44. Concretely, the overdrive processor 10 makes the process amount of the overdrive process increase as the motion vector mv increases, and makes the process amount of the overdrive process decrease as the motion vector mv decreases. By such an overdrive process, a motion blur and a hold blur in a display image can be suppressed.

[0426] Here, with reference to FIGS. 45 and 46, the reliability in detection of the motion vector mv will be described in detail. FIGS. 44 and 45 show an example of the relation between the presence/absence (MC ON/OFF signal) in detection of the motion vector mv and the reliability.

[0427] In FIG. 44, in the case where the value of MC ON/OFF signal is "0" (ON: the case where the motion vector can be detected) and does not change and in the case where the value changes from "1" (OFF: the case where no motion vector can be detected such as the case where the value is out of the search range (block matching range) of the motion vector) to "0", the value of reliability increases to "P (preceding value)+Y (change amount)". On the other hand, in the case where the value of the MC ON/OFF signal changes from "0" to "1" and in the case where the value is "1" and does not change, the value of reliability decreases to "P-Y".

[0428] With the configuration, for example, as shown in FIG. 45, during a period in which the value of the MC ON/OFF signal is "0", the reliability gradually increases from 0% to 100%. On the other hand, during a period in which the value of the MC ON/OFF signal is "1", the reliability gradually decreases from 100% to 0%.

[0429] By considering the reliability in detection of the motion vector mv, in the interpolation section 45, the imaging blur suppression processor 13, and the overdrive processor 10, it is set so that the process amount of the video signal process increases as the reliability increases, and on the other hand, the process amount of the video signal process decreases as the reliability decreases.

[0430] Concretely, the overdrive processor 10 sets so that as the reliability increases, the process amount of the overdrive process increases and, on the other hand, as the reliability decreases, the process amount of the overdrive process decreases. Meanwhile, it is also possible to change the process amount of the overdrive process in accordance with the distance of the interpolation position toward the video image of the closer original frame which is set in each of interpolation frames by the interpolation section 45 (to vary the degree of reduction in a motion blur and a hold blur in accordance with nonuniformity of the positions of interpolation frames

(strength of a judder)), and to perform the overdrive process in consideration of the reliability as well.

[0431] Further, the imaging blur suppression processor 13 sets so that the process amount of the imaging blur suppression process increases as the reliability increases and, on the other hand, the process amount of the imaging blur suppression process decreases as the reliability decreases. For example, like in the video signal processor 4C shown in FIG. 42 in the second embodiment, the process amount in the imaging blur suppression process may be changed in accordance with the distance of the interpolation position toward a video image of the closer original frame in interpolation frames, which is set by the interpolation section 45 (the degree of reducing the imaging blur is changed according to nonuniformity of positions of interpolation frames (strength of a judder)) and, in addition, the imaging blur suppressing process may be performed in consideration of such reliability.

[0432] Further, the interpolation section 45 changes the distance of setting the interpolation position toward a video image of the closer original frame in each of interpolation frames in consideration of reliability in detection of the motion vector mv. Thereby, nonuniformity of positions of interpolation frames (strength of a judder) can be changed in consideration of reliability in detection of the motion vector mv.

[0433] Meanwhile, in the case of converting the frame rate of a video signal by adding M interpolation frames (where M is an integer of 1 or larger) obtained by interpolating video images of original frames between the original frames neighboring along the time base using motion compensation in place of the interpolation section 45, for example, a frame rate converting process in consideration of reliability may be performed as shown in FIG. 46 (in the case of a 3:2 pulldown signal) and FIG. 47 (in the case of a 24 Hz film source signal).

[0434] Concretely, it may be set so that as the reliability increases, the gain multiplied with motion vectors MV1 to MV3 at the time of frame rate conversion increases, and, on the other hand, as the reliability decreases, the gain multiplied with the motion vectors MV1 to MV3 at the time of frame rate conversion decreases.

[0435] In such a manner, in the embodiment, the video signal process in the interpolation section 45, the imaging blur suppression processor 13, and the overdrive processor 10 is performed in consideration of the reliability in detection of the motion vector mv by the motion vector detector 44. It is set so that as the reliability increases, the process amount of the video signal process increases and, on the other hand, as the reliability decreases, the process amount of the video signal process decreases. Consequently, in the case of performing the video signal process using the motion vector, even when the motion vector lies out of the motion vector search range (block matching range), the video signal process according to the detection precision of a motion vector can be performed. Therefore, at the time of performing a predetermined video signal process, deterioration in the picture quality due to the motion vector detection precision can be suppressed.

Fourth Embodiment

[0436] A fourth embodiment of the present invention will now be described.

[0437] FIG. 48 shows an example of the configuration of an image display apparatus (a liquid crystal display 7) according to the embodiment. In addition, the same reference numerals

are designated to the same components as those in the foregoing embodiments and their description will not be repeated.

[0438] The liquid crystal display 7 displays a video image on the basis of a video signal subjected to the video signal process in the video signal processor 4 (or any one of the video signal processing apparatuses 4A to 4D) described in the first to third embodiments, and is a hold-type display apparatus. Concretely, the liquid crystal display 7 has the video signal processor 4 (4A to 4D), a liquid crystal display panel 70, a backlight driving unit 71, a backlight 72, a timing controller 73, a gate driver 74, and a data driver 75.

[0439] The backlight 72 is a light source of emitting light to the liquid crystal display panel 70 and includes, for example, a CCFL (Cold Cathode Fluorescent Lamp) and an LED (Light Emitting Diode).

[0440] The liquid crystal display panel 70 modulates irradiation light from the backlight 72 on the basis of a video signal. The liquid crystal display panel 70 includes a transmission-type liquid crystal layer (not shown), a pair of substrates (a TFT substrate and an opposite electrode substrate which are not shown) sandwiching the liquid crystal layer, and polarizing plates (not shown) laminated on each of the TFT substrate and the opposite electrode substrate on the side opposite to the liquid crystal layer.

[0441] The data driver 75 supplies a drive voltage based on the video signal to each of the pixel electrodes in a liquid crystal display panel 2. The gate driver 74 line-sequentially drives the pixel electrodes in the liquid crystal display panel 2 along not-shown horizontal scan lines. The timing controller 73 controls the data driver 75 and the gate driver 74 on the basis of the video signal supplied from the video signal processor 4 (4A to 4D). The backlight driving unit 71 controls the turn-on and turn-off operation of the backlight 72 (performs turn-on driving on the backlight 72) on the basis of the video signal supplied to the video signal processor 4 (4A to 4D).

[0442] The liquid crystal display 7 of the embodiment is constructed to perform a black inserting process of inserting a black display area into a display screen of the liquid crystal display panel 2 in accordance with at least one of the video signal substance in an original frame and luminance of a viewing environment for user. Concretely, for example, the black inserting process is performed for inserting a black display area into the display screen in the liquid crystal display panel 2 when the video signal in the original frame is a cinema signal (film signal). More concretely, the backlight driving unit 71 switches between turn-on and turn-off of the backlight 72 so that the process of inserting the black display on the display screen in the liquid crystal display panel 2 is performed. In addition, the backlight driving unit 71 determines, for example, whether the video signal in an original frame is a cinema signal or not by using contents information of the original frame included in an EPG (Electronic Program Guide) or on the basis of the frame rate of the original frame.

[0443] The black inserting method is performed as follows. For example, the black inserting process is performed on the frame unit basis as shown in FIGS. 49(A) and (B). The black inserting process is performed by black insertion line unit composed of a predetermined number of horizontal scan lines in the original frame as shown in FIGS. 50(A) and (B). For example, as shown in FIGS. 51(A) and (B), the black inserting process is performed by a combination of the black insertion line unit basis and the frame unit basis. In FIGS. 49 to 51 (and FIGS. 52 to 55 described later), (A) shows the substance of the video image (original frames A to C and interpolation

frames A' to C') in the liquid crystal display panel 2 (LCD), and (B) shows the light-on state of the backlight 72. The horizontal axis in the diagram shows time.

[0444] In the case of the black inserting process on the frame unit basis shown in FIG. 49, an entire frame is lighted on or off, so that the hold improvement effect increases. In the case of the black inserting process on the black insertion line unit basis shown in FIG. 50, display luminance can be adjusted by setting a black insertion ratio which will be described later, and the frame rate increases falsely. Consequently, as compared with the case of the frame unit basis, flicker is less-visible. In the case of the combination of the frame unit and the black insertion line unit shown in FIG. 51, moving image response becomes the highest.

[0445] In addition, in the case including the black inserting process on the black insertion line unit basis as shown in FIGS. 50 and 51, the black inserting process may be performed by a plurality of black insertion lines away from each other. In such a configuration, adjustment of the black insertion ratio and display luminance which will be described below is facilitated.

[0446] Further, for example, as shown in FIGS. 52 to 55, when performing the black inserting process, the backlight driving unit 71 may perform switching drive so that an areal ratio of a black display area in an entire display screen (=black insertion ratio) can be varied by changing the thickness of a black insertion line (the number of horizontal scan lines constructing a black insertion line). In such a configuration, the effect of reducing a hold blur is produced and the display luminance can be adjusted.

[0447] Further, the backlight driving unit 71 may perform the switching drive so that the luminance of the black display region is varied when performing the black inserting process. In such a configuration, while reducing a hold blur, the display luminance can be adjusted. Moreover, both of the black insertion ratio and luminance of the black display area may be varied.

[0448] In addition, in the case of making at least one of the black insertion ratio and the luminance of the black display region variable, the black insertion ratio and the luminance of the black display region may be changed in multiple stages or changed continuously. In the case of making such changes, reduction in the hold blur and adjustment of the display luminance is facilitated.

[0449] In such a manner, in the embodiment, the black inserting process of inserting a black display area into a display screen in the liquid crystal panel 2 is performed in accordance with at least one of the substance of the video signal in an original frame and luminance of the viewing environment for user. Thus, a hold blur can be reduced according to the circumstances.

[0450] In addition, for example, as shown in FIG. 56, according to a luminance histogram distribution in an original frame, whether the black inserting process is performed or not may be determined and the black insertion ratio and the luminance of the black display area may be changed. In such a configuration, adjustments become possible. For example, it is determined that the black inserting process is performed in a case such that decrease in the display luminance is not conspicuous in a dark image. By increasing the black insertion ratio or decreasing the luminance of the black display area, priority is given to the effect of reducing a hold blur.

[0451] Further, according to the magnitude of a motion vector in an original frame detected by the motion vector

detector 44 or the like, the black insertion ratio and the luminance of the black display area may be changed. In such a configuration, for example, adjustment such as suppression of a judder can be performed by increasing the black insertion ratio or decreasing luminance of the black display area in the case such that motion of a video image is large.

[0452] Further, for example, like in the liquid crystal display 7A shown in FIG. 57, by providing a brightness detector 76 for detecting brightness of the user's viewing environment (constructed by, for example, an illuminance sensor) or the like, whether the black inserting process is performed or not may be determined as described above or the black insertion ratio and the illuminance of the black display area may be changed according to the detected brightness of the user's viewing environment. In such a configuration, there is a case such that decrease in the display luminance is not conspicuous depending on the brightness of the viewing environment (for example, in the case where the viewing environment is a dark state). In such a case, the adjustment of placing priority on the effect of reducing a hold blur can be performed by determining that the black inserting process is performed or increasing the black insertion ratio or decreasing the luminance of the black display area.

[0453] In addition, in the case of providing the brightness detector 76, according to the detected brightness of the user's viewing environment, for example, the process amount of the imaging blur suppressing process by the imaging blur suppression processor 13 and degree of setting the interpolation position nearer to a video image of a closer original frame in each of the interpolation frames by the interpolation section 45 may be changed. In the case of changing the process amount of the imaging blur suppressing process by the imaging blur suppression processor 13, there is a case that an imaging blur is not conspicuous depending on the brightness of the viewing environment (for example, in the case where the viewing environment is a dark state). In such a case, the adjustment of decreasing the process amount of the imaging blur suppressing process can be performed. In the case of changing the degree of setting the interpolation position nearer to a video image of a closer original frame by the interpolation section 45, when a judder is not conspicuous depending on the brightness of the viewing environment (for example, in the case where the viewing environment is a dark state), by setting the interpolation position nearer to the original frame, a judder is left. In such a manner, for example, adjustment of creating realism peculiar to a movie is realized.

[0454] In addition, the embodiment has been described by the case where the hold-type image display apparatus is a liquid crystal display and the black inserting process (blinking process) is performed by the switch driving of the backlight driving unit 71. For example, in the case where a display apparatus is a light-emitting display apparatus other than a liquid crystal display (such as an organic EL display apparatus), the black inserting process may be performed by providing a black inserting processor (not shown) for performing a black inserting process on a video signal of an original frame in the video signal processor, and performing the video signal process by the black inserting processor.

[0455] Meanwhile, in the embodiment, whether the black inserting process can be executed or not, a change in the black insertion ratio, a change in illuminance in the black display area, and the like can be set by an operation of the user by providing, for example, predetermined operation means (setting means).

[0456] Further, the video signal processor in the embodiment is not limited to the video signal processor 4 (or any one of the video signal processors 4A to 4D) described in the first to third embodiments. Another video signal processor may be employed as long as it performs a predetermined video signal process on a plurality of original frames along the time base.

[0457] Further, the series of processes (or a part of the processes) described in the first to fourth embodiments can be executed by hardware or software.

[0458] In this case, all of the video signal processors 4 and 4A to 4D, the backlight driving unit 71, and the timing controller 73 or a part of them (for example, the imaging blur suppression processor 13 or the like) described in the above-mentioned embodiments 1 to 4 can be constructed by, for example, a computer as shown in FIG. 58.

[0459] In FIG. 58, a CPU (Central Processing Unit) 301 executes various processes in accordance with a program recorded on a ROM (Read Only Memory) 302, or a program loaded from a storage 308 to a RAM (Random Access memory) 303. In the RAM 303, data or the like necessary for the CPU 301 to execute various processes is also properly stored.

[0460] The CPU 301, ROM 302, and RAM 303 are connected to each other via a bus 304. To the bus 304, an input/output interface 305 is also connected.

[0461] To the input/output interface 305, an input unit 306 including a keyboard, a mouse, and the like, an output unit 307 such as a display, a storage 308 constructed by a hard disk or the like, and a communication unit 309 including a modem, a terminal adapter, and the like are connected. The communication unit 309 performs communication process with other devices via networks including the Internet.

[0462] As necessary, a drive 310 is also connected to the input/output interface 305. A removable recording medium 311 such as a magnetic disk, an optical disk, a magneto-optical disk, or a semiconductor memory is properly mounted on the input/output interface 305. A computer program read from the removable recording medium 311 is installed in the storage 308 as necessary.

[0463] In the case of executing a series of processes by software, a program constructing the software is installed from a network or a recording medium to, for example, a computer assembled in dedicated hardware or a general personal computer or the like capable of executing various functions by installing various programs.

[0464] The recording medium including such a program is not limited to the removable recording medium (package medium) 211 such as a magnetic disk (including a floppy disk), an optical disk (including a CD-ROM (Compact Disk-Read Only memory) and a DVD (Digital Versatile Disk)), a magneto-optical disk (including an MD (Mini-Disk)), or a semiconductor memory. It may be the ROM 302 in which a program is recorded, a hard disk included in the storage 308, or the like which is provided to the user in a state where it is pre-assembled in the apparatus body.

[0465] Meanwhile, in the specification, the steps describing a program to be recorded on a recording medium include, obviously, not only processes performed in time series in the order, but also processes which are not always performed in time series but are executed in parallel or individually.

[0466] Further, as described above, in the specification, the system refers to an entire apparatus constructed by a plurality of processing apparatuses and processors.

[0467] Further, the configurations and the like described in the foregoing embodiments and modified examples are not limited to the above-described combinations but can be arbitrarily combined.

1. An image display apparatus characterized by comprising:

video signal processing means for performing a predetermined video signal process to improve picture quality, on a plurality of original frames along time base; and display means for displaying a video image on the basis of a video signal subjected to the video signal process, wherein the display means is hold-type display means, and a black inserting process for inserting a black display area into a display screen in the display means is performed according to at least one of substance of a video signal in the original frame and brightness of viewing environment for user.

2. The image display apparatus according to claim 1, characterized in that the display means has:

a light source; and

a liquid crystal display panel for modulating light from the light source on the basis of the video signal in the original frame.

3. The image display apparatus according to claim 2, characterized by further comprising light source driving means for performing switching drive between turn-on and turn-off of the light source so that the black inserting process is performed on the display screen in the liquid crystal display panel.

4. The image display apparatus according to claim 3, characterized in that the light source driving means performs the switching drive so that an areal ratio of the black display area to the entire display screen (=black insertion ratio) is variable when performing the black inserting process on the original frame.

5. The image display apparatus according to claim 4, characterized in that the light source driving means performs the switching drive so that the black insertion ratio varies in multiple steps.

6. The image display apparatus according to claim 4, characterized in that the light source driving means performs the switching drive so that the black insertion ratio continuously varies.

7. The image display apparatus according to any one of claims 4 to 6, characterized by further comprising setting means for allowing user to vary the black insertion ratio.

8. The image display apparatus according to any one of claims 4 to 7, characterized in that the light source driving means performs switching drive so that the black insertion ratio varies according to a luminance histogram distribution in the original frame.

9. The image display apparatus according to any one of claims 4 to 8, characterized in that the light source driving means performs switching drive so that the black insertion ratio varies according to the brightness of viewing environment for user.

10. The image display apparatus according to any one of claims 4 to 9, characterized in that the light source driving means performs switching drive so that the black insertion ratio varies according to magnitude of a motion vector in the original frame.

11. The image display apparatus according to any one of claims 4 to 10, characterized in that the light source driving

means further performs switching drive so that luminance of the black display area is variable as well.

12. The image display apparatus according to claim 3, characterized in that the light source driving means performs switching drive so that luminance of the black display area is variable when performing the black inserting process on the original frame.

13. The image display apparatus according to claim 12, characterized in that the light source driving means performs switching drive so that luminance of the black display area varies in multiple steps.

14. The image display apparatus according to claim 12, characterized in that the light source driving means performs switching drive so that luminance of the black display area continuously varies.

15. The image display apparatus according to any one of claims 12 to 14, characterized by further comprising setting means for allowing user to vary luminance of the black display area.

16. The image display apparatus according to any one of claims 12 to 15, characterized in that the light source driving means performs switching drive so that luminance of the black display area varies according to a luminance histogram distribution in the original frame.

17. The image display apparatus according to any one of claims 12 to 16, characterized in that the light source driving means performs switching drive so that luminance of the black display area varies according to the brightness of the viewing environment for user.

18. The image display apparatus according to any one of claims 12 to 17, characterized in that the light source driving means performs switching drive so that luminance of the black display area varies according to magnitude of a motion vector in the original frame.

19. The image display apparatus according to any one of claims 3 to 18, characterized in that the light source driving means performs switching drive so that the black inserting process is performed by frame.

20. The image display apparatus according to any one of claims 3 to 18, characterized in that the light source driving means performs switching drive so that the black inserting process is performed by black insertion line unit, the unit being composed of a predetermined number of horizontal scan line or lines in the original frame.

21. The image display apparatus according to claim 20, characterized in that the display means or the video signal processing means performs switching drive so that the black inserting process is performed by black insertion line unit and by frame.

22. The image display apparatus according to claim 20, characterized in that the display means or the video signal processing means performs switching drive so that the black inserting process is performed by inserting a plurality of black insertion lines away from each other.

23. The image display apparatus according to any one of claims 2 to 22, characterized in that the light source includes an LED.

24. The image display apparatus according to claim 1, characterized in that the video signal processing means includes black inserting processing means for performing a black inserting process on a video signal of the original frame.

25. The image display apparatus according to any one of claims 1 to 24, characterized in that the video signal processing means includes frame rate converting means for convert-

ing frame rate of a video signal by adding M (M: integer of 1 or larger) interpolation frames into between original frames neighboring each other along time base, the interpolation frames being obtained from the video images in the original frames by using motion compensation.

26. The image display apparatus according to any one of claims **1** to **24**, characterized in that the video signal processing means includes interpolation position setting means for converting frame rate of a video signal by adding N (N: integer of 2 or larger) interpolation frames into between original frames neighboring each other along time base, the N interpolation frames being obtained from video images in original frames by using motion compensation, so that interpolation positions of the video images in the N interpolation frames are set to deviated position which is closer to the nearest video image in the original frames rather than equalized positions, the equalized positions being obtained by equally dividing, into (N+1) portions, magnitude of video image motion between an earlier original frame and a following original frame along the time base.

27. The image display apparatus according to any one of claims **1** to **26**, characterized by further comprising setting means for allowing user to execute the black inserting process.

28. The image display apparatus according to any one of claims **1** to **27**, characterized in that the black inserting process is executed when the video signal is a cinema signal.

29. The image display apparatus according to claim **28**, characterized in that whether a video signal in an original frame is a cinema signal or not is determined by using contents information of the original frame, the contents information being included in an EPG (Electronic Program Guide).

30. The image display apparatus according to claim **28**, characterized in that whether a video signal in an original frame is a cinema signal or not is determined on the basis of frame rate of the original frame.

31. The image display apparatus according to any one of claims **1** to **27**, characterized in that the black inserting process is performed according to a luminance histogram distribution in the original frame.

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专利名称(译)	图像显示装置		
公开(公告)号	US20090184916A1	公开(公告)日	2009-07-23
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[标]申请(专利权)人(译)	索尼公司		
申请(专利权)人(译)	索尼公司		
当前申请(专利权)人(译)	SATURN Licensing LLC的		
[标]发明人	MIYAZAKI SHINICHIRO MURAKAMI ICHIRO NISHI TORU		
发明人	MIYAZAKI, SHINICHIRO MURAKAMI, ICHIRO NISHI, TORU		
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其他公开文献	US8441468		
外部链接	Espacenet USPTO		

摘要(译)

本发明提供一种能够根据环境减少保持模糊的图像显示装置。根据原始帧中的视频信号的实质和用户的观看环境的亮度中的至少一个，执行用于将黑色显示区域插入液晶显示面板2中的显示屏幕的黑色插入处理。具体地，例如，当原始帧中的视频信号是电影信号（电影信号）时，执行将黑色显示区域插入液晶显示面板2中的显示屏幕的黑插入处理。更具体地，例如，背光驱动单元71在背光72的开启和关闭之间执行切换驱动，使得在液晶显示面板2中的显示屏幕上执行黑插入处理。

