

Fig. 1 Prior art

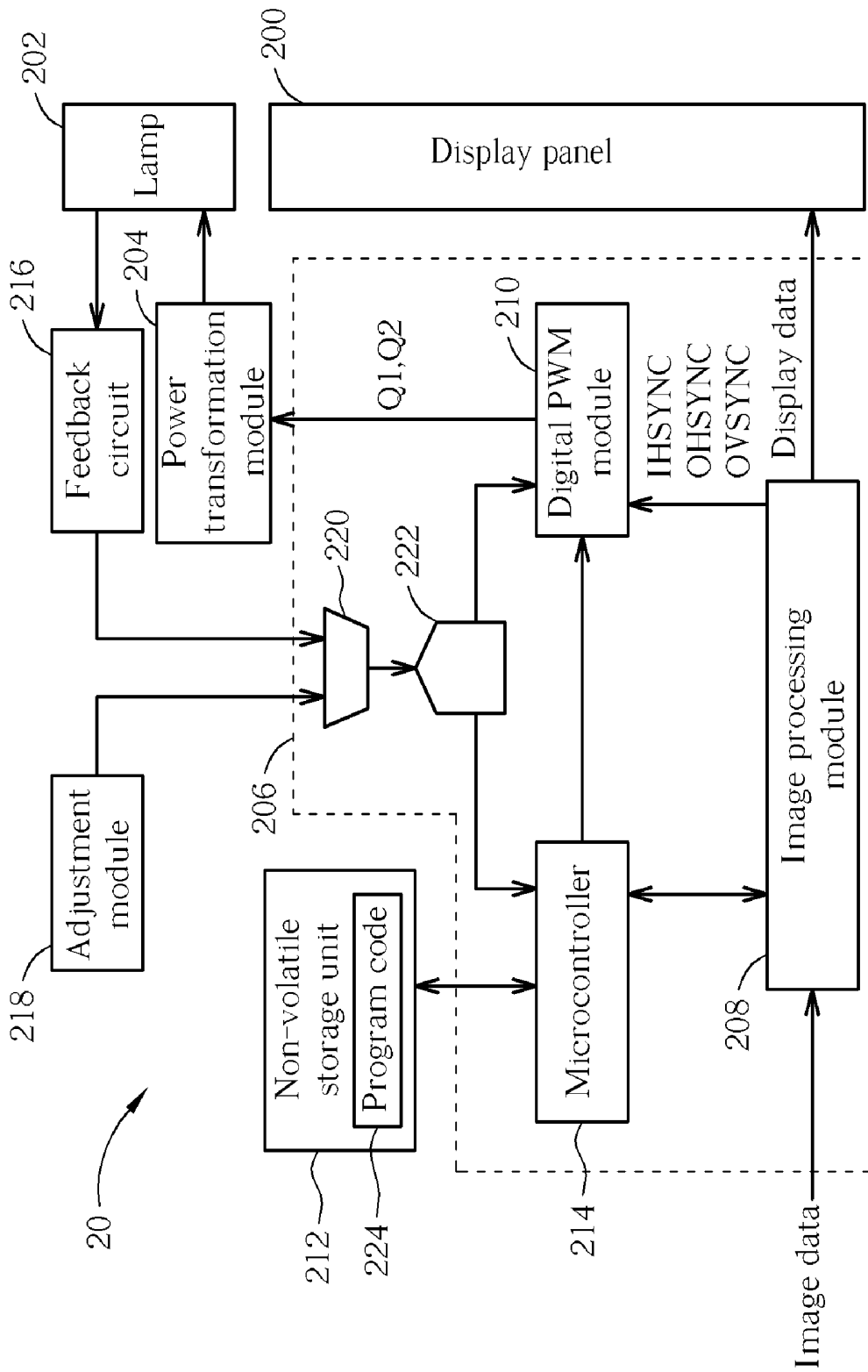


Fig. 2

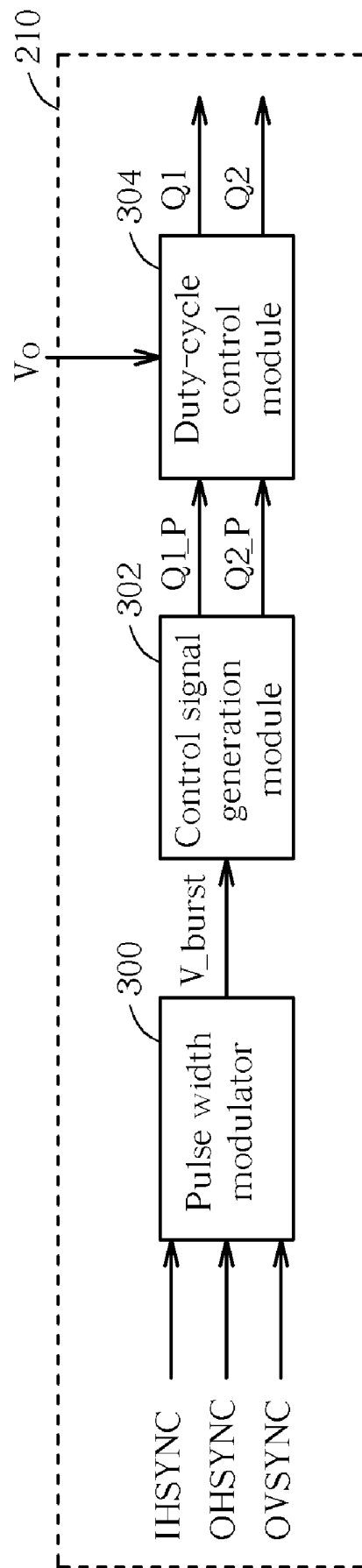


Fig. 3

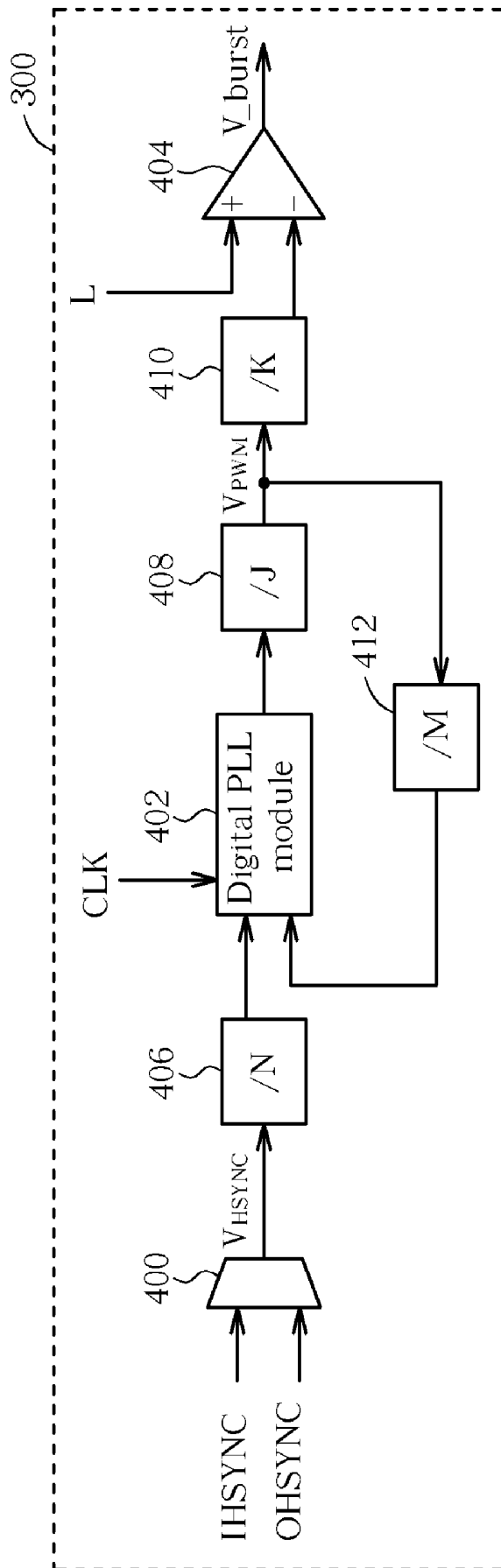


Fig. 4

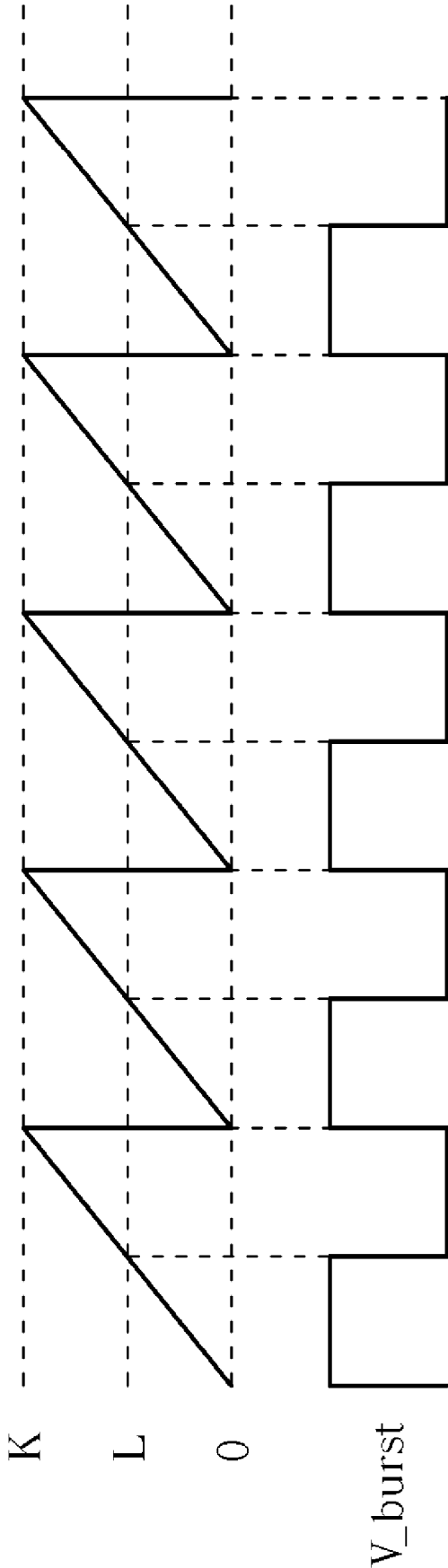


Fig. 5

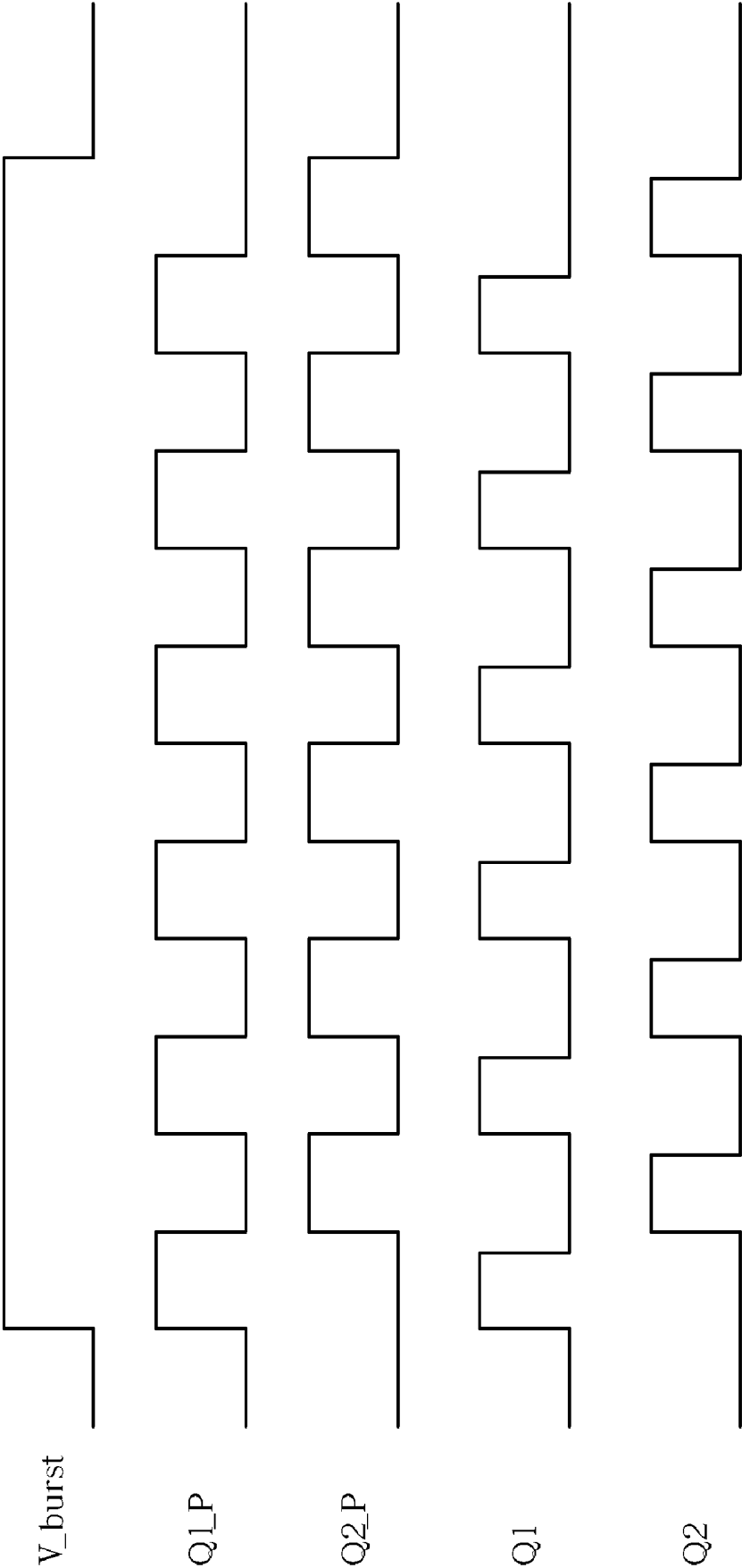


Fig. 6

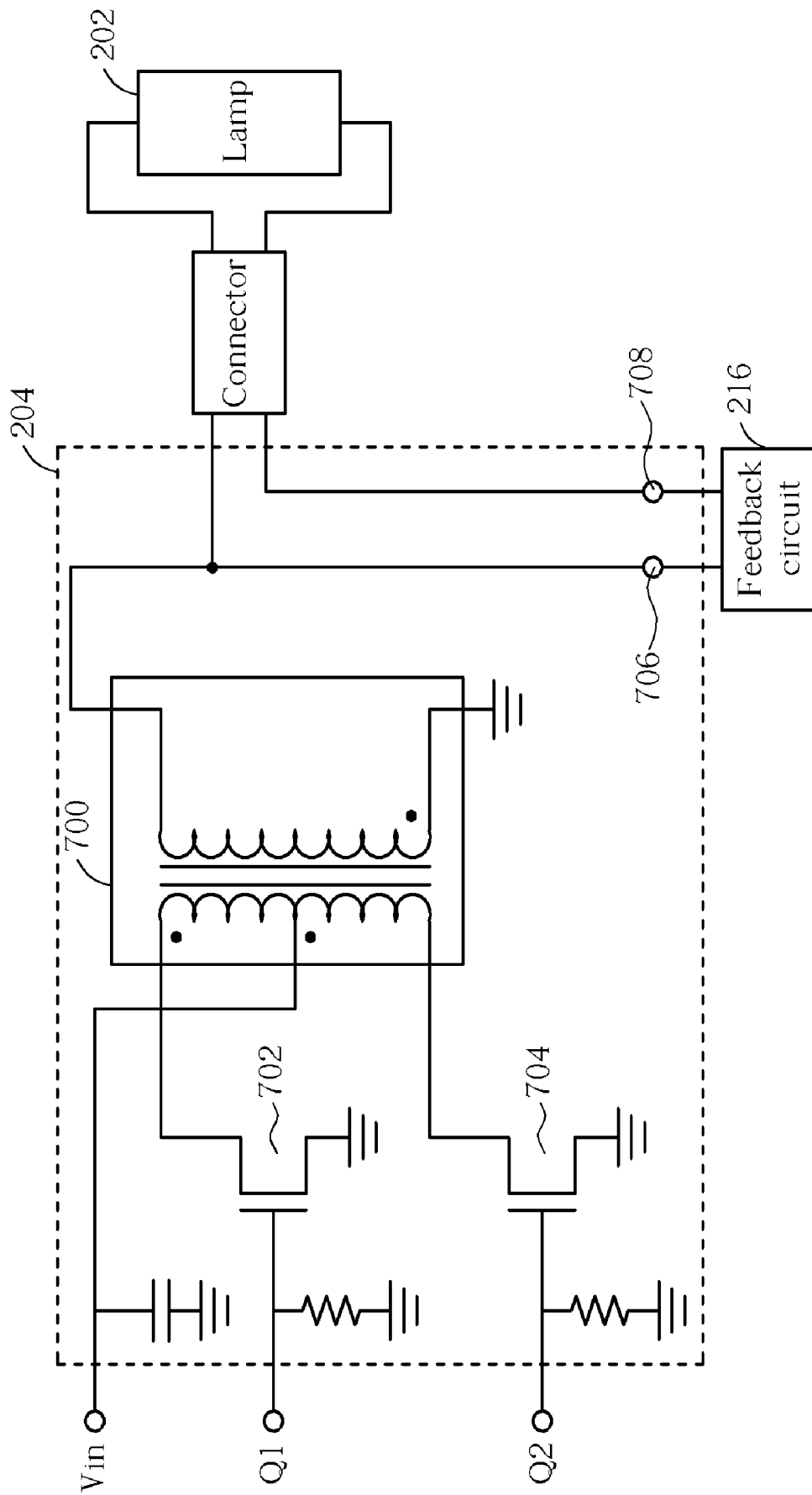


Fig. 7

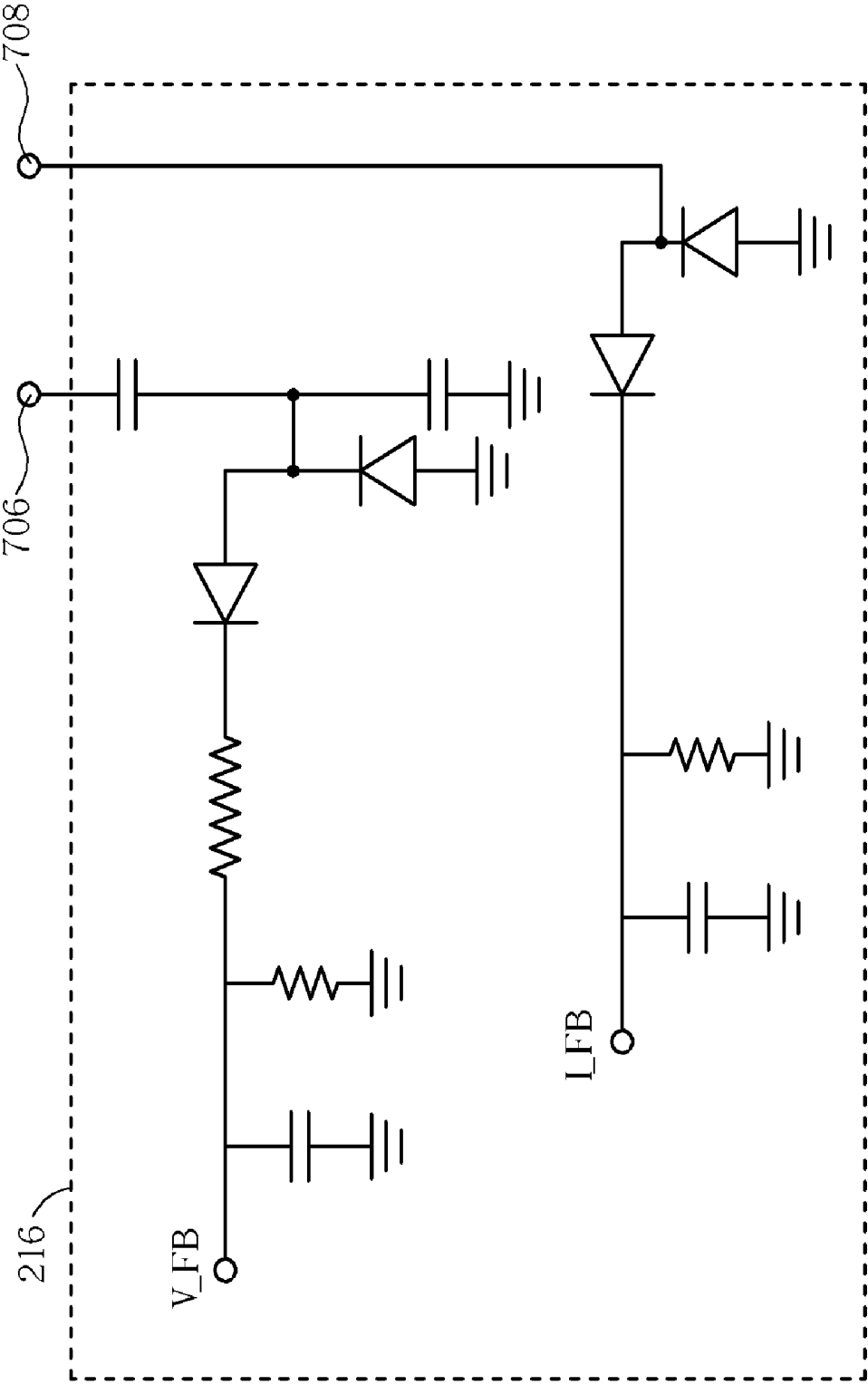


Fig. 8

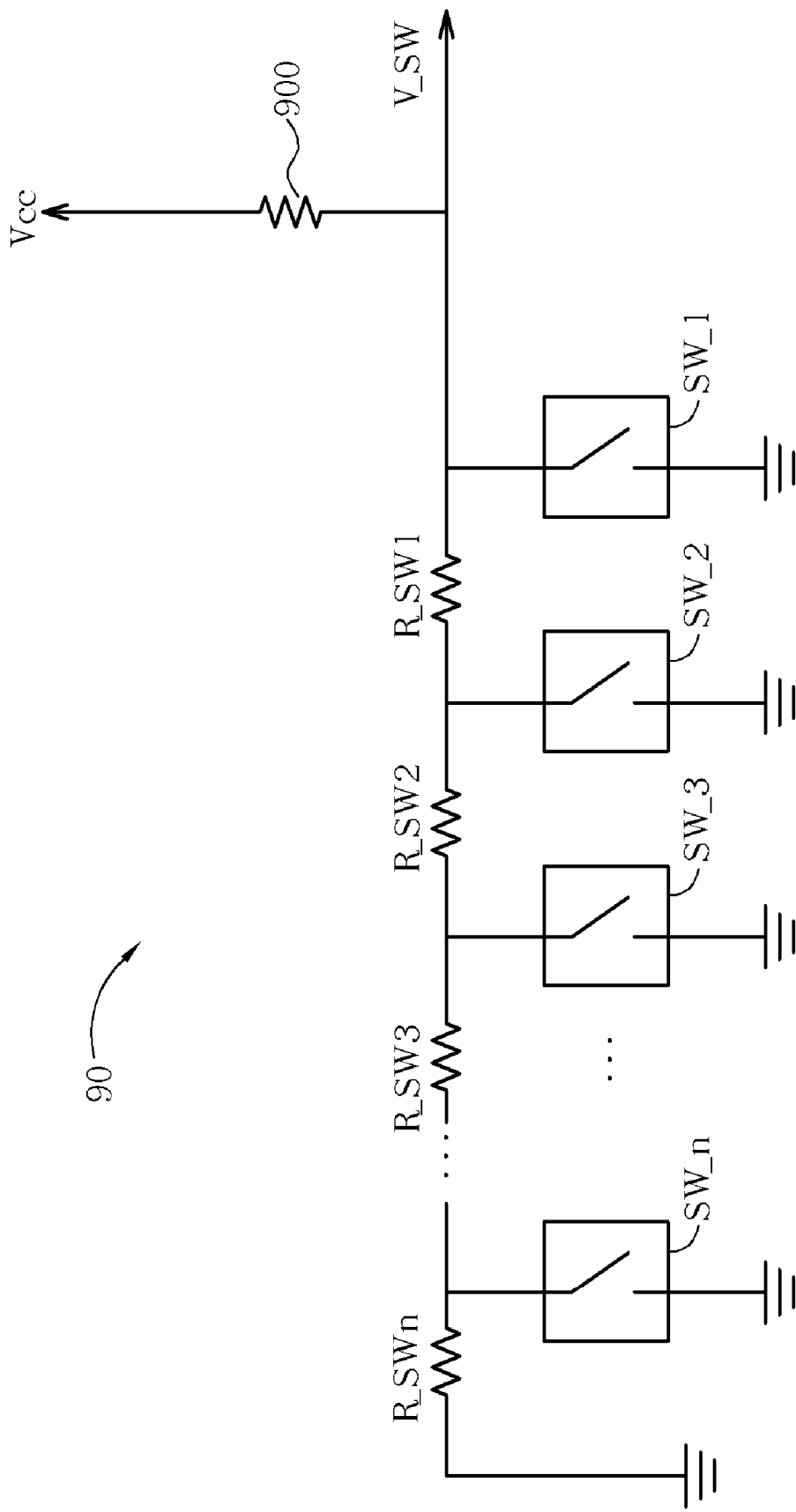


Fig. 9

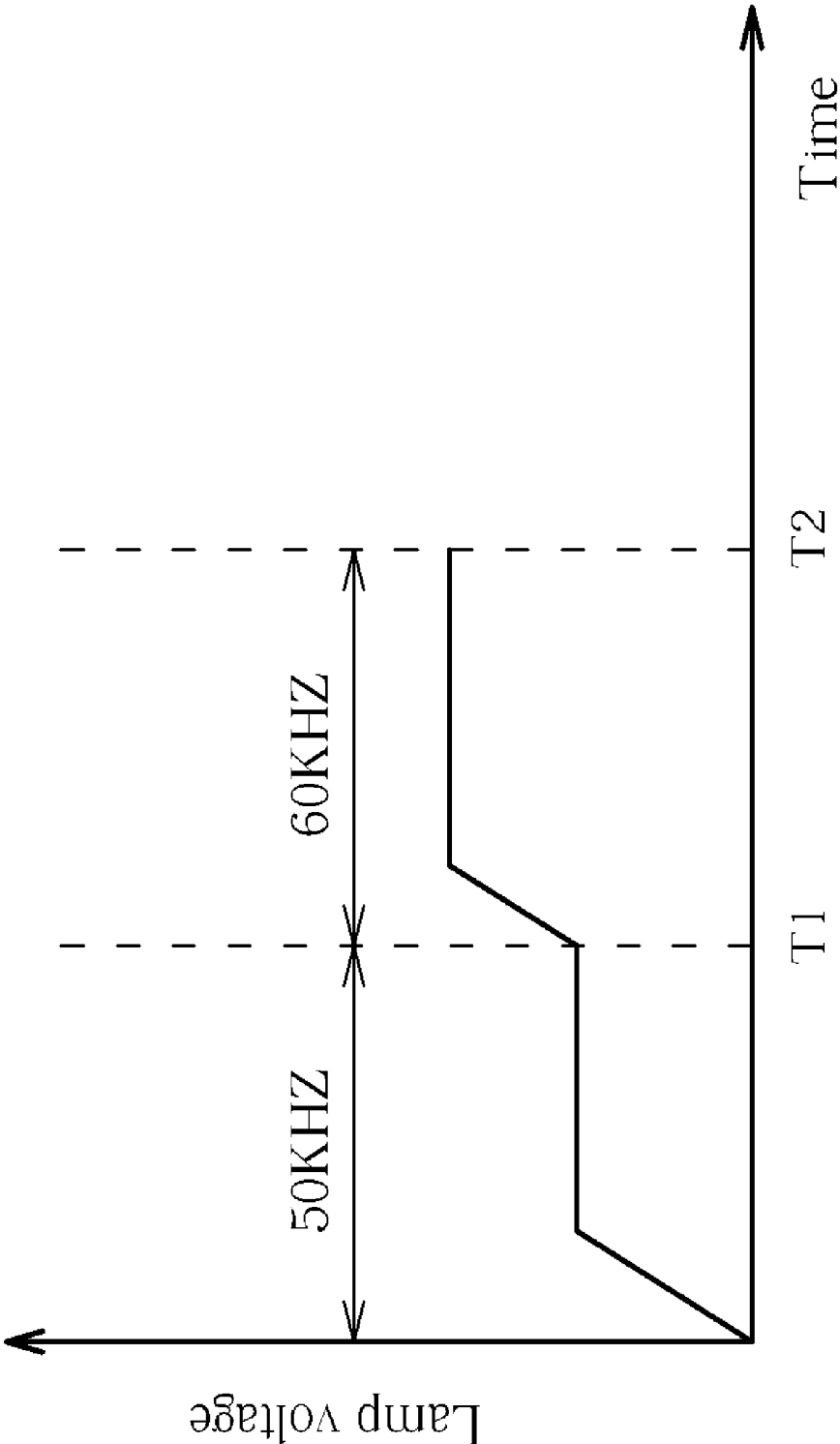


Fig. 10

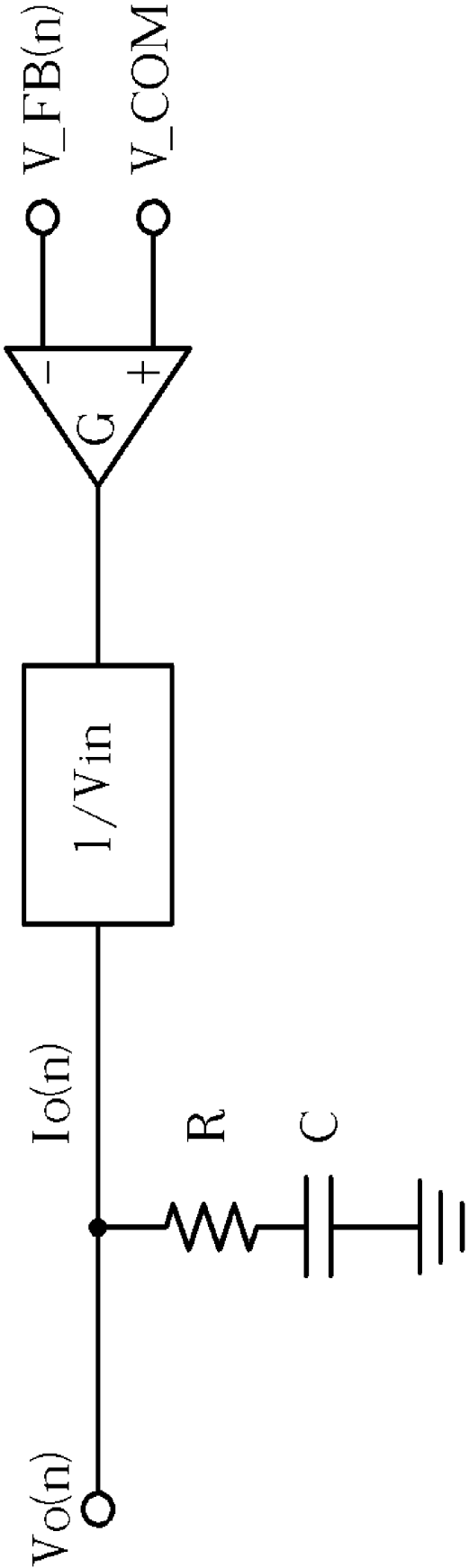


Fig. 11

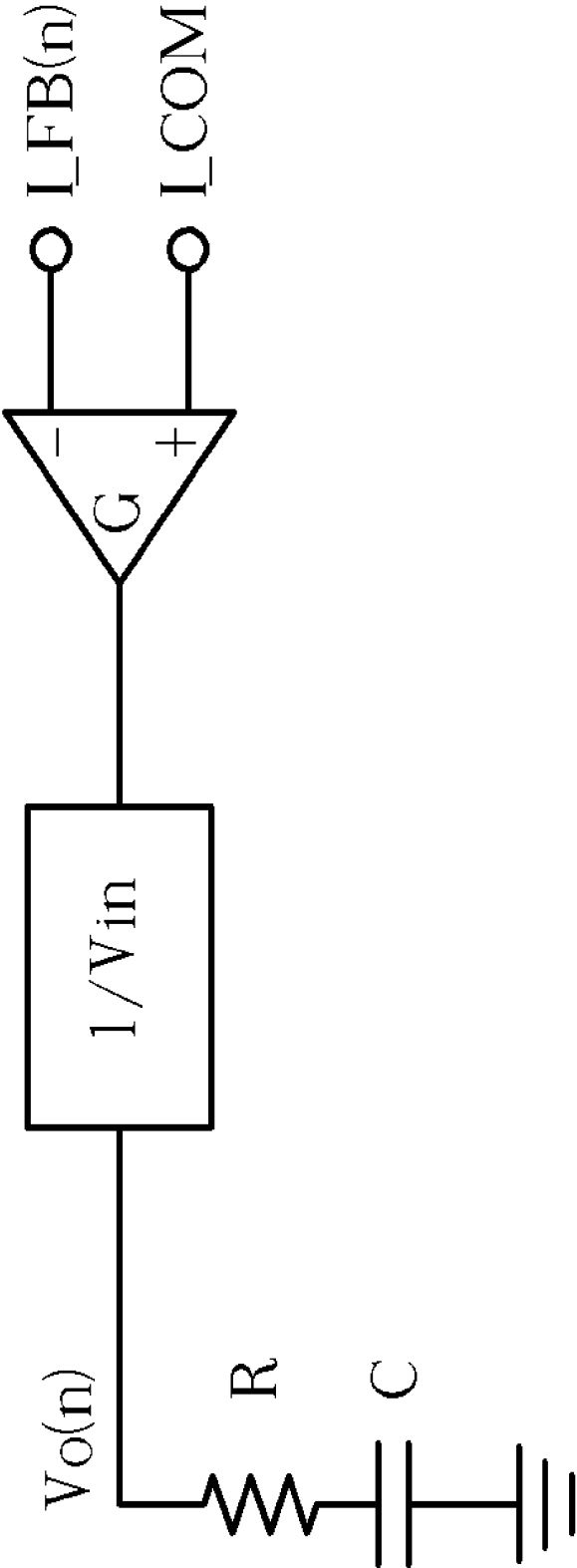


Fig. 12

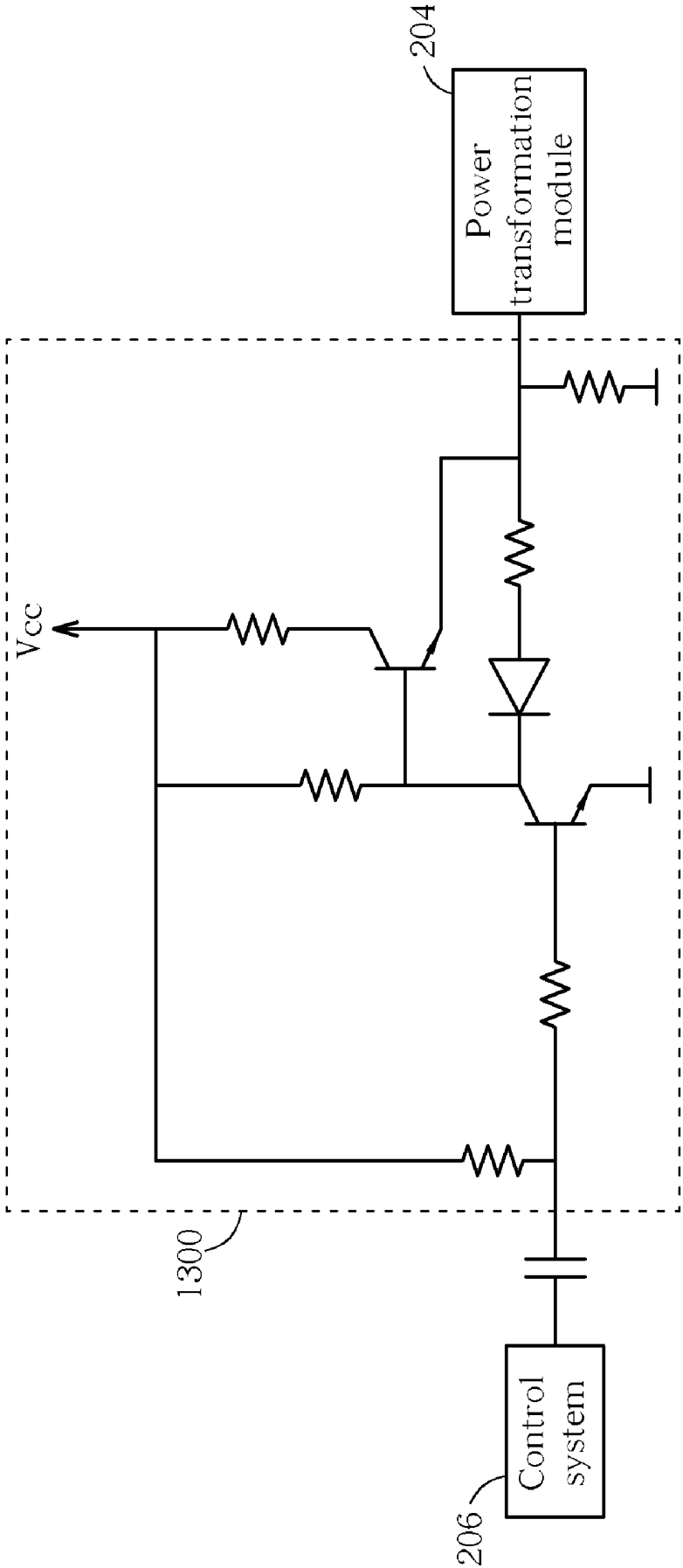


Fig. 13

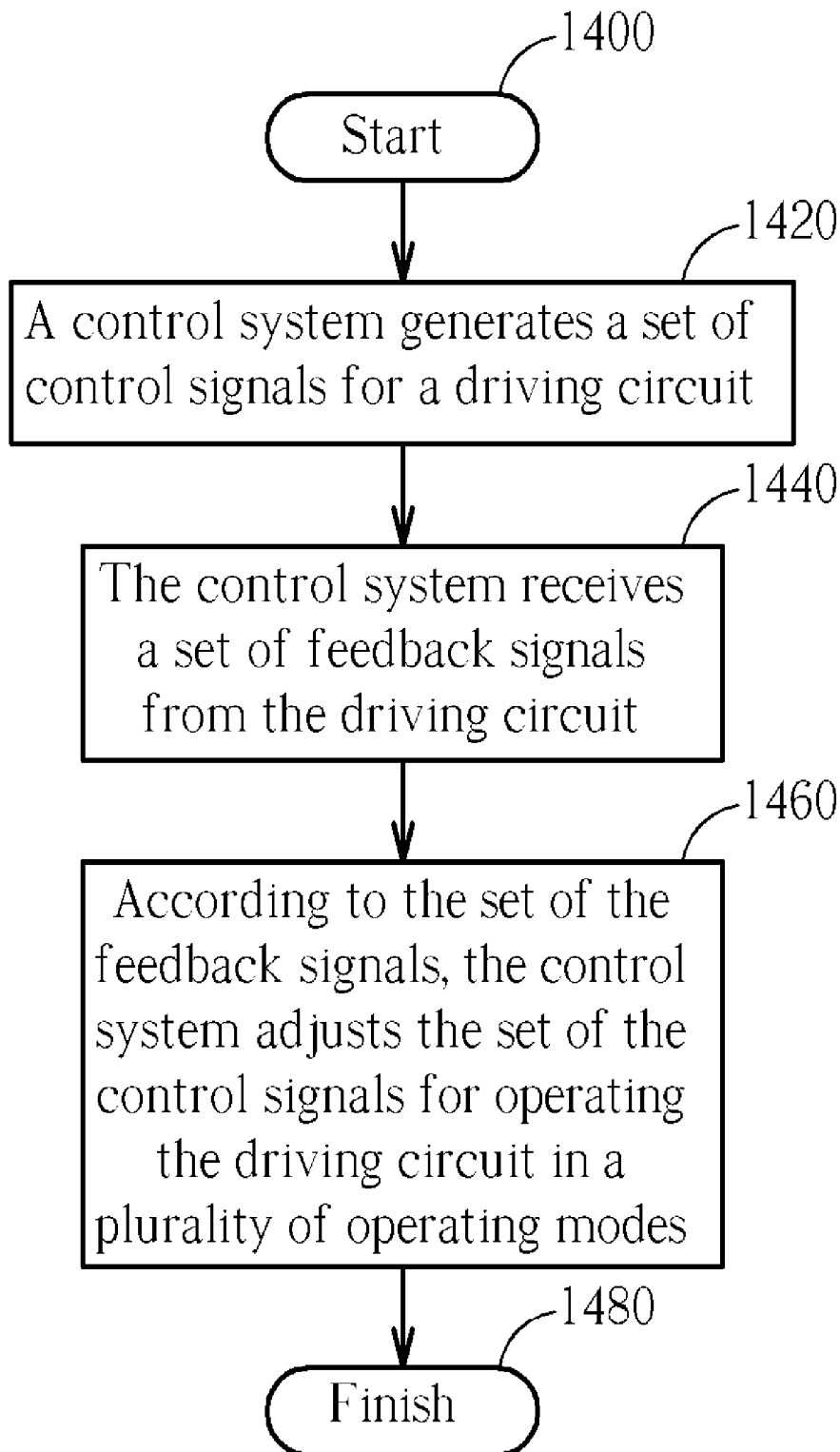


Fig. 14

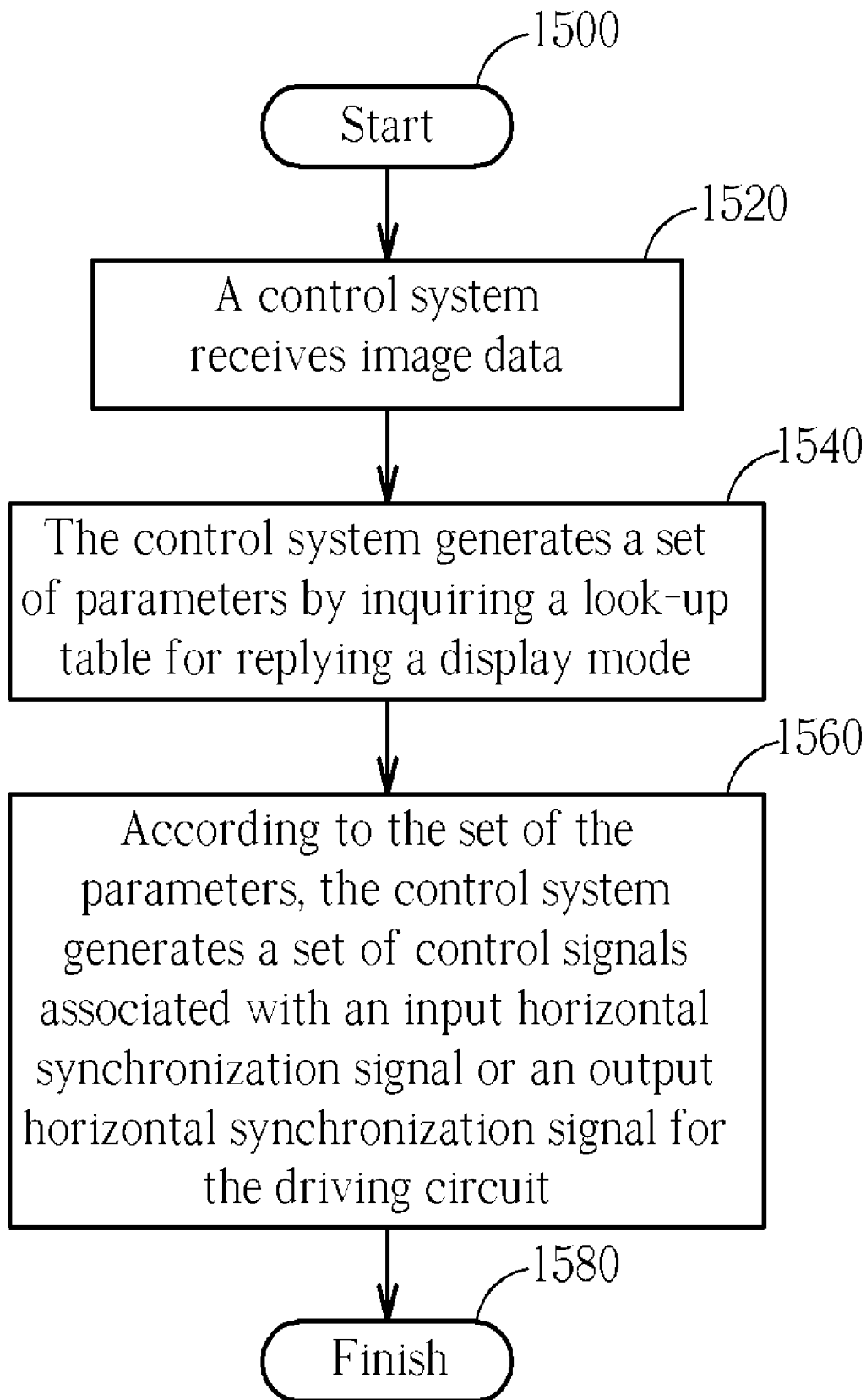


Fig. 15

**FLAT PANEL DISPLAY DEVICE, CONTROLLER,  
AND METHOD FOR DISPLAYING IMAGES**CROSS REFERENCE TO RELATED  
APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/694,687 and 60/596,141, filed Jun. 29, 2005 and Sep. 2, 2005 respectively, and included herein by reference.

## BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a flat panel display device, display controller, and method for displaying images, and more particularly, to a flat panel display device, display controller, and method for enhancing display quality by associating a frequency of a lamp with a display frequency.

[0004] 2. Description of the Prior Art

[0005] Liquid crystal display (LCD) monitors can be classified into reflective, transmissive, and transreflective LCD monitors. A reflective LCD monitor displays images with an external light source, which penetrates a display panel and is reflected by an internal reflector therein. A transmissive LCD monitor comprises a backlight source behind liquid crystal units, which emits light and penetrates liquid crystal units. A transreflective LCD monitor is a combination of the reflective LCD monitor and the transmissive LCD monitor.

[0006] In the transmissive LCD monitor, one or multiple cold cathode fluorescent lamps (CCFLs) are used as backlight sources. To emit light, the CCFL is driven by a high voltage source. Then, the CCFL excites mercury vapor therein to a high energy level by discharging the electricity. The excited mercury vapor returns to its initial energy state while the extra energy becomes ultraviolet. Finally, a phosphorescence material, spread on the inner surface of the CCFL, transforms ultraviolet into visible light.

[0007] FIG. 1 illustrates a block diagram of a prior art transmissive LCD monitor 100. The LCD monitor 100 includes an image processing circuit 102, a display panel 104, and a backlight module 106. The image processing circuit 102 controls R, G, and B (red, green, and blue) components for each pixel on the display panel 104 to display different color and contrast. The backlight module 106 includes a pulse width modulation (PWM) module 108, a voltage transformation circuit 110, a power source module 112, and a CCFL 114 to provide a light source for displaying images. To drive the CCFL 114, the voltage transformation circuit 110 transforms low-voltage DC power provided by the power source module 112 into high-voltage AC power with high-frequency. The PWM module 108 controls the AC power provided by the voltage transformation circuit 110 to adjust luminance of the CCFL 114. The PWM module 108 controls luminance of the CCFL 114 by adjusting on and off time of the CCFL 114 periodically. Therefore, the PWM module 108 provides a wider dimming range.

[0008] Conventionally, the image processing circuit 102 generates control signals through digital signal processing procedures, while the PWM module 108 is implemented by

additional analog circuits, so that the image processing circuit 102 and the PWM module 108, causing ripples on the display panel 104, and decreasing quality.

## SUMMARY OF THE INVENTION

[0009] It is therefore a primary objective of the claimed invention to provide a flat panel display device, display controller, and method for displaying images.

[0010] The present invention discloses a display controller comprising an image processing module for processing image data, and a digital pulse width modulation module coupled to the image processing module and an external application circuit, for controlling the external application circuit with reference to a synchronization signal. The display controller receives a set of feedback signals from the external application circuit for controlling the external application circuit to operate in a plurality of operating modes.

[0011] The present invention further discloses a method for controlling a backlight driving circuit, which comprises generating a set of control signals for the driving circuit by a display controller, receiving a set of feedback signals from the driving circuit by the display controller, and adjusting the set of the control signals by the display controller according to the set of the feedback signals, for operating the backlight driving circuit in a plurality of operating modes.

[0012] These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 illustrates a block diagram of a prior art transmissive LCD monitor.

[0014] FIG. 2 illustrates a block diagram of a flat panel display device in accordance with a preferred embodiment of the present invention.

[0015] FIG. 3 illustrates a block diagram of a preferred embodiment of the digital PWM module shown in FIG. 2.

[0016] FIG. 4 illustrates a block diagram of a preferred embodiment of the pulse width modulator shown in FIG. 3.

[0017] FIG. 5 illustrates a waveform diagram of signal waves corresponding to the pulse width modulator shown in FIG. 4.

[0018] FIG. 6 illustrates a waveform diagram of signals associated with the digital PWM module shown in FIG. 3.

[0019] FIG. 7 illustrates a schematic diagram of the power transformation module shown in FIG. 2.

[0020] FIG. 8 illustrates a schematic diagram of a feedback circuit.

[0021] FIG. 9 illustrates a schematic diagram of an adjustment module.

[0022] FIG. 10 illustrates a schematic diagram of operating frequency changes of the flat panel display device shown in FIG. 2 when operating in a voltage mode.

[0023] FIG. 11 illustrates an equivalent circuit diagram of program code of the flat panel display device at an ignition stage.

[0024] FIG. 12 illustrates an equivalent circuit diagram of program code of the flat panel display device at a current mode.

[0025] FIG. 13 illustrates a schematic diagram of a buffer circuit.

[0026] FIG. 14 illustrates a flowchart of a process for controlling a driving circuit of a backlight panel in accordance with a preferred embodiment of the present invention.

[0027] FIG. 15 illustrates a flowchart of a process for controlling a driving circuit of a backlight panel in accordance with another embodiment of the present invention.

#### DETAILED DESCRIPTION

[0028] Please refer to FIG. 2, which illustrates a block diagram of a flat panel display device 20 in accordance with a preferred embodiment of the present invention. The flat panel display device 20 includes a display panel 200, a lamp 202, a power transformation module 204, a non-volatile storage unit 212, and a display controller 206. The display controller 206 includes an image processing module 208, a digital PWM module 210, and a microcontroller 214. The flat panel display device 20 preferably includes a feedback circuit 216, an adjustment module 218, a multiplexer 220, and an A/D converter 222. The microcontroller 214 performs program code 224 stored in the non-volatile storage unit 212 to coordinate operations of the display controller 206, to control the display panel 200 and the lamp 202. In the display controller 206, the image processing module 208 receives a video source including an input horizontal synchronization signal IH SYNC, generates an output horizontal synchronization signal OH SYNC, an output vertical synchronization signal OV SYNC, and display data for the display panel 200. The image processing module 208 preferably transmits the input horizontal synchronization signal IH SYNC, the output horizontal synchronization signal OH SYNC, and the output vertical synchronization signal OV SYNC to the digital PWM module 210. The display data includes red, blue, and green signals R, G, and B. According to the input horizontal synchronization signal IH SYNC, the output horizontal synchronization signal OH SYNC, and the output vertical synchronization signal OV SYNC, the digital PWM module 210 controlled by the microcontroller 214 generates control signals Q1 and Q2, so as to control transistors of the power transformation module 204. In this embodiment, according to different operation modes, the digital PWM module 210 can adjust ON time of the transistors in the power transformation module 204 with the control signals Q1 and Q2, so as to control luminance of the lamp 202, while the digital PWM module 210 adjusts luminance of the lamp 202 according to signals outputted from the feedback circuit 216 and the adjustment module 218. Furthermore, the power transformation module 204 can further generate a plurality of DC voltages for different applications. Notice that, according to the present invention, those skilled in the art can recognize that the power transformation module 204 can be an inverter to control the lamp 202 or a voltage regulator to provide a plurality of voltage sources. The adjustment module 218 and the feedback circuit 216 can share the A/D converter 222 due to low-

speed operation, and saves logic gates. Alternatively, two independent A/D converters can be also implemented for converting signals from the adjustment module 218 and the feedback circuit 216 respectively. Moreover, the non-volatile storage unit 212 can be various kind of non-volatile memory, such as flash memory, EEPROM, etc., and the non-volatile storage unit 212 can be outside the display controller 206 or integrated in the display controller 206. Similarly, the microcontroller 214, such as 8051 microcontroller, can be outside the display controller 206 or integrated in the display controller 206. Furthermore, the power transformation module 204 can be utilized for driving not only a CCFL, but also other backlight sources, such as LEDs.

[0029] FIG. 3 illustrates a block diagram of a preferred embodiment of the digital PWM module 210 shown in FIG. 2. The digital PWM module 210 preferably includes a pulse width modulator 300, a control signal generation module 302, and a duty-cycle control module 304. According to the input horizontal synchronization signal IH SYNC, the output horizontal synchronization signal OH SYNC, and the output vertical synchronization signal OV SYNC, the pulse width modulator 300 generates a pulse signal V\_burst to the control signal generation module 302, and the microcontroller 214 controls a frequency of the pulse signal V\_burst. In this embodiment, the control signal generation module 302 toggles control signals Q1\_P and Q2\_P at high state of the pulse signal V\_burst. The duty-cycle control module 304 adjusts duty cycles of the control signals Q1\_P and Q2\_P to prevent overlapping of assertions between the control signals Q1\_P and Q2\_P. If the assertions of Q1 and Q2 are overlapped and received by the power transformation module 204, the power transformation module 204 will keep providing power for the lamp 202, which may burn out the power transformation module 204, such as an inverter circuitry. Through the duty-cycle control module 304, the assertions of Q1\_P and Q2\_P are prevented from overlapping, so are the control signals Q1 and Q2 received by the power transformation module 204. Preferably, the duty-cycle control module 304 adjusts the duty cycles of the control signals Q1 and Q2 according to an output voltage V<sub>o</sub>.

[0030] FIG. 4 illustrates a block diagram of a preferred embodiment of the pulse width modulator 300 shown in FIG. 3. The pulse width modulator 300 includes a multiplexer 400, a digital PLL module 402, a comparator 404, and dividers 406, 408, 410, and 412. The multiplexer 400 is controlled by the microcontroller 214, and utilized for outputting a signal V<sub>HSYNC</sub> to the divider 406 according to the input horizontal synchronization signal IH SYNC or the output horizontal synchronization signal OH SYNC. The dividers 406, 408, 410, and 412 divide received signals by divisors N, J, K, and M. The digital PLL module 402 receives a clock signal CLK, and adjusts a frequency of signals outputted to the divider 408 according to signals outputted from the dividers 406 and 412. In this embodiment, the divisors N, J, K, and M are determined by the microcontroller 214, obtained by inquiring a look-up table, and associated with the horizontal and vertical synchronization signals received by the multiplexer 400. Suppose that a frequency of the signal V<sub>HSYNC</sub> outputted from the multiplexer 400 is  $f_{HSYNC}$ , and a frequency of a signal V<sub>PWM</sub> outputted from the divider 408 is  $f_{PWM}$ , then a frequency of a signal inputted to the digital PLL module 402 is  $(f_{HSYNC} \times (M/N) \times J)$ . After being synchronized by the digital PLL module 402,  $f_{PWM} = f_{HSYNC} \times (M/N)$ , and a frequency of the

pulse signal  $V_{burst}$  is  $f_{burst}=f_{PWM}/K$ . Furthermore, the frequency  $f_{burst}$  of the pulse signal  $V_{burst}$  can be synchronized with the frequency  $f_{VSYNC}$  of the vertical synchronization signal  $VSYNC$ . For example, set  $(f_{HSYNC} \times M/N/K)$  is an integral multiple of the frequency  $f_{VSYNC}$ ; eg. 3 or 4 times, then the frequency of the signal outputted from the power transformation module 204 is associated with the frequencies of the vertical and horizontal synchronization signals, so as to prevent visible signal interference, such as ripples on the display panel 200. The comparator 404 determines the duty cycle of the pulse signal  $V_{burst}$  according to the signal  $L$  outputted from the microcontroller 214.

[0031] Please refer to FIG. 5, which illustrates a waveform diagram of signals associated with the pulse width modulator 300 shown in FIG. 4. As shown in FIG. 5, the divisor  $K$  determines the frequency of the pulse signal  $V_{burst}$ . The greater the divisor  $K$ , the longer the period of the pulse signal  $V_{burst}$  is. The parameter  $L$  determines a duty cycle of the pulse signal  $V_{burst}$ . The smaller the parameter  $L$ , the shorter the positive duration of each square wave of the pulse signal  $V_{burst}$  is. Therefore, by adjusting the divisor  $K$  and the parameter  $L$ , the frequencies and the duty cycles of the control signals  $Q1$  and  $Q2$  outputted to the power transformation module 204 are controlled, and thus luminance of the lamp can be adjusted.

[0032] Refer to FIG. 3 again, the control signal generation module 302 generates the square-wave signals  $Q1_P$  and  $Q2_P$  during positive square waves of the pulse signal  $V_{burst}$ , and the duty-cycle control module 304 can adjust the duty cycles of the square-wave signals  $Q1_P$  and  $Q2_P$ , so as to prevent the lamp 202 from burning out due to overlapping between the square-wave signals  $Q1_P$  and  $Q2_P$ . Please refer to FIG. 6, which illustrates a waveform diagram of signals associated with the digital PWM module 210 shown in FIG. 3. The control signal generation module 302 toggles the square-wave signals  $Q1_P$  and  $Q2_P$  during positive square waves of the pulse signal  $V_{burst}$ , and the duty-cycle control module 304 can adjust the duty cycles of the square-wave signals  $Q1_P$  and  $Q2_P$ . Preferably, the duty cycles of the square-wave signals  $Q1_P$  and  $Q2_P$  are 45%, and assertion durations of the control signals  $Q1$  and  $Q2$  are separated without overlapping.

[0033] Please refer to FIG. 7, which illustrates a schematic diagram of the power transformation module 204 shown in FIG. 2. According to the control signals  $Q1$  and  $Q2$  provided by the digital PWM module 210, the power transformation module 204 switches the transistors 702 and 704 to control a primary end of a transformer 700 and adjust luminance of the lamp 202 coupled to a secondary end of the transformer 700. As shown in FIG. 3, when the pulse signal  $V_{burst}$  outputted from the pulse width modulator 300 is high, the control signal generation module 302 toggles the control signals. As mentioned above, the frequency of the pulse signal  $V_{burst}$  is determined by the divisors  $N$ ,  $J$ ,  $K$ , and  $M$ , and the duty cycle of the pulse signal  $V_{burst}$  is determined by the parameter  $L$ . Therefore, by adjusting  $N$ ,  $J$ ,  $K$ ,  $M$ , and  $L$ , the frequencies and periods of the control signals  $Q1$  and  $Q2$  can be adjusted. For example, increasing a value of the parameter  $L$  can increase on time of the transformer 700 shown in FIG. 7, so that lighting period of the lamp 202 increases, and thus brightness of the lamp 202 is increased. Preferably, values of  $N$ ,  $J$ ,  $K$ ,  $M$ , and  $L$  corresponding to

different brightness can be stored in the non-volatile storage unit 212, and the microcontroller 214 can obtain the values of  $N$ ,  $J$ ,  $K$ ,  $M$ , and  $L$  corresponding to a required brightness when adjusting brightness of the lamp 202. Preferably, the secondary end of the transformer 700 and the lamp 202 provide feedback signals to the display controller 206 from the feedback circuit 216 through the terminals 706 and 708.

[0034] FIG. 8 illustrates a schematic diagram of the feedback circuit 216. The feedback circuit 216 can generate a feedback voltage  $V_{FB}$  and a feedback current  $I_{FB}$  according to signals outputted from the secondary end of the transformer 700 and the lamp 202. Moreover, the feedback circuit 216 can feedback an input voltage  $V_{in}$  provided to the power transformation module 204 and an open-lamp protection signal  $OLPZ$  (not shown in FIG. 8) to the display controller 206, which is useful for portable or multi-lamp applications.

[0035] FIG. 9 illustrates a schematic diagram of the adjustment module 218 shown in FIG. 2, including a resistor 900, switches  $SW_1$  to  $SW_n$ , and resistors  $R_{SW1}$  to  $R_{SWn}$ . The switches  $SW_1$  to  $SW_n$  are turned off initially, and corresponding to specific items respectively, such as menu, volume up, volume down, etc. If one of the switches  $SW_1$  to  $SW_n$  is turned on, resistance from a system voltage source  $V_{cc}$  to a system ground is changed, and a voltage  $V_{SW}$  outputted to the display controller 206 is changed accordingly. Therefore, according to the voltage  $V_{SW}$ , the microcontroller 214 can adjust an operating status of the display controller 206, such as brightness of the lamp 202, contrast of the display panel 200, etc.

[0036] In this embodiment, the digital PWM module 210 adjusts brightness of the lamp 202 according to the vertical and horizontal synchronization signals. Therefore, luminance frequency of the lamp 202 associates with display frequency of the display panel 200, and thus display quality can be improved. Take XGA for example, suppose that the display frequency of the flat panel display device 20 is 60 HZ, each frame includes 1344 horizontal lines and 804 vertical lines ( $V_{TOTAL}=804$ ), then the vertical synchronization signal and the pulse signal  $V_{burst}$  is synchronized as follows:

$$\begin{aligned} f_{VSYNC} &= 60 \text{ and } V_{TOTAL} = 804 \\ \text{then} \\ f_{HSYNC} &= f_{VSYNC} * V_{TOTAL} = 60 * 804 = 48240 \\ f_{PWM} &= (M/N) * 60 * 804 \\ \text{set } f_{burst} &= 4 * f_{VSYNC} = 240 \\ \text{then } (M/N) * (1/K) &= 4 / V_{TOTAL} = 4 / 804 \\ \text{choose} \\ M &= 1, N = 1, K = 201 \end{aligned}$$

[0037] Therefore,  $f_{burst}=240$  HZ, and  $f_{PWM}=48.24$  KHZ. Similarly, for SXGA, suppose that the display frequency of the flat panel display device 20 is 60 HZ, each frame includes 1688 horizontal lines and 1056 vertical lines ( $V_{TOTAL}=1056$ ), then:

$$\begin{aligned} f_{VSYNC} &= 60 \text{ and } V_{TOTAL} = 1056 \\ \text{then} \\ f_{HSYNC} &= 60 * 1056 = 63360 \\ f_{PWM} &= (M/N) * 60 * 804 \\ \text{set } f_{burst} &= 4 * f_{VSYNC} = 240 \end{aligned}$$

then  $(M/N) \times (1/K) = 4/V_{TOTAL} = 4/1056$

choose

$M=5, N=6, K=220$

[0038] Therefore,  $f_{BURST}=240$  HZ, and  $f_{PWM}=52.8$  KHZ. Then, according to the values of M, N, and K corresponding to the display qualities (ex. XGA and SXGA) stored in the non-volatile storage unit 212, the microcontroller 214 can synchronize the luminance frequency of the lamp 202 and the display frequency of the display panel 200. Moreover, increasing or decreasing brightness of the lamp 202 can be achieved by adjusting the value of the parameter L for changing the operation cycles of the control signals Q1 and Q2.

[0039] In other words, the operation cycles of the control signals Q1 and Q2 associate with the frequency  $f_{HSYNC}$  of the horizontal synchronization signal HSYNC and the  $f_{VSYNC}$  of the vertical synchronization signal VSYNC, and thus an ignition frequency (or starting frequency) of the lamp 202 associates with the frequencies  $f_{HSYNC}$  and  $f_{VSYNC}$ . Therefore, ripples caused by non-synchronization between the display frequency and the ignition frequency of the lamp 202 can be relieved.

[0040] Preferably, the flat panel display device 20 can operate in a plurality of operation modes, and associated operation program code 224 is designed and stored in the non-volatile storage unit 212 in advance. Please refer to FIG. 10, at an ignition stage, the flat panel display device 20 operates in a voltage mode, and operating frequencies are 50 KHZ from time points 0 to T1 and 60 KHZ from time points T1 to T2. Please refer to FIG. 11, which illustrates an equivalent circuit diagram of the program code 224 at the ignition stage. Notice that, elements of the circuit shown in FIG. 11 are utilized for narrating the operation of the program code 224, but are not required physically. An algorithm of the voltage mode is concluded as follows, where  $V_{FB}(n)$ ,  $V_{in}(n)$  are results of the voltages  $V_{FB}$  and  $V_{in}$  after being converted by the A/D converter 222, and T represents sampling time:

$$I_o(n) = (V_{COM} - V_{FB}(n)) \times G / V_{in}(n)$$

$$V_o(n+1) = I_o(n) \times R + V_c(n) + I_o(n) \times T / C$$

[0041] Wherein  $V_c(0)=0$  begins soft start.

[0042] Being divided by  $V_{in}(n)$  is to compensate variation of the input voltage  $V_{in}$ . After the open-lamp protection signal OLPZ stays in a high level for a predetermined duration, the program code 224 can then entering a current mode. Please refer to FIG. 12, which illustrates an equivalent circuit diagram of the program code 224 at the current mode. An algorithm of the current mode is as follows:

$$I_o(n) = (I_{COM} - I_{FB}(n)) \times G / V_{in}(n)$$

$$V_o(n+1) = I_o(n) \times R + V_c(n) + I_o(n) \times T / C$$

[0043] When  $V_c(0)=0$ , soft start.

[0044] In FIGS. 11 and 12, the blocks of  $1/V_{in}(n)$  compensate variation of the input voltage  $V_{in}$ , especially for flat panel display devices having unstable input voltages, such as portable or vehicle flat panel display devices. Of course, for flat panel display devices having stable input voltages, the block of  $1/V_{in}(n)$  is unnecessary. Note that, the circuits shown in FIGS. 11 and 12 are equivalent circuits of the program code 224, but are not required physically, so that the present invention can realize any desired performance of

the flat panel display device 20 by flexibly adjusting resistors and capacitors in the equivalent circuits.

[0045] In the current mode, the present invention can preferably drive the flat panel display device 20 in a burst mode, in which the operating frequency is synchronized with an integral multiple, e.g. 3 or 4 of the frequency of the vertical synchronization signal. In the voltage mode, stable voltages are provided, so as to drive the lamp 202 at the ignition stage. In the current mode, stable currents are provided, so as to drive the lamp 202 with highest luminance. In the burst mode, luminance of the lamp 202 can be well-controlled by adjusting the resistor R, the capacitor C, and the gain G of the equivalent circuit of the program code 224. For example, when the raising and descending speeds of the output voltage  $V_o$  are high, dimming control of the lamp 202 is efficient. When the raising and descending speeds of the output voltage  $V_o$  are low, audible noises of the transformer can be eliminated.

[0046] Regarding fail-safe protection, the present invention can reset the transformer 700 when a user adjusts the display panel through the adjustment module 218 or turns on and off AC power. In order to prevent the microcontroller 214 from dead lock, an output pin of the display controller 206 can be coupled to a buffering circuit, such as a buffering circuit 1300 shown in FIG. 13, through a de-coupling capacitor. Preferably, the control signals Q1 and Q2 are set to the high level when the microcontroller 214 is in an uncertain state or just started.

[0047] FIG. 14 illustrates a flowchart of a method for controlling a backlight driving circuit in accordance with a preferred embodiment of the present invention. The driving circuit can be used for driving a CCFL. The method starts at step 1400 and finishes at step 1480. In a step 1420, a display controller generates a set of control signals for the driving circuit, preferably including the first transistor control signal Q1 and the second transistor control signal Q2 shown in FIG. 2, which are separated without overlapping. The set of the control signals are associated with an input horizontal synchronization signal or an output horizontal synchronization signal, preferably in an integral multiple of frequency or in an rising edge or falling edge alignment relationship, so as to remove visible interference on a display panel. In a step 1440, the display controller receives a set of feedback signals from the driving circuit, preferably including a current feedback signal  $I_{FB}$ , a voltage feedback signal  $V_{FB}$ , an input voltage signal  $V_{in}$ , and an open-circuit detection signal OPLZ.

[0048] In a step 1460, according to the set of the feedback signals, the display controller adjusts the set of the control signals for operating the driving circuit in a plurality of operation modes, preferably including a voltage mode, a current mode, and a burst mode. For example, when the CCFL is at an ignition stage, the step 1460 adjusts the set of the control signals to operate the driving circuit in the voltage mode with stable voltages. When the CCFL is at a normal operation stage, the step 1460 adjusts the set of the control signals to operate the driving circuit in the current mode with sufficient current. When the CCFL is at a dimming stage, the step 1460 adjusts the set of the control signals to operate the driving circuit in the burst mode, so as to adjust luminance of the CCFL by changing duty cycles of the control signals. For example, a digital PWM module

generates the set of the control signals for the driving circuit, including the first transistor control signal Q1 and the second transistor control signal Q2. The display controller calculates an output voltage  $V_o(n+1)$  according to the set of the feedback signals, and the digital PWM module adjusts duty cycles of the set of the control signals according to the output voltage  $V_o(n+1)$ .

[0049] In the voltage mode, signals  $V_{FB}(n)$  and  $V_{in}(n)$  are obtained by sampling the voltage feedback signal  $V_{FB}$  and the input voltage signal  $V_{in}$ , and the output voltage  $V_o(n+1)$  can be calculated as follows:

$$I_o(n) = (V_{COM} - V_{FB}(n)) \times G / V_{in}(n)$$

$$V_o(n+1) = I_o(n) \times R + V_c(n) + I_o(n) \times T / C$$

[0050] where R, C, and G represents parameters of a resistor, a capacitor, and a gain,  $V_{COM}$  represents a voltage comparison value, T represents time,  $I_o(n)$  represents a sampled output current, and  $V_c(n)$  represents a crossing voltage between two ends of the capacitor with an initial value  $V_c(0)=0$ .

[0051] In the current mode, signals  $I_{FB}(n)$  and  $V_{in}(n)$  are obtained by sampling the current feedback signal  $I_{FB}$  and the input voltage signal  $V_{in}$ , and the output voltage  $V_o(n+1)$  can be calculated as follows:

$$I_o(n) = (I_{COM} - I_{FB}(n)) \times G / V_{in}(n)$$

$$V_o(n+1) = I_o(n) \times R + V_c(n) + I_o(n) \times T / C$$

[0052] wherein R, C, and G represents parameters of a resistor, a capacitor, and a gain,  $I_{COM}$  represents a reference current value, T represents time,  $I_o(n)$  represents a sampled output current, and  $V_c(n)$  represents a crossing voltage of the capacitor with an initial value  $V_c(0)=0$ .

[0053] FIG. 15 illustrates a flowchart of a process for controlling a backlight driving circuit in accordance with an embodiment of the present invention. The driving circuit can be used for driving a CCFL. The process starts from a step 1500 and finishes at a step 1580. In a step 1520, a display controller receives a video source. In a step 1540, the display controller generates a set of parameters by inquiring a look-up table for replying a display mode, preferably including VGA, XGA, SXGA, WGA, WXGA, etc. The set of the parameters can be the associated parameters shown in FIG. 4. In a step 1560, according to the set of the parameters, the display controller generates a set of control signals associated with an input horizontal synchronization signal or an output horizontal synchronization signal for the backlight driving circuit.

[0054] In summary, the frequencies of the control signals Q1 and Q2 generated by the digital PWM module 210 associates with the display frequency of the display panel 200, so that a switching frequency of the lamp 202 is associated with the display frequency of the display panel 200. Thus, the visible interference on the display is effectively relieved, and display quality is improved. Preferably, the digital PWM module 210 is integrated into the display controller 206. Persons skilled in the art can realize that the digital PWM module 210 can drive the power transformation module 204 to light up not only the CCFL, but also other kinds of backlight sources, such as LED. Also, the resistor R, the capacitor C, and the gain G can be adjusted to reach any required performance of system manufacturers.

[0055] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A display controller, comprising:

an image processing module for processing image data; and

a digital pulse width modulation module coupled to the image processing module and an external application circuit, for controlling the external application circuit with reference to a synchronization signal;

wherein the display controller receives a set of feedback signals from the external application circuit for controlling the external application circuit to operate in a plurality of operating modes.

2. The display controller of claim 1, wherein the set of the feedback signals comprises a current feedback signal and a voltage feedback signal.

3. The display controller of claim 1, wherein the external application circuit is a power transformation module for driving a lamp.

4. The display controller of claim 1, wherein the synchronization signal is an input horizontal synchronization signal.

5. The display controller of claim 1, wherein the synchronization signal is an output horizontal synchronization signal.

6. The display controller of claim 2, wherein the set of the feedback signals further comprises an input voltage signal.

7. The display controller of claim 6, wherein the set of the feedback signals further comprises an open-circuit detection signal.

8. The display controller of claim 3, wherein the lamp is a cold cathode fluorescent lamp.

9. The display controller of claim 8, wherein the operating modes comprise a voltage mode, a current mode, and a burst mode.

10. The display controller of claim 9, wherein the digital pulse width modulation module generates a set of control signals having a predetermined duty cycle for the external application circuit.

11. The display controller of claim 10, wherein the set of the control signals comprises a first transistor control signal and a second transistor control signal.

12. The display controller of claim 11, wherein the display controller calculates a voltage value  $V_o(n+1)$  according to the set of the feedback signals, and the digital pulse width modulation module adjusts the duty cycle according to the voltage value  $V_o(n+1)$ .

13. The display controller of claim 12, wherein when the display controller operates in an ignition stage, the digital pulse width modulation module operates the power transformation module in the voltage mode.

14. The display controller of claim 12, wherein when the display controller operates in a normal operation stage, the digital pulse width modulation module operates the power transformation module in the current mode.

15. The display controller of claim 12, wherein when the display controller operates in a dimming stage, the digital pulse width modulation module operates the power trans-

formation module in the burst mode, so as to control the power transformation module to adjust luminance of the cold cathode fluorescent lamp.

16. The display controller of claim 13, wherein the set of the feedback signals comprises a voltage feedback signal  $V_{FB}$  and an input voltage signal  $V_{in}$ , signals  $V_{FB}(n)$  and  $V_{in}(n)$  are obtained by sampling the voltage feedback signal  $V_{FB}$  and the input voltage signal  $V_{in}$  respectively, and the voltage mode calculates the voltage value  $V_o(n+1)$  by following equations:

$$I_o(n) = (V_{COM} - V_{FB}(n)) \times G / V_{in}(n)$$

$$V_o(n+1) = I_o(n) \times R + V_c(n) + I_o(n) \times T / C$$

wherein R, C, and G represent parameters of a resistor, a capacitor, and a gain,  $V_{COM}$  represents a voltage comparison value, T represents time,  $I_o(n)$  represents an output current value after sampling,  $V_c(n)$  represents a cross voltage value of the capacitor, and an initial value of  $V_c(n)$  is  $V_c(0)=0$ .

17. The display controller of claim 14, wherein the set of the feedback signals comprises a voltage feedback signal  $V_{FB}$  and an input voltage signal  $V_{in}$ , signals  $V_{FB}(n)$  and  $V_{in}(n)$  are obtained by sampling the voltage feedback signal  $V_{FB}$  and the input voltage signal  $V_{in}$  respectively, and the current mode calculates the voltage value  $V_o(n+1)$  by following equations:

$$I_o(n) = (I_{COM} - I_{FB}(n)) \times G / V_{in}(n)$$

$$V_o(n+1) = I_o(n) \times R + V_c(n) + I_o(n) \times T / C$$

wherein R, C, and G represent parameters of a resistor, a capacitor, and a gain,  $V_{COM}$  represents a voltage comparison value, T represents time,  $I_o(n)$  represents an output current value after sampling,  $V_c(n)$  represents a cross voltage value of the capacitor, and an initial value of  $V_c(n)$  is  $V_c(0)=0$ .

18. The display controller of claim 1, further comprising:

a multiplexer; and

an analog to digital converter coupled to the multiplexer;

wherein the multiplexer receives the set of the feedback signals and an external keypad signal, and selectively transmits the set of the feedback signals and the external keypad signal to the analog to digital converter for transforming into a digital signal.

19. The display controller of claim 18, wherein the analog to digital converter is coupled to the digital pulse width modulation module and a microcontroller and outputs the digital signal to the digital pulse width modulation module or the microcontroller.

20. The display controller of claim 1, further comprising an analog to digital converter coupled to the digital pulse width modulation module, for transforming the set of the feedback signals to a digital signal for the digital pulse width modulation module.

21. The display controller of claim 20, further comprising an analog to digital converter coupled to a microcontroller, for receiving an external keypad signal, and transforming the external keypad signal to a digital signal for the microcontroller.

22. The display controller of claim 1, wherein the external application circuit is a power transformation module for driving a plurality of light emitting diodes.

23. A method for controlling a backlight driving circuit, comprising:

generating a set of control signals for the driving circuit by a display controller;

receiving a set of feedback signals from the driving circuit by the display controller; and

adjusting the set of the control signals by the display controller according to the set of the feedback signals, for operating the driving circuit in a plurality of operating modes.

24. The method of claim 23, wherein the set of the control signal is associated with an input horizontal synchronization signal.

25. The method of claim 23, wherein the set of the control signal is associated with an output horizontal synchronization signal.

26. The method of claim 23, wherein the display controller adjusts luminance of a lamp by adjusting a duty cycle of the set of the control signals.

27. The method of claim 23, wherein the set of the feedback signals comprises a current feedback signal, a voltage feedback signal, and an input voltage signal.

28. The method of claim 23, wherein the operating modes comprise a voltage mode, a current mode, and a burst mode.

29. The method of claim 23, wherein the driving circuit drives a cold cathode fluorescent lamp.

30. The method of claim 23, wherein the driving circuit drives a plurality of light emitting diodes.

31. The method of claim 30, wherein the set of the control signals are adjusted to operate the driving circuit in the voltage mode when the cold cathode fluorescent lamp operates in an ignition stage.

32. The method of claim 31, wherein the set of the control signals are adjusted to operate the driving circuit in the current mode when the cold cathode fluorescent lamp operates in a normal operation stage.

33. The method of claim 32, wherein the set of the control signals are adjusted to operate the driving circuit in the burst mode when the cold cathode fluorescent lamp operates in a dimming stage.

\* \* \* \* \*

专利名称(译)	平板显示设备，控制器和显示图像的方法		
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#### 摘要(译)

提供了一种平板显示装置，LCD控制器和相关方法。平板显示装置包括显示面板，用于为显示面板提供背光源的灯，用于为灯提供电源的电源转换模块，用于存储程序代码的非易失性存储单元，以及显示控制器。显示控制器包括：图像处理模块，用于处理图像数据并将处理结果输出到显示面板；以及数字脉冲宽度调制模块，用于参考同步信号调节电力变换模块的接通和断开时间。

