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Fallot-Burghardt et al.(10) **Pub. No.: US 2003/0122760 A1**(43) **Pub. Date: Jul. 3, 2003**(54) **CIRCUIT ARRANGEMENT FOR THE
VOLTAGE SUPPLY OF A LIQUID CRYSTAL
DISPLAY DEVICE****Publication Classification**(51) **Int. Cl.⁷** **G09G 3/36**(52) **U.S. Cl.** **345/89**(76) Inventors: **Wolfgang Fallot-Burghardt**, Zuerich
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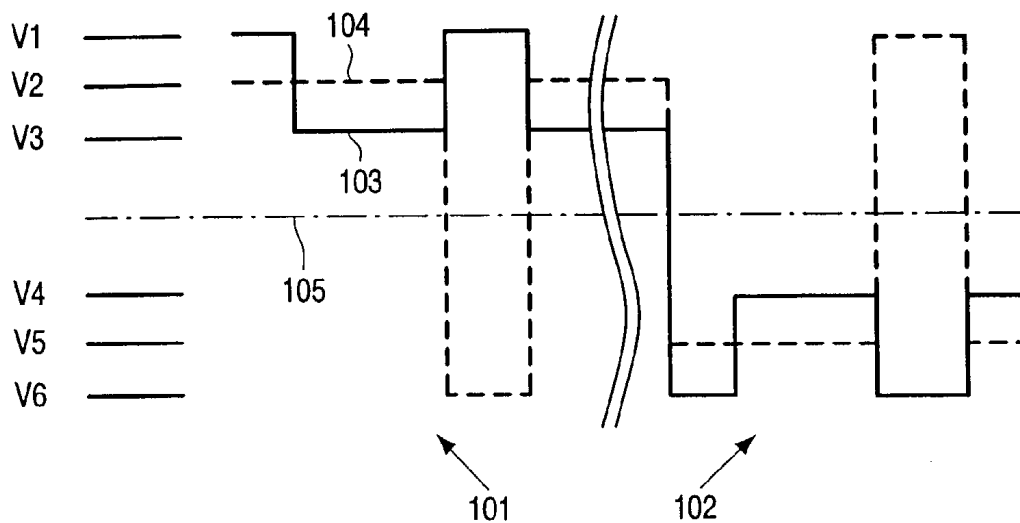
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(57) **ABSTRACT**

The circuit arrangement serves for the voltage supply of the row and column drivers of a liquid crystal display device. It comprises a voltage divider (1) having a plurality of series-connected resistors (R1-R5) and having voltage pick-offs (22-25) arranged between the resistors (R1-R5) for picking off different voltage levels (V2-V5). A single one (25) of the voltage pick-offs (22-25) is provided with means (3) for fine-tuning of the voltage level (V5) picked off there. By individually calibrating each individual circuit arrangement once, the one voltage level (V5) may be fine-tuned such that crosstalk caused by asymmetrical voltage levels, i.e. mutual interaction of pixel contents, is reduced. The advantages of the circuit arrangement come into their own in particular when it is used in liquid crystal display devices with a gray-stage display or color display.



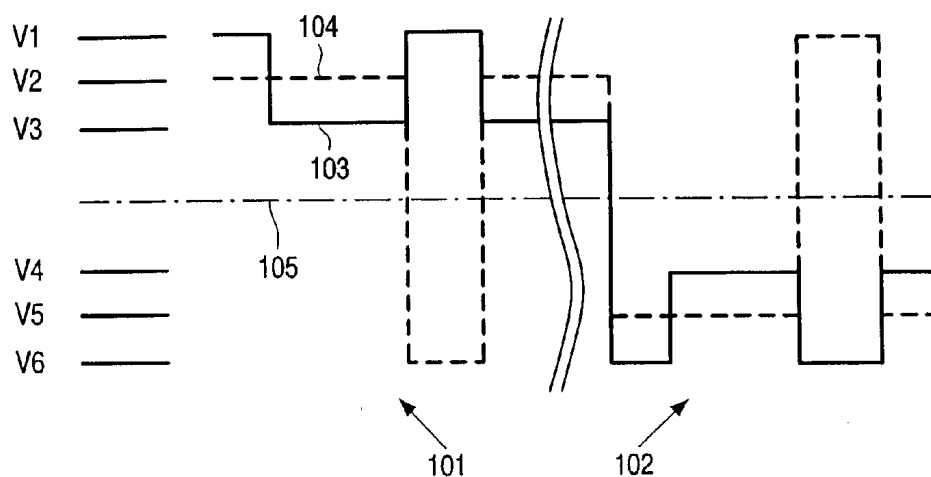


FIG. 1

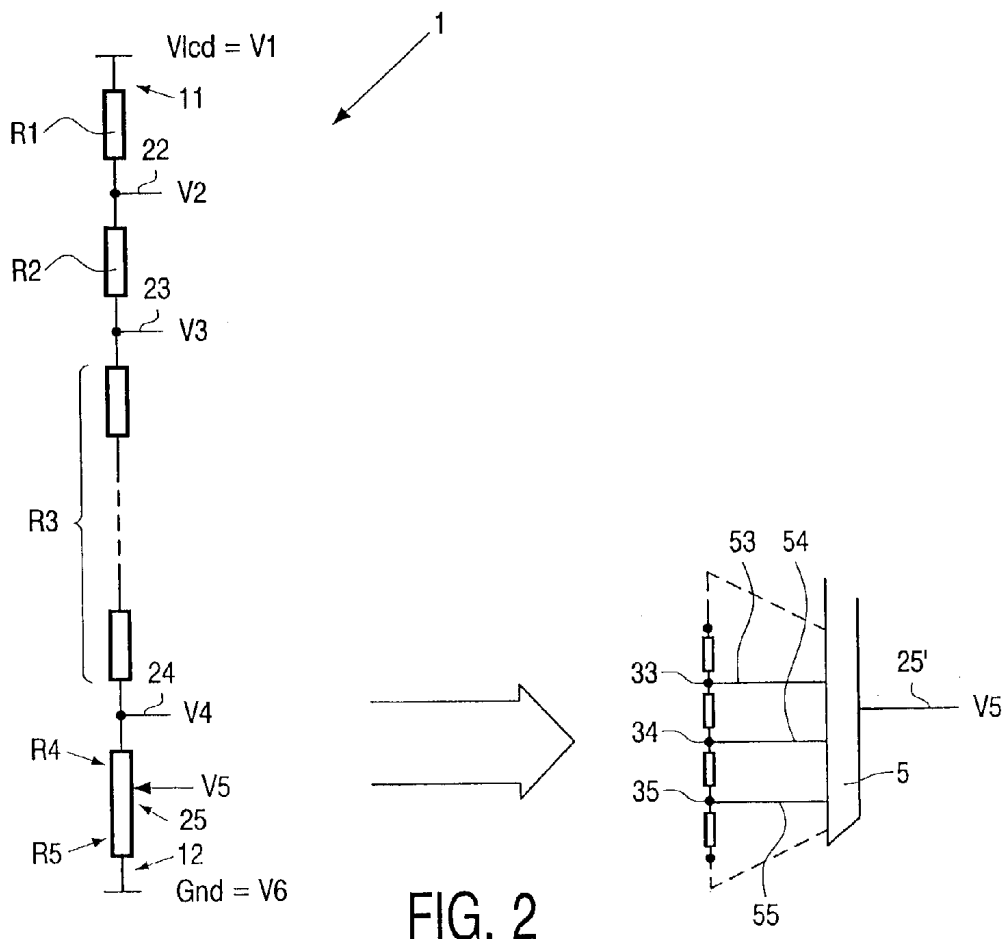


FIG. 2

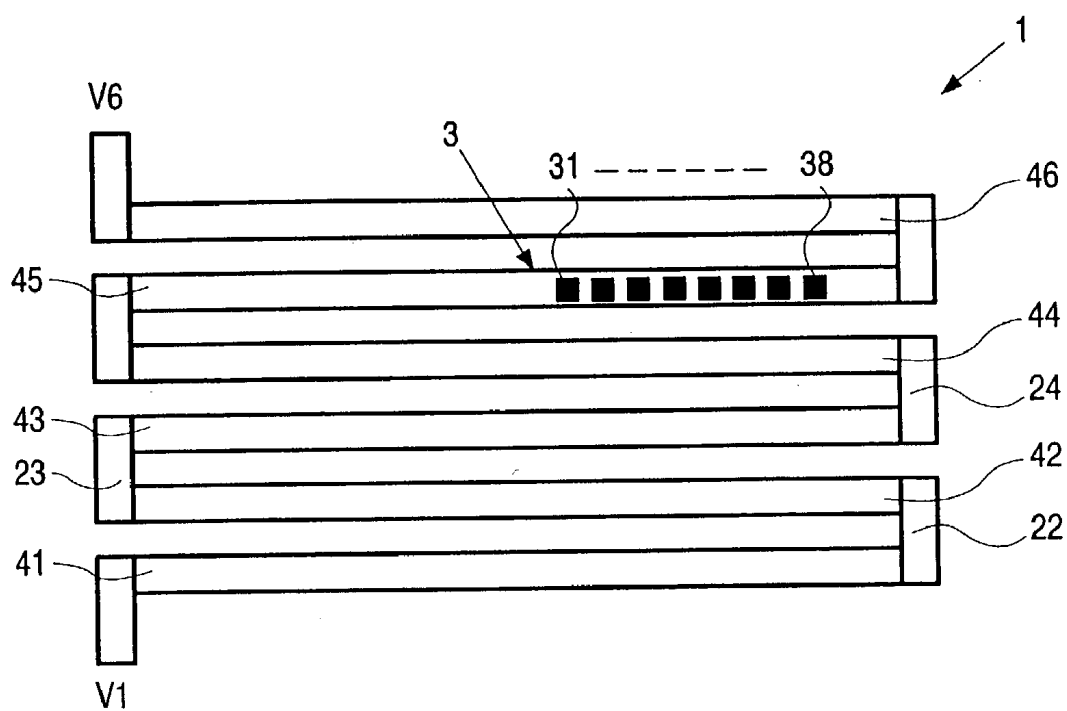


FIG. 3

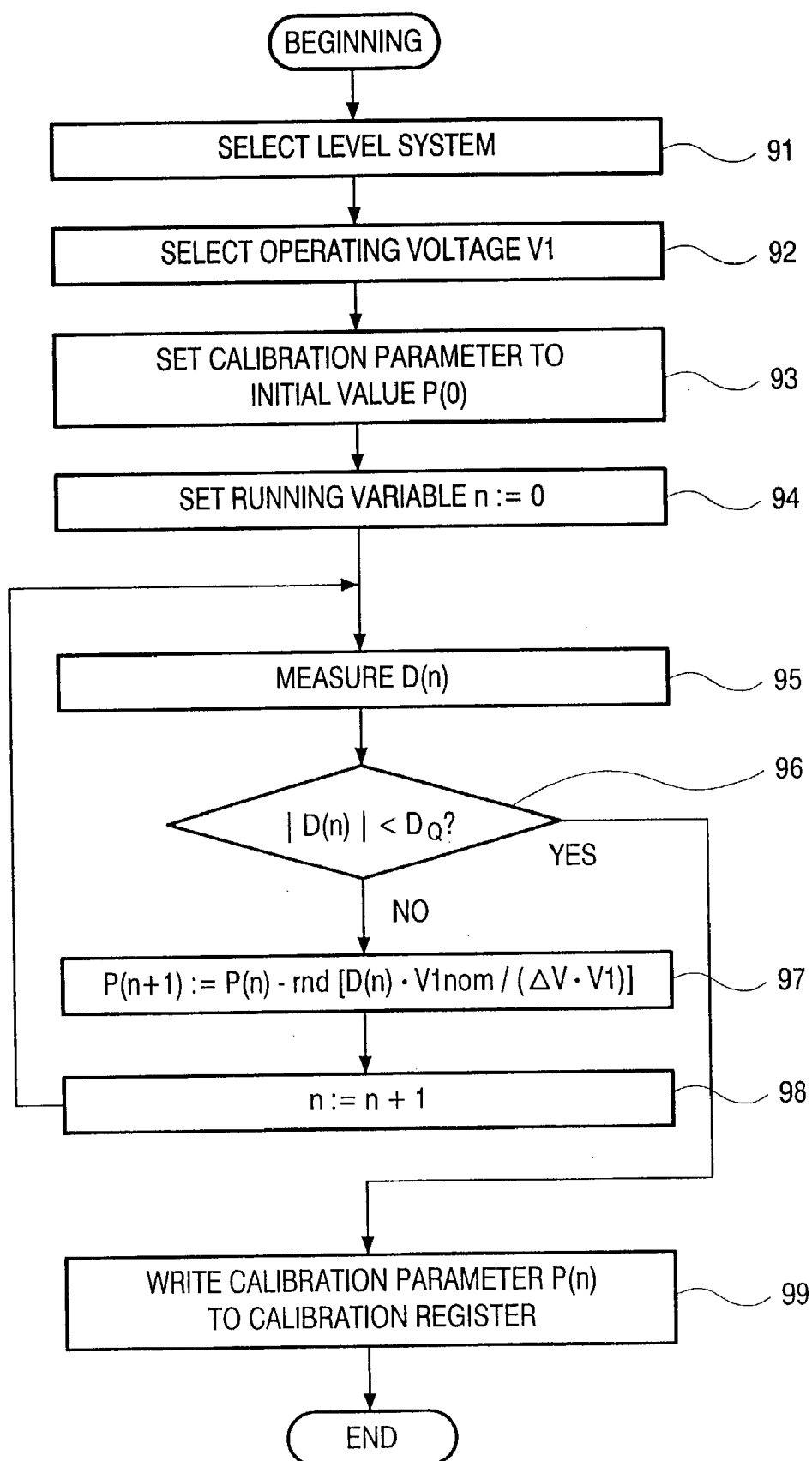


FIG. 4

CIRCUIT ARRANGEMENT FOR THE VOLTAGE SUPPLY OF A LIQUID CRYSTAL DISPLAY DEVICE

[0001] The invention relates to a circuit arrangement for the voltage supply of a liquid crystal display device, a liquid crystal display device comprising this circuit arrangement, and a method of calibrating the circuit arrangement.

[0002] A liquid crystal display device (LCD) conventionally comprises two glass plates attached parallel to one another, between which there is arranged a layer of liquid crystals. The two glass panels each carry electrodes on the side facing the liquid crystal layer, which electrodes may be exposed to different voltages, in order to change the optical characteristics of the liquid crystals located between the electrodes. These optical characteristics are essentially those which influence light transmitting capacity. In the case of dot matrix liquid crystal display devices, the electrodes take the form of dot-like areas (picture elements, pixels), which are connected together on the one side of the liquid crystal layer in rows and on the other side in columns. They are activated by suitable electrical circuits, which comprise a row and column driver. Such row and column drivers activate the electrodes cyclically with different voltages of different polarities. For this, a plurality of different intermediate voltages, for example, six are required. These intermediate voltages are conventionally generated by an appropriate voltage divider, the outputs of which are connected to the row and column drivers. The voltage divider typically comprises a plurality of series-connected resistors, between which the different voltage levels may in each case be picked off.

[0003] The problem to be solved by the present invention is illustrated with reference to **FIG. 1**, which comprises a schematic diagram of six voltage levels **V1** to **V6**. The voltage level **V1** is conventionally identical to an LCD operating voltage **V_{lcd}**, and **V6** may be identical to ground. A row voltage waveform **103** and a column voltage waveform **104** typical of commercially available liquid crystal display devices are illustrated schematically. When the electrodes are activated cyclically, it is possible to distinguish between two half-periods **101**, **102**:

[0004] During an "even" half-period **101**, the column voltage **104** is kept at the level **V2** ("unselected") or set to **V6** ("selected"). For switched-on (for example black) pixels, the row driver generates the voltage **V1**, for switched-off (for example white) pixels the voltage **V3**, such that the voltage **V1-V2** or **V3-V2**, or **V1-V6** or **V3-V6** is applied to the corresponding liquid crystals.

[0005] During an "odd" half-period **102**, similar conditions apply, except that the voltages are mirrored in relation to an axis of symmetry **105** located at $(V1-V6)/2$. The voltage **V6-V5** or **V4-V5**, or **V6-V1** or **V4-V1** is then applied to the corresponding liquid crystals.

[0006] For the time average for all the pixels of one column to be identical, irrespective of the number of switched-on or -off pixels in a column, the voltages arising in a half-period should be symmetrical, i.e. the following should apply:

$$V1-V2=V2-V3; V4-V5=V5-V6. \quad (1)$$

[0007] Moreover, in an ideal case, the voltage levels should be equidistant as follows:

$$V1-V2=V2-V3=V4-V5=V5-V6=V_d, \quad (2)$$

[0008] Wherein **V_d** is the constant difference voltage (equidistance). If only one of the six voltage levels deviates from the ideal value, for example as a result of production fluctuations, and violates the equidistance conditions (1) or (2), asymmetries will occur, which yield differing contributions from switched-on and switched-off pixels. This leads to undesirable image distortions, which are easily visible to the eye and reduce image quality. This type of distortion is known as "crosstalk", because it depends on the mutual interaction of pixel contents.

[0009] Liquid crystal display devices with gray stage displays or color displays are particularly sensitive to this type of crosstalk. In these, the gray stages lie on the steep slope of the characteristic curve (**V_T** curve) of the liquid crystal. In this case, deviations of a few millivolts from the equidistance conditions (1) or (2) are visible to the eye and perceived as disturbing.

[0010] For a complete correction of all the errors causing crosstalk by means of calibration, a circuit would be necessary which allowed an independent setting of all the voltage levels relative to a reference voltage, for example ground. However, such a circuit would be extremely expensive, would occupy a large area, and would consume a relatively large amount of electrical power. It would therefore be unsuited to practical application.

[0011] **JP-A-10-062743** discloses a circuit for a liquid crystal display device, which is designed to eliminate crosstalk. The circuit is so designed that two voltage levels are always changed at the same time. This is achieved by means of two embodiments. In a first embodiment, two resistors from a plurality of series-connected resistors are changed. This requires an increased hardware expenditure and/or greater accuracy of resistor chain pick-offs. In a second embodiment, one resistor is changed from each of two parallel-connected resistor chains. This entails an increased power consumption and/or an increased space requirement.

[0012] It is an object of the invention to provide a circuit arrangement for the voltage supply of a liquid crystal display device or to provide a liquid crystal display device which reduces crosstalk to an acceptable degree and at the same time is of a simple construction and is space- and power-saving. A further object of the invention is to provide a method of calibrating such a circuit arrangement. These objects are achieved by the circuit arrangement, liquid crystal display device, and calibration method as defined in the independent claims. Advantageous embodiments are indicated in the dependent claims.

[0013] The circuit arrangement according to the invention for voltage supply of the row and column drivers of a liquid crystal display device comprises a voltage divider having a plurality of series-connected resistors and having voltage pick-offs arranged between the resistors for picking off different voltage levels. A single one of the voltage pick-offs is provided with means for fine-tuning of the voltage level picked off there.

[0014] The liquid crystal display device according to the invention comprises a liquid crystal layer, row and column

drivers, and a circuit arrangement for voltage supply of the row and column drivers. The circuit arrangement is in this case an above-described circuit arrangement according to the invention.

[0015] The method according to the invention for calibrating the circuit arrangement according to the invention comprises the following steps:

- [0016] (a) selection of an initial fine-tuned setting;
- [0017] (b) measurement of the value of a quality parameter characterizing the voltage level overall;
- [0018] (c) establishing whether the measured quality parameter value lies within a specified quality interval;
- [0019] (d) if the result of step (c) is negative: recursive determination of a new fine-tuned setting and repetition of steps (b) and (c); and
- [0020] (e) if the result of step (c) is positive: storage of current fine-tuned setting.

[0021] Calibration is performed once, individually for each instance of the circuit arrangement.

[0022] The invention is based on a detailed analysis of the accuracy of the voltage level and the different influences and parameters which influence this accuracy. As a result of this analysis, it may be noted that both systematic and random errors impair voltage level accuracy. As an example of random impairment, mention may be made here of the random fluctuations of the contact resistances in the resistor chain, which have a direct effect on the voltage levels picked off from the resistor chain.

[0023] On the basis of these insights, an attempt was made, according to the laws of error calculation, to indicate an upper limit for the differences in average voltage values of black and/or white pixels which arise due to voltage level inaccuracies. The result is the so-called D formula:

$$D = \frac{V1 - 2V2 + V3 - V4 + 2V5 - V6}{2} \quad (3)$$

[0024] The quantity D may be understood to be a "quality parameter" characterizing the quality of the voltage levels overall. According to the invention, crosstalk is reduced by varying or fine-tuning of one of the voltage levels V2, V3, V4 or V5 in order to minimize the absolute value |D|. In other words, one of the voltage levels is varied until the measured quality parameter value D lies within a specified quality interval: $|D| < D_G$. As a means of fine-tuning of the one voltage level, analog multiplexers are preferably used, which consist merely of a series of N-channel MOS switches and are therefore particularly simple and compact. The resulting resistance of the resistor chain is not changed by such a variation in voltage level. The voltage level V5 or V2 is preferably varied; it will be noted that the D formula (3) is (anti)symmetrical relative to the voltages V2, V5. Variation of V2 or V5 has the greatest effect on the quality parameter D, because these voltages are multiplied in the D formula (3) by a factor of 2; moreover, variation of V2 or V5 also has practical advantages as far as the design of the circuit is concerned.

[0025] These and further aspects of the invention will be clarified with reference to the embodiments described below.

[0026] The invention will be further described with reference to embodiments shown in the drawings to which, however, the invention is not restricted.

[0027] FIG. 1 is a schematic diagram of six voltage levels V1 to V6 and a column voltage waveform typical of commercial liquid crystal display devices.

[0028] FIG. 2 is a schematic representation of a circuit diagram of part of the circuit arrangement according to the invention.

[0029] FIG. 3 shows a schematic plan view of part of the layout of the circuit arrangement according to the invention.

[0030] FIG. 4 shows a flow chart of the calibration method according to the invention.

[0031] A schematic circuit diagram of part of the circuit arrangement according to the invention, namely of the voltage divider 1, is shown in FIG. 2. The voltage divider 1 comprises a chain of, for example, five series-connected resistors R1-R5. To a first end 11 of the resistor chain there is applied a voltage V1, to a second end 12 a voltage V6, wherein the second end is preferably applied to ground Gnd (i.e. grounded, $V6=0$) and V1 is identical to V1cd, the operating voltage of the liquid crystal display device. Between the resistors R1-R5, voltage pick-offs 22-25 are arranged for picking off different voltage levels V2-V5. Thus, a voltage level $V2 < V1$ is picked off at a voltage pick-off 22 between the resistors R1 and R2, a voltage level $V3 < V2$ is picked off at a voltage pick-off 23 between the resistors R2 and R3, etc. A single one 25 of the voltage pick-offs 22-25 is so designed that the voltage level picked off there, in the present example V5, is capable of fine-tuning.

[0032] Means 3 for fine-tuning of the one voltage level V5 may, for example, take the form of a plurality of pick-off contacts on a resistive path. FIG. 3 shows an embodiment comprising eight equidistant pick-off contacts 31-38 in a resistive path 45. The position of this group 3 of eight pick-off contacts 31-38 in the path 45 may vary, depending on which voltage level system is selected. A voltage level system is characterized by the ratio $V5/V1$, which may typically assume the values $1/4, 1/5, \dots, 1/11$. A plurality of groups of pick-off contacts could also be provided in the path 45, wherein each group is associated with a voltage level system, such that a particular voltage level system may be selected by selecting a particular group.

[0033] All the elements of the circuit arrangement are preferably accommodated on a common substrate, such that the circuit arrangement is an integrated circuit. The resistors R1-R5 may be produced, for example, by means of implanted strips 41-45 of semiconductor material of a first conductivity type, for example p^+ , in a semiconductor material of a second conductivity type, for example n ; other examples are n^+ or n^- in p^- or Poly-Si. It should be noted, in this case, that a resistor need not correspond exactly to one strip; rather, a resistor in the sense used here is defined by the two pick-offs which delimit it. Thus, the variable resistor R5 in the example of FIG. 3 is delimited by one of the pick-off contacts 31-38 on the one hand and the grounding contact 12 on the other hand, such that it comprises part of the strip 45 and the entire strip 46.

[0034] It will be explained below, with reference to an example, how the number and spacing of the pick-off contacts 31-38 may be selected. A liquid crystal display device is considered, the liquid crystal of which has a transition region with a width of 200 mV. For the purpose of simplification, it is assumed that the characteristic curve extends in linear manner in the entire transition region, i.e. its slope has a constant incline of $-1/(200 \text{ mV})$. Differences in the transmittance of two pixels of more than approx. 2% are known to be visible to the eye. Consequently, the real transmittances of two pixels with the same nominal transmittance should differ by 2% at most, which corresponds to a voltage difference of at most 4 mV (2% of 200 mV) or a quality interval $(-D_Q, +D_Q)$ with $D_Q=4 \text{ mV}$. To ensure that the quality parameter D comes to lie within the quality interval $(-D_Q, +D_Q)$, the spacing of the pick-off contacts 31-38 has thus to be selected in such a way that the voltage difference $\Delta V=2D_Q=8 \text{ mV}$ is applied between two pick-off contacts. In the case of eight pick-off contacts 31-38, the quality parameter D may thus be varied within a range of from $7\Delta V=56 \text{ mV}$, which is sufficient for most applications. In this embodiment with eight pick-off contacts 31-38, 3 bits are necessary in order to store the optimum fine-tuning. Of course, other configurations are possible, for example a 4-bit calibration with 16 pick-off contacts, between which a voltage difference $\Delta V=4 \text{ mV}$ is in each case present.

[0035] As the right-hand half of FIG. 2 shows symbolically, each pick-off contact 31-38 is connected to a respective input 51-58 of a static analog multiplexer 5, which consists, for example, of a series of N-channel MOS switches and is therefore particularly simple. The multiplexer 5 is preferably controlled by a read-only memory programmable once or repeatedly (such as, for example, one-time programmable read-only memory, OTP; programmable read-only memory, PROM; erasable programmable read-only memory, EPROM; electrically erasable programmable read-only memory, EEPROM, etc.). This has the task of storing an optimum fine-tuning for the voltage level V5, once found, i.e. of connecting the respectively optimum pick-off contact to the output 25' of the voltage pick-off 25 for V5.

[0036] FIG. 4 shows a flow chart of the calibration method according to the invention. To begin with, a suitable voltage level system 91 (cf. explanations relating to FIG. 3) and a suitable operating voltage V1, 92, for example $V1=9 \text{ V}$, are selected. A calibration parameter P is set to an initial value P(0), 93. The calibration parameter P characterizes the current fine-tuning of the variable voltage level V5. In the embodiment in FIG. 3, P may thus be a number between 0 and 7, which indicates which of the eight pick-off contacts 31-38 is currently connected to the output 25' of the voltage pick-off 25 for V5, this number being preferably stored in binary or hexadecimal representation. As an initial value P(0), that value is preferably selected with which the equidistance condition (2) would be fulfilled in the ideal case. A running variable n ($n=0, 1, 2, \dots$) (used purely internally for the subsequent loop 95-98) is set initially to zero, 94.

[0037] An iteration loop 95-98 is now run through one or more times, in which the calibration parameter P is recursively optimized with reference to the quality parameter D. To this end, the current value D(n) of the quality parameter D is firstly determined, 95, by measuring the current voltages V1-V6 and inserting them in the D formula (3). The current value D(n) is examined, 96, as to whether it lies within a specified quality interval $(-D_Q, +D_Q)$, wherein, for

example, $D_Q=2 \text{ mV}$ may be selected. If this is the case, the current calibration parameter P(n) is written to a calibration register, 99, for example stored in an OTP ROM. If D(n) does not lie in the quality interval, a new calibration parameter P(n+1) is calculated recursively from the old calibration parameter P(n), 97. This may be performed for example according to the formula

$$P(n+1) := P(n) - \text{rnd}[D(n) \cdot V1_{\text{nom}} / (\Delta V \cdot V1)] \quad (4)$$

[0038] wherein ΔV is a voltage interval width at a nominal operating voltage $V1_{\text{nom}}$, for example, $\Delta V=4 \text{ mV}$ at $V1_{\text{nom}}=9 \text{ V}$, and the operator $\text{rnd}[X]$ effects rounding of the operand X to the next whole number. The operand X in the square brackets in equation (4) essentially indicates the number of pick-off contacts by which the fine-tuning setting has to be changed in an iteration step. It is composed of the factors $D(n)/\Delta V$ and $V1_{\text{nom}}/V1$, wherein the latter factor is a correction with which it is intended to scale the voltage interval width ΔV with V1. After calculation 97 of the new calibration parameter P(n+1), the running variable n is increased by one, 98, and the iteration loop 95-98 is run through again. This is repeated until the current quality parameter value D(n) lies in the specified quality interval $(-D_Q, +D_Q)$.

[0039] The above-described calibration is performed once for each individual circuit by the circuit manufacturer or by the manufacturer of the liquid crystal display device. In the latter case, a special probe for contacting the electrodes on the glass plates could be used, or the different voltage levels V1-V6 could be connected one after the other to a particular output contact. All the voltage measurements required for calibration should be measured across the highest possible load impedance, in order not to falsify the measured values.

[0040] The circuit arrangement according to the invention and the calibration method according to the invention reduce crosstalk of pixels to an acceptable degree. These advantages come into their own especially in the case of display devices with gray-stage display or color display devices. The circuit arrangement is of a simple construction and is space- and power-saving.

1. A circuit arrangement for the voltage supply of the row and column drivers of a liquid crystal display device, comprising a voltage divider (1) having a plurality of series-connected resistors (R1-R5) and having voltage pick-offs (22-25) arranged between the resistors (R1-R5) for picking off different voltage levels (V2-V5), wherein a single one (25) of the voltage pick-offs (22-25) is provided with means (3) for fine-tuning of the voltage level (V5) picked off there.

2. A circuit arrangement as claimed in claim 1, wherein the fine-tuning means (3) comprise a plurality of pick-off contacts (31-38) and means (5) for selecting a pick-off contact.

3. A circuit arrangement as claimed in claim 2, wherein the selection means (5) take the form of an analog multiplexer, the inputs (51-58) of which are connected to the pick-off contacts (31-38).

4. A circuit arrangement as claimed in claim 3, wherein the circuit arrangement comprises a once or repeatedly programmable read-only memory for controlling the multiplexer (5).

5. A circuit arrangement as claimed in any one of the preceding claims, wherein the voltage pick-off (25) provided with the fine-tuning means (3) is one of the two voltage pick-offs (22, 25) which lie closest to the two ends (11, 12) of the voltage divider (1).

6. A circuit arrangement as claimed in any one of the preceding claims, wherein the voltage divider (1) comprises precisely four voltage pick-offs (22-25).

7. A circuit arrangement as claimed in any one of the preceding claims, wherein all the elements of the circuit arrangement are accommodated on a common substrate.

8. A circuit arrangement as claimed in claim 7, wherein the resistors (R1-R5) are produced by means of implanted strips (41-46) of semiconductor material of a first conductivity type (p⁺) in a semiconductor material of a second conductivity type (n).

9. A liquid crystal display device comprising a liquid crystal layer, row and column drivers, and a circuit arrangement for the voltage supply of the row and column drivers, wherein the circuit arrangement is a circuit arrangement as claimed in any one of the preceding claims.

10. A method of calibrating a circuit arrangement as claimed in any one of the claims 1 to 8, comprising the following steps:

- (a) selection (93) of an initial fine-tuning;
- (b) measurement (95) of the value (D(n)) of a quality parameter (D) characterizing the voltage level overall (V1-V6);
- (c) establishing (96) whether the measured quality parameter value (D(n)) lies within a specified quality interval (-D_O, +D_O);

(d) if the result (96) of step (c) is negative: recursive determination (97) of a new fine-tuning (P(n+1)) and repetition of steps (b) and (c);

(e) if the result (96) of step (c) is positive: storage (99) of the current fine-tuning (P(n)).

11. A method as claimed in claim 10, wherein a first operating voltage V1 is applied to one end (11) of the voltage divider (1) and a second operating voltage V6 to the other end (12) of the voltage divider (2), the voltage divider (1) comprises four voltage pick-offs (22-25) for picking off four voltage levels (V2, V3, V4, V5), and the quality parameter (D) is defined in step (b) by

$$D = \frac{V1 - 2V2 + V3 - V4 + 2V5 - V6}{2}.$$

12. A method as claimed in claim 11, wherein the fine-tuning relates to the voltage level V2 or V5.

13. A method as claimed in any one of the claims 10 to 12, wherein the quality interval (-D_O, +D_O) in step (c) is selected such that, for quality parameter values (D(n)) lying within this quality interval (-D_O, +D_O), the real transmittances of two pixels with the same nominal transmittance differ by at most 2%.

14. A method as claimed in any one of the claims 10 to 13, wherein the fine-tuned setting (P(n)) is stored (99) in a once or repeatedly programmable read-only memory.

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专利名称(译)	用于液晶显示装置的电压供应的电路装置		
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摘要(译)

该电路装置用于液晶显示装置的行和列驱动器的电压供应。它包括分压器(1)，该分压器具有多个串联连接的电阻器(R1-R5)并且具有布置在电阻器(R1-R5)之间的电压传感器(22-25)，用于拾取不同的电压电平(V2-V5)。单个(25)电压传感器(22-25)设有装置(3)，用于微调从那里拾取的电压电平(V5)。通过一次单独校准每个单独的电路装置，可以微调一个电压电平(V5)，使得由不对称电压电平(即像素内容的相互作用)引起的串扰减小。特别是当它用于具有灰阶显示器或彩色显示器的液晶显示器件时，电路装置的优点逐渐形成。

