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Kim et al.

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(45) **Date of Patent: *Jun. 21, 2011**

(54) **LIQUID CRYSTAL DISPLAY**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

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(30) **Foreign Application Priority Data**

Mar. 6, 2003 (KR) 10-2003-0014017

(51) **Int. Cl.**
G02F 1/136 (2006.01)
G02F 1/1343 (2006.01)

(52) **U.S. Cl.** **349/43**; 349/42; 349/139

(58) **Field of Classification Search** 349/139, 349/42–43, 143
See application file for complete search history.

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(74) *Attorney, Agent, or Firm* — Cantor Colburn LLP

(57) **ABSTRACT**

A pixel electrode and a direction control electrode capacitively coupled to the pixel electrode are provided in a pixel. A pixel thin film transistor is connected to a gate line, a data line, and the pixel electrode. A direction control electrode thin film transistor is connected to a previous gate line, a previous data lines or a next data line, and the direction control electrode. The gate lines are supplied with scanning signals, and each scanning signal includes first and second pulses in a frame. The first pulse of a scanning signal is synchronized with the second pulse of a previous scanning signal.

4 Claims, 31 Drawing Sheets

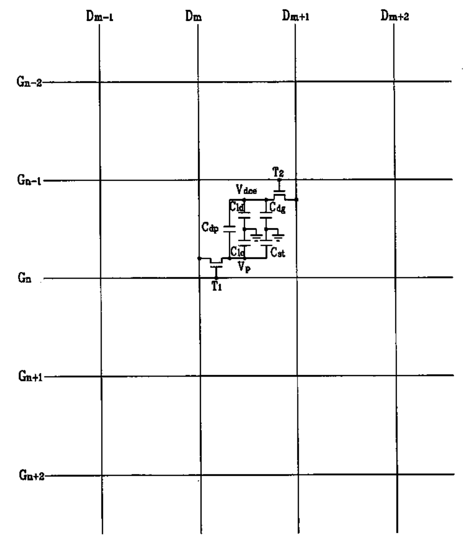
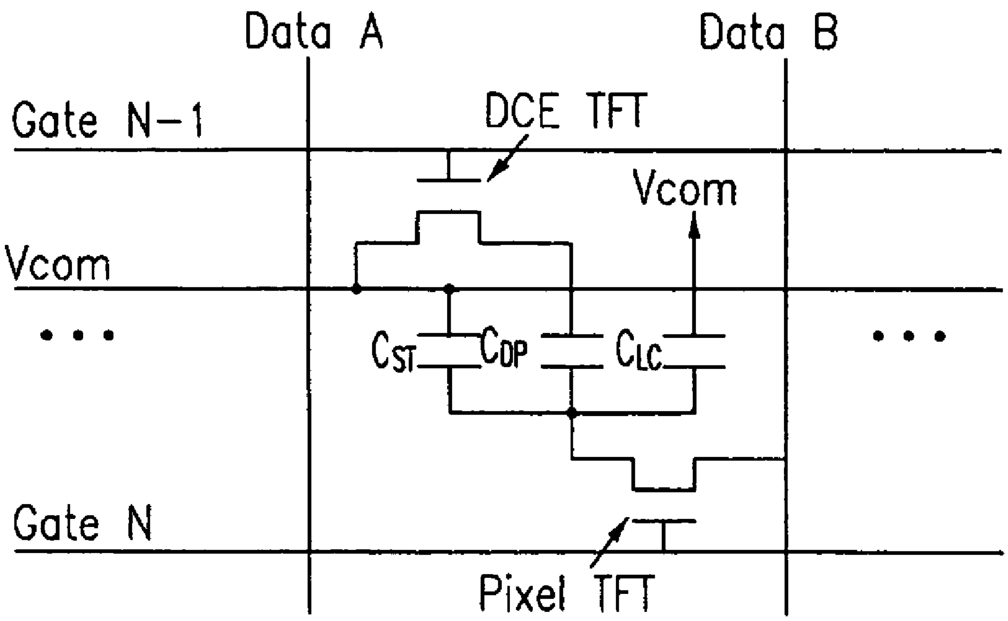


FIG.1



Data A
Data B
Gate N-1
DCE TFT
Vcom
Vcom
CST
CDP
CLC
Gate N
Pixel TFT

FIG.2A

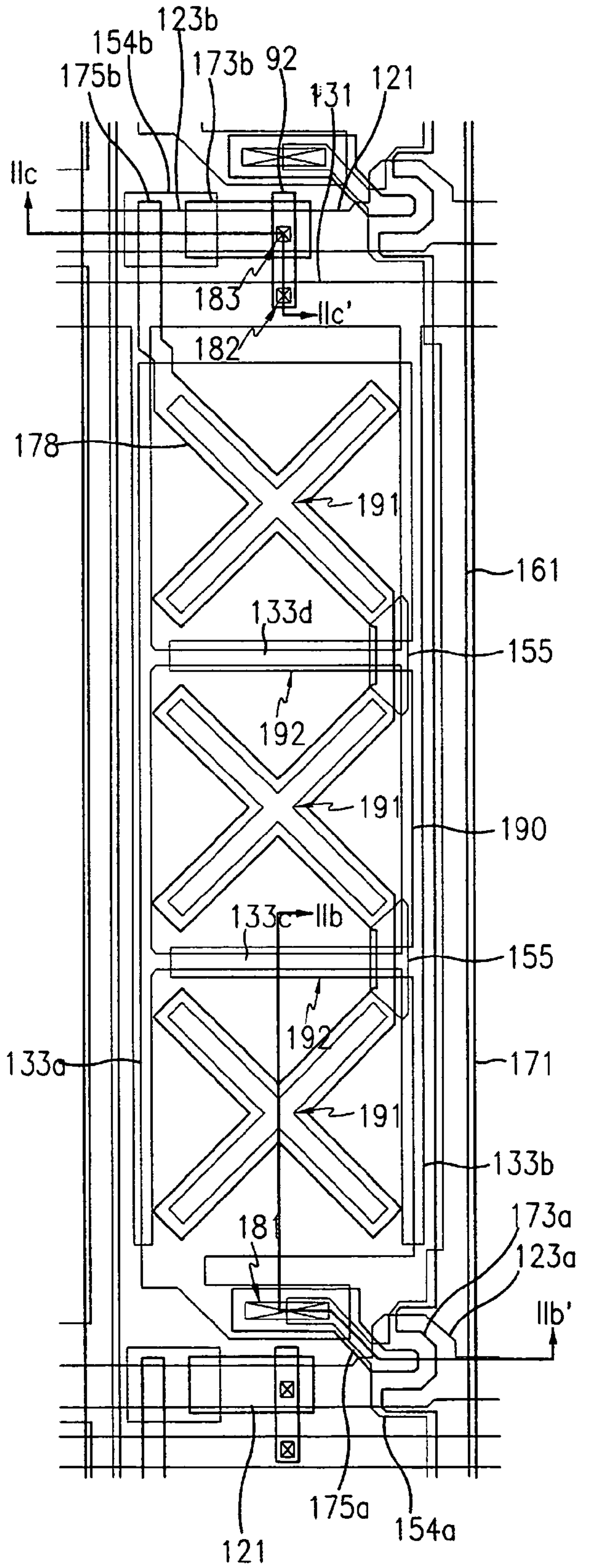
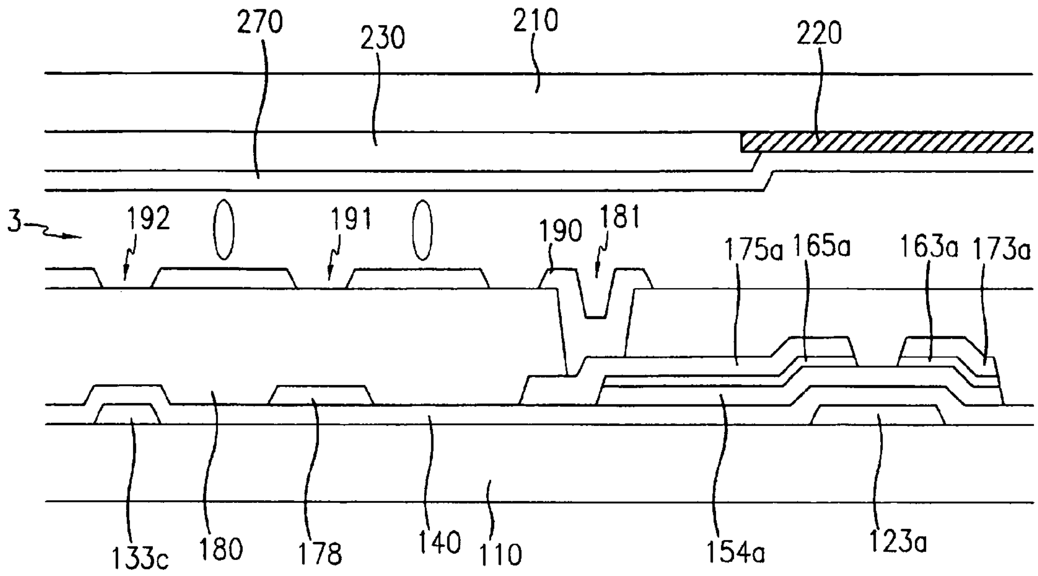
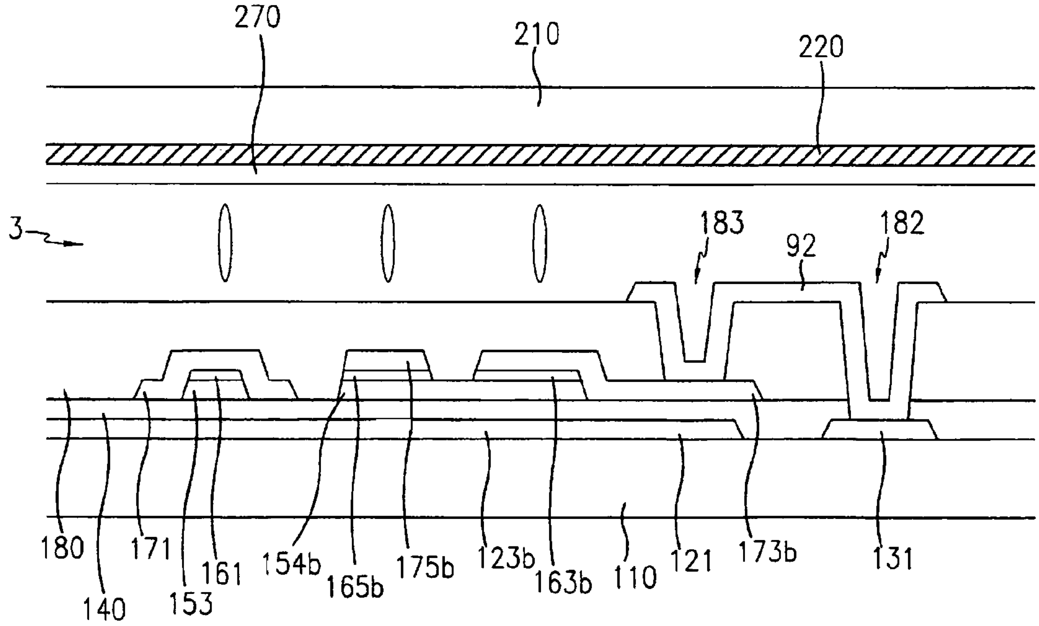

123b
154b
173b
92
175b
131
121
IIc
183
IIc'
182
178
191
161
133d
155
192
191
190
133c
IIb
155
192
133a
171
191
133b
181
173a
123a
IIb'
121
175a
154a

FIG.2B



도 2c

FIG.2C



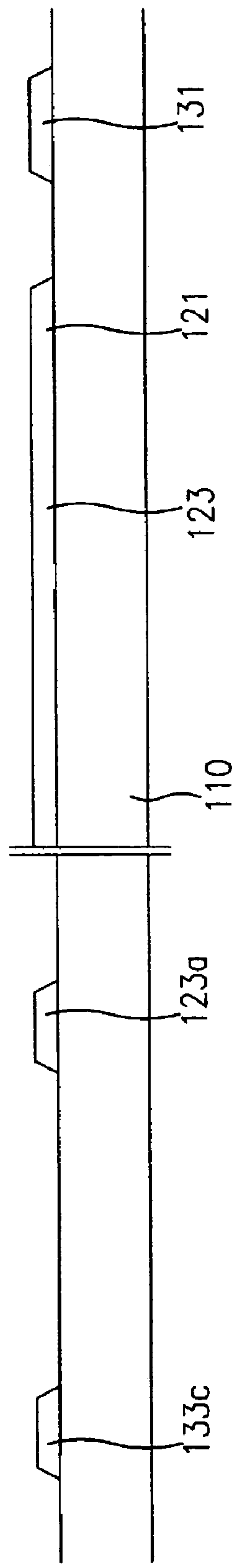


FIG.3A

FIG.3B

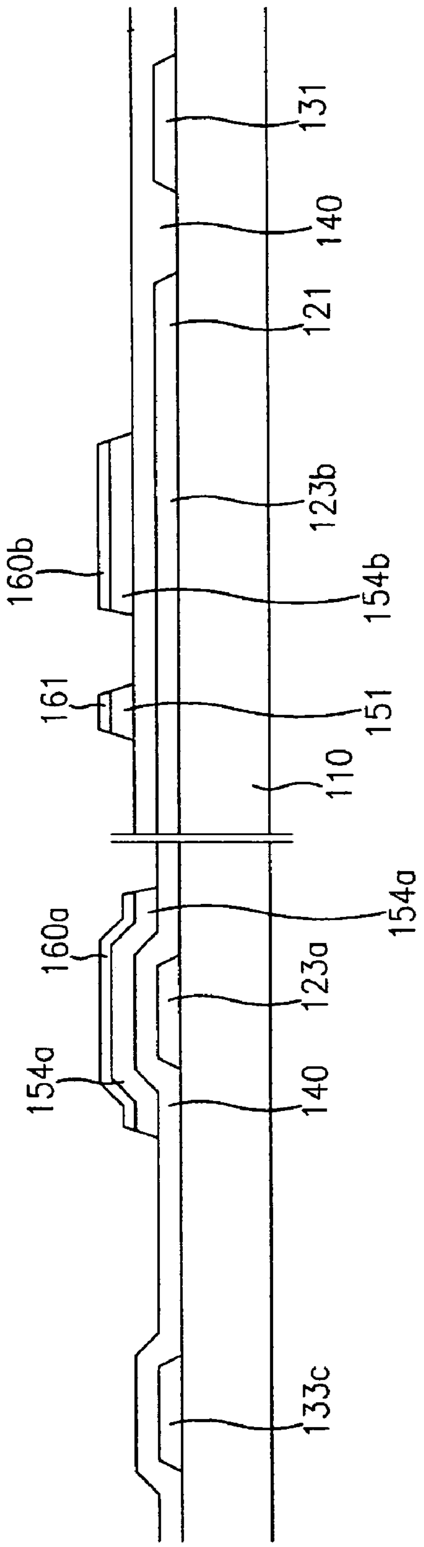

131
140
121
123b
160b
154b
161
151
110
154a
160a
123a
154a
140
133c

FIG.3C

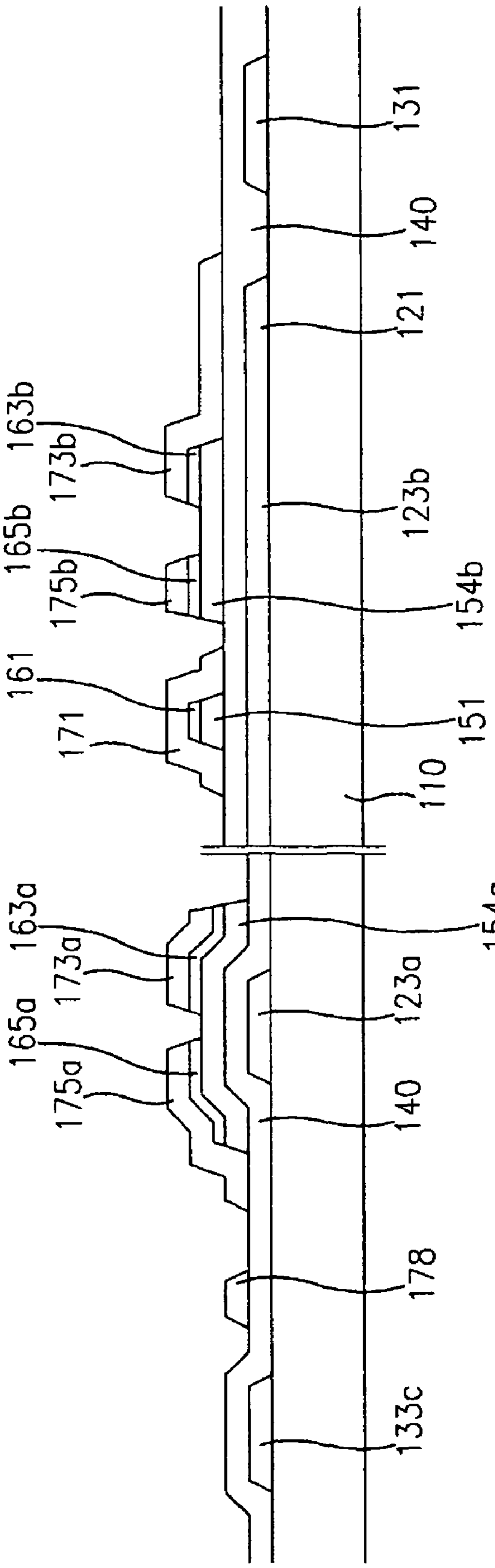

131
140
121
163b
173b
123b
165b
175b
154b
161
171
151
110
163a
173a
154a
123a
165a
175a
140
178
133c

FIG.3D

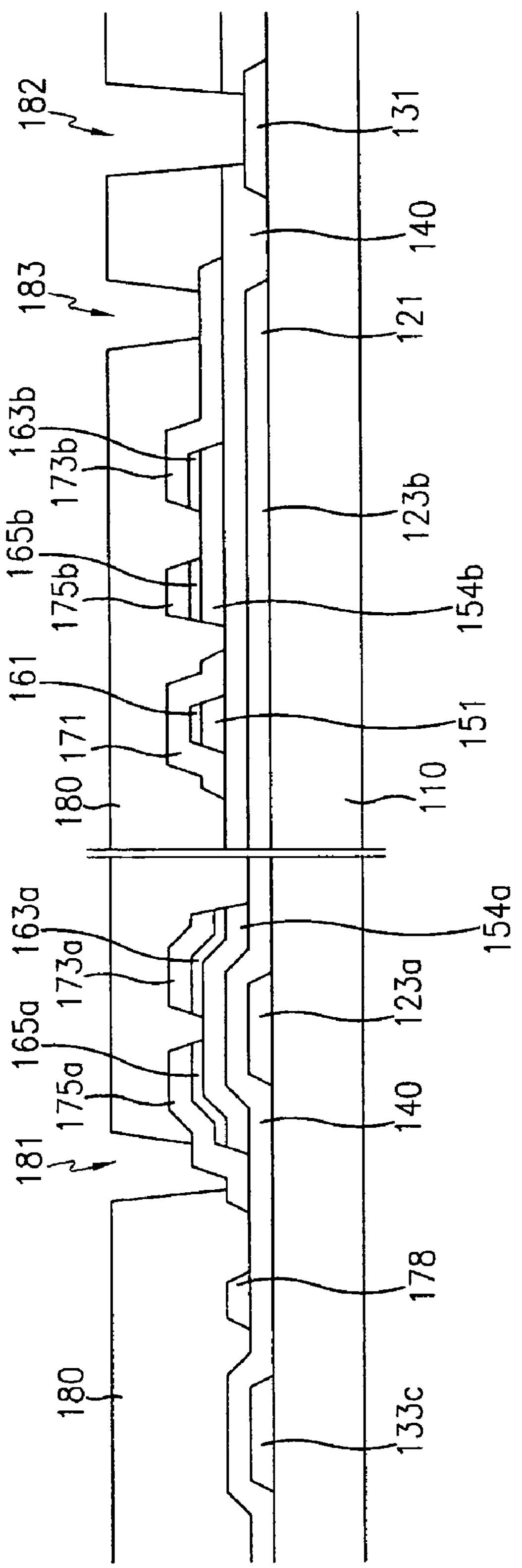

182
131
140
183
121
163b
173b
123b
165b
175b
154b
161
171
151
180
110
163a
173a
154a
165a
123a
175a
140
181
178
180
133c

FIG.4

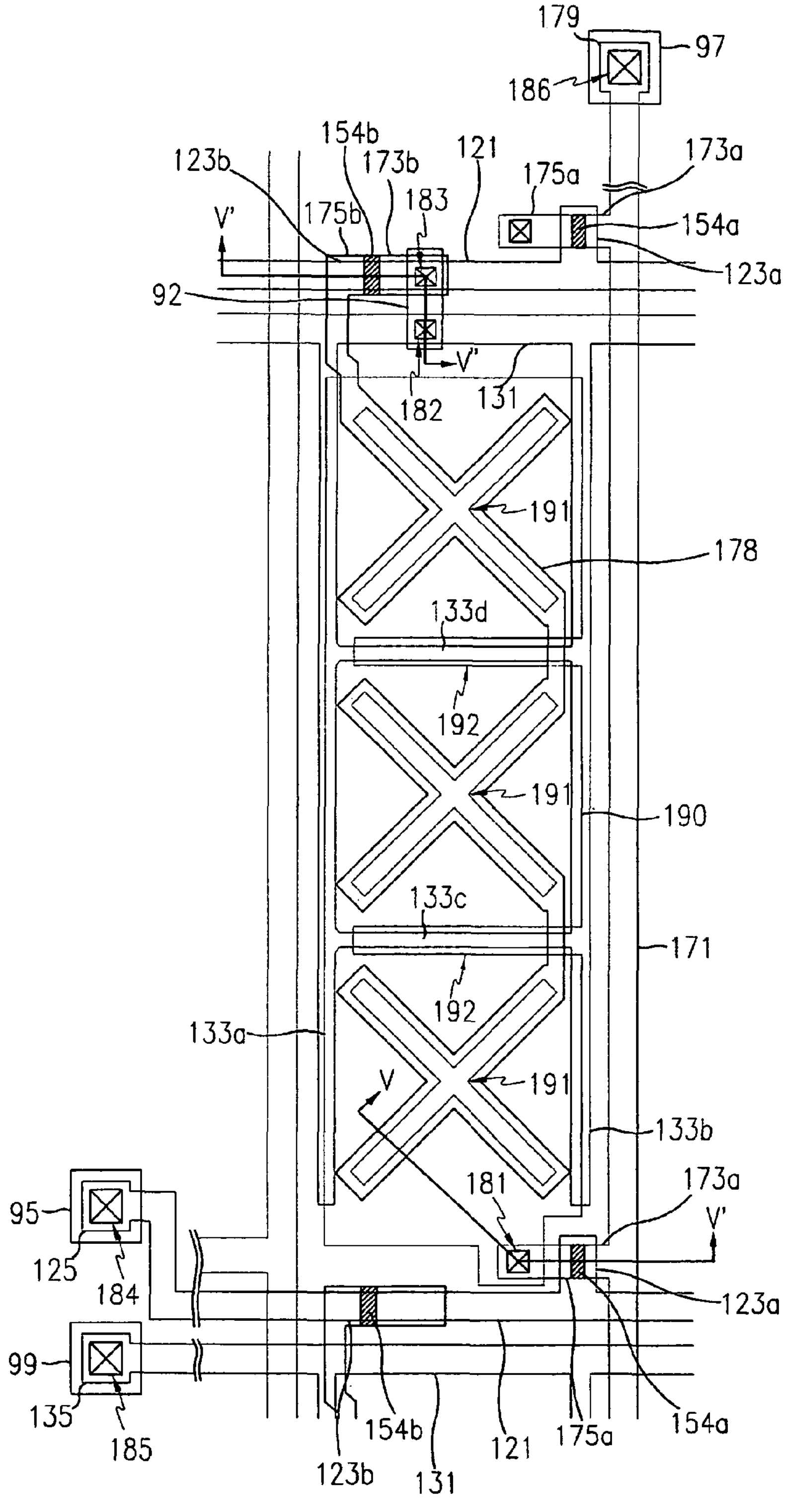

179
97
186
154b
173b
121
173a
123b
175a
183
154a
V'
175b
123a
92
V'
182
131
191
178
133d
192
191
190
133c
171
192
133a
191
V
133b
181
173a
V'
95
123a
125
184
99
135
185
154b
121
175a
154a
123b
131

FIG. 5

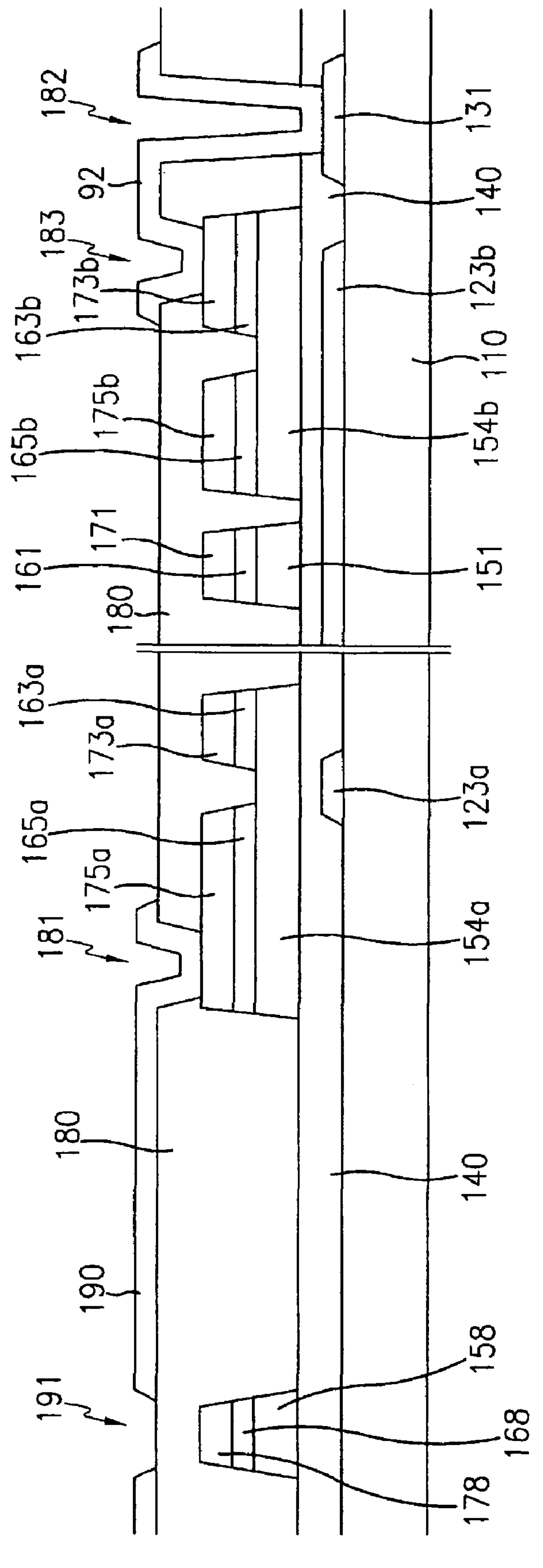
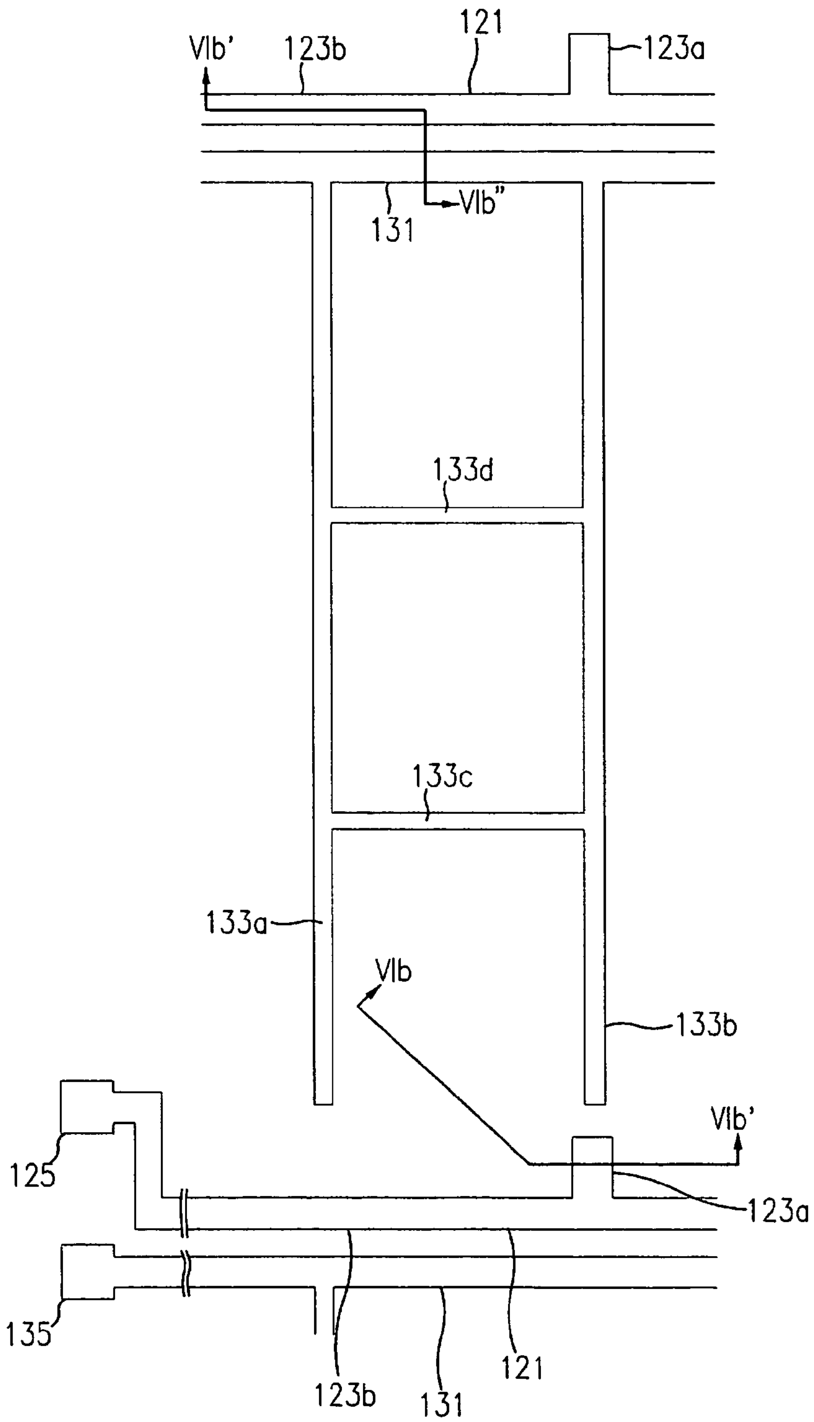

182
92
183
173b
163b
175b
165b
171
161
180
163a
173a
165a
175a
181
180
190
191
131
140
123b
110
154b
151
123a
154a
140
158
168
178

FIG.6A


121
VIb'
123b
123a
VIb"
131
133d
133c
133a
VIb
133b
VIb'
125
123a
135
123b
131
121

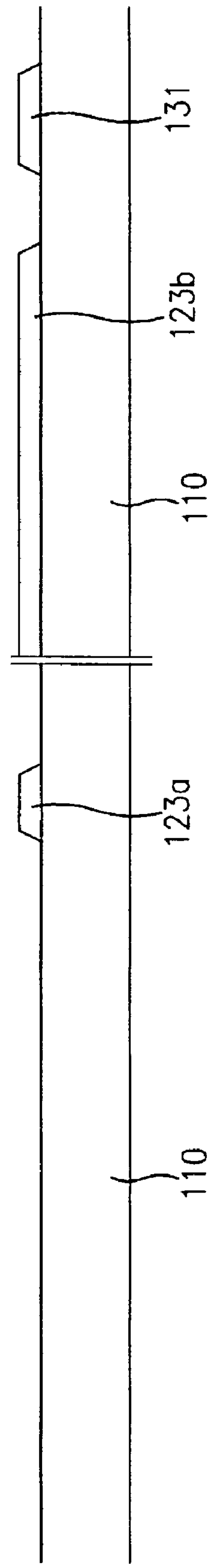


FIG.6B

FIG.7

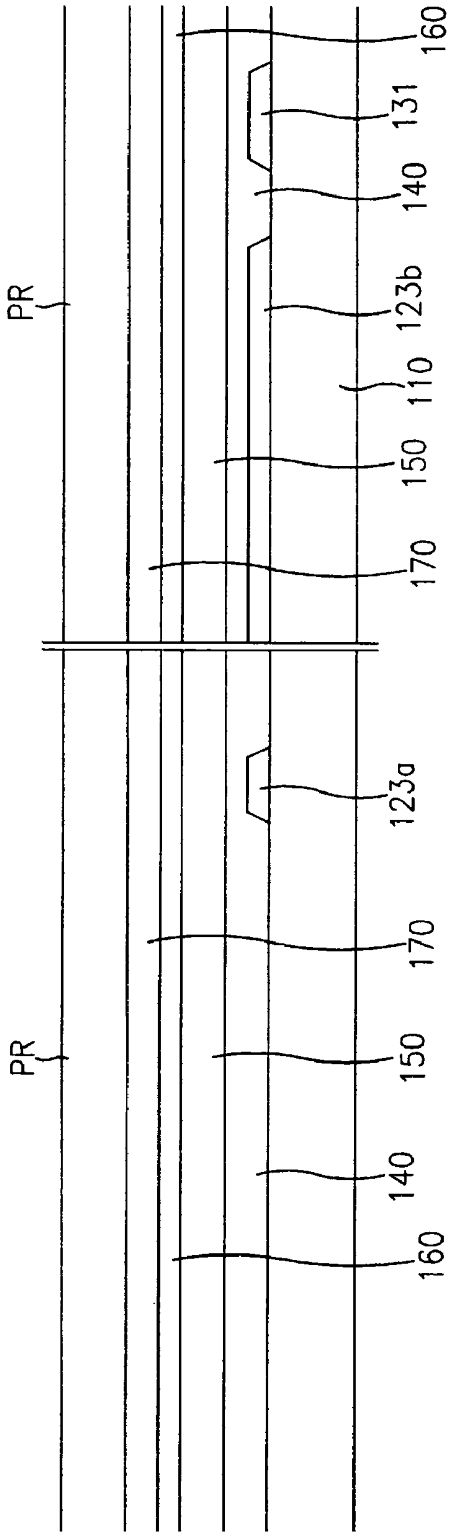


FIG.8A

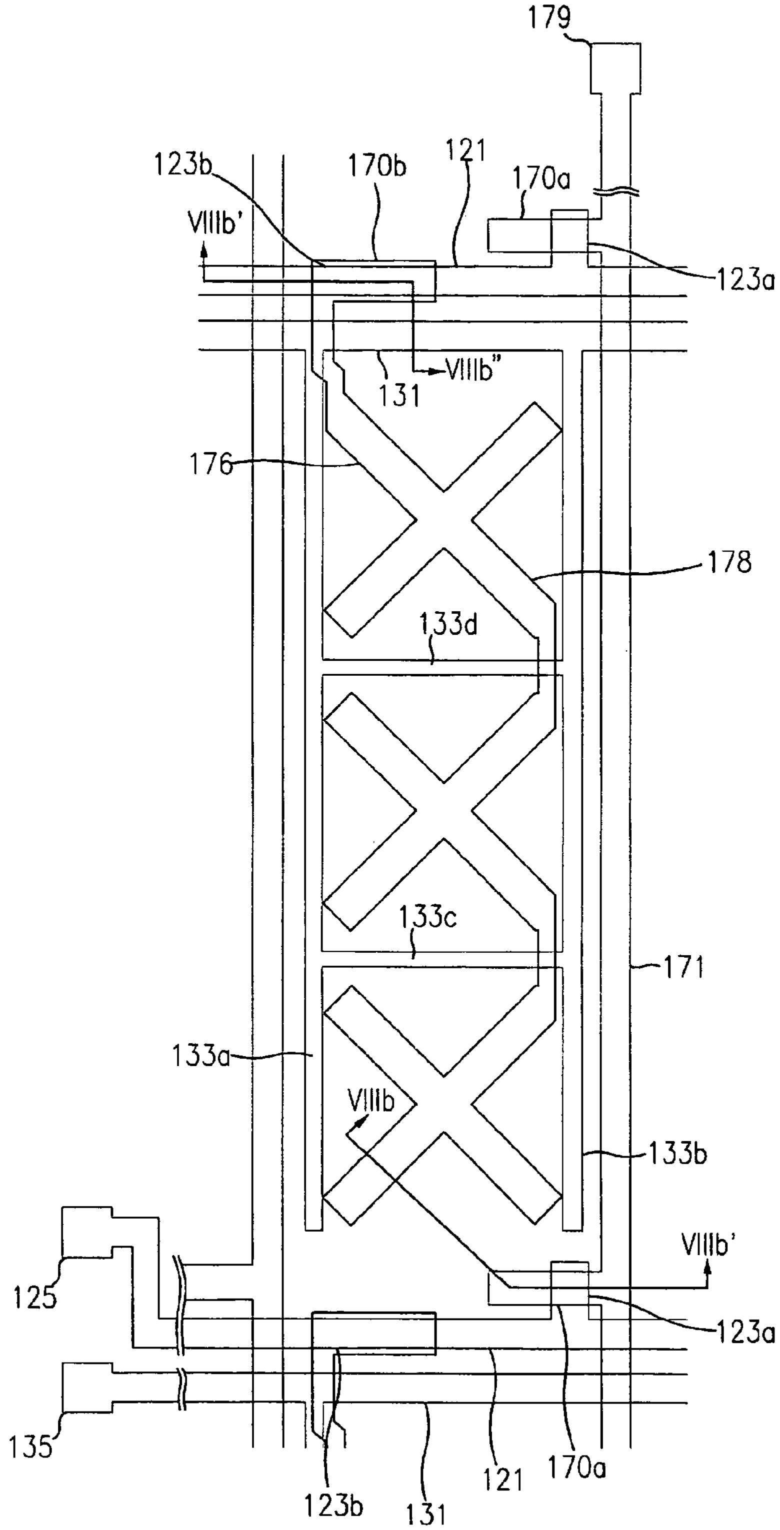

179
123b
170b
121
170a
VIIIb'
123a
131
VIIIb"
176
178
133d
133c
171
133a
VIIIb
133b
VIIIb'
125
123a
135
123b
131
121
170a

FIG.8B

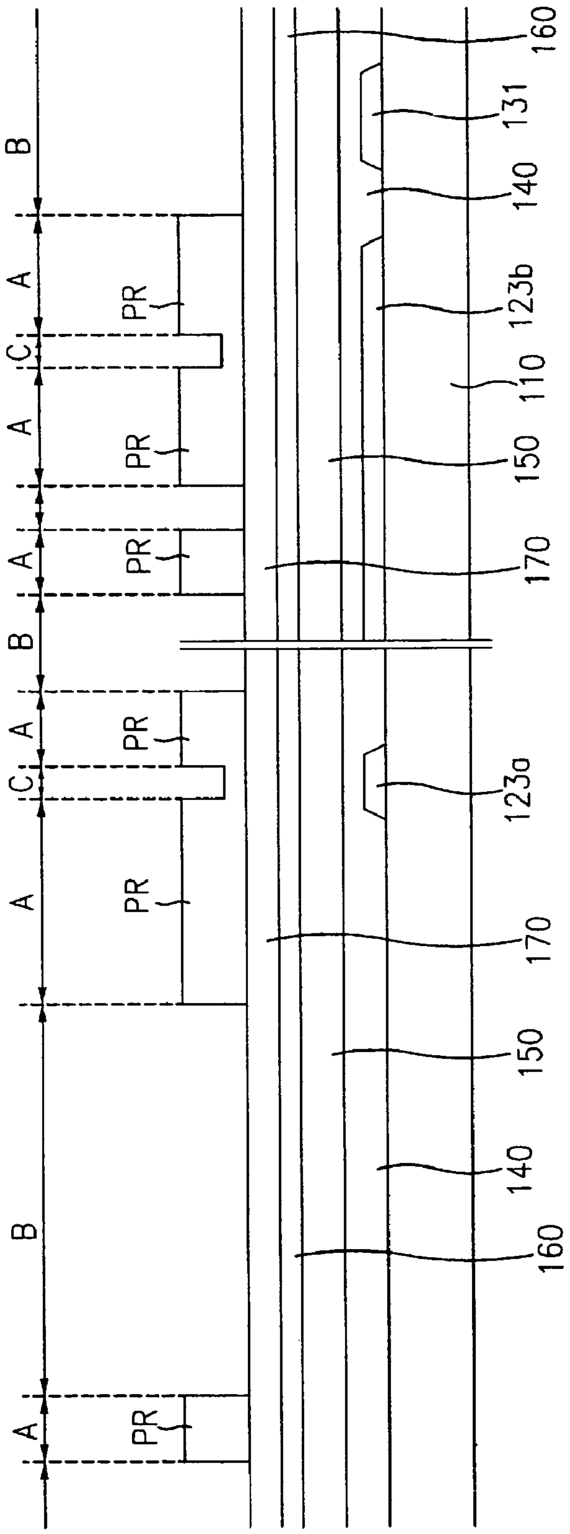

B
A
PR
C
A
PR
A
PR
B
A
PR
C
A
PR
B
A
PR
160
131
140
123b
110
150
170
123a
170
150
140
160

FIG. 9

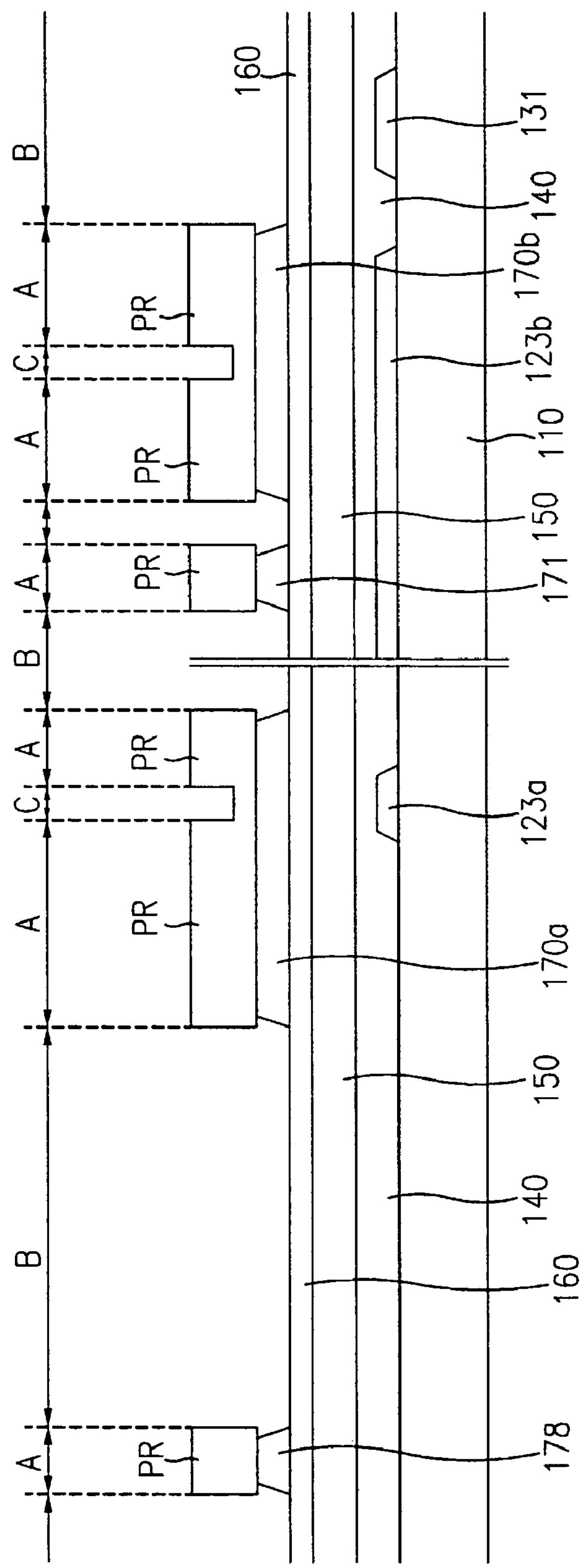


FIG.10

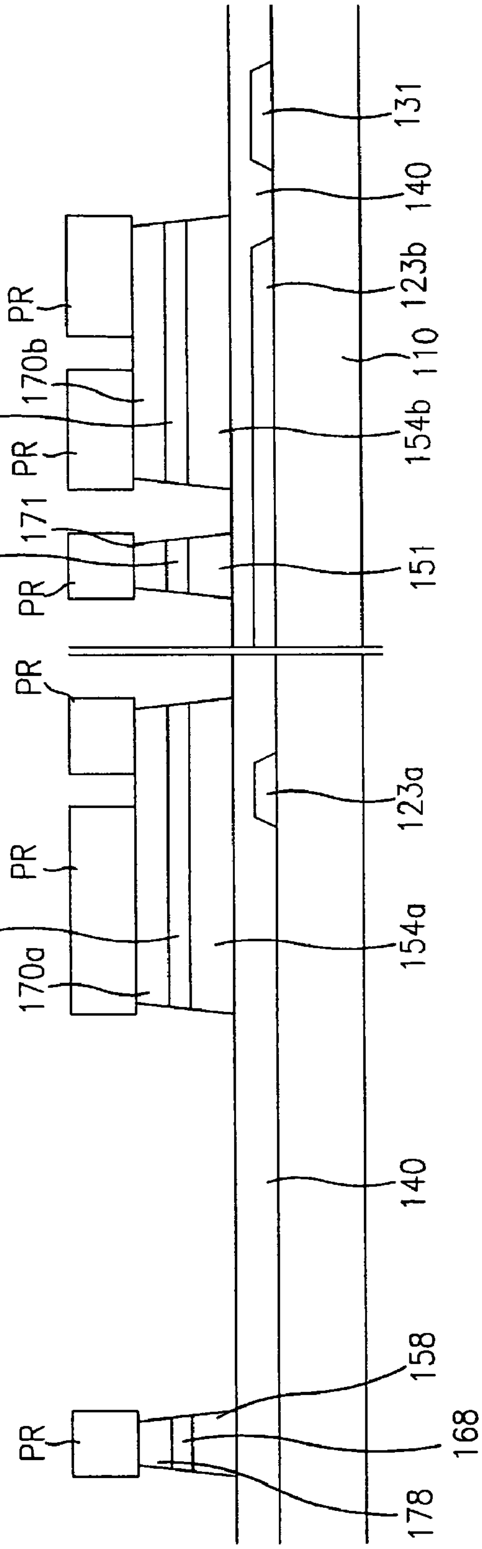
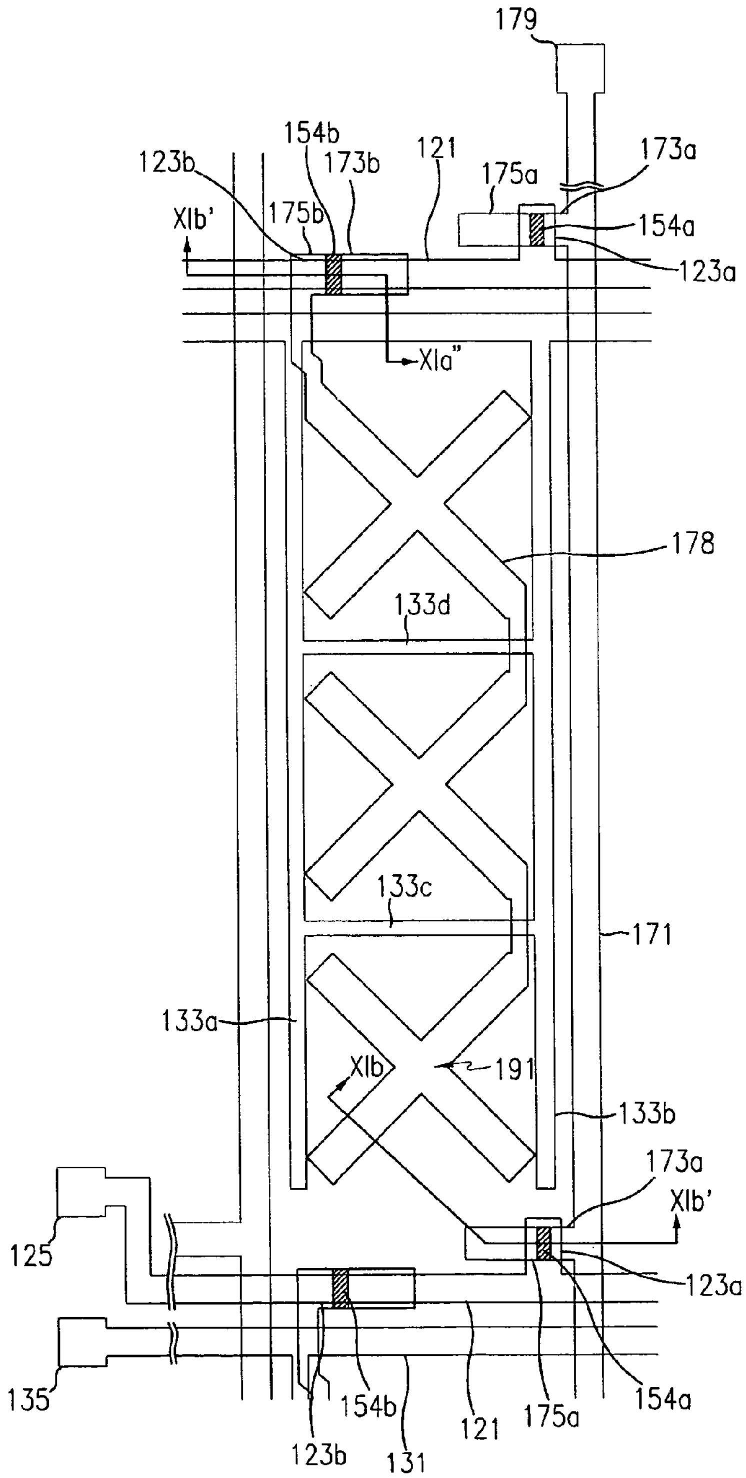

PR
170a
160a
154a
PR
123a
PR
161
171
151
PR
160b
170b
154b
PR
110
123b
140
131
140
PR
158
168
178

FIG.11A



179
154b
173b
121
173a
123b
175a
XIb'
175b
154a
123a
XIa"
178
133d
133c
171
133a
XIb
191
133b
173a
XIb'
125
123a
135
154b
121
175a
154a
123b
131

FIG.11B

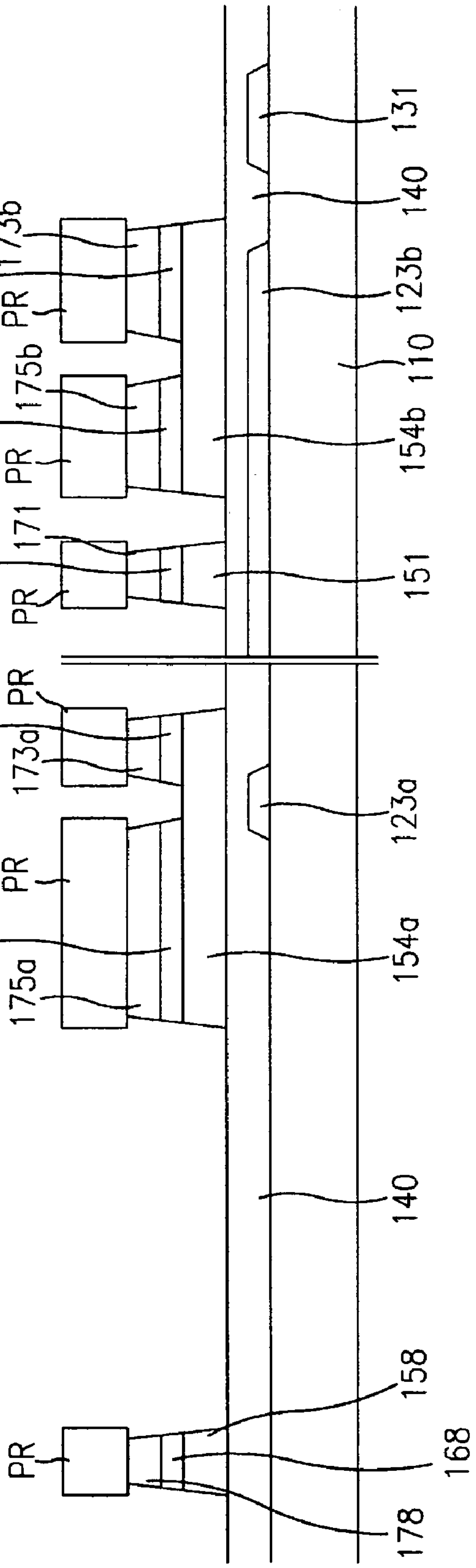

163b
173b
PR
165b
175b
PR
161
171
PR
PR
163a
173a
PR
165a
175a
PR
158
168
178
131
140
123b
110
154b
151
123a
154a
140

FIG.12

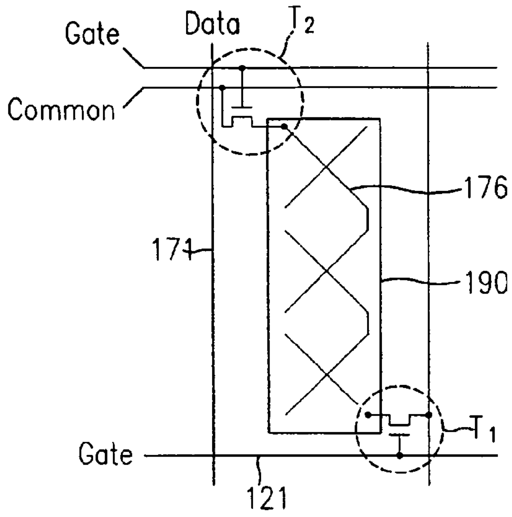

Gate
Data
T2
Common
176
171
190
T1
Gate
121

FIG.13

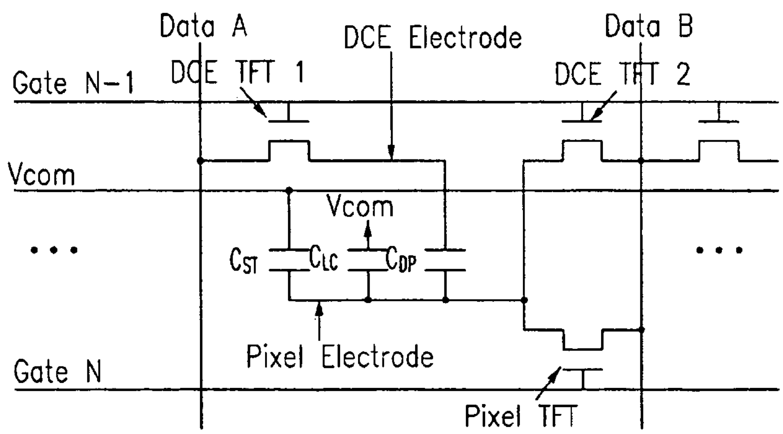
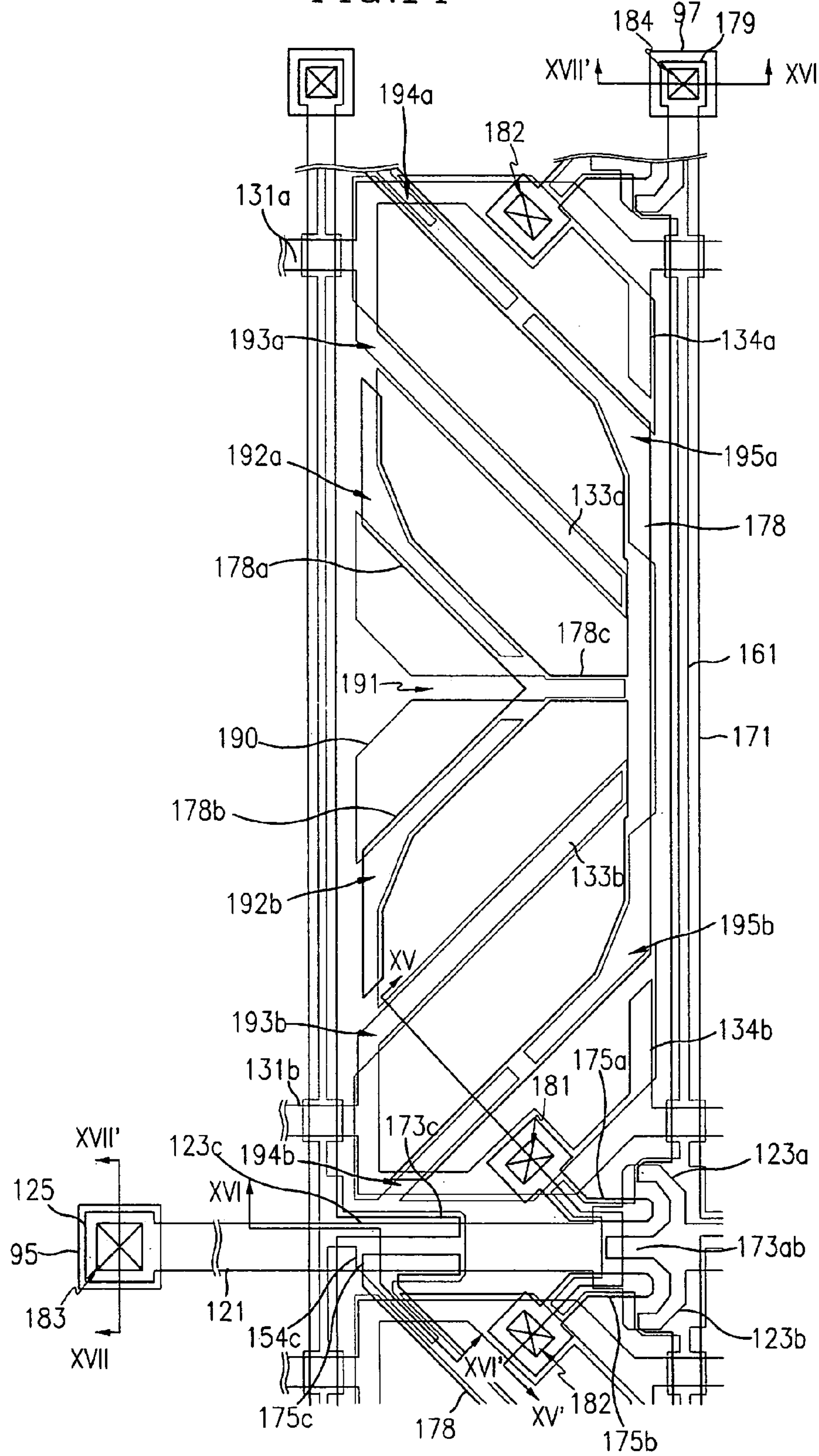
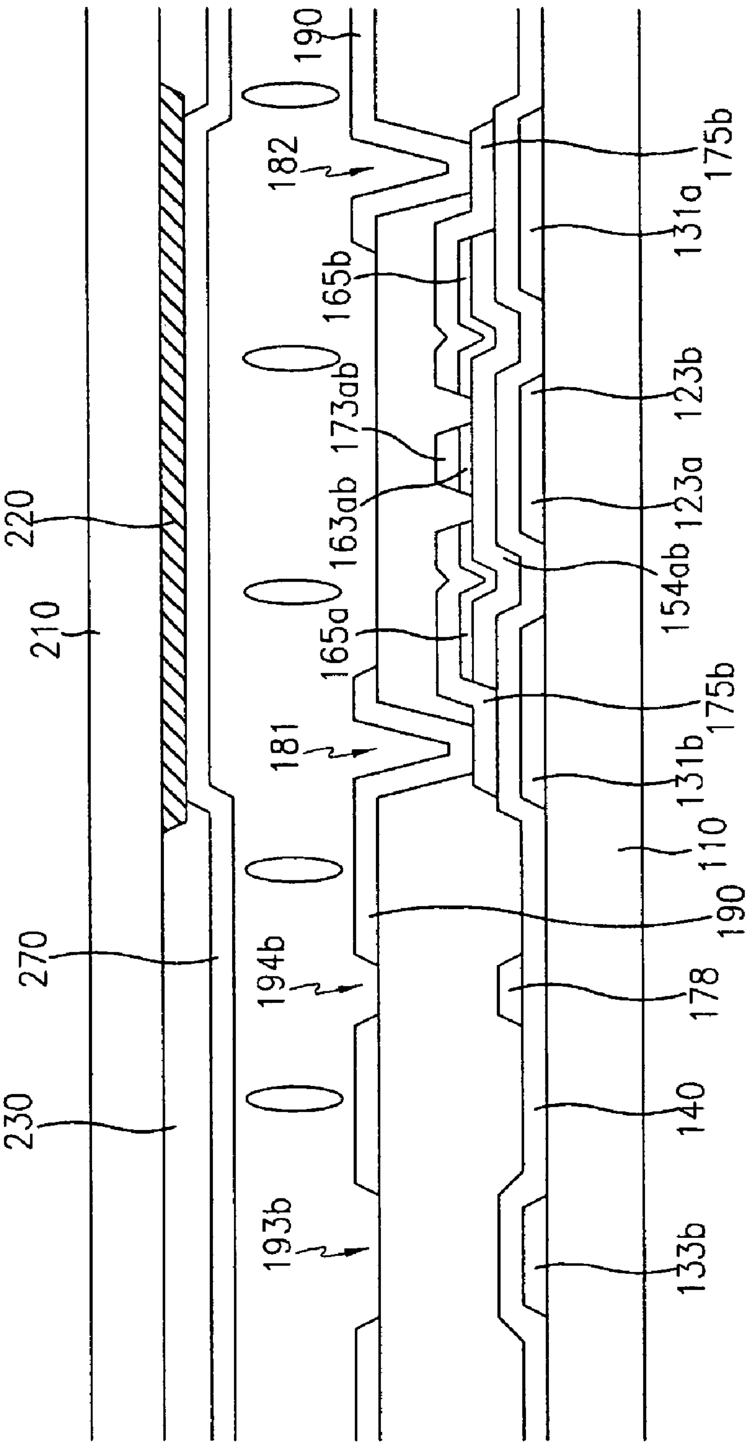

Data A
DCE Electrode
Data B
Gate N-1
DCE TFT 1
DCE TFT 2
Vcom
Vcom
CST
CLC
CDP
Pixel Electrode
Gate N
Pixel TFT

FIG.14



184
97
179
XVII'
XVII"
194a
182
131a
193a
134a
192a
195a
133a
178
178a
178c
161
191
190
171
178b
133b
192b
195b
XV
193b
134b
175a
131b
181
173c
123c
194b
123a
XVII'
XVI
125
173ab
95
121
183
154c
123b
XVI'
182
XVII
175c
178
XV'
175b

FIG.15



220
210
270
230
190
182
165b
173ab
163ab
165a
181
194b
193b
175b
131a
123b
123a
154ab
131b
110
178
140
133b

FIG.16

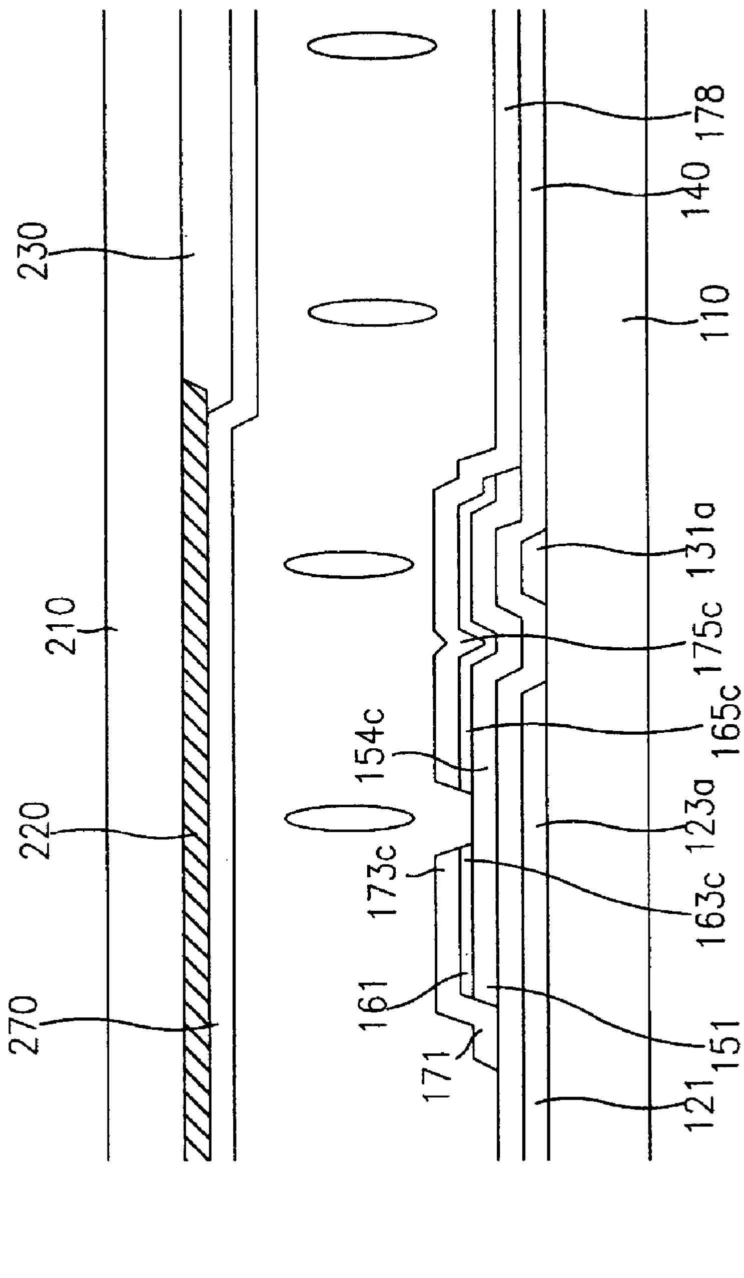

230
210
220
270
178
140
110
131a
175c
165c
154c
123a
163c
173c
161
151
171
121

FIG.17

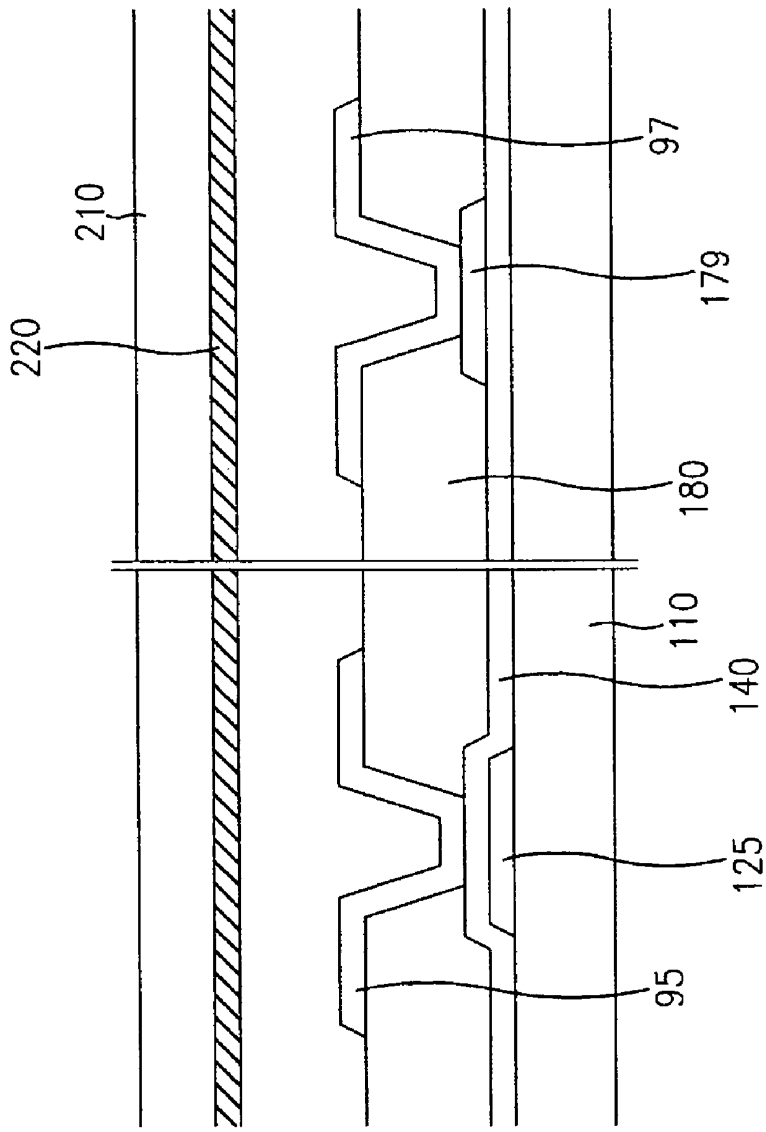
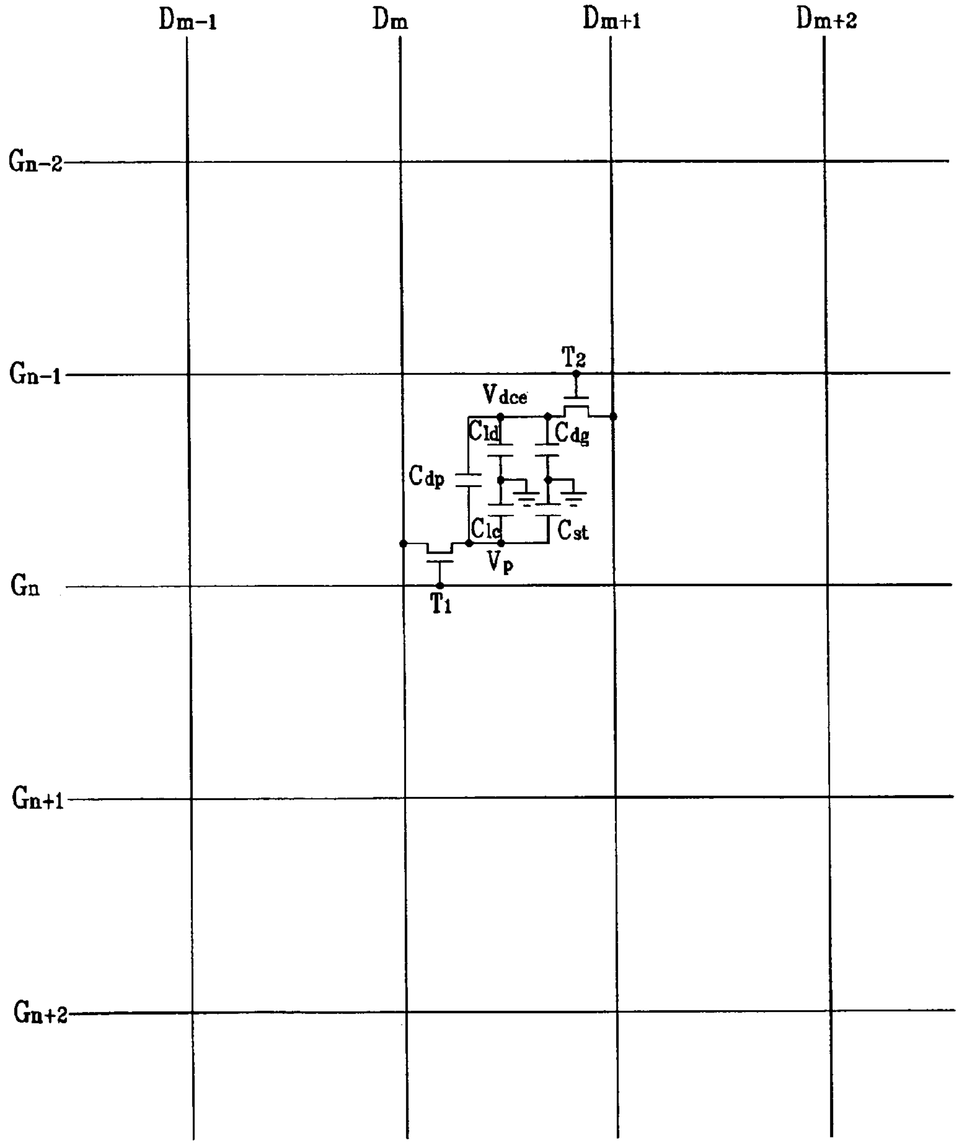


FIG.18



Dm-1
Dm
Dm+1
Dm+2
Gn-2
Gn-1
Gn
Gn+1
Gn+2
T2
Vdce
Cld
Cdg
Cdp
Clc
Cst
Vp
T1

FIG.19

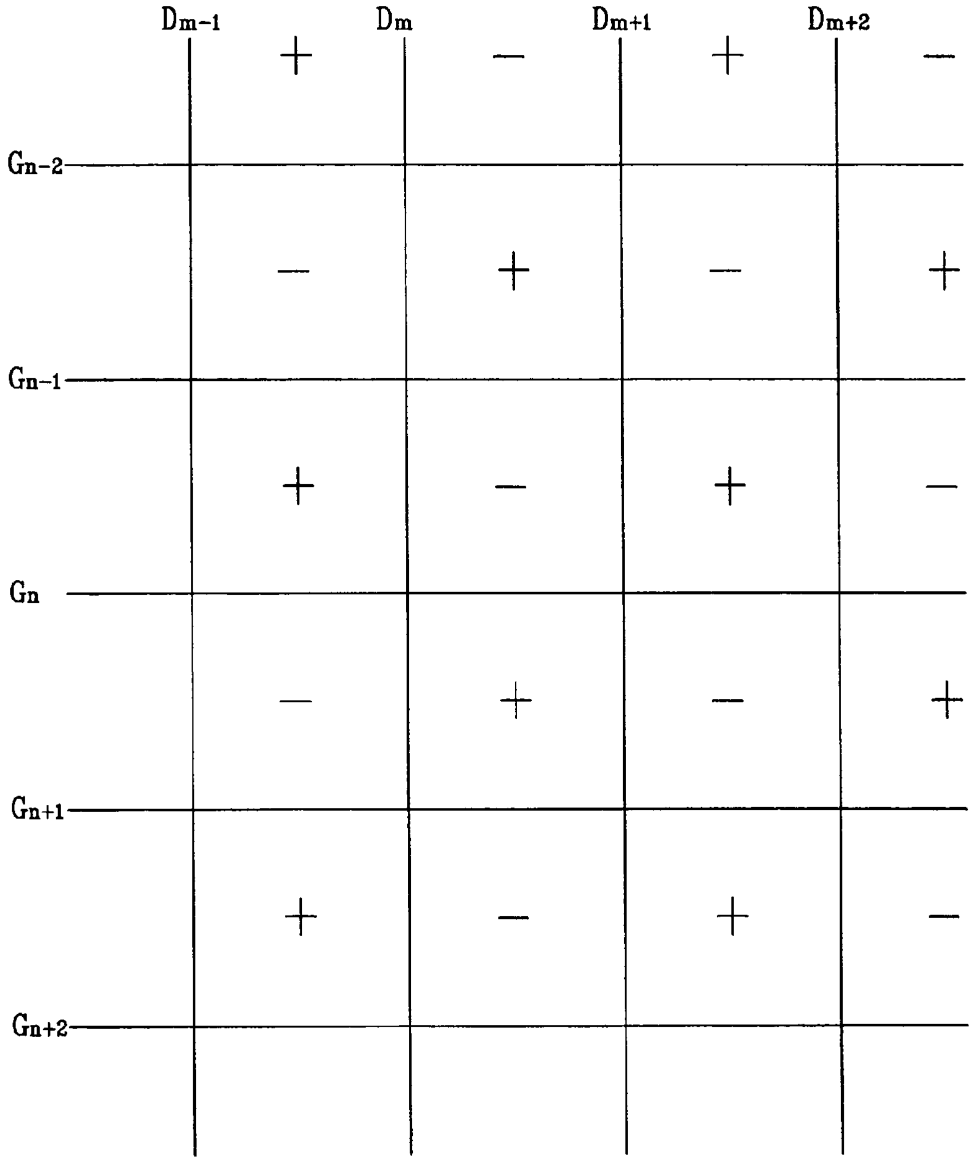


FIG.20

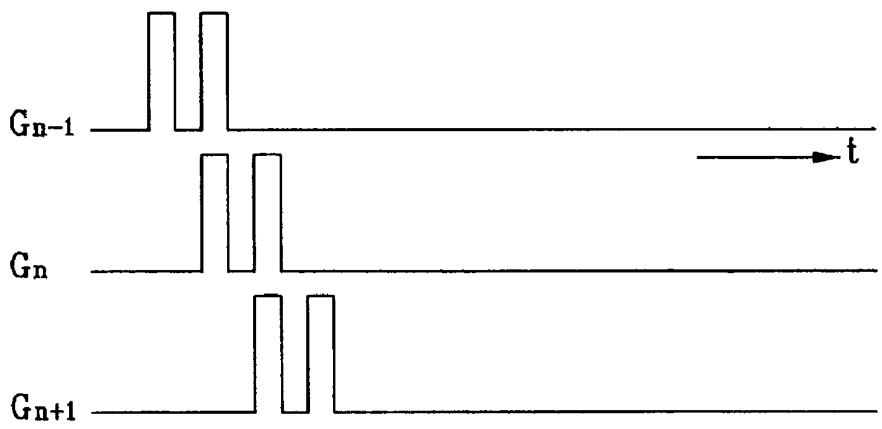
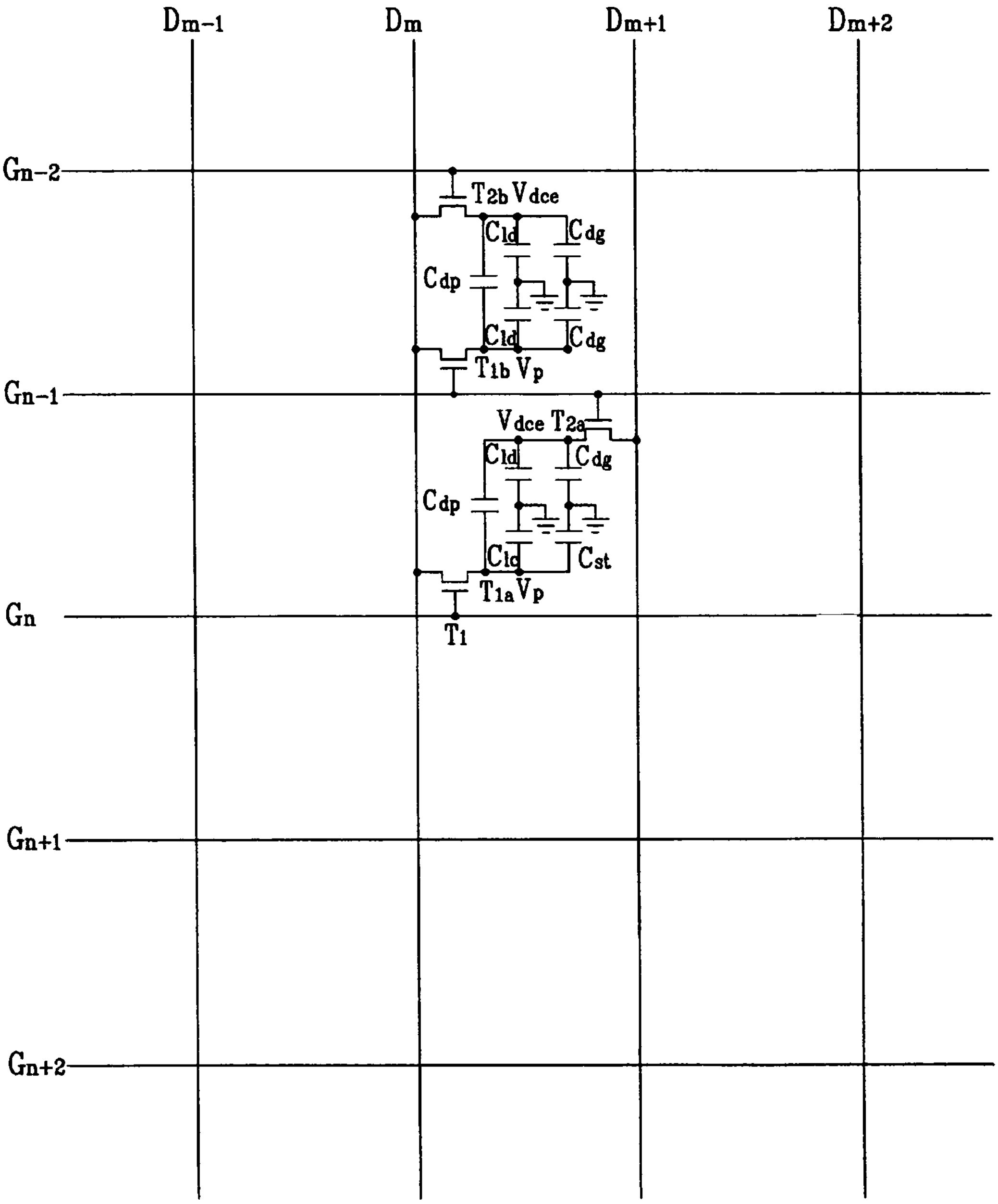


FIG.21



Dm-1
Dm
Dm+1
Dm+2
Gn-2
T2b Vdce
Cld
Cdg
Cdp
Cld
Cdg
T1b Vp
Gn-1
Vdce T2a
Cld
Cdg
Cdp
Clc
Cst
T1a Vp
Gn
T1
Gn+1
Gn+2

FIG.22

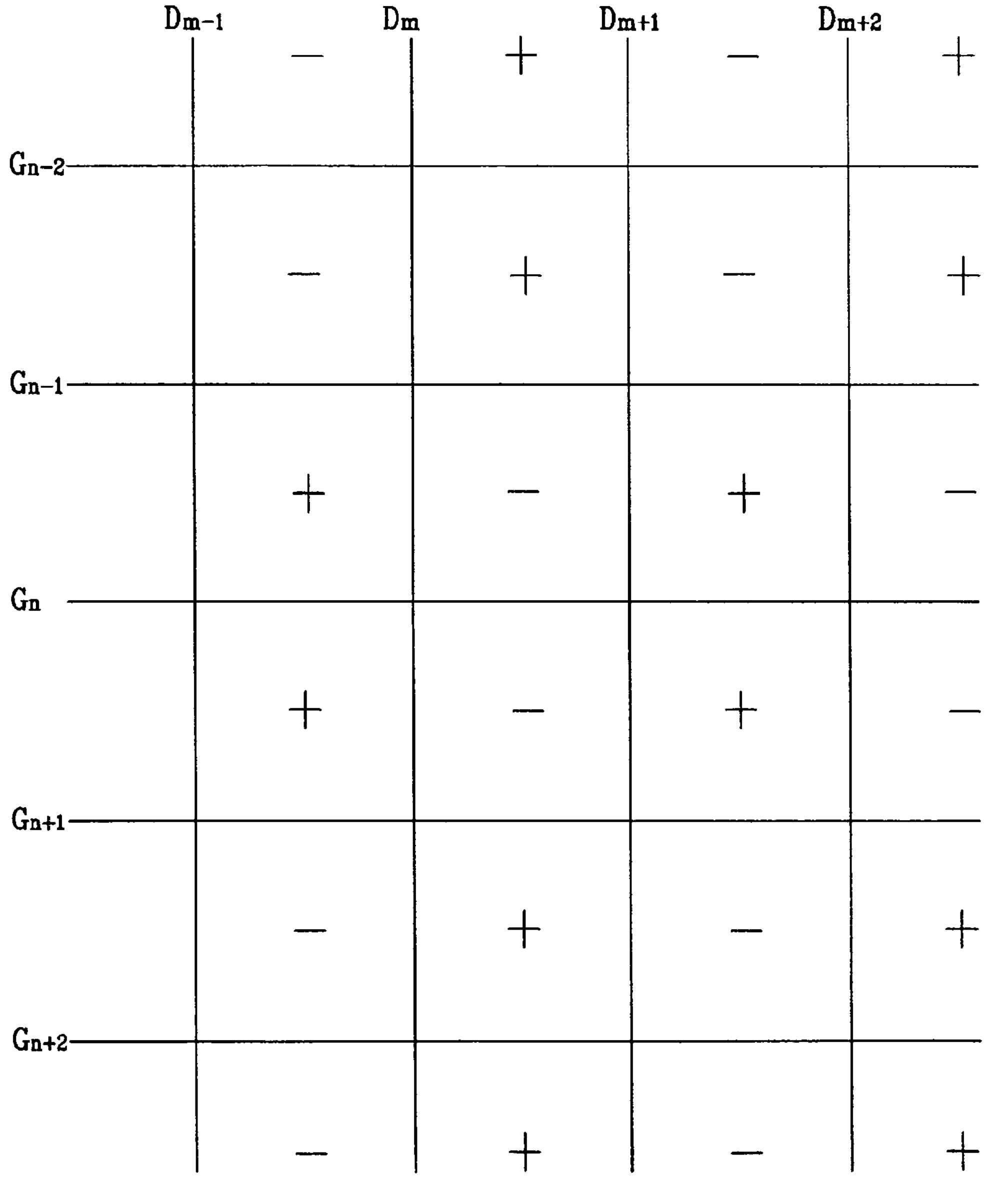


FIG.23

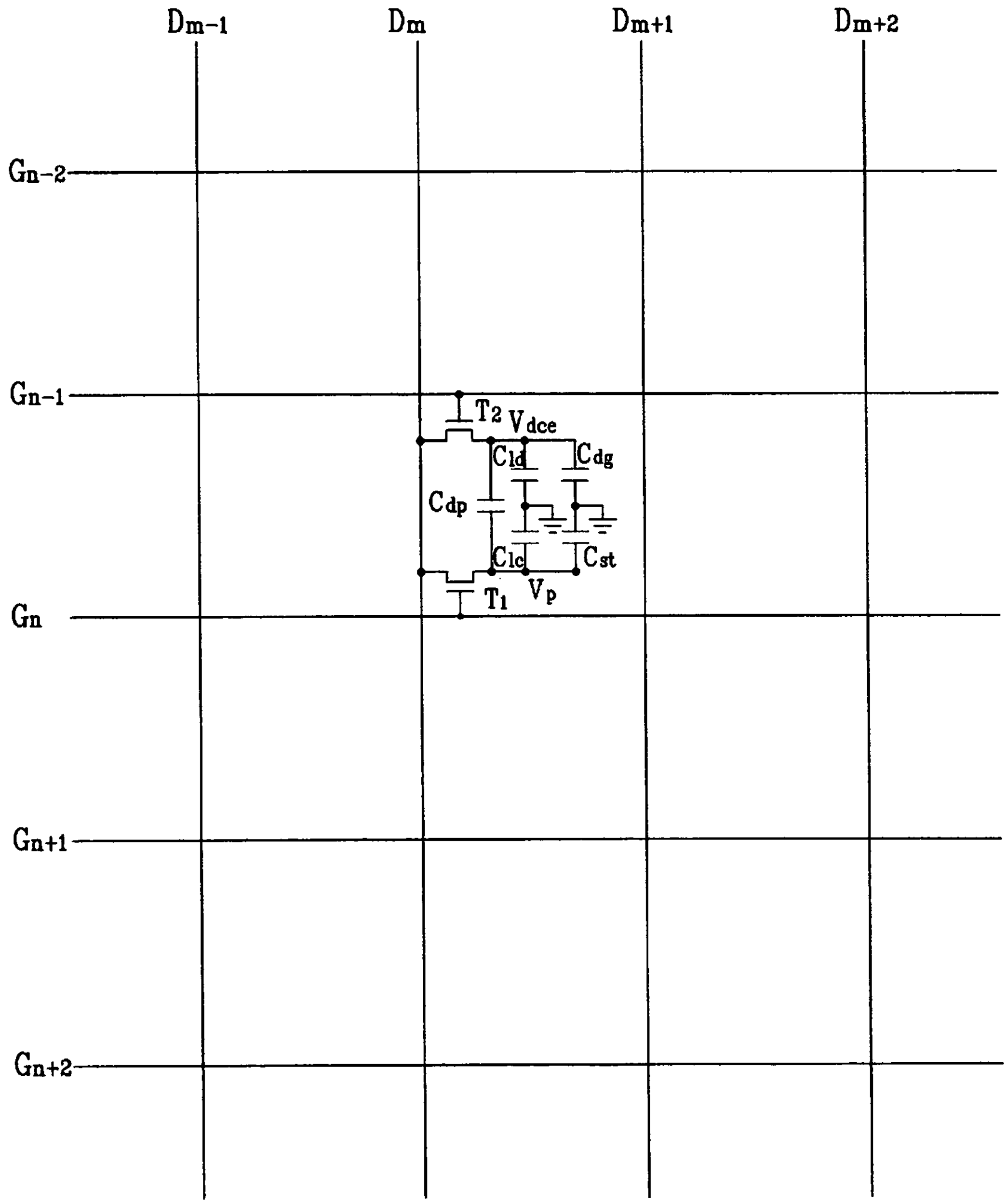

Dm-1
Dm
Dm+1
Dm+2
Gn-2
Gn-1
Gn
Gn+1
Gn+2
T2
Vdce
Cld
Cdg
Cdp
Clc
Cst
T1
Vp

FIG.24

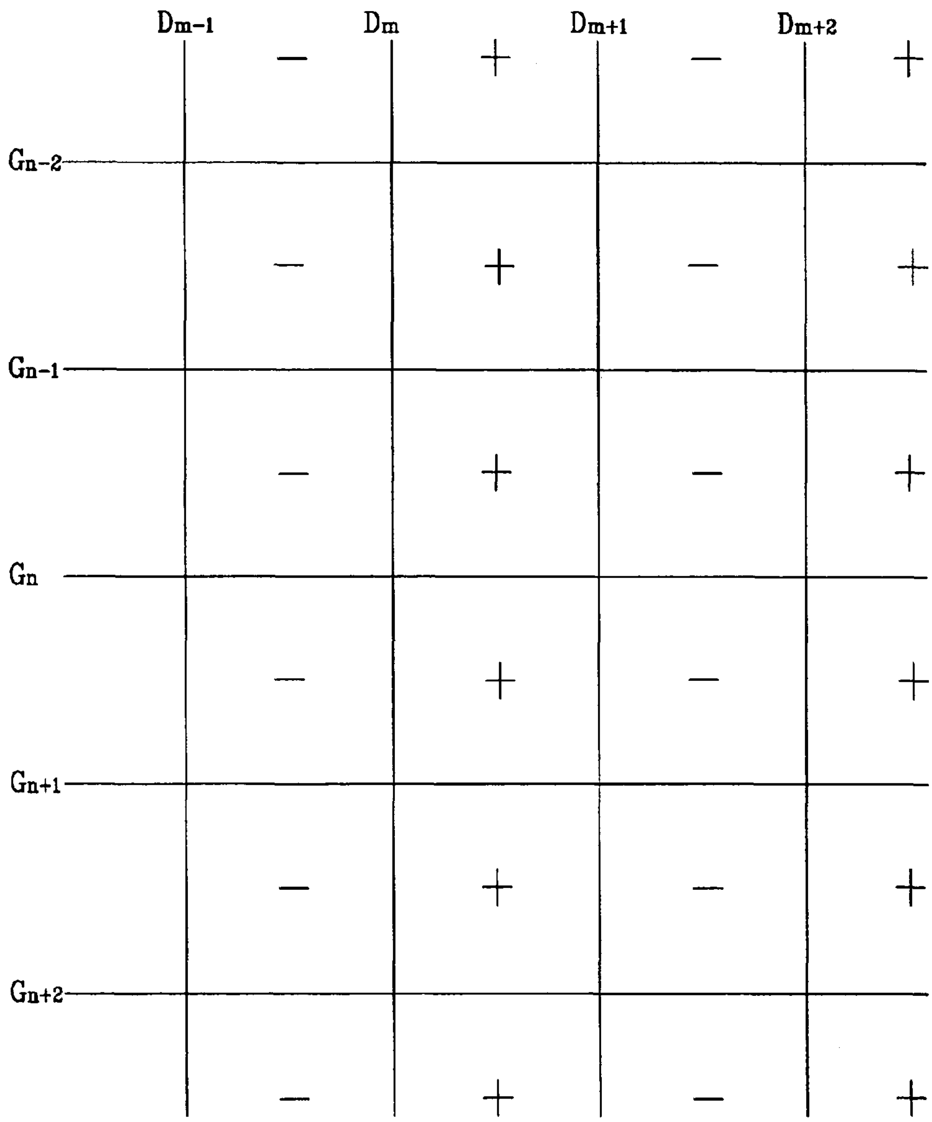
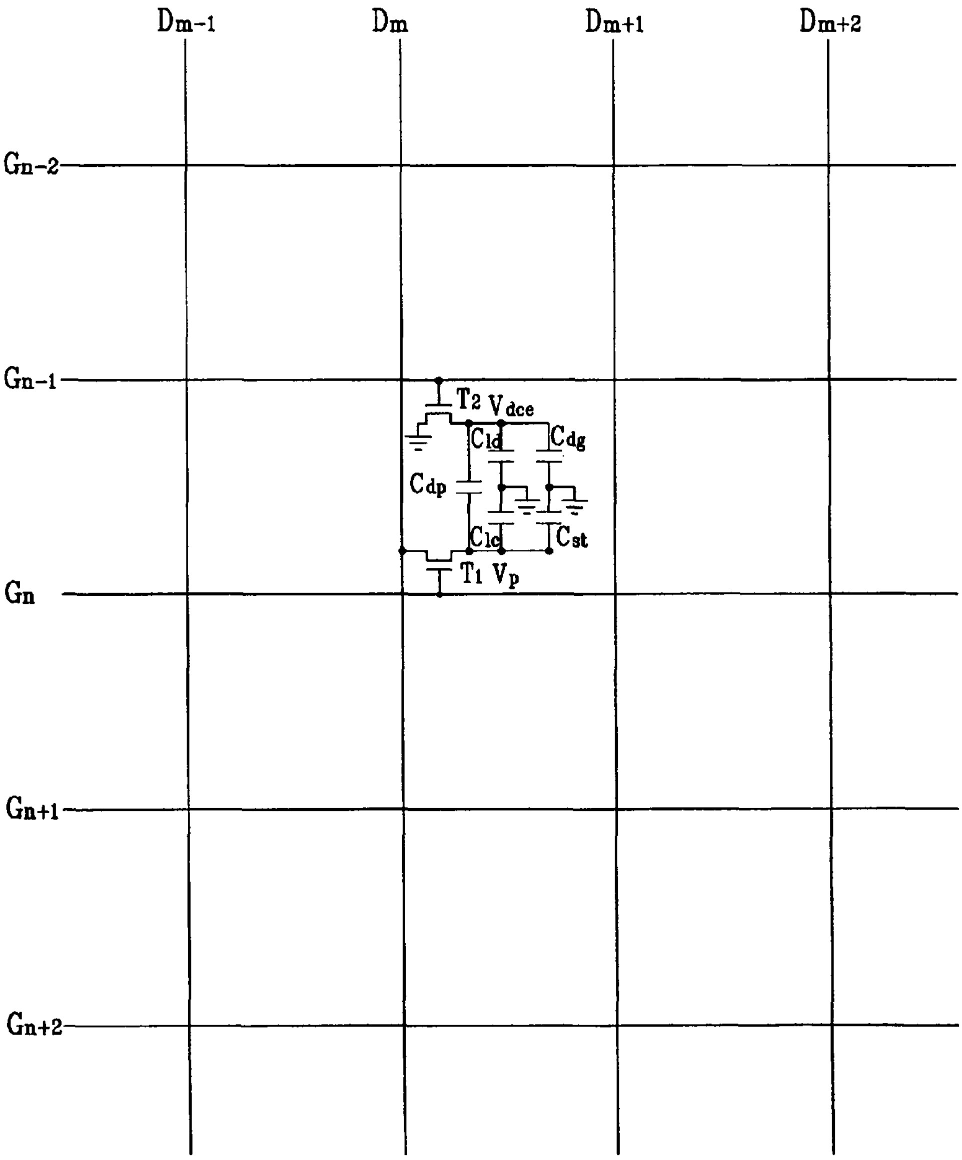


FIG.25


Dm-1
Dm
Dm+1
Dm+2
Gn-2
Gn-1
Gn
Gn+1
Gn+2
T2
Vdce
Cld
Cdg
Cdp
Clc
Cst
T1
Vp

LIQUID CRYSTAL DISPLAY

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to a liquid crystal display.

(b) Description of the Related Art

A typical liquid crystal display ("LCD") includes an upper panel provided with a common electrode and an array of color filters, a lower panel provided with a plurality of thin film transistors ("TFTs) and a plurality of pixel electrodes, and a liquid crystal layer is interposed therebetween. The pixel electrodes and the common electrode are applied with electric voltages and the voltage difference therebetween causes electric field. The variation of the electric field changes the orientations of liquid crystal molecules in the liquid crystal layer and thus the transmittance of light passing through the liquid crystal layer. As a result, the LCD displays desired images by adjusting the voltage difference between the pixel electrodes and the common electrode.

The LCD has a major disadvantage of its narrow viewing angle, and several techniques for increasing the viewing angle have been developed. Among these techniques, the provision of a plurality of cutouts or a plurality of projections on the pixel electrodes and the common electrode opposite each other along with the vertical alignment of the liquid crystal molecules with respect to the upper and the lower panels is promising.

The cutouts provided both at the pixel electrodes and the common electrode give wide viewing angle by generating fringe field to adjust the tilt directions of the liquid crystal molecules.

The provision of the projections both on the pixel electrode and the common electrode distorts the electric field to adjust the tilt directions of the liquid crystal molecules.

The fringe field for adjusting the tilt directions of the liquid crystal molecules to form a plurality of domains is also obtained by providing the cutouts at the pixel electrodes on the lower panel and the projections on the common electrode on the upper panel.

Among these techniques for widening the viewing angle, the provision of the cutouts has problems that an additional mask for patterning the common electrode is required, an overcoat is required for preventing the effect of the pigments of the color filters on the liquid crystal material, and severe disclination is generated near the edges of the patterned electrode. The provision of the projections also has a problem that the manufacturing method is complicated since it is required an additional process step for forming the projections or a modification of a process step. Moreover, the aperture ratio is reduced due to the projections and the cutouts.

SUMMARY OF THE INVENTION

A liquid crystal display is provided, which includes: a first substrate; a plurality of first signal lines formed on the first substrate and supplied with scanning signals; a plurality of second signal lines formed on the first substrate and supplied with data voltages; a plurality of pixel electrodes formed on the first substrate; a plurality of direction control electrodes formed on the first substrate; a plurality of first thin film transistors, each first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines, and a relevant one of the pixel electrodes; a second thin film transistors, each second thin film transistor connected to a previous one of the first signal lines, a previous one or a next one of the second signal lines, and a relevant one

of the direction control electrodes; a second substrate facing the first substrate; and a common electrode formed on the second substrate.

Preferably, the liquid crystal display is subjected to a dot inversion and each scanning signal has first and second pulses in a frame. The first pulse in a scanning signal preferably synchronized with the second pulse in a previous scanning signal.

Each pixel electrode may have a cutout overlapping one of the direction control electrodes at least in part.

A liquid crystal display is provided, which includes: a plurality of first signal lines transmitting scanning signals; a plurality of second signal lines transmitting data voltages; and a plurality of first and second pixels connected to the first and the second signal lines, wherein each of the first pixels has a pixel electrode, a direction control electrode, a first thin film transistor having a gate electrode connected to a relevant first signal line, a source electrode connected to a relevant second signal line, and a drain electrode connected to the pixel electrode, and a second thin film transistor having a gate electrode connected to a previous first signal line or a next first signal line, a source electrode connected to a next second signal line, and a drain electrode connected to the direction control electrode; and wherein each of the second pixels has a pixel electrode, a direction control electrode, a first thin film transistor having a gate electrode connected to a relevant first signal line, a source electrode connected to a relevant second signal line, and a drain electrode connected to the pixel electrode, and a second thin film transistor having a gate electrode connected to a previous first signal line, a source electrode connected to a relevant second signal line, and a drain electrode connected to the direction control electrode.

Preferably, the liquid crystal display is subjected to a double-dot inversion and each scanning signal has first and second pulses in a frame.

The first pixels form a plurality of first pixel rows and the second pixels form a plurality of second pixel rows, and the first pixel rows and the second pixel rows may be alternately arranged.

It is preferable that adjacent two of the first and the second pixel rows are supplied with data voltages having equal polarity in pairs and a first pixel row in each pair is supplied with a scanning signal prior to a second pixel row in the pair.

A liquid crystal display is provided, which includes: a first substrate; a plurality of first signal lines formed on the first substrate and supplied with scanning signals; a plurality of second signal lines formed on the first substrate and intersecting the first signal lines; a plurality of pixel electrodes formed on the first substrate; a plurality of direction control electrodes formed on the first substrate; a plurality of first thin film transistors, each first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines, and a relevant one of the pixel electrodes; a plurality of second thin film transistor, each second thin film transistor connected to a previous one of the first signal lines, a relevant one of the second signal lines, and a relevant one of the direction control electrodes; a second substrate facing the first substrate; and a common electrode formed on the second substrate.

Preferably, the liquid crystal display is subjected to a column inversion and each scanning signal has first and second pulses in a frame.

A liquid crystal display is provided, which includes: a first substrate; a plurality of first signal lines formed on the first substrate and supplied with scanning signals, each scanning signal having first and second pulses in a frame; a plurality of second signal lines formed on the first substrate and intersecting the first signal lines; a plurality of third signal lines formed on the first substrate, intersecting the second signal lines, and supplied with a common voltage; a plurality of pixel electrodes formed on the first substrate; a plurality of direction control electrodes formed on the first substrate; a plurality of first thin film transistors, each first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines, and a relevant one of the pixel electrodes; a plurality of second thin film transistor, each second thin film transistor connected to a previous one of the first signal lines, a relevant one of the third signal lines, and a relevant one of the direction control electrodes; a second substrate facing the first substrate; and a common electrode formed on the second substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will become more apparent by describing embodiments thereof in detail with reference to the accompanying drawings in which:

FIG. **1** is an equivalent circuit diagram of an LCD according to an embodiment of the present invention;

FIG. **2**A is a layout view of a TFT array panel for an LCD according to a first embodiment of the present invention;

FIGS. **2**B and **2**C are sectional views of the TFT array panel shown in FIG. **2**A taken along the lines IIb-IIb' and IIc-IIc', respectively;

FIGS. **3**A to **3**D are sectional views of a TFT array panel for an LCD sequentially illustrating a manufacturing method thereof according to a first embodiment of the present invention;

FIG. **4** is a layout view of a TFT array panel for an LCD according to a second embodiment of the present invention;

FIG. **5** is a sectional view of the TFT array panel shown in FIG. **4** taken along the lines V-V' and V'-V";

FIGS. **6**A to **11**B are layout views and sectional views of a TFT array panel for an LCD sequentially illustrating a manufacturing method thereof according to a second embodiment of the present invention;

FIG. **12** is a schematic diagram of TFT array panels for an LCD according to first and second embodiments of the present invention;

FIG. **13** is an equivalent circuit diagram of an LCD according to a third embodiment of the present invention;

FIG. **14** is a layout view of an LCD according to a third embodiment of the present invention;

FIG. **15** is a sectional view of the LCD shown in FIG. **14** taken along the line XV-XV';

FIG. **16** is a sectional view of the LCD shown in FIG. **14** taken along the line XVI-XVI';

FIG. **17** is a sectional view of the LCD shown in FIG. **14** taken along the lines XVII-XVII' and XVII'-XVII";

FIG. **18** is a circuit diagram of an LCD according to a fourth embodiment of the present invention;

FIG. **19** illustrates polarity of the pixels of the LCD according to the fourth embodiment of the present invention;

FIG. **20** shows waveforms of scanning signals of the LCD according to the fourth embodiment of the present invention;

FIG. **21** is a circuit diagram of an LCD according to a fifth embodiment of the present invention;

FIG. **22** illustrates polarity of the pixels of the LCD according to the fifth embodiment of the present invention;

FIG. **23** is a circuit diagram of an LCD according to a sixth embodiment of the present invention;

FIG. **24** illustrates polarity of the pixels of the LCD according to the sixth embodiment of the present invention; and

FIG. **25** is a circuit diagram of an LCD according to a seventh embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the inventions invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Now, LCDs according to embodiments of this invention will be described in detail with reference to the accompanying drawings.

FIG. **1** is an equivalent circuit diagram of an LCD according to a first embodiment of the present invention.

An LCD according to a first embodiment of the present invention includes a TFT array panel, a color filter array panel opposite the TFT array panel, and a liquid crystal layer interposed therebetween. The TFT array panel is provided with a plurality of gate lines and a plurality of data lines intersecting each other to define a plurality of pixels, and a plurality of storage electrode lines extending parallel to the gate lines. The gate lines transmit scanning signals and the data lines transmit image signals. A common voltage Vcom is applied to the storage electrode lines. Each pixel is provided with a pixel TFT for a pixel electrode and a direction-control-electrode TFT DCETFT for a direction control electrode ("DCE"). The pixel TFT includes a gate electrode connected to one of the gate lines, a source electrode connected to one of the data lines, and a drain electrode connected to one of a plurality of pixel electrodes, while the DCE TFT includes a gate electrode connected to a previous gate line, a source electrode connected to one of the storage electrode lines, and a drain electrode connected to one of a plurality of direction control electrodes.

The DCE and the pixel electrode are capacitively coupled, and the capacitor therebetween or its capacitance is represented by C_{DP}. The pixel electrode and a common electrode provided on the color filter array panel form a liquid crystal capacitor, and the liquid crystal capacitor or its capacitance is represented by C_{LC}. The pixel electrode and a storage electrode connected to one of the storage electrode lines form a storage capacitor, and the storage capacitor or its capacitance is represented by C_{ST}.

Although it is not shown in the circuit diagram, the pixel electrode according to an embodiment of the present invention has a cutout overlapping the DCE such that the electric field due to the DCE flows out through the cutout. The electric field flowing out through the cutout makes the liquid crystal molecules have pretilt angles. The pretilted liquid crystal molecules are rapidly aligned without dispersion along predetermined directions upon the application of the electric field due to the pixel electrode.

In order to obtain the pretilted liquid crystal molecules using the electric field generated by the DCE, the potential of the DCE relative to the potential of the common electrode (referred to as the "DCE voltage" hereinafter) is larger than the potential of the pixel electrode relative to the potential of the common electrode (referred to as the "pixel voltage" hereinafter) by a predetermined value. The LCD according to an embodiment of the present invention easily satisfies this requirement by isolating the DCE after applying the potential applied to the storage electrode lines to the DCE. The reason will be described now.

The pixel TFT and the DCE TFT are in off state before applying a gate-on voltage to the previous gate line G_{i-1}. Upon application of the gate-on voltage to the previous gate line G_{i-1}, the common voltage is applied to the DCE. Accordingly, the voltage Vp of the pixel electrode becomes to have a value lower than the voltage V_{DCE} of the DCE. When the DCE TFT is turned off after charging, the DCE floats to make the voltage charged in the DCE capacitor C_{DP} constant. Accordingly, the voltage V_{DCE} of the floating DCE is always larger than the voltage Vp of the pixel electrode irrespective of the potential change of the pixel electrode. For example, when the voltage Vp of the pixel electrode is increased when the pixel TFT is turned on, the voltage V_{DCE} of the DCE follows the voltage increase of the pixel electrode in order to maintain the potential difference between the DCE and the pixel electrode.

This is described in terms of a circuital relation.

A voltage across a capacitor in an electrical circuit is given by

$$V_C = V_0 + \frac{1}{C}\int_0^t i\,d(t)$$

A floating electrode is equivalent to an electrode connected to a resistor having infinite resistance (R=∞). Therefore, i=0 and V__C=V__0, that is, the initial voltage across the capacitor is maintained. In other words, the potential of a floating electrode increases or decreases coupled with the potential of the other electrode.

Similarly, the voltage V_{DCE} of the floating DCE maintains lower than the negative voltage Vp of the pixel electrode regardless of the voltage Vp of the pixel electrode.

According to an embodiment of the present invention, the DCE TFT is connected to the storage electrode lines such that the common voltage is applied to the DCE. Hence, the potentials of the two electrodes increases or decreases to have substantially the same polarity irrespective of the polarity of the potential applied to the pixel electrode in the next frame. As a result, the present invention is applied any inversion type such as line inversion and dot inversion.

For the same gray, there is no variation of the potential difference between the DCE and the pixel electrode irrespective of the grays of previous and next frames, thereby ensuring stability of image quality.

The disconnection of the DCE TFTs from the data lines prevents the increase of the load of the data lines.

Now, a detailed embodiment of the present invention is described with reference to FIGS. **2**A to **2**C.

FIG. **2**A is a layout view of an LCD according to an embodiment of the present invention, and FIGS. **2**B and **2**C are sectional views of the LCD shown in FIG. **2**A taken along the lines IIB-IIB' and IIC-IIC'.

An LCD according to a first embodiment of the present invention includes a lower panel, an upper panel facing the lower panel, and a vertically (or homeotropically) aligned liquid crystal layer interposed between the lower panel and the upper panel.

The lower panel will now be described more in detail.

A plurality of gate lines **121** are formed on an insulating substrate **110** and a plurality of data lines **171** are formed thereon. The gate lines **121** and the data lines **171** are insulated from each other and intersect each other to define a plurality of pixel areas.

Each pixel area is provided with a pixel TFT, a DCE TFT, a DCE and a pixel electrode. The pixel TFT has three terminals, a first gate electrode **123***a*, a first source electrode **173***a* and a first drain electrode **175***a* while the DCE TFT has three terminals, a second gate electrode **123***b*, a second source electrode **173***b* and a second drain electrode **175***b*. The pixel TFT is provided for switching the signals transmitted to the pixel electrode **190** while the DCE TFT is provided for switching the signals entering the DCE **178**. The gate electrode **123***a*, the source electrode **173***a* and the drain electrode **175** of the pixel TFT are connected to corresponding one of the gate lines **121**, one of the data lines **171** and the pixel electrode **190**, respectively. The gate electrode **123***b*, the source electrode **173***b* and the drain electrode **175***b* of the DCE TFT are connected to previous one of the gate lines **121**, corresponding one of the storage electrode lines **131** and the DCE **178**, respectively. The DCE **178** is applied with a direction-controlling voltage for controlling the pre-tilts of the liquid crystal molecules to generate a direction-controlling electric field between the DCE **178** and the common electrode **270**. The DCE **178** is formed in a step for forming the data lines **171**.

The layered structure of the lower panel will be described in detail.

A plurality of gate lines **121** extending substantially in a transverse direction are formed on an insulating substrate **110**, and a plurality of first and second gate electrodes **123***a* and **123***b* are connected to the gate lines **121**. A plurality of storage electrode lines **131** and a plurality of sets of first to fourth storage electrodes **133***a*-**133***d* are also formed on the insulating substrate **110**. The storage electrode lines **131** extend substantially in the transverse direction, and the first and the second storage electrodes **133***a* and **133***b* extend from the storage electrode line **131** in a longitudinal direction. The third and the fourth storage electrodes **133***c* and **133***d* extend in the transverse direction and connect the first storage electrode **133***a* and the second storage electrode **133***b*.

The gate wire **121**, **123***a* and **123***b* and the storage electrode wire **131** and **133***a*-**133***d* are preferably made of Al, Cr or their alloys, Mo or Mo alloy. If necessary, the gate wire **121**, **123***a* and **123***b* and the storage electrode wire **131** and **133***a*-**133***d* include a first layer preferably made of Cr or Mo alloys having excellent physical and chemical characteristics and a second layer preferably made of Al or Ag alloys having low resistivity.

A gate insulating layer **140** is formed on the gate wire **121**, **123***a* and **123***b* and the storage electrode wire **131** and **133***a*-**133***d*.

A semiconductor layer **151**, **154***a*, **154***b* and **155** preferably made of amorphous silicon is formed on the gate insulating layer **140**. The semiconductor layer **151**, **154***a*, **154***b* and **155** includes a plurality of first and second channel semiconductors **154***a* and **154***b* forming channels of TFTs, a plurality of data-line semiconductors **151** located under the data lines **171**, and a plurality of intersection semiconductors **155** located near the intersections of DCEs **178** and the storage electrodes **133***c* and **133***d* for ensuring insulation therebetween.

An ohmic contact layer **161**, **163***a*, **163***b*, **165***a* and **165***b* preferably made of silicide or n+ hydrogenated amorphous silicon heavily doped with n type impurity is formed on the semiconductor layer **151**, **154***a*, **154***b* and **155**.

A data wire **171**, **173***a*, **173***b*, **175***a* and **175***b* is formed on the ohmic contact layer **161**, **163***a*, **163***b*, **165***a* and **165***b* and the gate insulating layer **140**. The data wire **171**, **173***a*, **173***b*, **175***a* and **175***b* includes a plurality of data lines **171** extending in the longitudinal direction and intersecting the gate lines **121** to form a plurality of pixels, a plurality of first source electrodes **173***a* branched from the data lines **171** and extending onto portions **163***a* of the ohmic contact layer, a plurality of first drain electrodes **175***a* disposed on portions **165***a* of the ohmic contact layer, located opposite the first source electrodes **173***a* with respect to the first gate electrodes **123***a* and separated from the first source electrodes **173***a*, and a plurality of second source electrodes **173***b* and a plurality of second drain electrodes **175***b* disposed on respective portions **163***b* and **165***b* opposite each other with respect to the second gate electrodes **123***b*. One end portion of each data line **171** is widened for connection to an external circuit.

A plurality of DCEs **178** are formed in the pixel areas defined by the intersections of the gate lines **121** and the data lines **171**. Each DCE **178** includes a plurality of X-shaped metal pieces connected to one another and is connected to the second drain electrode **175***b*. The data wire **171**, **173***a*, **173***b*, **175***a* and **175***b* and the DCEs **178** are preferably made of Al, Cr or their alloys, Mo or Mo alloy. If necessary, the data wire **171**, **173***a*, **173***b*, **175***a* and **175***b* and the DCEs **178** include a first layer preferably made of Cr or Mo alloys having excellent physical and chemical characteristics and a second layer preferably made of Al or Ag alloys having low resistivity.

A passivation layer **180** preferably made of silicon nitride or organic insulator is formed on the data wire **171**, **173***a*, **173***b*, **175***a* and **175***b*.

The passivation layer **180** is provided with a plurality of contact holes **181** exposing the first drain electrodes **175***a*, a plurality of contact holes **182** extending to the gate insulating layer **140** and exposing the storage electrode lines **131**, and a plurality of contact holes **183** exposing the second source electrodes **173***b*.

A plurality of pixel electrodes **190** are formed on the passivation layer **180**. Each pixel electrode **190** is connected to the first drain electrode **175***a* through the contact hole **181** and has a plurality of X-shaped cutouts **191** and a plurality of linear cutouts **192**. The X-shaped cutouts **191** overlap the X-shaped portions of the DCE **178** while the linear cutouts **192** overlap the third and the fourth storage electrodes **133***c* and **133***d*. The DCE **178** broadly overlaps peripheries of the cutouts **191** as well as the cutouts **191** themselves to form a storage capacitance along with the pixel electrode **190**.

A plurality of bridges **92** connecting the storage electrode lines **131** and the second source electrodes **173***b* through the contact holes **182** and **183** are also formed on the passivation layer. Furthermore, a plurality of contact assistants (not shown) connected to the end portions of the gate lines **121** and the data lines **171** are formed on the passivation layer **180**. The pixel electrodes **190**, the bridges **92**, and the contact assistants are preferably formed of indium zinc oxide ("IZO"). Alternatively, the pixel electrodes **190**, the bridges **92**, and the contact assistants are preferably made of indium tin oxide ("ITO").

To summarize, each pixel electrode **190** has the plurality of cutouts **191** and **192** for partitioning a pixel region into a plurality of domains, and the first cutouts **191** overlap the DCE **178** while the second cutouts **192** overlap the storage electrodes **133***c* and **133***d*. The DCE **178** and the first cutouts **191** are aligned such that the DCE **178** is exposed through the first cutouts **191** to be seen in front view. The storage electrode line **131** and the DCE **178** are connected via the DCE TFT while the data line **171** and the pixel electrode **190** are connected via the pixel TFT, and the pixel electrode **190** and the DCE **178** are aligned to form a storage capacitance.

According to another embodiment of the present invention, the DCEs **178** include substantially the same layer as the gate wire **121**, **123***a* and **123***b*. The portions of the passivation layer **180** on the DCEs **178** may be removed to form a plurality of openings.

The upper substrate **210** will no be described in detail.

A black matrix **220** for preventing light leakage, a plurality of red, green and blue color filters **230**, and a common electrode **270** preferably made of a transparent conductor such as ITO or IZO are formed on an upper substrate **210** preferably made of transparent insulating material such glass.

A plurality of liquid crystal molecules contained in the liquid crystal layer **3** is aligned such that their director is perpendicular to the lower and the upper substrates **110** and **210** in absence of electric field. The liquid crystal layer **3** has negative dielectric anisotropy.

The lower substrate **110** and the upper substrate **210** are aligned such that the pixel electrodes **190** exactly match and overlap the color filters **230**. In this way, a pixel region is divided into a plurality of domains by the cutouts **191** and **192**. The alignment of the liquid crystal layer **3** in each domain is stabilized by the DCE **178**.

This embodiment illustrates the liquid crystal layer **3** having negative dielectric anisotropy and homeotropic alignment with respect to the substrates **110** and **210**. However, the liquid crystal layer **3** may have positive dielectric anisotropy and homogeneous alignment with respect to the substrates **110** and **210**.

A method of manufacturing a TFT array panel of an LCD having the above-described structure will be described.

FIGS. **3**A to **3**D are sectional views of a TFT array panel for an LCD sequentially illustrating a manufacturing method thereof according to a first embodiment of the present invention.

First, as shown in FIG. **3**A, a conductive layer preferably made of metal is deposited by sputtering and either dry-etched or wet-etched by a first photo-etching step using a mask to form a gate wire and a storage electrode wire on a substrate **110**. The gate wire includes a plurality of gate lines **121** and a plurality of gate electrodes **123**, and the storage wire includes a plurality of storage electrode lines **131** and a plurality of storage electrodes **133***a*-**133***d*.

As shown in FIG. **3**B, a gate insulating layer 140 with 1,500-5,000 Å thickness, a hydrogenated amorphous silicon layer with 500-2,000 Å thickness, and a doped amorphous silicon layer with 300-600 Å thickness are sequentially deposited by chemical vapor deposition ("CVD"). The doped amorphous silicon layer and the amorphous silicon layer are patterned by a photo-etching step using a mask to form an ohmic contact layer **160***a*, **160***b* and **161** and an amorphous silicon layer **151**, **154***a* and **154***b*.

Thereafter, as shown in FIG. **3**C, a conductive layer with 1,500-3,000 Å thickness preferably made of metal is deposited by sputtering and patterned by a photo-etching step using a mask to form a data wire and a plurality of DCEs **178**. The data wire includes a plurality of data lines **171**, a plurality of source electrodes **173***a* and **173***b*, and a plurality of drain electrodes **175***a* and **175***b*.

Then, portions of the ohmic contact layer **160***a* and **160***b*, which are not covered by the source electrodes **173***a* and **173***b* and the drain electrodes **175***a* and **175***b*, are removed such that an ohmic contact layer **163***a*, **163***b*, **165***a* and **165***b* including a plurality of separated portions is formed and portions of the semiconductor layer **151** between the source electrodes **173***a* and **173***b* and the drain electrodes **175***a* and **175***b* are exposed.

As shown in FIG. **3**D, a passivation layer **180** is formed by coating an organic insulating material having low dielectric constant and good planarization characteristic or by CVD of low dielectric insulating material such as SiOF or SiOC having a dielectric constant equal to or less than 4.0. The passivation layer **180** together with the gate insulating layer **140** is patterned by a photo-etching step using a mask to form a plurality of contact holes **181**, **182** and **183**.

Finally, as shown in FIG. **2**A, an ITO layer or an IZO layer with thickness of 1500-500 Å is deposited and photo-etched using a mask to form a plurality of pixel electrodes **190**, a plurality of connecting bridges **92**, and a plurality of contact assistants (not shown).

This technique is applied to a manufacturing method using five masks as described above. However, the technique may be well adapted for a method of a TFT array panel for an LCD using four masks. It is described in detail with reference to the drawings.

FIG. **4** is a layout view of a TFT array panel for an LCD according to a second embodiment of the present invention, and FIG. **5** is a sectional view of the TFT array panel shown FIG. **4** taken along the lines V-V' and V'-V''.

A TFT array panel for an LCD according to a second embodiment of the present invention is manufactured by using four masks and has a feature compared with a TFT array panel manufactured by using five masks, which will be described now.

An ohmic contact layer **161**, **163***a*, **163***b*, **165***a* and **165***b* formed under a plurality of DCEs **178** and a data wire including a plurality of data lines **171**, a plurality of source electrodes **173***a* and **173***b*, and a plurality of the drain electrodes **175***a* and **175***b* has substantially the same shape as the data wire **171**, **173***a*, **173***b*, **175***a*, **175***b* and **179** and the DCEs **178**. An amorphous silicon layer **151**, **154***a*, **154***b* and **158** has substantially the same shape as the data wire and the DCEs **178** except that channel portions between the source electrodes **173***a* and **173***b* and the drain electrodes **175***a* and **175***b* are connected. Remaining structure is substantially the same as a TFT array panel manufactured by a five-mask process.

FIG. **4** illustrates an expanded end portion **125** of the gate line **121**, an expanded end portion **135** of the storage electrode line **131**, and an expanded end portion **179** of the data line **171** as well as contact assistants **95**, **99** and **97**.

A method of manufacturing a TFT array panel will be now described.

FIGS. **6**A to **11**B are layout views and sectional views of a TFT array panel for an LCD sequentially illustrating a manufacturing method thereof.

First, as shown in FIGS. **6**A and **6**B, Al, Ag, their alloys or the like is deposited and photo-etched to form a gate wire including a plurality of gate lines **121** and **125** and a plurality of gate electrodes **123**, and a storage electrode wire **131** and **133***a*-**133***d*. (First Mask)

As shown in FIG. **7**, a silicon nitride gate insulating layer **140** with 1,500-5,000 Å thickness, an amorphous silicon layer **150** with 500-2,000 Å thickness, and a contact layer **160** with 300-600 Å thickness are sequentially deposited by CVD. A conductive layer **170** preferably made of Al, Ag or their alloys is deposited by preferably sputtering, and a photoresist film PR with thickness of 1-2 microns is coated thereon.

Thereafter, the photoresist film PR is exposed to light through a mask and is developed to form a photoresist pattern PR as shown in FIGS. **8**A and **8**B. Each portion of the photoresist pattern PR located on a channel area C of a TFT, which is placed between a source electrode **173***a* or **173***b* and a drain electrode **175***a* or **175***b*, is thicker than each portion of the photoresist pattern PR located on a data area A where a data wire will be formed. All portions of the photoresist film PR on the remaining areas B are removed. Here, the ratio of the thickness of the photoresist pattern PR on the channel area C and on the data area A is adjusted depending on process conditions of subsequent etching steps described later, and it is preferable that the thickness of the former is equal to or less than a half of that of the latter, for example, equal to or less than 4,000 Å. (Second Mask)

The position-dependent thickness of the photoresist pattern is obtained by several techniques. A slit pattern, a lattice pattern or a translucent film is provided on the mask in order to adjust the light transmittance in the area C.

When using a slit pattern, it is preferable that width of the slits and a gap between the slits is smaller than the resolution of an exposer used for the photolithography. In case of using a translucent film, thin films with different transmittances or different thickness may be used to adjust the transmittance on the masks.

When a photoresist film is exposed to light through such a mask, polymers of a portion directly exposed to the light are almost completely decomposed, and those of a portion exposed to the light through a slit pattern or a translucent film are not completely decomposed because the amount of a light irradiation is small. The polymers of a portion of the photoresist film blocked by a light-blocking film provided on the mask are hardly decomposed. After the photoresist film is developed, the portions containing the polymers, which are not decomposed, is left. At this time, the thickness of the portion with less light exposure is thinner than that of the portion without light exposure. Since too long exposure time decomposes all the molecules, it is necessary to adjust the exposure time.

The small thickness of the photoresist film may be obtained using reflow. That is, the photoresist film is made of a reflowable material and exposed to light through a normal mask having opaque and transparent portions. The photoresist film is then developed and subject to reflow such that portions of the photoresist film flows down onto areas without photoresist, thereby forming thin portions.

Next, the photoresist pattern PR and the underlying layers including the conductive layer **170**, the contact layer **160** and the semiconductor layer **150** are etched such that the data wire and the underlying layers are left on the data areas A, only the semiconductor layer is left on the channel areas C, and all the three layers **170**, **160** and **150** are removed to expose the gate insulating layer **140** on the remaining areas B.

First, as shown in FIG. **9**, the exposed portions of the conductive layer **170** on the other areas B are removed to expose the underlying portions of the contact layer **160**. Both dry etch and wet etch are selectively used in this step and preferably performed under the condition that the conductive layer **170** is easily etched and the photoresist pattern PR are hardly etched. However, since it is hard to identify the above-described condition for dry etch, and the dry etch may be performed under the condition that the photoresist pattern PR and the conductive layer **170** are etched simultaneously. In this case, the portions of the photoresist pattern PR on the channel areas C for dry etch are preferably made to be thicker than those for the wet etch to prevent the removal of the portions of the photoresist pattern PR on the channel areas C and thus the exposure of the underlying portions of the conductive layer **170**.

As a result, as shown in FIG. **9**, only the portions **171**, **170***a* and **170***b* of the conductive layer **170** on the channel areas C and the data areas A are left and the portions of the conductive layer **170** on the remaining areas B are removed to expose the underlying portions of the contact layer **160**. Here, the data-wire conductors **171**, **170***a* and **170***b* have substantially the same planar shapes as the data wire **171**, **173***a*, **173***b*, **175***a*, **175***b* and **179** except that the source electrodes **173***a* and **173***b* and the drain electrodes **175***a* and **175***b* are not disconnected from but connected to each other. When using dry etch, the thickness of the photoresist pattern PR is reduced to an extent.

Next, as shown in FIG. **9**, the exposed portions of the contact layer **160** and the underlying portions of the amorphous silicon layer **150** on the areas B as well as the portions of the photoresist pattern PR on the channel areas C are removed by dry etch. The etching is performed under the conduction that the photoresist pattern PR, the contact layer **160** and the semiconductor layer **150** are easily etched and the gate insulating layer **140** is hardly etched. (It is noted that etching selectivity between the intermediate layer and the semiconductor layer is nearly zero.) In particular, it is preferable that the etching ratios for the photoresist pattern PR and the semiconductor layer **150** are nearly the same. For instance, the etched thicknesses of the photoresist pattern PR and the semiconductor layer **150** can be nearly the same by using a gas mixture of SF_6 and HCl, or a gas mixture of SF_6 and O_2. When the etching ratios for the photoresist pattern PR and for the semiconductor pattern **150** are the same, the initial thickness of the portions of the photoresist pattern PR on the channel areas C is equal to or less than the sum is of the thickness of the semiconductor layer **150** and the thickness of the contact layer **160**.

Consequently, as shown in FIG. **10**, the portions of the photoresist pattern PR on the channel areas C are removed to expose the underlying portions of source/drain ("S/D") conductors **170***a* and **170***b*, and the portions of the contact layer **160** and the semiconductor layer **150** on the remaining areas B are removed to expose the underlying portions of the gate insulating layer **140**. In the meantime, the portions of the photoresist pattern PR on the data areas A are also etched to become thinner. Moreover, the semiconductor pattern **151**, **154***a*, **154***b* and **158** is completed in this step. A plurality of ohmic contacts **161**, **160***a*, **160***b* and **168** are formed on the semiconductor pattern **151**, **154***a*, **154***b* and **158**.

Then, photoresist remnants left on the surface of the S/D conductors **170***a* and **170***b* on the channel areas C are removed by ashing.

Next, as shown in FIGS. **11**A and **11**B, portions of the S/D conductors **170***a* and **170***b* and the underlying portions of the S/D ohmic contacts **160***a* and **160***b* on the channel areas C are etched to be removed. Here, the etching of both the S/D conductors **170***a* and **170***b* and the S/D ohmic contacts **160***a* and **160***b* may be done using only dry etching. Alternatively, the S/D conductors **170***a* and **170***b* are etched by wet etching and the S/D ohmic contacts **160***a* and **160***b* are etched by dry etching. In the former case, it is preferable to perform the etching under the condition that etching selectivity between the S/D conductors **170***a* and **170***b* and the S/D ohmic contacts **160***a* and **160***b* is high. It is because the low etching selectivity makes the determination of the etching finish point difficult, thereby causing the adjustment of the thickness of the portions of the semiconductor pattern **154***a* and **154***b* left on the channel areas C to be difficult. In the latter case alternately applying wet etching and dry etching, a stepwise lateral sidewall is formed since the wet etch etches the lateral sides of the S/D conductors **170***a* and **170***b*, while the dry etch hardly etches the lateral sides of the S/D ohmic contacts **160***a* and **160***b*. Examples of etching gases used for etching the S/D ohmic contacts **160***a* and **160***b* are a gas mixture of CF_4 and HCl and a gas mixture of CF_4 and O_2. Use of the gas mixture of CF_4 and O_2 enables to obtain uniform thickness of etched portions of the semiconductor pattern **154***a* and **154***b*. In this regard, the exposed portions of the semiconductor pattern **154***a* and **154***b* are etched to have a reduced thickness, and the portions of the photoresist pattern PR on the data-wire areas A are also etched to have a reduced thickness. This etching is performed under the condition that the gate insulating layer **140** is not etched, and it is preferable that the photoresist pattern PR is thick enough to prevent the portions of the photoresist pattern PR on the data-wire areas A from being removed to expose the underlying portions of the data wire **171**, **173***a*, **173***b*, **175***a*, **175***b* and **179**.

Accordingly, the source electrodes **173***a* and **173***b* and the drain electrodes **175***a* and **175***b* are separated from each other, and, simultaneously, the data wire **171**, **173***a*, **173***b*, **175***a*, **175***b* and **179** and the ohmic contact pattern **161**, **163***a*, **163***b*, **165***a* and **165***b* thereunder are completed.

Finally, the portions of the photoresist pattern PR left on the data areas A are removed. Alternatively, the portions of the photoresist pattern PR on the data areas A are removed after the portions of the S/D conductors **170***a* and **170***b* on the channel areas C are removed and before the underlying portions of the S/D ohmic contacts **160***a* and **160***b* are removed.

As described above, wet etching and dry etching may be performed one after the other, but only dry etching may be used. The latter is relatively simple but it is not easy to find a proper etching condition compared with the former. On the contrary, it is easy to find a proper etching condition for the former case but the former is relatively complicated compared with the latter.

Thereafter, as shown in FIGS. **4** and **5**, a passivation layer **180** is formed by growing a-Si:C:O or a-Si:O:F by CVD, by depositing silicon nitride, or by coating an organic insulating material such as acryl-based material. When forming an a-Si:C:O layer, $SiH(CH_3)_3$, $SiO_2(CH_3)_4$, $(SiH)_4O_4(CH_3)_4$, $Si(C_2H_5O)_4$ or the like used as basic source, oxidant such as N_2O or O_2, and Ar or He are mixed in gaseous states to flow for the deposition. For an s-Si:O:F layer, the deposition is performed with flowing a gas mixture including SiH_4, SiF_4 or the like and an additional gas of O_2. CF_4 may be added as a secondary source of fluorine.

As shown in FIGS. **4** and **5**, the passivation layer **180** together with the gate insulating layer **140** is photo-etched to form a plurality of contact holes **181**, **182**, **183**, **184**, **185** and **186** exposing the first drain electrodes **175***a*, the second source electrodes **173***b*, the storage electrode lines **131**, the expanded end portions **125** of the gate lines **121**, the expanded end portions **135** of the storage electrode lines **131**, and the expanded end portions **179** of the data lines **171**. It is preferable that the area of the contact holes **184**, **185** and **186** exposing the end portions **125**, **179** and **135** is equal to or larger than 0.5 mm×15 μm and not larger than 2 mm×60 μm. (Third Mask)

Finally, an ITO layer or an IZO layer with a thickness of 1500-500 Å is deposited and photo-etched to form a plurality of pixel electrodes **190** connected to the drain electrodes **175**, a plurality of contact assistants **95** connected to the expanded end portions **125** of the gate lines **121**, a plurality of contact assistants **97** connected to the expanded end portions **179** of the data lines **171**, and a plurality of bridges **92** connecting the second source electrodes **173***b* and the storage electrode lines **131**. (Fourth Mask)

Since Cr etchant can be used as an etchant for an IZO layer, the exposed portions of the metal for the data wire and the gate wire through the contact holes are not corroded in the photo-etching step for forming the pixel electrodes **190**, the contact assistants **95** and **97** and the bridges **92** from the IZO layer. An example of the Cr etchant is $(HNO_3/(NH_4)_2Ce(NO_3)_6/H_2O)$. The IZO layer is deposited at temperature preferably in a range from a room temperature to 200° C. for minimizing the contact resistance at the contacts. A preferred example of a target for the IZO layer includes In_2O_3 and ZnO. The content of ZnO is preferably in a range between 15 atm % and 20 atm %.

Meanwhile, nitrogen gas is preferably used for the preheating process before the deposition of the ITO layer or the IZO layer. This is to prevent the formation of metal oxides on portions of the metallic layers exposed through the contact holes **181**, **182**, **183**, **184**, **185** and **186**.

FIG. **12** is a schematic diagram of the TFT array panels for an LCD shown in FIGS. **2**A and **4** according to an embodiment of the present invention.

A TFT T**1** connected to a data line **171** switches signals transmitted to a pixel electrode **190** while a TFT T**2** connected to a storage electrode line switches signals entering a DCE **178**. The pixel electrode **190** and the DCE **178** is capacitively coupled. For the same gray, there is no variation of the potential difference between the DCE **178** and the pixel electrode **190**. Therefore, stability of image quality is ensured irrespective of inversion types such as line inversion, dot inversion or the like.

A source electrode of a DCE TFT according to the first and the second embodiments of the present invention is connected to a storage electrode line. However, the source electrode may be connected to a previous data line, which has some problems.

First, the application of the gate-on voltage to a previous gate line (represented as Gate N-**1** in FIG. **1**) causes a pixel electrode located diagonal to a relevant pixel applied with a gray voltage and a DCE of the relevant pixel applied with an initial voltage. The initial voltage of the DCE is equal to the gray voltage of the diagonally-located pixel electrode. Accordingly, the potential difference V_{DP} between the DCE and a pixel electrode of the relevant pixel is determined by the gray voltage of the diagonally-located pixel electrode. For example, a low gray voltage such as a black voltage applied to the diagonally-located pixel electrode causes the low initial voltage of the DCE, thereby resulting in a low V_{DP}. A low V_{DP} means that the potential difference between the DCE and the pixel electrode is small, and thus lateral field due to the DCE is weak. Accordingly, the arrangement of the liquid crystal molecules is unstable, thereby causing unstable texture. In order to short response time, the texture is preferably stable, which is obtained by the potential difference V_{DP} higher than about 5 V.

Next, the V_{DP} is defined by a voltage across a capacitor CDP, which is serially connected to an equivalent capacitor of C_{LC} and C_{ST}. Accordingly, the value of V_{DP} increases as the capacitance C_{DP} decreases. For reducing the capacitance CDP, the overlapping area between the pixel electrode and the DCE is designed to be minimized. However, this may cause image quality to be sensitively varied by misalignment of a mask during a manufacturing process and light leakage near the DCE. For the former case, the mask misalignment changes the overlapping area of the pixel electrode and the DCE, and this directly affect on the image quality. The latter case occurs when the initial voltage of the DCE is high (that is, the gray voltage applied to the diagonally-located pixel electrode is high) and a black voltage is applied to the relevant pixel. The high voltage of the DCE forces to move the liquid crystal molecules to yield light leakage, which may not be blocked by the narrow DCE. The light leakage decreases contrast ratio.

A third embodiment for solving these problems will be described now.

FIG. **13** is an equivalent circuit diagram of an LCD according to a third embodiment of the present invention.

An LCD according to an embodiment of the present invention includes a TFT array panel, a color filter array panel opposite the TFT array panel, and a liquid crystal layer interposed therebetween. The TFT array panel is provided with a plurality of gate lines and a plurality of data lines intersecting each other to define a plurality of pixels, and a plurality of storage electrode lines extending parallel to the gate lines. The gate lines transmit scanning signals and the data lines transmit image signals. A common voltage Vcom is applied to the storage electrode lines. Each pixel is provided with a pixel TFT for a pixel electrode and first and second DCE TFTs DCETFT**1** and DCETFT**2** for a DCE. The pixel TFT includes a gate electrode connected to a relevant gate line, a source electrode connected to a relevant data line, and a drain electrode connected to a relevant pixel electrode. The first DCE TFT includes a gate electrode connected to a previous gate line, a source electrode connected to a previous data line, and a drain electrode connected to a relevant DCE, while the second DCE TFT includes a gate electrode connected to the previous gate line, a source electrode connected to the relevant data line, and a drain electrode connected to the relevant pixel electrode.

The DCE is capacitively coupled with the pixel electrode, and the capacitor therebetween or its capacitance is represented by C_{DP}. The pixel electrode and a common electrode provided on the color filter array panel form a liquid crystal capacitor, and the liquid crystal capacitor or its capacitance is represented by C_{LC}. The pixel electrode and a storage electrode connected to one of the storage electrode lines form a storage capacitor, and the storage capacitor or its capacitance is represented by C_{ST}.

Although it is not shown in the circuit diagram, the pixel electrode according to an embodiment of the present invention has a cutout overlapping the DCE such that the electric field due to the DCE flows out through the cutout. The electric field flowing out through the cutout makes the liquid crystal molecules have pretilt angles. The pretilted liquid crystal molecules are rapidly aligned without dispersion along predetermined directions upon the application of the electric field due to the pixel electrode.

The LCD is assumed to be subject to dot inversion. The application of a gate-on signal to the previous gate line Gate N-**1** turns on both the DCE TFTs DCETFT**1** and DCETFT**2** to make the DCE have a (+) gray voltage and to make the pixel electrode have a (−) gray voltage. The initial voltage of the DCE is the difference between the positive gray voltage and the negative gray voltage from the data lines Data A and Data B, respectively, which is twice or more the initial voltage of the DCE without the second DCE TFT DCETFT**2**. When the pixel TFT is turned on and the DCE TFTs DCETFT**1** and DCETFT**2** are turned off upon application of the gate-on signal to the relevant gate line Gate N, the DCE floats and thus the potential of the DCE also increases with maintaining the potential difference V_{DP} from the potential of the pixel electrode. Accordingly, the structure according to the third embodiment ensures higher V_{DP} to enhance the stability of the arrangement of the liquid crystal molecules, thereby stabilizing the texture.

Furthermore, since the V_{DP} is determined by the gray voltages of two adjacent previous pixels and is rarely affected by the capacitance C_{DP}, the capacitance C_{DP} need not be reduced to allow the DCE to have a sufficient width for overlapping the pixel electrode. Accordingly, the light leakage near the DCE is blocked and the image quality is not considerably affected by the mask misalignment.

In addition, the high VDP improves the response time and the afterimage.

The structure shown in FIG. **13** is suitable for dot inversion and line inversion, while other structures having modified connections of three TFTs may be adapted for other types of inversion.

Now, an exemplary TFT array panel for an LCD according to the third embodiment of the present invention is described in detail with reference to FIGS. **14** to **17**.

FIG. **14** is a layout view of an LCD according to the third embodiment of the present invention, FIG. **15** is a sectional view of the LCD shown in FIG. **14** taken along the line XV-XV', FIG. **16** is a sectional view of the LCD shown in FIG. **14** taken along the line XVI-XVI', FIG. **17** is a sectional view of the LCD shown in FIG. **14** taken along the lines XVII-XVII' and XVII'-XVII".

An LCD according to a third embodiment of the present invention includes a lower panel, an upper panel facing the lower panel, and a vertically aligned liquid crystal layer interposed between the lower panel and the upper panel.

The lower panel will now be described more in detail.

A plurality of gate lines **121** are formed on an insulating substrate **110** and a plurality of data lines **171** are formed thereon. The gate lines **121** and the data lines **171** are insulated from each other and intersect each other to define a plurality of pixel areas.

Each pixel area is provided with a pixel TFT, a first DCE TFT, a second DCE TFT, a DCE and a pixel electrode. The pixel TFT has three terminals, a first gate electrode **123***a*, a first source electrode **173***ab* and a first drain electrode **175***a*. The first DCE TFT has three terminals, a second gate electrode **123***b*, the first source electrode **173***ab* and a second drain electrode **175***b* while the second DCE TFT has three terminals, a third gate electrode **123***c*, a second source electrode **173***c* and a third drain electrode **175***c*. The first source electrode **173***ab* is used both for the pixel TFT and the first DCE TFT. The pixel TFT and the first DCE TFT are provided for switching the signals transmitted to the pixel electrode **190** while the second DCE TFT is provided for switching the signals entering the DCE **178**. The gate electrode **123***a*, the source electrode **173***a* and the drain electrode **175** of the pixel TFT are connected to relevant one of the gate lines **121**, relevant one of the data lines **171** and the pixel electrode **190**, respectively. The gate electrode **123***b*, the source electrode **173***b* and the drain electrode **175***b* of the first DCE TFT are connected to previous one of the gate lines **121**, the relevant data line **171** and the pixel electrode **190**, respectively. The gate electrode **123***c*, the source electrode **173***c* and the drain electrode **175***c* of the second DCE TFT are connected to the previous gate line **121**, previous one of the data lines **171** and the DCE **178**, respectively. The DCE **178** is applied with a direction-controlling voltage for controlling the pre-tilts of the liquid crystal molecules to generate a direction-controlling electric field between the DCE **178** and the common electrode **270**. The DCE **178** is formed in a step for forming the data lines **171**.

The layered structure of the lower panel will be described in detail.

A plurality of gate lines **121** extending substantially in a transverse direction are formed on an insulating substrate **110**, and a plurality of first to third gate electrodes **123***a*-**123***c* are connected to the gate lines **121**. One end portion **125** of each gate line **121** is widened.

A plurality of first and second storage electrode lines **131***a* and **131***b* and a plurality of sets of first to fourth storage electrodes **133***a*, **133***b*, **133***c* and **133***d* are also formed on the insulating substrate **110**. The first and the second storage electrode lines **131***a* and **131***b* extend substantially in the transverse direction. The first and the second storage electrodes **133***a* and **133***b* extend from the first and the second storage electrode lines **131***a* and **131***b* in a longitudinal direction and are curved to extend in an oblique direction while the third and the fourth storage electrodes **134***a* and **134***b* extend in the longitudinal direction. A first storage wire including the first storage electrode lines **131***a* and the first and the third electrodes **133***a* and **134***a* and a second storage wire including the second storage electrode lines **131***b* and the second and the fourth electrodes **133***b* and **134***b* have inversion symmetry.

The gate wire **121**, **123***a*-**123***c* and **125** and the storage electrode wire **131**, **133***a*, **133***b*, **134***a* and **134***b* are preferably made of Al, Cr or their alloys, Mo or Mo alloy. If necessary, the gate wire **121**, **123***a* and **123***b* and the storage electrode wire **131** and **133***a*-**133***d* include a first layer preferably made of Cr or Mo alloys having excellent physical and chemical characteristics and a second layer preferably made of Al or Ag alloys having low resistivity.

A gate insulating layer **140** is formed on the gate wire **121**, **123***a*-**123***c* and **125** and the storage electrode wire **131**, **133***a*, **133***b*, **134***a* and **134***b*.

A semiconductor layer **151**, **154***ab* and **154***c* preferably made of amorphous silicon is formed on the gate insulating layer **140**. The semiconductor layer **151**, **154***ab* and **154***c* includes a plurality of first and second channel semiconductors **154***ab* and **154***c* forming channels of TFTs and a plurality of data-line semiconductors **151** located under the data lines **171**.

An ohmic contact layer **161**, **163***ab*, **163***c* and **165***a*-**165***c* preferably made of silicide or n+ hydrogenated amorphous silicon heavily doped with n type impurity is formed on the semiconductor layer **151**, **154***ab* and **154***c*.

A data wire **171**, **173***ab*, **173***c*, **175***a*-**175***c* and **179** is formed on the ohmic contact layer **161**, **163***ab*, **163***c* and **165***a*-**165***c* and the gate insulating layer **140**. The data wire **171**, **173***ab*, **173***c*, **175***a*-**175***c* and **179** includes a plurality of data lines **171** extending in the longitudinal direction and intersecting the gate lines **121** to form a plurality of pixels, a plurality of first source electrodes **173***ab* branched from the data lines **171** and extending onto portions **163***ab* of the ohmic contact layer, a plurality of first and second drain electrodes **175***a* and **175***b* disposed on portion **165***a* and **165***b* of the ohmic contact layer, located opposite the first source electrodes **173***ab* and separated from the first source electrodes **173***ab*, and a plurality of second source electrodes **173***c* and a plurality of third drain electrodes **175***c* disposed on respective portions **163***c* and **165***c* opposite each other with respect to the third gate electrodes **123***c*. One end portion of each data line **171** is widened for connection to an external circuit.

A plurality of DCEs **178** and **178***a*-**178***c* are formed in the pixel areas defined by the intersections of the gate lines **121** and the data lines **171**. Each DCE **178** and **178***a*-**178***c* includes a V-shaped stem **178** and a chevron-shaped branch **178***a*-**178***c* and is connected to the third drain electrode **175***c*. The data wire **171**, **173***ab*, **173***c*, **175***a*-**175***c* and **179** and the DCEs **178** and **178***a*-**178***c* are preferably made of Al, Cr or their alloys, Mo or Mo alloy. If necessary, the data wire **171**, **173***ab*, **173***c*, **175***a*-**175***c* and **179** and the DCEs **178** and **178***a*-**178***c* include a first layer preferably made of Cr or Mo alloys having excellent physical and chemical characteristics and a second layer preferably made of Al or Ag alloys having low resistivity.

A passivation layer **180** preferably made of silicon nitride or organic insulator is formed on the data wire **171**, **173***ab*, **173***c*, **175***a*-**175***c* and **179**.

The passivation layer **180** is provided with a plurality of first and second contact holes **181** and **182** exposing the first and the second drain electrodes **175***a* and **175***b*, a plurality of third contact holes **183** extending to the gate insulating layer **140** exposing the end portions **125** of the gate lines **121**, and a plurality of fourth contact holes **184** exposing the end portions **179** of the data lines **171**. The contact holes exposing the end portions **125** and **179** may have various shapes such as polygon or circle. The area of the contact hole is preferably equal to or larger than 0.5 mm×15 μm and not larger than 2 mm×60 μm.

A plurality of pixel electrodes **190** are formed on the passivation layer **180**. Each pixel electrode **190** is connected to the first and the second drain electrode **175***a* and **175***b* through the first and the second contact holes **181** and **182**, respectively. The pixel electrode **190** has a transverse cutout **191** and a plurality of oblique cutouts **192***a*, **192***b*, **193***a*, **193***b*, **194***a*, **194***b*, **195***a* and **195***b*. The transverse cutout **191** bisects the pixel electrode **190** into upper and lower halves, and the oblique cutouts **192***a*, **192***b*, **193***a*, **193***b*, **194***a*, **194***b*, **195***a* and **195***b* have inversion symmetry with respect to the transverse cutout **191**. Some cutouts **191**, **192***a*, **192***b*, **194***a*, **194***b*, **195***a* and **195***b* overlap the DCE **178** and **178***a*-**178***c* while the other cutouts **193***a* and **193***b* overlap the storage electrodes **133***a* and **133***b*.

Furthermore, a plurality of contact assistants **95** and **97** are formed on the passivation layer **180**. The contact assistants **95** and **97** are connected to the end portions **125** and **179** through the contact holes **183** and **184**, respectively. The pixel electrodes **190** and the contact assistants **95** and **97** are preferably formed of IZO. Alternatively, the pixel electrodes **190** and the contact assistants **95** and **97** are preferably made of ITO.

To summarize, each pixel electrode **190** has the plurality of cutouts **191**, **192***a*, **192***b*, **193***a*, **193***b*, **194***a*, **194***b*, **195***a* and **195***b* for partitioning a pixel region into a plurality of domains, and the cutouts **191**, **192***a*, **192***b*, **194***a*, **194***b*, **195***a* and **195***b* overlap the DCE **178** and **178***a*-**178***c*. The DCE **178** and **178***a*-**178***c* and the cutouts **191**, **192***a*, **192***b*, **194***a*, **194***b*, **195***a* and **195***b* are aligned such that the DCE **178** and **178***a*-**178***c* is exposed through the cutouts **191**, **192***a*, **192***b*, **194***a*, **194***b*, **195***a* and **195***b* to be seen in front view. The DCE **178** and **178***a*-**178***c* is connected to the second DCE TFT while the pixel electrode **190** is connected to the first DCE TFT the pixel TFT, and the pixel electrode **190** and the DCE **178** are aligned to form a storage capacitance.

According to another embodiment of the present invention, the DCEs **178** and **178***a*-**178***c* include substantially the same layer as the gate wire **121**, **123***a*-**123***c* and **125**. The portions of the passivation layer **180** on the DCEs **178** and **178***a*-**178***c* may be removed to form a plurality of openings.

The upper substrate **210** will no be described in detail.

A black matrix **220** for preventing light leakage, a plurality of red, green and blue color filters **230**, and a common electrode **270** preferably made of a transparent conductor such as ITO or IZO are formed on an upper substrate **210** preferably made of transparent insulating material such glass.

A plurality of liquid crystal molecules contained in the liquid crystal layer **3** is aligned such that their director is perpendicular to the lower and the upper substrates **110** and **210** in absence of electric field. The liquid crystal layer **3** has negative dielectric anisotropy.

The lower substrate **110** and the upper substrate **210** are aligned such that the pixel electrodes **190** exactly match and overlap the color filters **230**. In this way, a pixel region is divided into a plurality of domains by the cutouts **191**, **192***a*, **192***b*, **193***a*, **193***b*, **194***a*, **194***b*, **195***a* and **195***b*. The alignment of the liquid crystal layer **3** in each domain is stabilized by the DCE **178** and **178***a*-**178***c*.

This embodiment illustrates the liquid crystal layer **3** having negative dielectric anisotropy and homeotropic alignment with respect to the substrates **110** and **210**. However, the liquid crystal layer **3** may have positive dielectric anisotropy and homogeneous alignment with respect to the substrates **110** and **210**.

A TFT array panel according to the third embodiment of the present invention may be manufactured using four photo-etching steps. In this case, a data wire and DCEs have a triple-layered structure including an amorphous silicon layer, an ohmic contact layer and a metal layer, and the triple layers have substantially the same planar shape, which is resulted from the patterning of the amorphous silicon layer, the ohmic contact layer and the metal layer using a photoresist film. Since such a manufacturing method is described in detail in the description about the second embodiment of the present invention, the manufacturing method is understood in view of the fact that the patterns made of the same layer(s) are formed in the same step and thus the detailed description thereof is omitted.

The third embodiment provides three TFTs in each pixel for improve the low voltage difference V_{DP} in case of connecting the source electrode of the DCE TFT to the previous data line, the sensitive change of image quality due to misalignment of the mask during the manufacturing process, the light leakage near the DCE, and so on.

However, the increase of the number of the TFTs in each pixel decreases the aperture ratio and makes it difficult to providing a repairing mechanism for repairing wire defects in the manufacturing process.

The following embodiments suggest driving mechanisms that make two TFTs comparing with three TFTs.

FIG. **18** is a circuit diagram of an LCD according to a fourth embodiment of the present invention, FIG. **19** illustrates polarity of the pixels of the LCD according to the fourth embodiment of the present invention, and FIG. **20** shows waveforms of scanning signals of the LCD according to the fourth embodiment of the present invention.

An LCD according to a fourth embodiment of the present invention also includes a TFT array panel, a color filter array panel opposite the TFT array panel, and a liquid crystal layer interposed therebetween. The TFT array panel is provided with a plurality of gate lines and a plurality of data lines intersecting each other to define a plurality of pixels. The gate lines transmit scanning signals and the data lines transmit image signals. Each pixel is provided with a pixel TFT T**1** for a pixel electrode and a DCE TFT T**2** for a DCE. The pixel TFT T**1** includes a gate electrode connected to a relevant gate line G_n, a source electrode connected to a relevant data line D_m, and a drain electrode connected to a relevant pixel electrode. The DCE TFT T**2** includes a gate electrode connected to a previous gate line G_{n-1}, a source electrode connected to a next data line D_{m+1}, and a drain electrode connected to a relevant DCE. The source electrode of the DCE TFT T**2** may be connected to a previous data line D_{m-1}.

The DCE is capacitively coupled with the pixel electrode, and the capacitor therebetween or its capacitance is represented by Cdp. The pixel electrode and a common electrode provided on the color filter array panel form a liquid crystal capacitor, and the liquid crystal capacitor or its capacitance is represented by Clc. The pixel electrode and a storage electrode, which is indicated as a ground, form a storage capacitor, and the storage capacitor or its capacitance is represented by Cst. The DCE forms capacitors along with the common electrode and the storage electrode, and the capacitors or their capacitances are represented by Cld and Cdg, respectively.

Although it is not shown in the circuit diagram, the pixel electrode according to this embodiment of the present invention has a cutout overlapping the DCE such that the electric field due to the DCE flows out through the cutout. The electric field flowing out through the cutout makes the liquid crystal molecules tilt along predetermined directions like the previous embodiments.

A dot inversion shown in FIG. **19** and dual-pulse gate signals shown in FIG. **20** can make the LCD shown in FIG. **18** function like the LCD according to the third embodiment.

A dual-pulse gate signal has two consecutive gate-on pulses in a frame, the first pulse for charging the DCE and the second pulse for applying data voltages to the pixel electrode. The first pulse of a gate signal is synchronized with the second pulse of a gate signal for a previous gate line.

The charging of the LCD shown in FIGS. **18-20** is described in detail.

Let us assume that a pixel electrode and a DCE of a pixel in the n-th row and the m-th column are charged with −5V and −15V, respectively. Now, the pixel electrode will be refreshed by a voltage +5V.

The voltage Vp of the pixel electrode and the voltage Vdce of the DCE are

$$Vp=-5\text{V and } Vdce=-15V. \tag{1}$$

When the pixels in the (n−2)-th row are refreshed, the gate line G_{n-2} is supplied with the second pulse, while the gate line G_{n-1} is supplied with the first pulse. In addition, the data line D_{m+1} is supplied with −5V under the dot inversion. Then, the DCE TFT T**2** of the pixel in the n-th row and the m-th column having a gate electrode and a source electrode respectively connected to the gate line G_{n-1} and the data line D_{m+1} is turned on to supply a voltage of −5V to the DCE, thereby charging the capacitor Cdp and the capacitors Clc and Cst in series.

$$Vp>-5V \text{ and } Vdce=-5V. \tag{2}$$

When the pixels in the (n−1)-th row are refreshed, the gate line G_{n-1} is supplied with the second pulse, while the gate line G_n is supplied with the first pulse. In addition, the data lines D_{m+1}, and D_m are supplied with +5V and −5V, respectively, under the dot inversion. Then, both the pixel TFT T**1** and the DCE TFT T**2** of the pixel in the n-th row and the m-th column are turned on to supply a voltage of −5V to the pixel electrode and a voltage of +5V to the DCE.

$$Vp=-5V \text{ and } Vdce=+5V. \tag{3}$$

When the pixels in the n-th row are refreshed, the gate line G_n is supplied with the second pulse, while the gate line G_{n-1} is supplied with no pulse. In addition, the data lines D_m are supplied with +5V. Then, only the pixel TFT T**1** of the pixel in the n-th row and the m-th column are turned on to supply a voltage of +5V to the pixel electrode. If Cld+Cdg<<Cdp, the voltage of the DCE, which is floating to maintain the voltage difference from the pixel electrode, increases along that of the pixel electrode to have a value of +15V.

$$Vp=+5V \text{ and } Vdce=+15V. \tag{4}$$

To summarize, the dual-pulse gate signals enables two TFTs to function as three TFTs. That is, it is possible to obtain a sufficiently high voltage difference Vdp regardless of the capacitance Cdp.

The fourth embodiment facilitates the charging of the DCE by providing stepwise charging as well as reducing a TFT. That is, the second charging step (2) that is not obtained in the third embodiment may enable the smooth charging of the DCE.

FIG. **21** is a circuit diagram of an LCD according to a fifth embodiment of the present invention, and FIG. **22** illustrates polarity of the pixels of the LCD according to the fifth embodiment of the present invention.

An LCD according to a fifth embodiment of the present invention also includes a TFT array panel, a color filter array panel opposite the TFT array panel, and a liquid crystal layer interposed therebetween. The TFT array panel is provided with a plurality of gate lines and a plurality of data lines intersecting each other to define a plurality of pixels.

Each pixel is provided with two TFTs, and the pixels are classified into two kinds depending on the connection of the TFTs.

A first pixel includes a pixel TFT T**1***a* having a gate electrode connected to a relevant gate line G_n, a source electrode connected to a relevant data line D_m, and a drain electrode connected to a relevant pixel electrode and a DCE TFT T**2***a* having a gate electrode connected to a previous gate line G_{n-1}, a source electrode connected to a next data line D_{m+1}, and a drain electrode connected to a relevant DCE.

A second pixel includes a pixel TFT T**1***b* having a gate electrode connected to a relevant gate line G_{n-1} a source electrode connected to a relevant data line D_m, and a drain electrode connected to a relevant pixel electrode and a DCE TFT T**2***b* having a gate electrode connected to a previous gate line G_{n-1}, a source electrode connected to the relevant data line D_m, and a drain electrode connected to a relevant DCE.

The first pixels and the second pixel are alternately arranged along a column direction.

Although it is not shown in the circuit diagram, the pixel electrode according to this embodiment of the present invention has a cutout overlapping the DCE such that the electric field due to the DCE flows out through the cutout. The electric field flowing out through the cutout makes the liquid crystal molecules tilt along predetermined directions like the previous embodiments.

A double-dot inversion shown in FIG. **22** and the dual-pulse gate signals shown in FIG. **20** can make the LCD shown in FIG. **21** function like the LCD according to the fourth embodiment.

In adjacent rows of the first and the second pixels supplied with the data voltages having the same polarity, the first pixels are supplied with the scanning signal prior to the second pixels.

FIG. **23** is a circuit diagram of an LCD according to a sixth embodiment of the present invention, and FIG. **24** illustrates polarity of the pixels of the LCD according to the sixth embodiment of the present invention.

An LCD according to a sixth embodiment of the present invention also includes a TFT array panel, a color filter array panel opposite the TFT array panel, and a liquid crystal layer interposed therebetween. The TFT array panel is provided with a plurality of gate lines and a plurality of data lines intersecting each other to define a plurality of pixels.

Each pixel is provided with a pixel TFT T**1** for a pixel electrode and a DCE TFT T**2** for a DCE. The pixel TFT T**1** includes a gate electrode connected to a relevant gate line G_n, a source electrode connected to a relevant data line D_m, and a drain electrode connected to a relevant pixel electrode. The DCE TFT T**2** includes a gate electrode connected to a previous gate line G_{n-1}, a source electrode connected to the relevant data line D_{m+1}, and a drain electrode connected to a relevant DCE.

Although it is not shown in the circuit diagram, the pixel electrode according to this embodiment of the present invention has a cutout overlapping the DCE such that the electric field due to the DCE flows out through the cutout. The electric field flowing out through the cutout makes the liquid crystal molecules tilt along predetermined directions like the previous embodiments.

A column inversion shown in FIG. **24** and the dual-pulse gate signals shown in FIG. **20** can make the LCD shown in FIG. **23** function like the LCD according to the fourth embodiment.

The dual-pulse gate signals can be applied to cases that the DCE is supplied with a voltage from a storage electrode line, which will be described hereinafter.

FIG. **25** is a circuit diagram of an LCD according to a seventh embodiment of the present invention.

Each pixel of an LCD according to a seventh embodiment of the present invention is provided with a pixel TFT T**1** for a pixel electrode and a DCE TFT T**2** for a DCE. The pixel TFT T**1** includes a gate electrode connected to a relevant gate line G_n, a source electrode connected to a relevant data line D_m, and a drain electrode connected to a relevant pixel electrode. The DCE TFT T**2** includes a gate electrode connected to a previous gate line G_{n-1}, a source electrode connected to a common voltage, and a drain electrode connected to a relevant DCE.

This configuration is substantially the same as those according to the first and the second embodiments since the common voltage is transmitted to the TFT array panel by the storage electrode line.

The dual-pulse gate signals shown in FIG. **20** can make the LCD shown in FIG. **25** function like the LCD according to the fourth to the sixth embodiments. Any of the dot inversion, the double-dot inversion, the column inversion, etc., will have an effect.

The charging of the LCD shown in FIG. **25** is described in detail. For descriptive convenience, the inversion type is limited to the dot inversion.

Let us assume that a pixel electrode and a DCE of a pixel in the n-th row and the m-th column are charged with −5V and −15V, respectively. Now, the pixel electrode will be refreshed by a voltage +5V.

The voltage Vp of the pixel electrode and the voltage Vdce of the DCE are

$$Vp=-5\,V \text{ and } Vdce=-15\,V. \tag{5}$$

When the pixels in the (n−2)-th row are refreshed, the gate line G_{n-2} is supplied with the second pulse, while the gate line G_{n-1}, is supplied with the first pulse. Then, the DCE TFT T**2** of the pixel in the n-th row and the m-th column having a gate electrode connected to the gate line G_{n-1} is turned on to supply the common voltage of 0V (for convenience) to the DCE, thereby charging the capacitor Cdp and the capacitors Clc and Cst in series.

$$Vp>-5\,V \text{ and } Vdce=0\,V. \tag{6}$$

When the pixels in the (n−1)-th row are refreshed, the gate line G_{n-1} is supplied with the second pulse, while the gate line G_n is supplied with the first pulse. In addition, the data line D_m is supplied with −5V under the dot inversion. Then, both the pixel TFT T**1** and the DCE TFT T**2** of the pixel in the n-th row and the m-th column are turned on to supply a voltage of −5V to the pixel electrode and the common voltage of 0V to the DCE.

$$Vp=-5\,V \text{ and } Vdce=0\,V. \tag{7}$$

When the pixels in the n-th row are refreshed, the gate line G_n is supplied with the second pulse, while the gate line G_{n-1} is supplied with no pulse. In addition, the data lines D_m are supplied with +5V. Then, only the pixel TFT T**1** of the pixel in the n-th row and the m-th column are turned on to supply a voltage of +5V to the pixel electrode. The voltage of the DCE, which is floating to maintain the voltage difference from the pixel electrode, increases along that of the pixel electrode to have a value of +10V.

$$Vp=+5\,V \text{ and } Vdce=+10\,V. \tag{8}$$

To summarize, the dual-pulse gate signals enables to obtain a sufficiently high voltage difference Vdp regardless of the capacitance Cdp when the DCE is supplied with the common voltage through the storage electrode line.

As described above, a DCE TFT switching the signals transmitted to a DCE and a pixel electrode to generate initial direction-control voltage, thereby ensuring stable brightness.

Although preferred embodiments of the present invention have been described in detail hereinabove, it should be clearly understood that many variations and/or modifications of the basic inventive concepts herein taught which may appear to those skilled in the present art will still fall within the spirit and scope of the present invention, as defined in the appended claims.

What is claimed is:

1. A liquid crystal display comprising:

a first substrate;

a plurality of first signal lines formed on the first substrate and supplied with scanning signals;

a plurality of second signal lines formed on the first substrate and supplied with data voltages;

a plurality of pixel electrodes formed on the first substrate;

a plurality of direction control electrodes formed on the first substrate;

a plurality of first thin film transistors, each first thin film transistor connected to a relevant one of the first signal lines, a relevant one of the second signal lines, and a relevant one of the pixel electrodes;

a plurality of second thin film transistors, each second thin film transistor connected to a previous one of the first signal lines, a previous one or a next one of the second signal lines, and a relevant one of the direction control electrodes;

a second substrate facing the first substrate; and

a common electrode formed on the second substrate.

2. The liquid crystal display of claim **1**, wherein the liquid crystal display is subjected to a dot inversion and each scanning signal has first and second pulses in a frame.

3. The liquid crystal display of claim **2**, wherein the first pulse in a scanning signal is synchronized with the second pulse in a previous scanning signal.

4. The liquid crystal display of claim **1**, wherein each pixel electrode has a cutout overlapping one of the direction control electrodes at least in part.

* * * * *

专利名称(译)	液晶显示器		
公开(公告)号	US7965345	公开(公告)日	2011-06-21
申请号	US10/793860	申请日	2004-03-08
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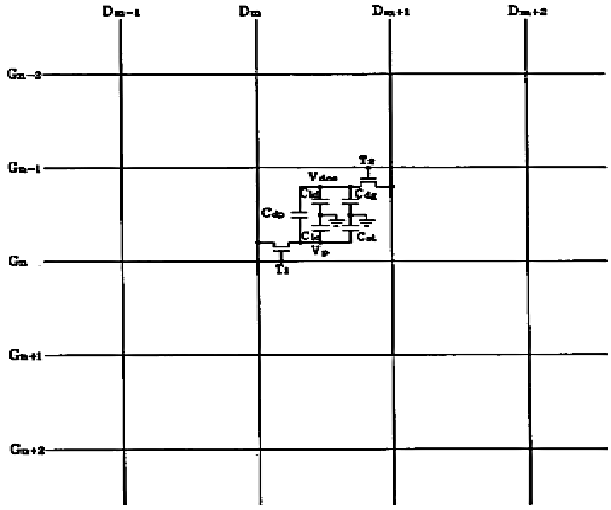
摘要(译)

像素电极和电容耦合到像素电极的方向控制电极设置在像素中。像素薄膜晶体管连接到栅极线，数据线和像素电极。方向控制电极薄膜晶体管连接到前一栅极线，前一数据线或下一数据线，以及方向控制电极。向栅极线提供扫描信号，并且每个扫描信号包括帧中的第一和第二脉冲。扫描信号的第一脉冲与先前扫描信号的第二脉冲同步。



Dm-1
Dm
Dm+1
Dm+2
Gn-2
Gn-1
Gn
Gn+1
Gn+2
T2
Cdp
Vp
T1