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(54) LIQUID CRYSTAL PANEL HAVING COMPENSATION CAPACITORS FOR BALANCING RC DELAY EFFECT

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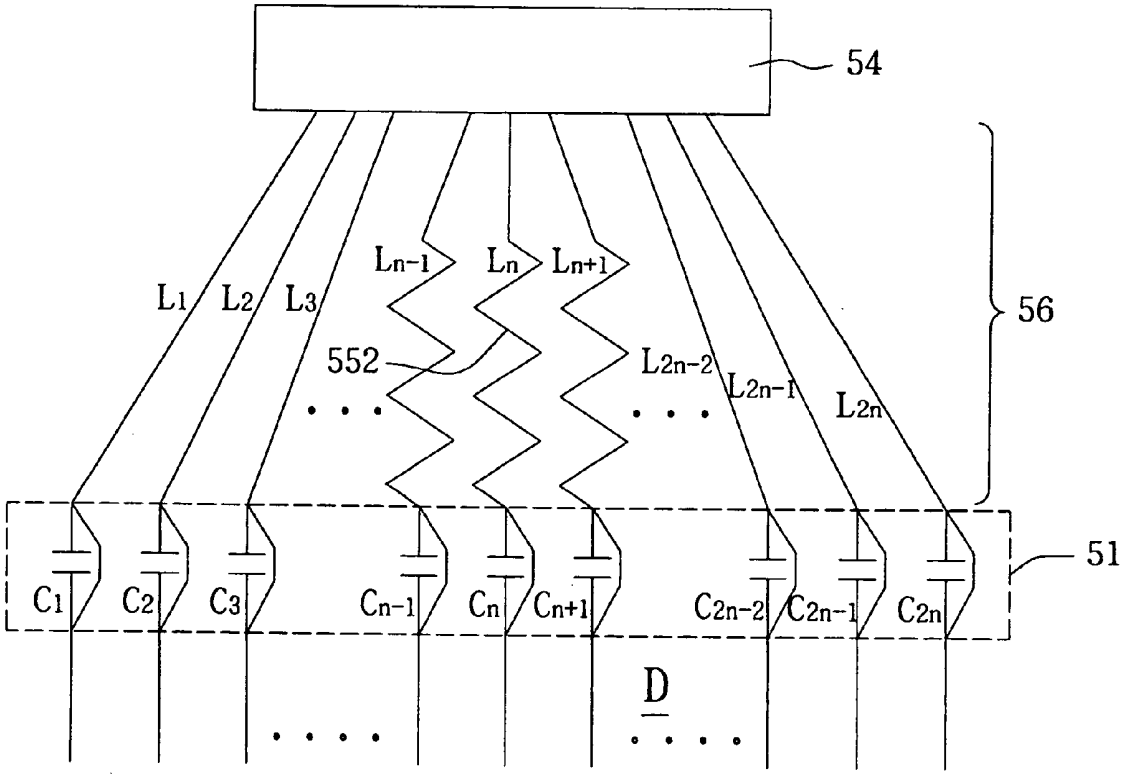
(52) **U.S. Cl.** **313/38**

(57) **ABSTRACT**

A liquid crystal panel comprises an active matrix substrate, an opposing substrate facing the active matrix substrate, and a liquid crystal layer disposed between the active matrix substrate and the opposing substrate. On the active matrix substrate, a plurality of parallel signal lines and a plurality of parallel scanning lines are arranged for forming a matrix of pixels called an active area. A plurality of pads are formed in outer-lead bonding areas located on the periphery of the active area, and are used for mounting driving devices. Each of the OLB areas is separately connected to one of fan-out areas including a plurality of leads. Each compensation capacitor with a predetermined capacitance is connected to each lead so as to minimize variation of RC delay effect between all leads.



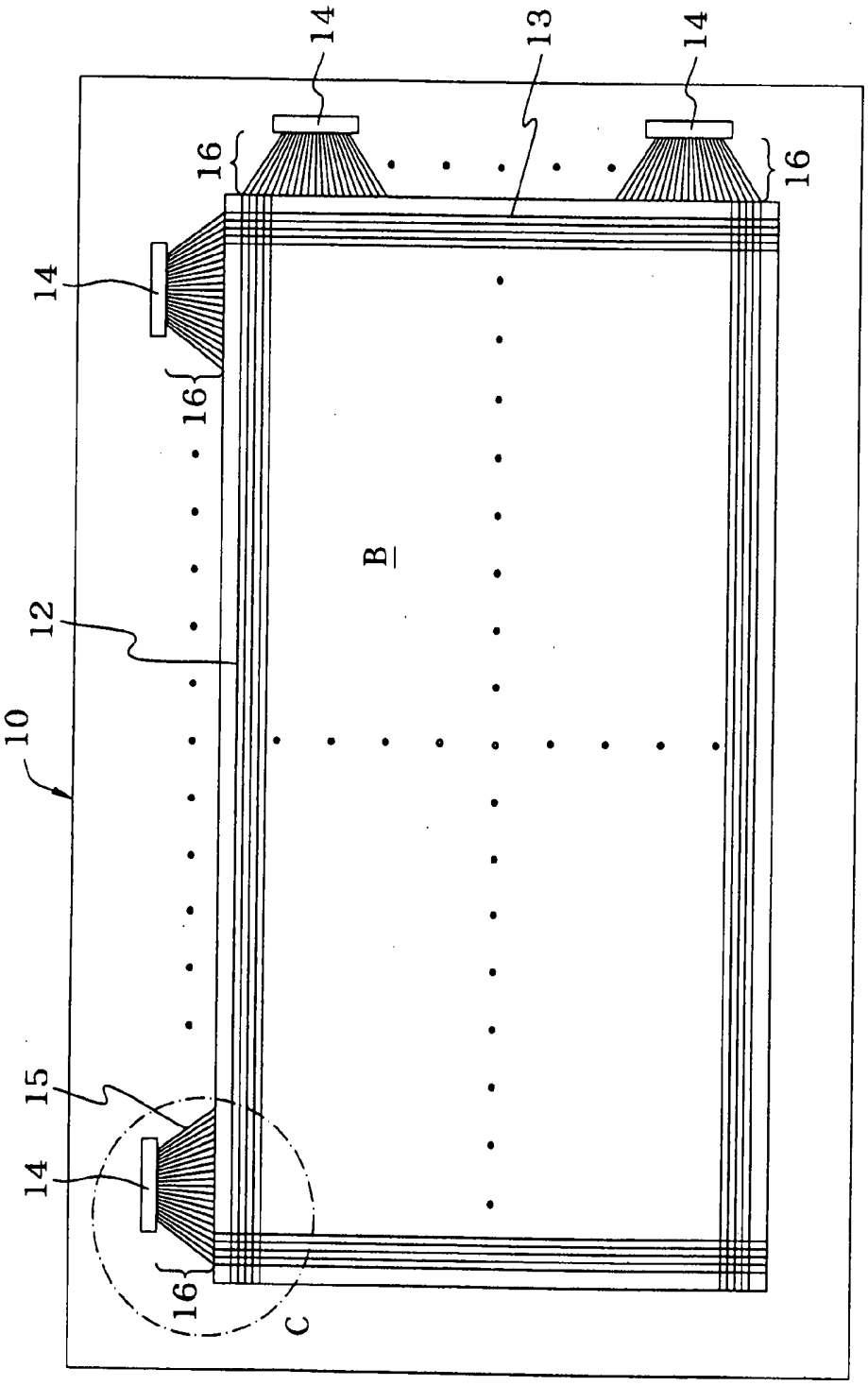


FIG. 1 (Background Art)

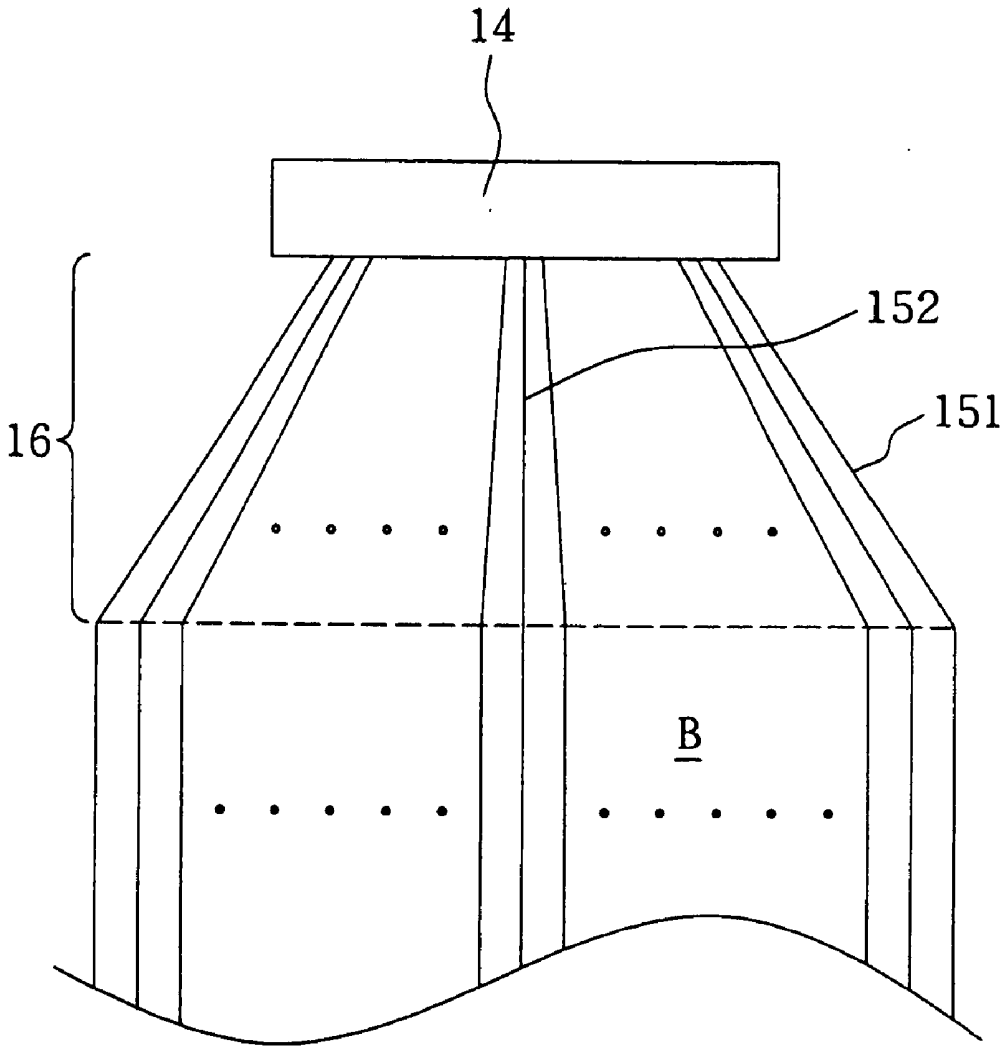


FIG. 2 (Background Art)

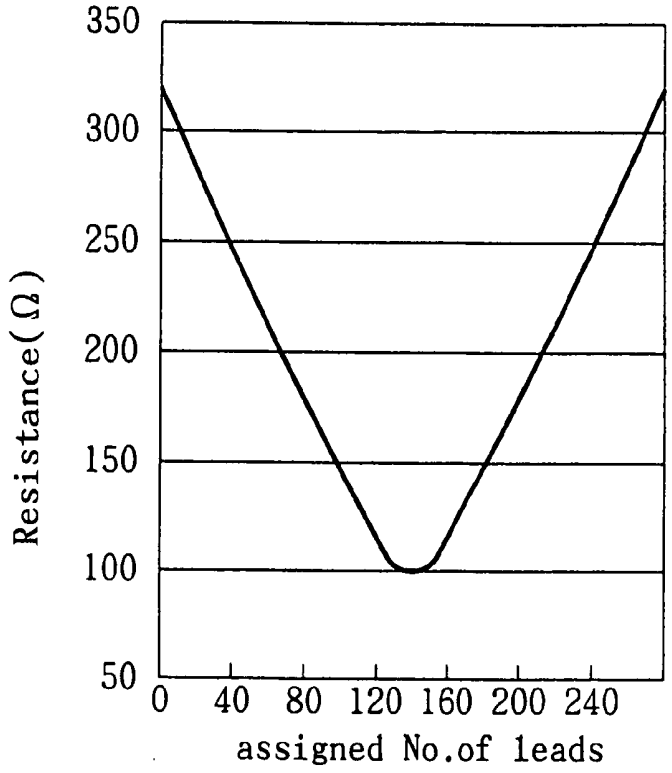


FIG. 3(a) (Background Art)

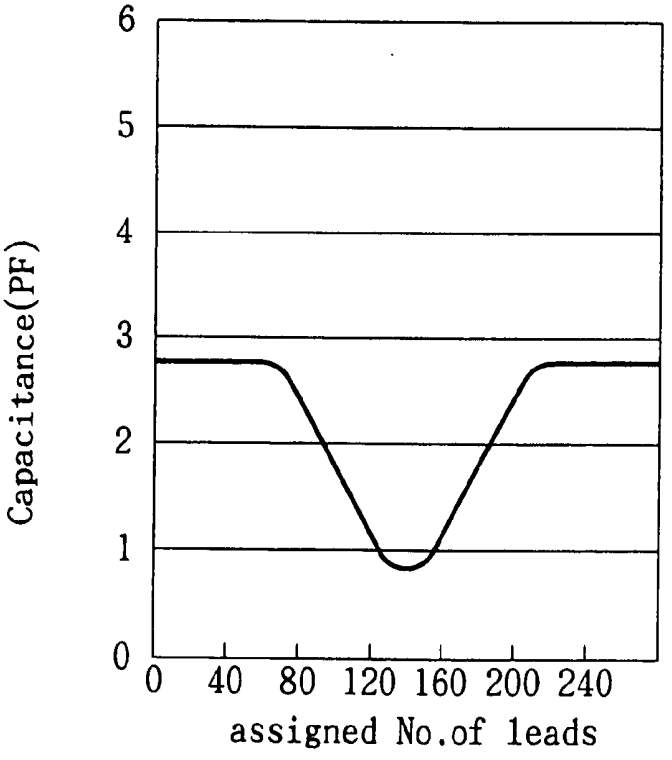


FIG. 3(b) (Background Art)

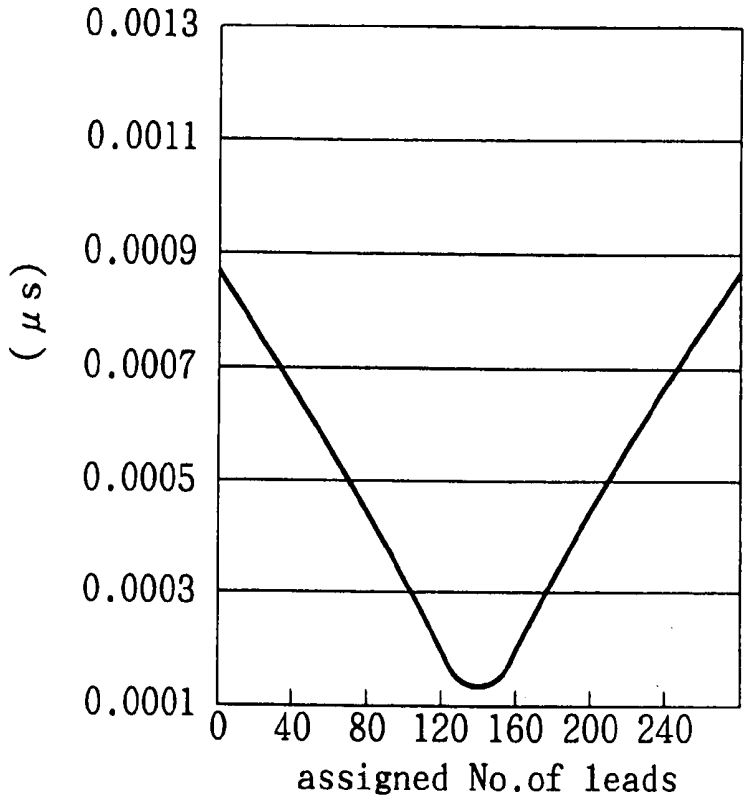


FIG. 3(c) (Background Art)

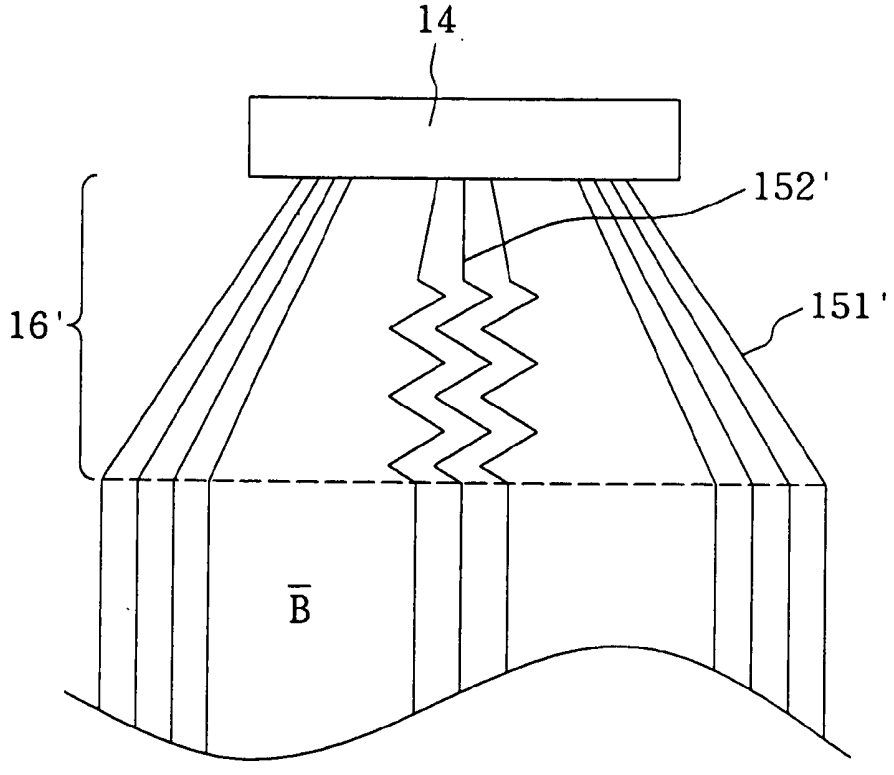


FIG. 4 (Background Art)

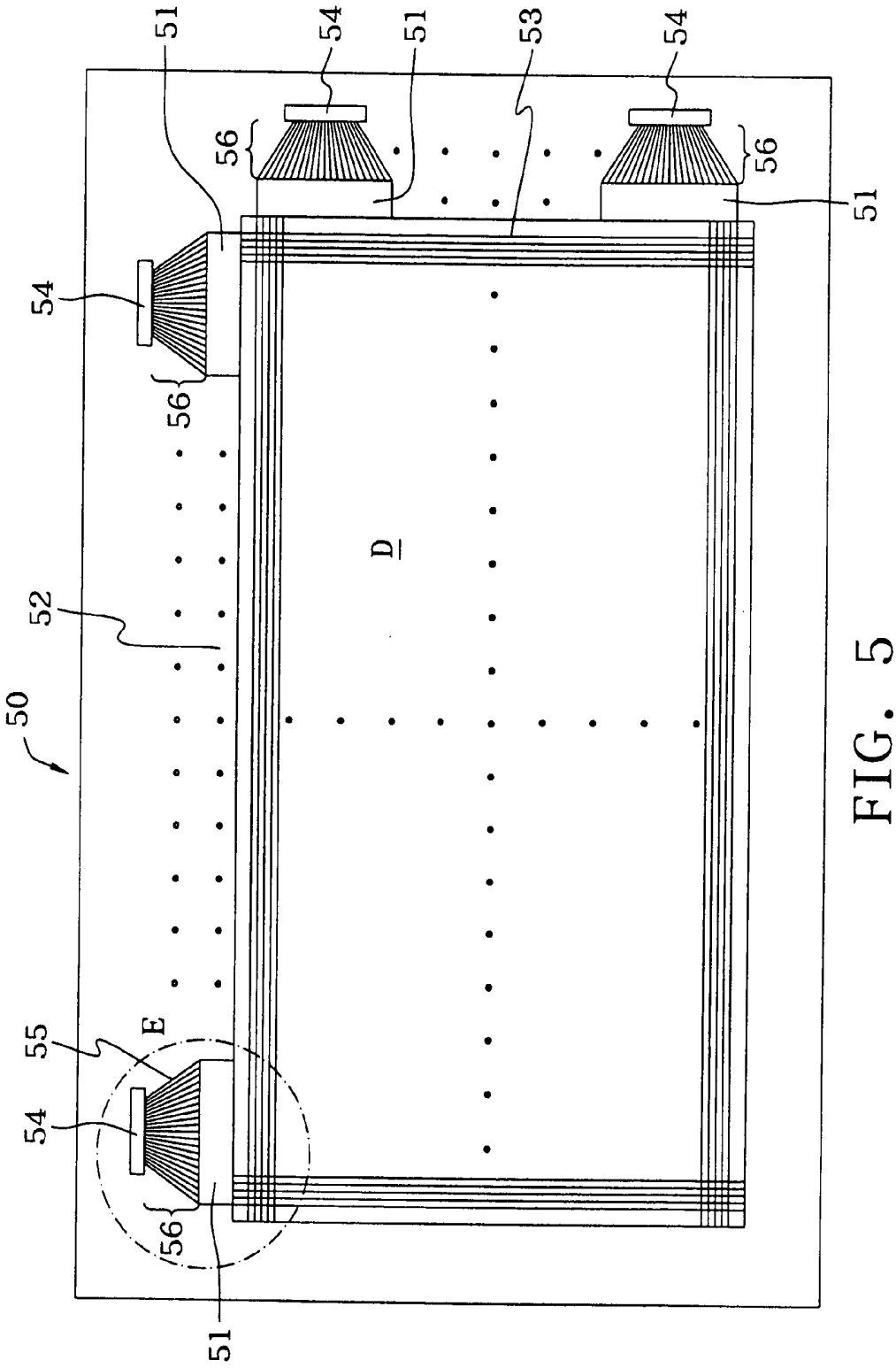


FIG. 5

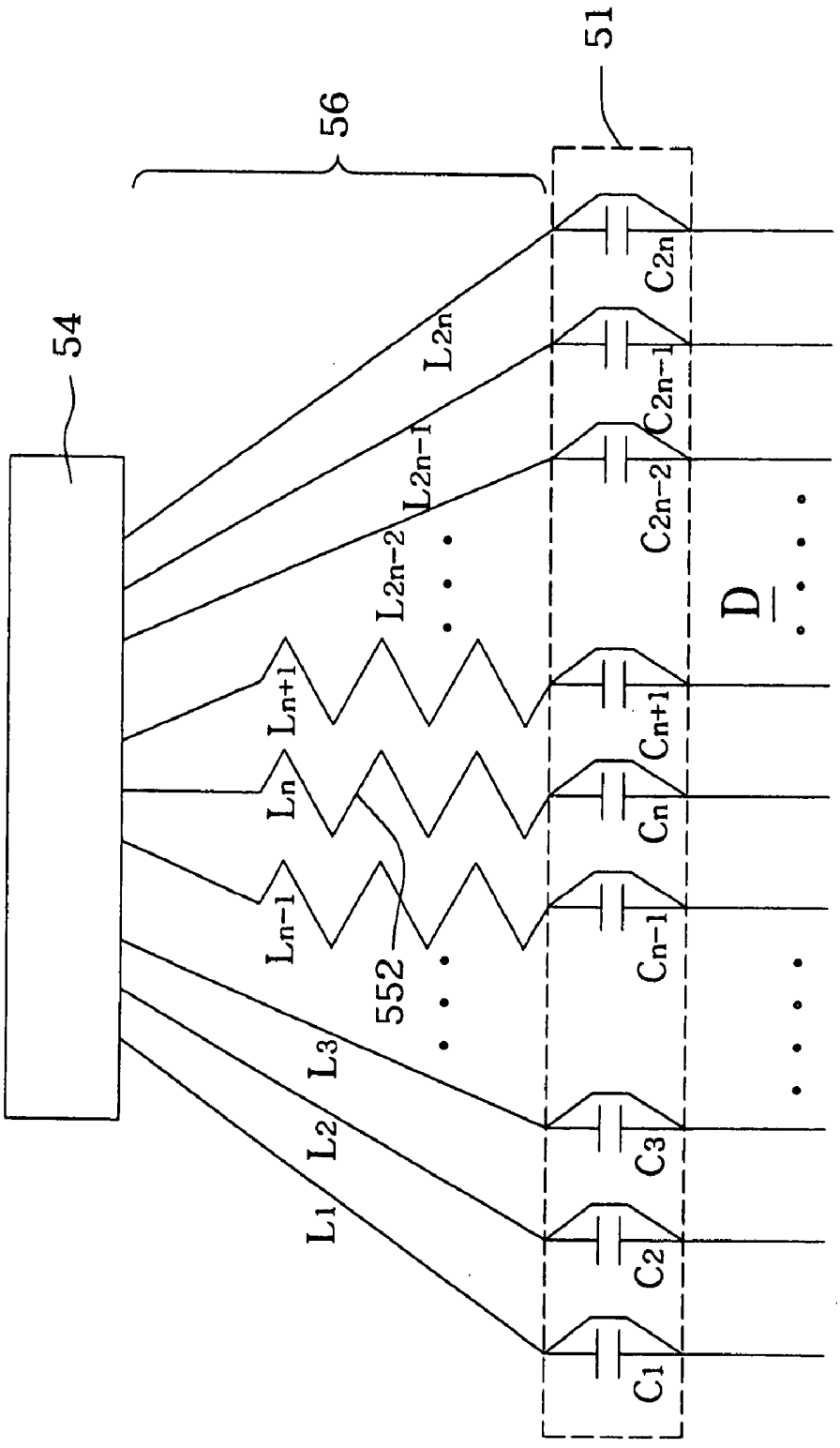

51
56
54
552
D
L2n
L2n-1
L2n-2
Ln+1
Ln
Ln-1
L3
L2
L1
C2n
C2n-1
C2n-2
Cn+1
Cn
Cn-1
C3
C2
C1

FIG. 6(a)

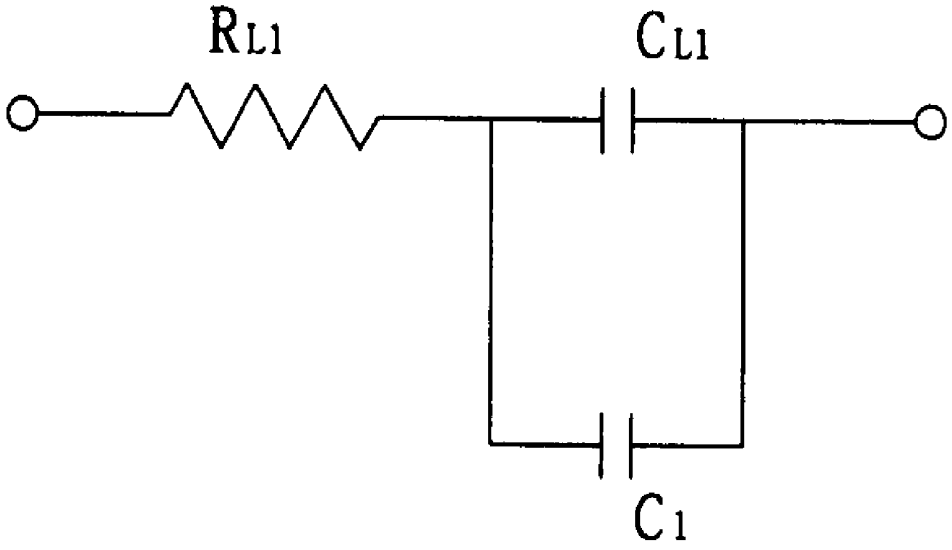


FIG. 6(b)

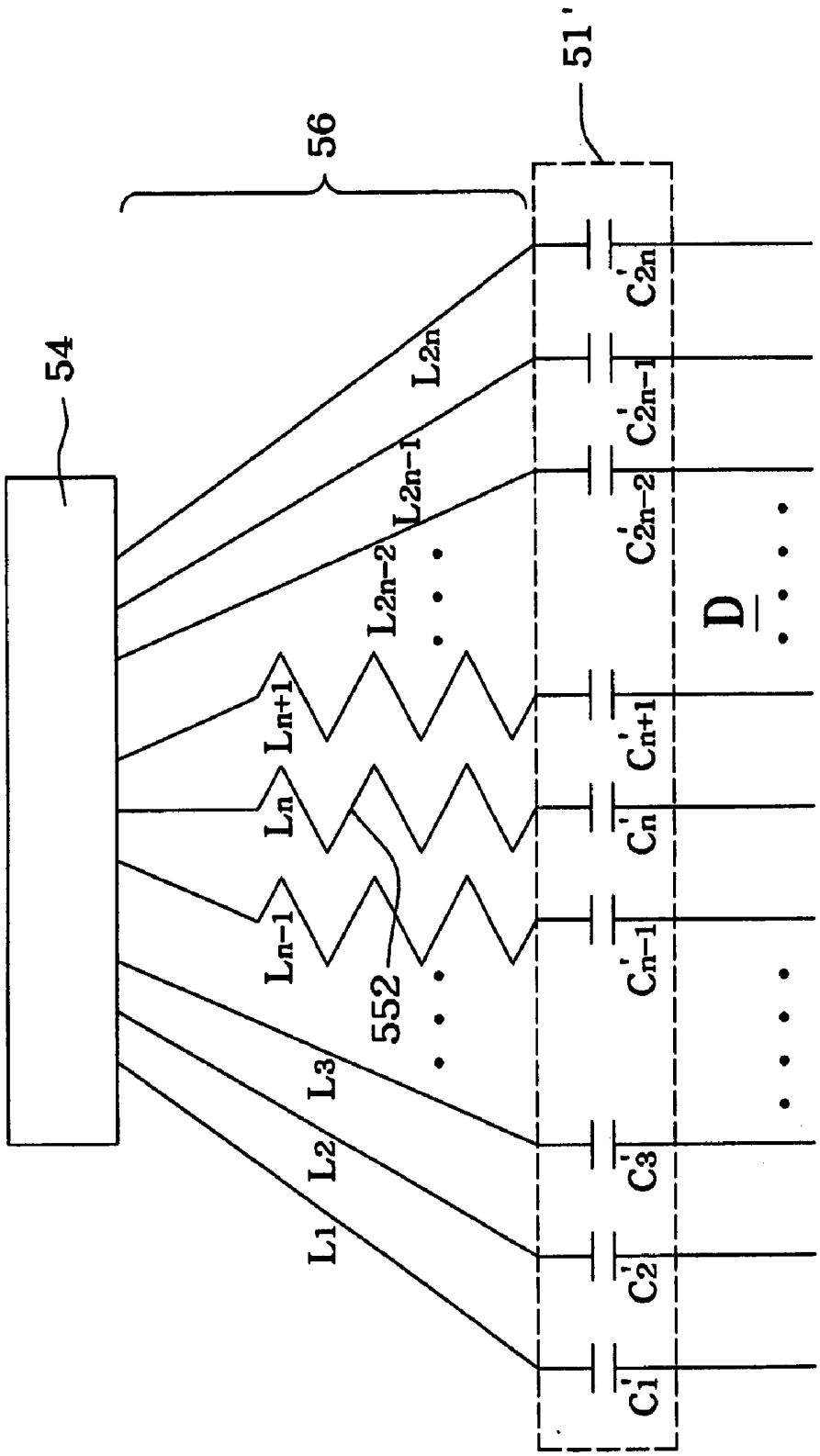

51'
56
54
552
D
L1
L2
L3
Ln-1
Ln
Ln+1
L2n-2
L2n-1
L2n
C'1
C'2
C'3
C'n-1
C'n
C'n+1
C'2n-2
C'2n-1
C'2n

FIG. 6(c)

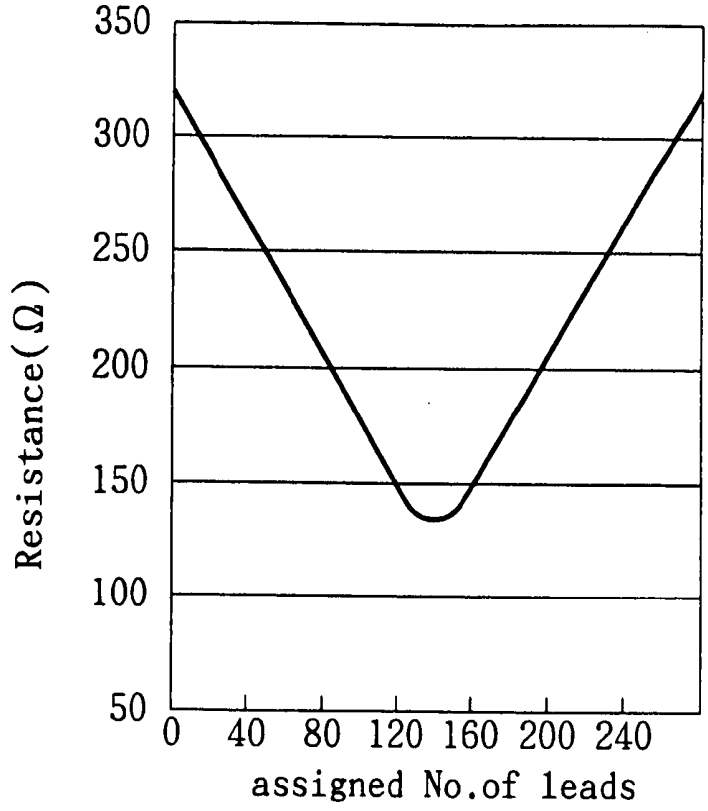

350
300
250
200
150
100
50
Resistance(Ω)
0 40 80 120 160 200 240
assigned No.of leads

FIG. 7(a)

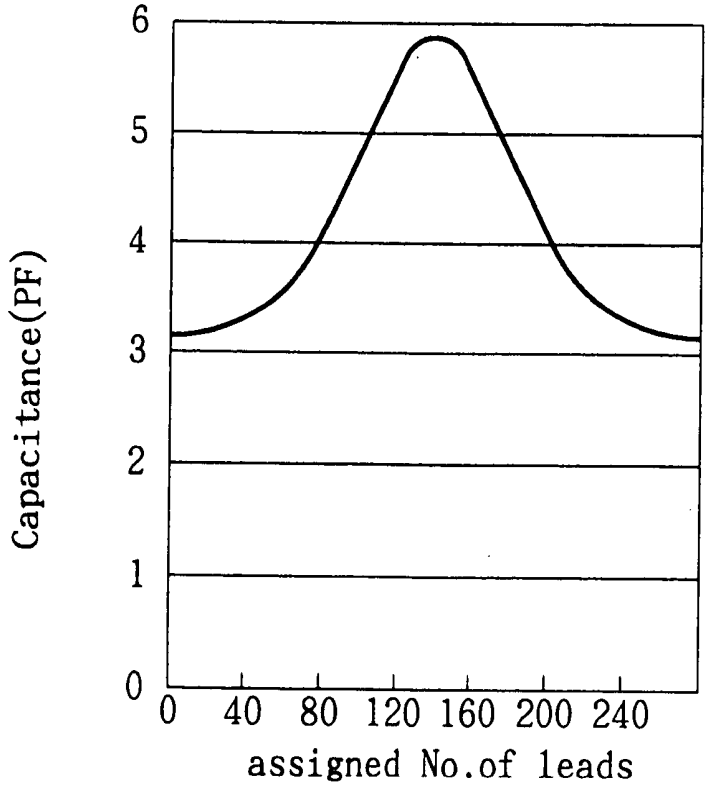

6
5
4
3
2
1
0
Capacitance(PF)
0 40 80 120 160 200 240
assigned No.of leads

FIG. 7(b)

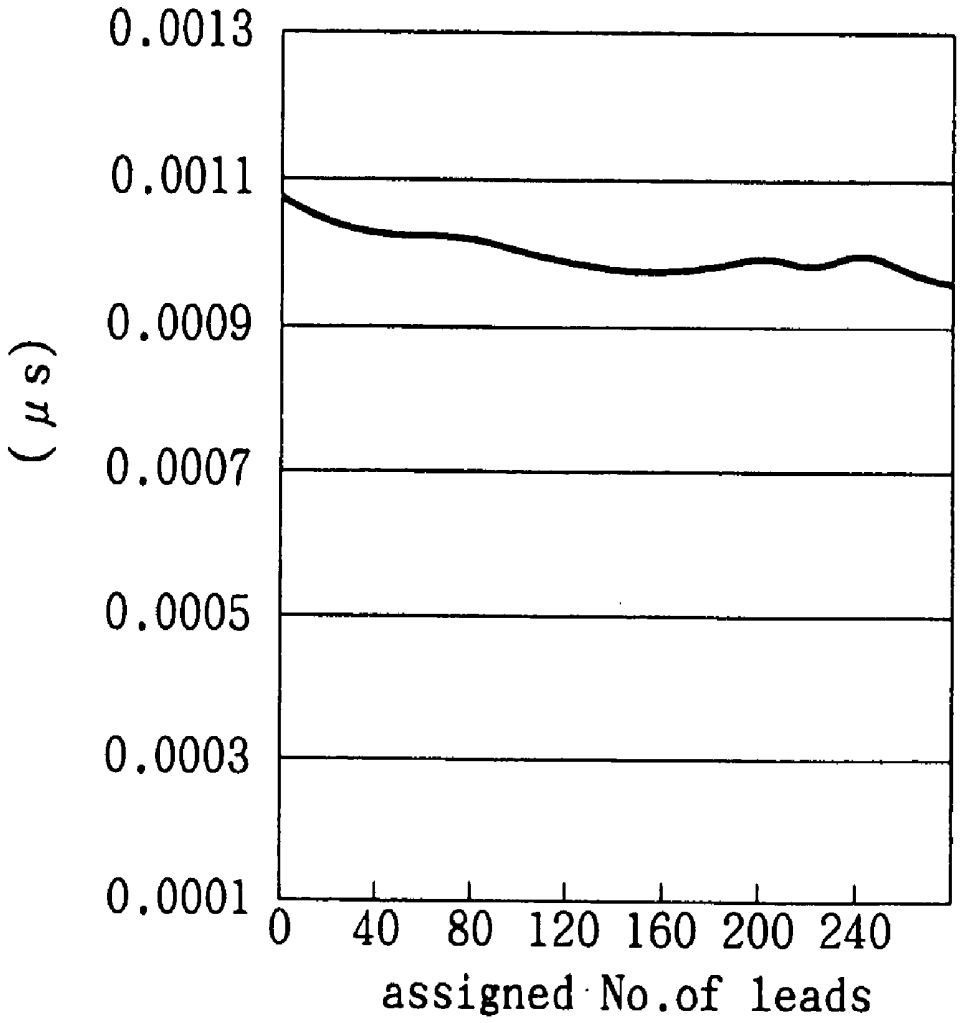

0.0013
0.0011
0.0009
0.0007
0.0005
0.0003
0.0001
(μs)
0
40
80
120
160
200
240
assigned No.of leads

FIG. 7(c)

LIQUID CRYSTAL PANEL HAVING COMPENSATION CAPACITORS FOR BALANCING RC DELAY EFFECT

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a liquid crystal panel having compensation capacitors for balancing RC delay effect, and more particularly to a liquid crystal panel with uniform delay times in all control lines.

[0003] 2. Description of the Related Art

[0004] Typically, a liquid crystal panel includes an active matrix substrate **10** having a plurality of data lines **13** and scanning lines **12**, and the data lines **13** are perpendicular to the scanning lines **12**, as shown in **FIG. 1**. A plurality of thin film transistors (TFTs) are formed in an active area B in which the data lines **13** and the scanning lines **12** cross each other at right angle.

[0005] The data lines **13** and the scanning lines **12** extend out of the active area B for transmitting signals from driving devices. A plurality of pads are formed in outer-lead bonding (OLB) areas **14** located on the periphery of the active area B, and are used for mounting the driving devices. Each of the OLB areas **14** is separately connected to one of fan-out areas **16** including a plurality of leads **15**.

[0006] **FIG. 2** shows an enlarged diagram of portion C in accordance with **FIG. 1**. The leads **15** run in straight lines and have equal thickness and width. The resistances of the leads **15** are different from each other because the lengths from the most outside lead **151** to middle lead **152** are apparently different, as shown in **FIG. 3**(*a*). The resistance of the lead **15** may be calculated as follows:

$$R = \rho \frac{L}{S},$$

[0007] where ρ, L and S respectively represent resistance, length, and cross sectional area of the lead **15**.

[0008] The transverse axle in **FIG. 3**(*a*) represents the assigned numbers of the leads **15** from the leftmost one to the rightmost one with regard to **FIG. 2**. Furthermore, **FIG. 3**(*b*) shows a graph of the variable capacitances of all the leads **15**. The product of resistance R and capacitance C is directly related to the delay time of a signal transmitted by either one of the data lines **13** or one of the scanning lines **12**. Therefore, the delay time caused by RC delay effect is variable from the most outside lead **151** to the middle lead **152**, as shown in **FIG. 3**(*c*).

[0009] Unfortunately, the variation of the delay time in the scanning lines **12** gives rise to a flicker phenomenon so as to deteriorate image quality. Therefore, the zigzag configuration of a fan-out area **16'** is provided for only reducing the variation of resistances, as shown in **FIG. 4**. Because all the leads is enclosed by the certain area of the fan-out area **16'**, the total length of a zigzag middle lead **152'** is still shorter than the length of a straight outside lead **151'**. In conclusion, the product R×C of the lead **151'** is different from that of the lead **152'**. That is, the flicker phenomenon also exists in the liquid crystal panel with zigzag leads.

SUMMARY OF THE INVENTION

[0010] An objective of the present invention is to provide a liquid crystal panel having compensation capacitors for balancing RC delay effect. Each compensation capacitor with a predetermined capacitance is connected to each lead so as to minimize the variation of RC delay effect between all leads.

[0011] In order to achieve the objective, the present invention discloses a liquid crystal panel having compensation capacitors for balancing RC delay effect, which comprises an active matrix substrate, an opposing substrate facing the active matrix substrate, and a liquid crystal layer disposed between the active matrix substrate and the opposing substrate. On the active matrix substrate, a plurality of parallel signal lines and a plurality of parallel scanning lines are arranged for forming a matrix of pixels called an active area.

[0012] A plurality of pads are formed in outer-lead bonding (OLB) areas located on the periphery of the active area, and are used for mounting driving devices. Each of the OLB areas is separately connected to one of fan-out areas including a plurality of leads. Each compensation capacitor with a predetermined capacitance is connected to each lead so as to minimize variation of RC delay effect between all leads.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] The invention will be described according to the appended drawings in which: **FIG. 1** is a planer view illustrating a configuration of an active matrix substrate in accordance with a prior art reference;

[0014] **FIG. 2** is an enlarged diagram illustrating portion C of the active matrix substrate in **FIG. 1**;

[0015] **FIG. 3**(*a*) is a graph illustrating variation of resistances of the leads of the fan-out area in **FIG. 2**;

[0016] **FIG. 3**(*b*) is a graph illustrating variation of capacitances of the leads of the fan-out area in **FIG. 2**;

[0017] **FIG. 3**(*c*) is a graph illustrating variation of the products of resistances and capacitances between all the leads in **FIG. 2**;

[0018] **FIG. 4** is a schematic diagram illustrating a fan-out area with a zigzag configuration in accordance with another prior art reference;

[0019] **FIG. 5** is a planer view illustrating a configuration of an active matrix substrate in accordance with the present invention;

[0020] **FIG. 6**(*a*) is an enlarged diagram of portion E in **FIG. 5**;

[0021] **FIG. 6**(*b*) is an equivalent circuit diagram of the lead L_1 and the capacitor C_1 in **FIG. 6**(*a*);

[0022] **FIG. 7**(*a*) is a graph illustrating variation of resistances of the leads in **FIG. 6**;

[0023] **FIG. 7**(*b*) is a graph illustrating variation of capacitances of the leads in **FIG. 6**; and

[0024] **FIG. 7**(*c*) is a graph illustrating variation of the products of resistances and capacitances between all the leads in **FIG. 6**.

PREFERRED EMBODIMENT OF THE PRESENT INVENTION

[0025] **FIG. 5** is a planer view illustrating a configuration of an active matrix substrate in accordance with the present invention. A liquid crystal panel includes an active matrix substrate **50** having a plurality of data lines **53** and scanning lines **52**, and the data lines **53** are perpendicular to the scanning lines **52**. A plurality of thin film transistors (TFTs) (not shown) are formed in an active area D in which the data lines **53** and the scanning lines **52** cross each other at right angles. The liquid crystal panel further includes an opposing substrate (not shown) facing the active matrix substrate **50**, and a liquid crystal layer (not shown) disposed between the active matrix substrate **50** and the opposing substrate.

[0026] The data lines **53** and the scanning lines **52** extend out of the active area D for transmitting signals from driving devices. A plurality of pads are formed in outer-lead bonding areas **54** near the periphery of the active area D, and are used for mounting the driving devices. Each of the OLB areas **54** is separately connected to one of fan-out areas **56**. A plurality of leads **55** are enclosed in each of the fan-out areas **56**.

[0027] In comparison with the active matrix substrate **10** in **FIG. 1**, the active matrix substrate **50** further comprises compensation circuit areas **51** between the OLB areas **54** and the active area D. As shown in **FIG. 6**, the enlarged diagram of portion E illustrates detailed circuits of the compensation circuit area **51**. Each of compensation capacitors C_1-C_{2n} is separately connected to each of leads L_1-L_{2n}, and has its corresponding capacitance predetermined by a circuit simulation. The capacitances of the compensation capacitors C_1-C_{2n} have to balance RC delay effect between all the leads L_1-L_{2n}. That is, variation of the products of resistances and capacitances between all leads is minimized when the adequate compensation capacitors C_1-C_{2n} is added to original circuits.

[0028] In this case, each of the compensation capacitors C_1-C_{2n} is separately connected to corresponding one of the leads L_1-L_{2n} in parallel (connection in series is another embodiment). **FIG. 6**(*b*) shows an equivalent circuit diagram of the lead L_1 and the capacitor C_1, wherein R_{L1} and C_{L1} separately represent an equivalent resistance and an equivalent capacitance of the lead L_1. The total capacitance C_T of these capacitors in parallel can be present as follows:

$$C_T=C_{L1}+C_1$$

[0029] **FIG. 7**(*a*) is a graph illustrating variation of the resistances of leads in **FIG. 6**. The transverse axle in **FIG. 7**(*a*) represents the assigned numbers of the leads **55** from the leftmost one L_1 to the rightmost one L_{2n} with regard to **FIG. 6**, wherein 2n, for example, is equal to two hundred and forty. A minimum resistance appears on a middle lead L_n because the middle lead L_n is shorter than the other leads even though it has a zigzag trace.

[0030] Apparently, we can determine that a compensation capacitor with a maximum capacitance is connected to the middle lead L_n, and one with a minimum capacitance is connected to the most outside lead L_1 or L_{2n}. FIG. **7**(*b*) is a graph illustrating variation of the predetermined capacitances. From the most outside lead L_1 to the middle lead L_n, the corresponding capacitances gradually increase in order to balance the RC delay effect of these leads.

[0031] The product of resistance and capacitance is directly related to the delay time of a signal transmitted by one of the data lines **53**. **FIG. 7**(*c*) is a graph illustrating variation of the products of resistances and capacitances between all leads in **FIG. 6**. From the leftmost lead L_1 to the rightmost lead L_{2n}, the products of resistances and capacitances regarding all these leads are uniform. Therefore, the RC delay effect of these leads are similar, and flicker phenomenon is reduced due to minimizing the difference of the delay times between each other.

[0032] The above-described embodiments of the present invention are intended to be illustrative only. Numerous alternative embodiments may be devised by persons skilled in the art without departing from the scope of the following claims.

1. A liquid crystal panel having compensation capacitors for balancing RC delay effect, comprising:

a substrate;

a plurality of data lines;

a plurality of signal lines crossing the plurality of data lines so as to form a plurality of pixels on the substrate;

at least one outer-lead bonding area formed on the substrate, the outer-lead bonding area including a plurality of bonding pads therein;

a plurality of leads each having a resistance for connecting the plurality of bonding pads to the plurality of signal lines or data lines; and

a plurality of compensation capacitors having electrodes, all of which electrodes are connected to the plurality of leads,

each capacitor having a capacitance and there being a product of resistance and capacitance for each lead,

the capacitances being such that differences among the products are minimized.

2. The liquid crystal panel having compensation capacitors for balancing RC delay effect of claim 1, wherein the plurality of leads are connected to the plurality of compensation capacitors in series.

3. The liquid crystal panel having compensation capacitors for balancing RC delay effect of claim 1, wherein the plurality of leads are connected to the plurality of compensation capacitors in parallel.

4. The liquid crystal panel having compensation capacitors for balancing RC delay effect of claim 1, wherein the plurality of leads have straight traces.

5. The liquid crystal panel having compensation capacitors for balancing RC delay effect of claim 1, wherein the plurality of leads have zigzag traces.

* * * * *

专利名称(译)	具有补偿电容器的液晶面板，用于平衡RC延迟效应		
公开(公告)号	US20040256966A1	公开(公告)日	2004-12-23
申请号	US10/464089	申请日	2003-06-18
[标]申请(专利权)人(译)	SU LEE DEUK TE CHENG CHUNG 林铭田 廖嘉TE		
申请(专利权)人(译)	SU LEE DEUK TE-CHUNG CHENG 林铭田 廖嘉TE		
当前申请(专利权)人(译)	SU LEE DEUK TE-CHUNG CHENG 林铭田 廖嘉TE		
[标]发明人	SU LEE DEUK TE CHENG CHUNG LIN MING TIEN LIAO CHIA TE		
发明人	SU, LEE DEUK TE-CHENG, CHUNG LIN, MING TIEN LIAO, CHIA TE		
IPC分类号	G02F1/1343 G02F1/1345		
CPC分类号	G02F1/1345 G02F1/13452		
其他公开文献	US6842200		
外部链接	Espacenet USPTO		

摘要(译)

液晶面板包括有源矩阵基板，与该有源矩阵基板相对的对置基板，以及配置在该有源矩阵基板和对置基板之间的液晶层。在有源矩阵基板上，排列多条平行信号线和多条平行扫描线，以形成称为有源区的像素矩阵。多个焊盘形成在位于有源区域的外围上的外部引线接合区域中，并且用于安装驱动器件。每个OLB区域分别连接到包括多个引线的扇出区域中的一个。具有预定电容的每个补偿电容器连接到每个引线，以便最小化所有引线之间的RC延迟效应的变化。