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(54) METHODS OF OPERATING SOURCE DRIVING CIRCUITS HAVING D/A CONVERTER TEST CAPABILITIES FOR LIQUID CRYSTAL DISPLAY DEVICES AND RELATED SOURCE DRIVING CIRCUITS

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(57) **ABSTRACT**

An LCD source driving circuit includes a gray voltage generator and a D/A converter. The gray voltage generator receives reference gray voltages to generate gray voltages having 2^n different voltage levels. The D/A converter has 2^n conversion paths and selects one gray voltage according to a received n-bit data among the 2^n gray voltages to output the selected gray voltage. The source driving circuit may adjust voltage differences between the neighboring conversion paths when testing the D/A converter.

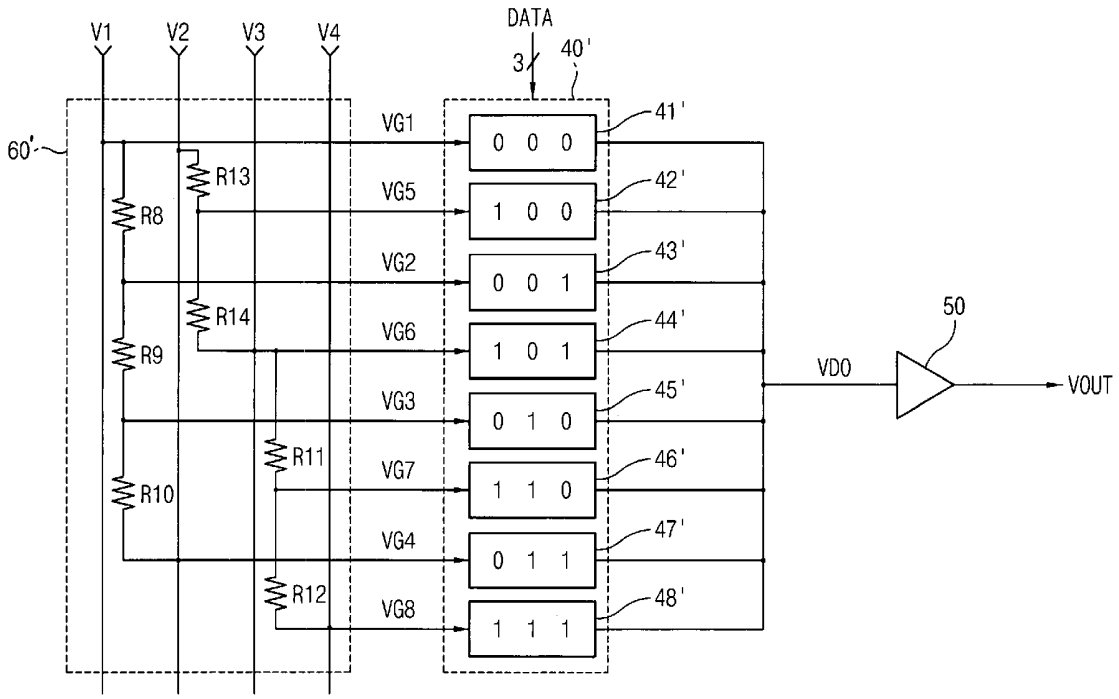


FIG. 1
(PRIOR ART)

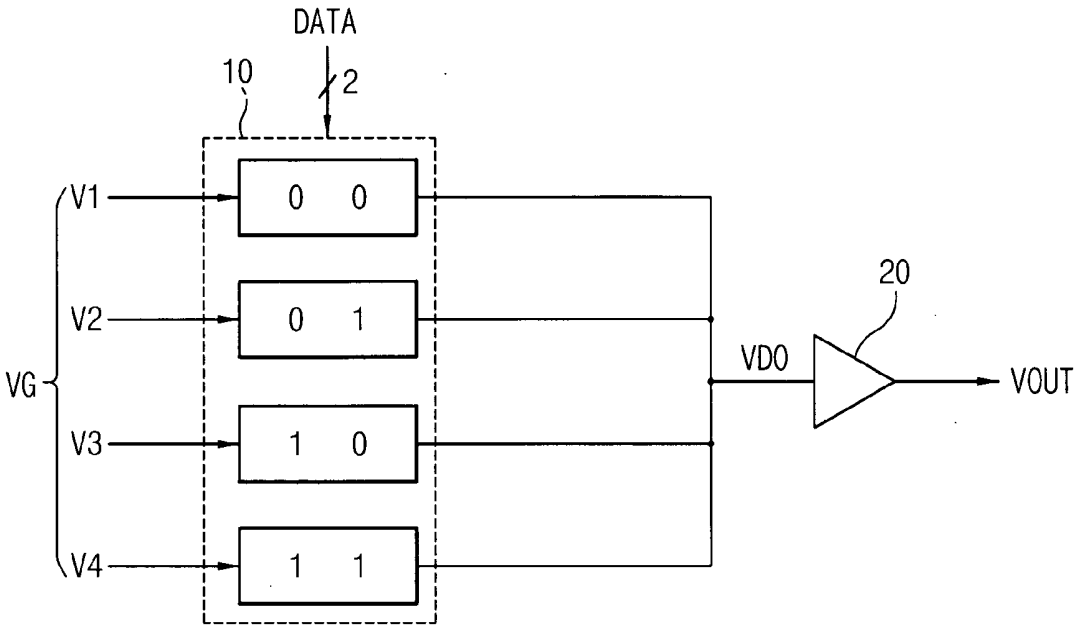


FIG. 2
(PRIOR ART)

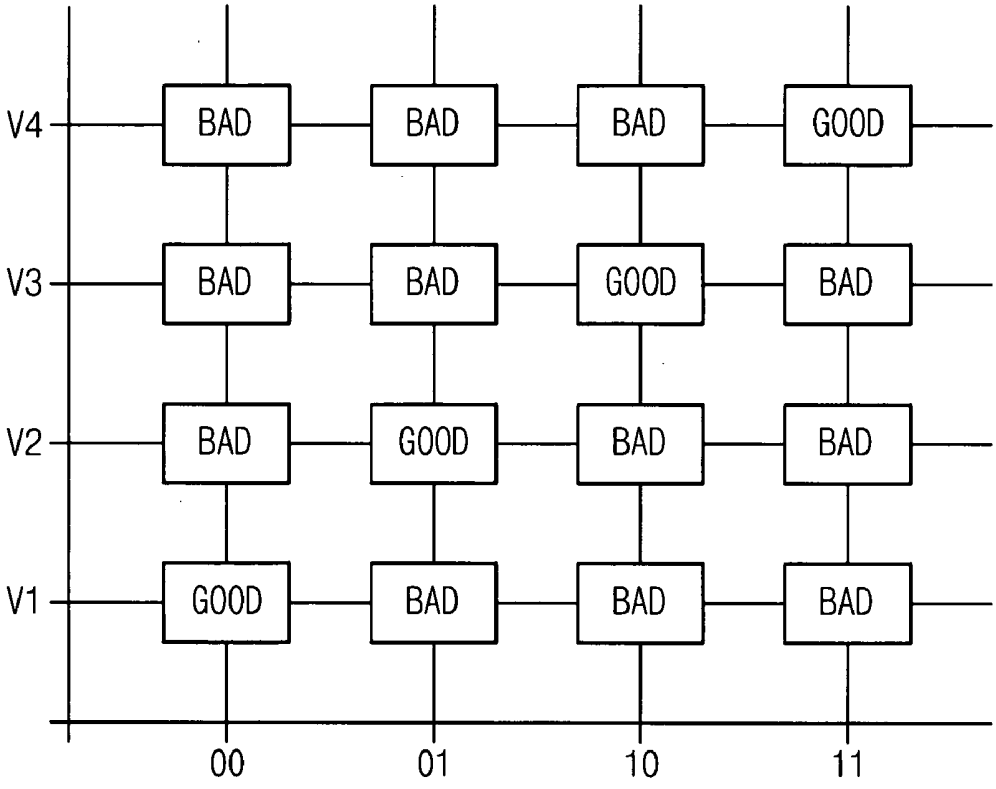


FIG. 3
(PRIOR ART)

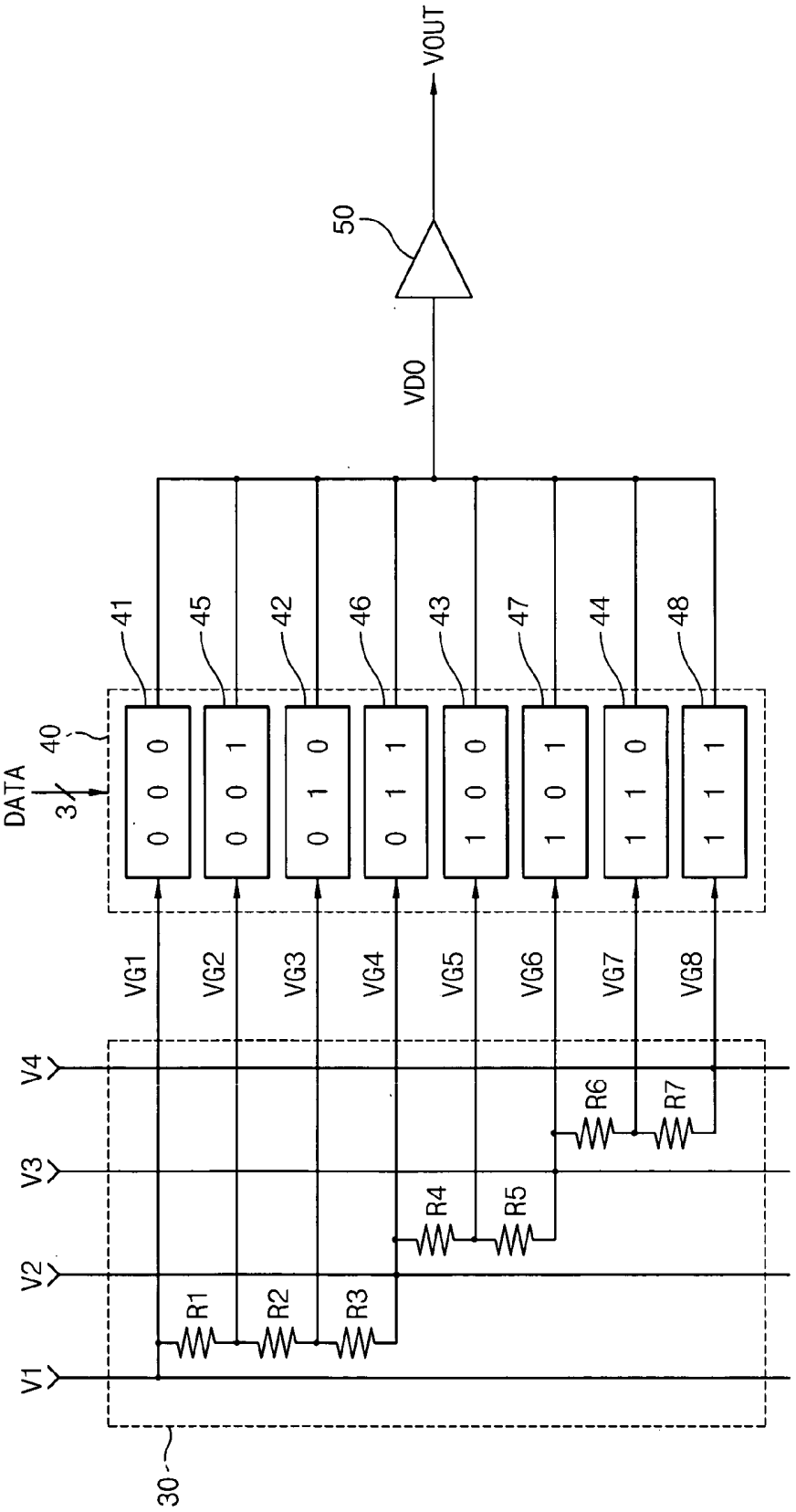


FIG. 4

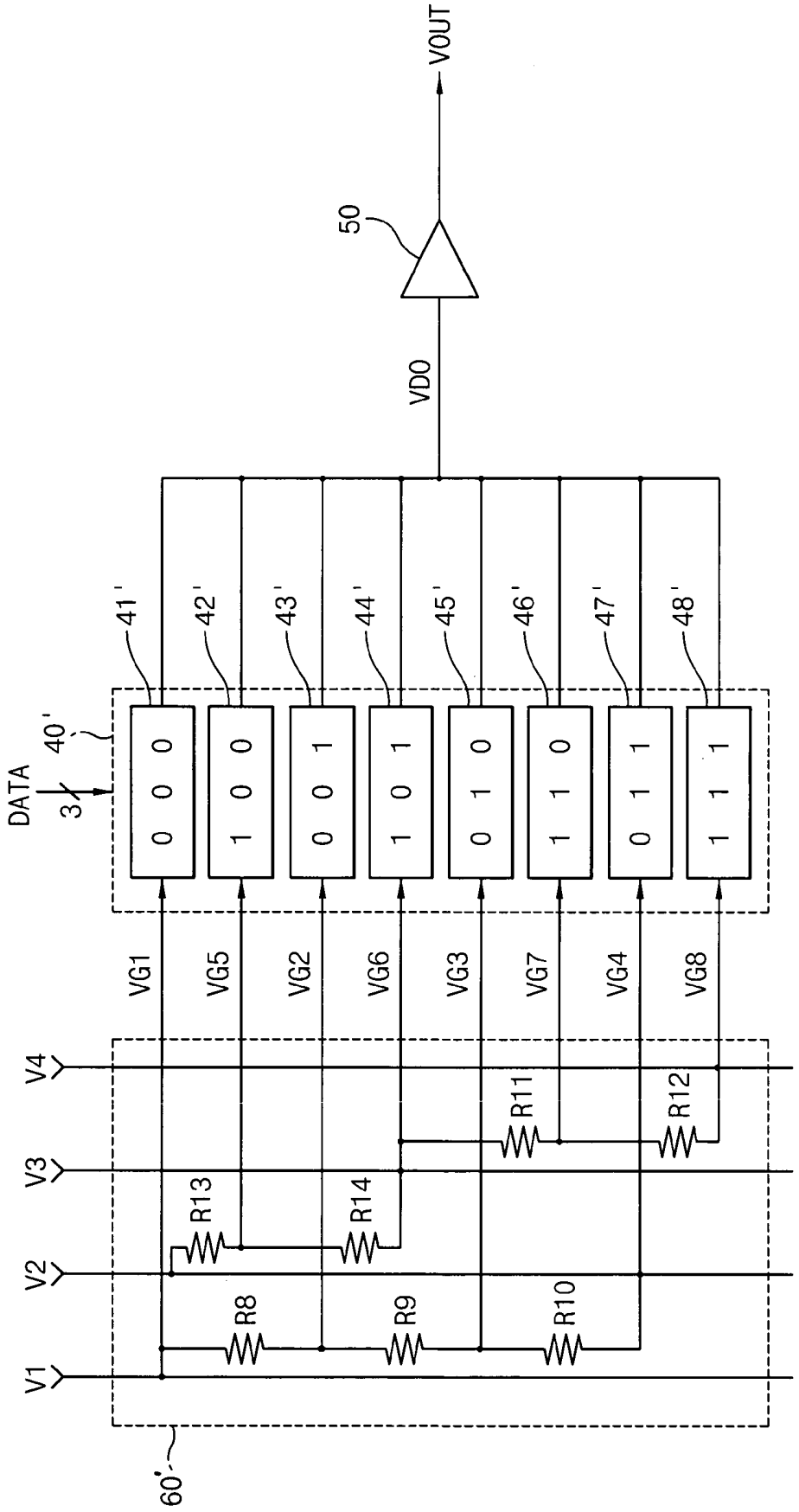

VOUT
50
VDO
41'
42'
43'
44'
45'
46'
47'
48'
40'
DATA
3
0 0 0
1 0 0
0 0 1
1 0 1
0 1 0
1 1 0
0 1 1
1 1 1
VG1
VG5
VG2
VG6
VG3
VG7
VG4
VG8
V4
V3
V2
V1
R11
R12
R13
R14
R8
R9
R10
60'

FIG. 5

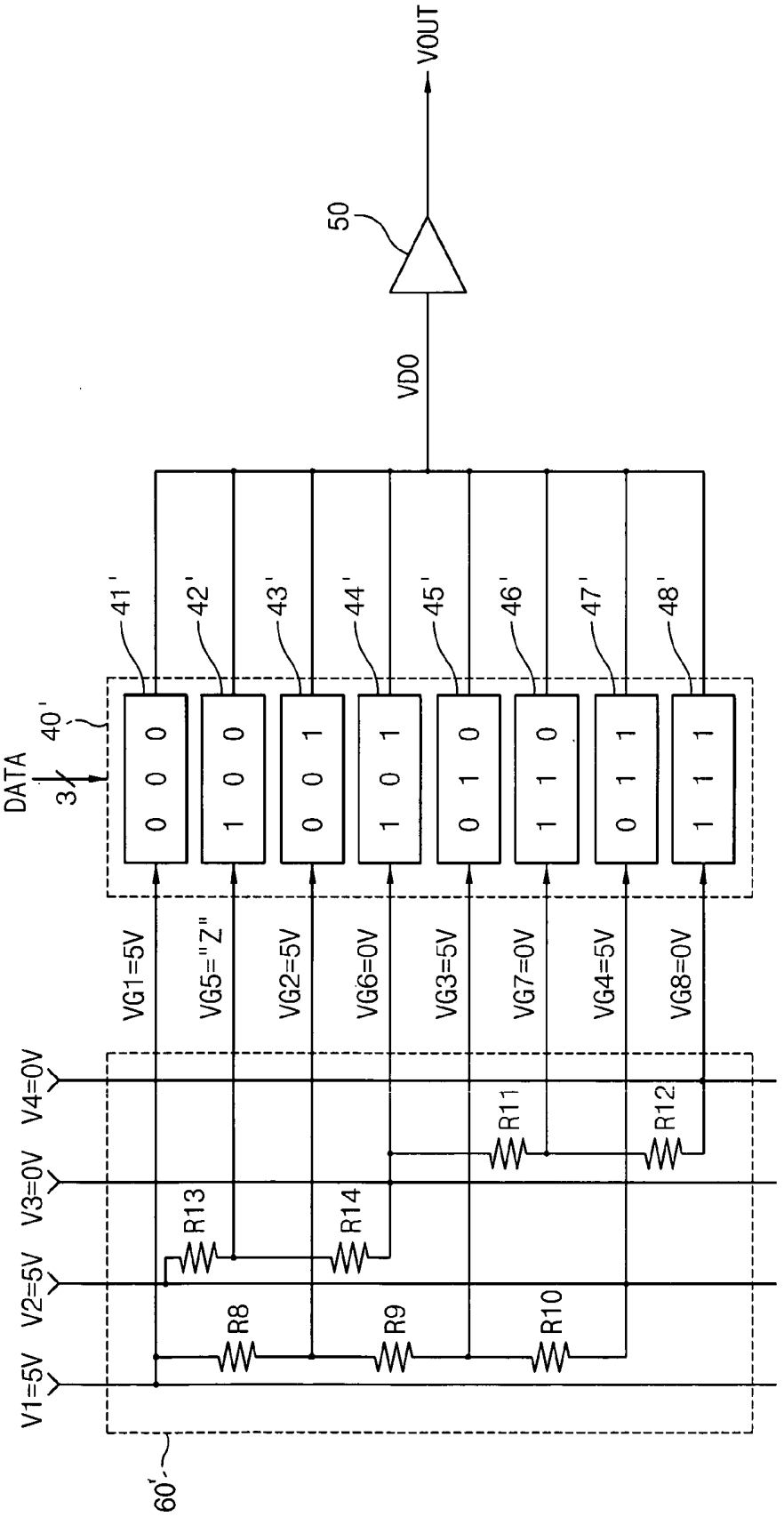
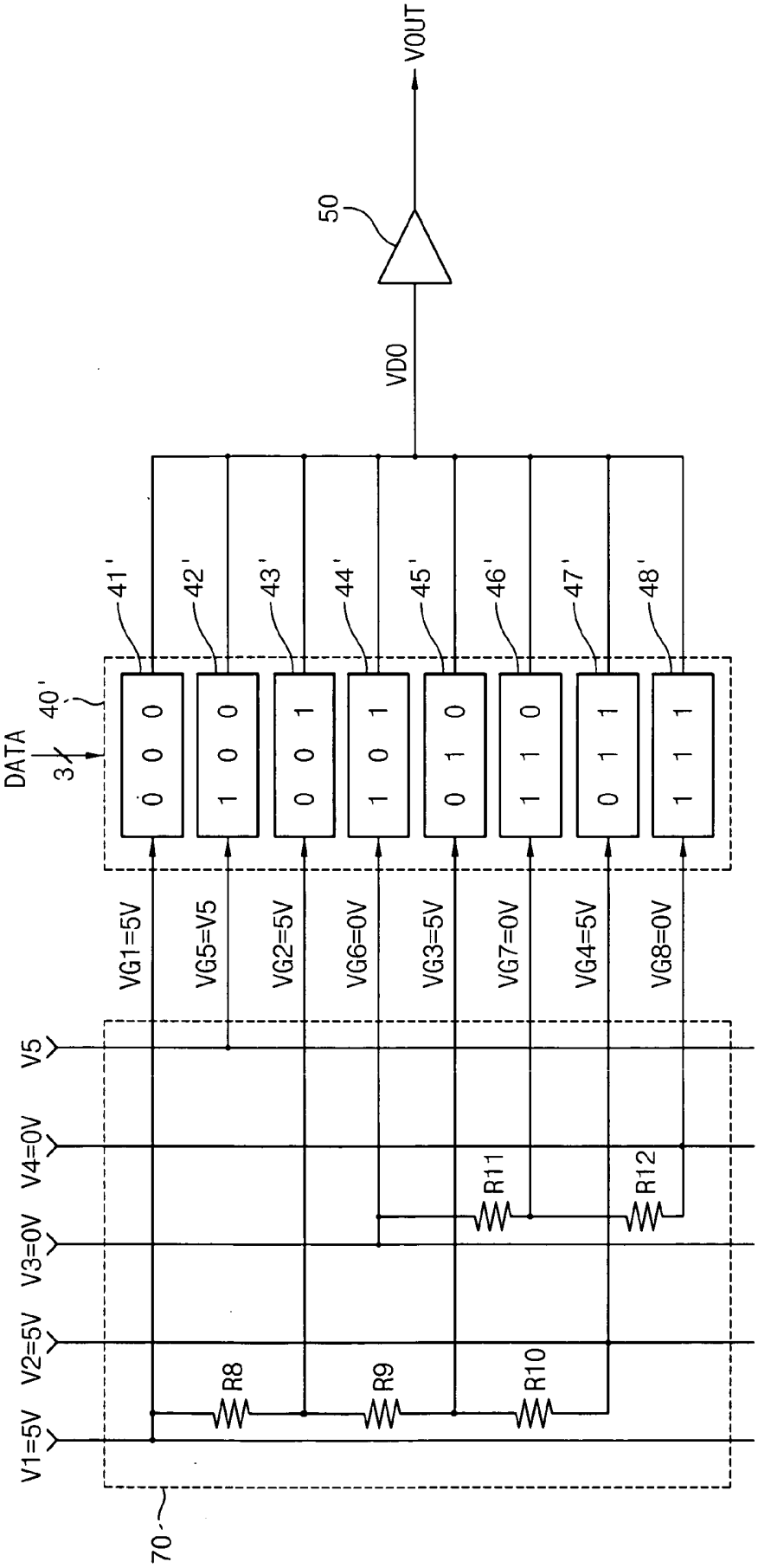

VOUT
50
VDO
41'
42'
43'
44'
45'
46'
47'
48'
40'
DATA
3
0 0 0
1 0 0
0 0 1
1 0 1
0 1 0
1 1 0
0 1 1
1 1 1
VG1=5V
VG5="Z"
VG2=5V
VG6=0V
VG3=5V
VG7=0V
VG4=5V
VG8=0V
V4=0V
V3=0V
V2=5V
V1=5V
R11
R12
R13
R14
R8
R9
R10
60'

FIG. 6


VOUT
50
VDO
41'
42'
43'
44'
45'
46'
47'
48'
40'
DATA
3
0 0 0
1 0 0
0 0 1
1 0 1
0 1 0
1 1 0
0 1 1
1 1 1
VG1=5V
VG5=V5
VG2=5V
VG6=0V
VG3=5V
VG7=0V
VG4=5V
VG8=0V
V5
V4=0V
V3=0V
V2=5V
V1=5V
R8
R9
R10
R11
R12
70

METHODS OF OPERATING SOURCE DRIVING CIRCUITS HAVING D/A CONVERTER TEST CAPABILITIES FOR LIQUID CRYSTAL DISPLAY DEVICES AND RELATED SOURCE DRIVING CIRCUITS

FIELD OF THE INVENTION

[0001] The present invention relates to liquid crystal displays (LCD) and, more particularly, to methods of operating source driving circuits for LCDs and related source driving circuits.

BACKGROUND OF THE INVENTION

[0002] In recent years, liquid crystal displays (LCD) have started to replace cathode ray tube devices in many applications. By way of example, many television screens and computer monitors are now implemented using LCD devices, which are typically thinner and lighter than cathode ray tube screens.

[0003] Both passive and active matrix LCD devices are known in the art. Active matrix LCD devices have multiple active elements that are coupled, respectively, to multiple pixel electrodes that are aligned within a matrix of the LCD device. Active matrix LCD devices typically have higher contrast ratios than passive matrix LCD devices. Thin film transistors (TFT) are widely used as the active element that connects to the pixel electrodes of the active matrix LCD device.

[0004] FIG. **1** is a schematic diagram illustrating a conventional source driving circuit for an LCD device that includes a 2-bit digital-to-analog (D/A) converter **10**. As shown in FIG. **1**, the D/A converter **10** has four conversion paths. The D/A converter **10** has four gray voltage inputs, V**1** through V**4**. The D/A converter **10** selects and outputs one of these gray voltages V**1** through V**4** based on a received data code DATA. The output signal VDO of the D/A converter **10** is buffered by a buffer **20** before it is output. The output signal VOUT is coupled to one of source lines (not shown) in an LCD panel.

[0005] FIG. **2** is a diagram illustrating how the D/A converter of FIG. **1** should operate. As indicated in FIG. **2**, when a data code **00** is input to the D/A converter **10**, the D/A converter **10** will output voltage V**1**, so long as it is working properly. Likewise, when that data codes **01**, **10** and **11** are input, the D/A converter will output voltages V**2**, V**3** and V**4**, respectively, when operating properly, as reflected by the boxes labeled "GOOD" in FIG. **2**. In FIG. **2**, the boxes labeled "BAD" indicate instances where the D/A converter does not operate properly.

[0006] An error in the signal VOUT may occur because of (1) a malfunction with respect to the D/A converter **10** or (2) a malfunction in the buffer **20**. If the buffer **20** fails, the output of the D/A converter will typically fail for each of the conversion paths. Accordingly, the D/A converter may be tested to determine if it is operating properly by confirming that each of the conversion paths output the correct signal. The conventional method for testing the D/A converter **10** and the buffer **20** is to serially input the data code DATA that selects each conversion path of the D/A converter **10** and then measure the DC voltage levels of the output signal VOUT to determine if the proper voltage was output. This testing may be done, for example, as part of a chip-based test of a source driving circuit of an LCD device.

SUMMARY OF THE INVENTION

[0007] Pursuant to embodiments of the present invention, methods of operating a source driving circuit of an LCD device are provided. Pursuant to these methods, a first set of gray voltage levels is provided to respective ones of a plurality of conversion paths of a D/A converter of the source driving circuit when the circuit is used to drive the LCD device. In contrast, a second set of gray voltage levels, that is different from the first set of gray voltage levels, is provided to respective of the plurality of conversion paths of the D/A converter when the D/A converter is tested.

[0008] In certain embodiments, at least eight conversion paths are provided, and the second set of gray voltage levels may have at most three different gray voltage levels that are provided to the at least eight conversion paths. In other embodiments, the differences between the gray voltage levels provided to at least some pairs of neighboring conversion paths during testing of the D/A converter may be greater than the differences between the gray voltage levels provided to the same pairs of neighboring conversion paths when the source driving circuit is used to drive the LCD device. In some embodiments, at least two of the gray voltages in the second set of gray voltage levels may have the same value. In certain specific embodiments, at least two of the gray voltages in the second set of gray voltage levels may be equal to the voltage level of a first reference voltage that is provided to the source driving circuit. In some embodiments, the gray voltage level provided to all or all but one of the conversion paths during testing of the D/A converter may be either the voltage level of the first reference voltage or the voltage level of a second reference voltage provided to the source driving circuit.

[0009] Pursuant to further embodiments of the present invention, methods of operating a source driving circuit of an LCD device are provided in which a different gray voltage level is provided to each of the 2^n conversion paths of a D/A converter of the source driving circuit when the source driving circuit is used to drive the LCD device. In contrast, the same gray voltage level is provided to at least two of the 2^n conversion paths during testing of the D/A converter. In these methods, the difference between the gray voltage level provided to a first of the conversion paths and the gray voltage level provided to a second of the conversion paths that is adjacent the first conversion path during testing of the D/A converter may be approximately equal to a difference between a highest reference voltage applied to a gray voltage generator circuit of the source driving circuit and a lowest reference voltage applied to the gray voltage generator circuit. In certain specific embodiments, the gray voltage level provided to at least 2^n-1 of the conversion paths during testing of the D/A converter is either the highest reference voltage or the lowest reference voltage.

[0010] Pursuant to further embodiments of the present invention, source driving circuits for an LCD device are provided that include a gray voltage generator that is configured to output at least eight distinct gray voltage levels on respective ones of at least eight output lines when the source driving circuit is used to drive the LCD device. These source driving circuits further include a D/A converter that has at

least eight conversion paths that are coupled to respective ones of the at least eight output lines. The output lines are matched to the conversion paths so that the difference between the gray voltage levels provided to any two adjacent conversion paths exceeds the smallest difference between any two of the eight gray voltage levels.

[0011] Pursuant to still further embodiments of the present invention, source driving circuits for an LCD device are provided that include a gray voltage generator that is responsive to a plurality of reference gray voltages. The gray voltage generator may be configured to generate gray voltages having 2^n different voltage levels. A D/A converter having 2^n conversion paths is also provided, the D/A converter configured to select and output one of the 2^n gray voltages based on a received n-bit data. In these embodiments, n is an integer number, a respective one of the 2^n gray voltages corresponds to each of the 2^n conversion paths, and the voltage differences between the gray voltages corresponding to neighboring conversion paths may be adjustable for testing the D/A converter.

[0012] The D/A converter may be functionally tested by using the voltage differences between the neighboring conversion paths. The gray voltage generator may include first to fourth lines respectively provided with the first to the fourth reference gray voltages. A first resistor may be connected between the first line and a first node, a second resistor may be connected between the first node and a second node, a third resistor may be connected between the second node and the second line, a fourth resistor may be connected between the third line and a third node, a fifth resistor may be connected between the third node and the fourth line, a sixth resistor may be connected between the second line and a fourth node, and a seventh resistor may be connected between the fourth node and the third line. The gray voltage generator also may generate first to eighth gray voltages, the first gray voltage indicating a voltage level of the first line, the second gray voltage indicating a voltage level of the first node, the third gray voltage indicating a voltage level of the second node, the fourth gray voltage indicating a voltage level of the second line, the fifth gray voltage indicating a voltage level of the fourth node, the sixth gray voltage indicating a voltage level of the third line, the seventh gray voltage indicating a voltage level of the third node, and the eighth gray voltage indicating a voltage level of the fourth line.

[0013] The D/A converter may include first to eighth conversion paths configured to respectively output the first to the eighth gray voltages corresponding to a 3-bit data. The first and the second reference gray voltages may be about 5V, and the third and the fourth reference gray voltages may be about 0V.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. **1** is a schematic diagram illustrating a conventional source driving circuit for an LCD device that includes a 2-bit digital-to-analog (D/A) converter.

[0015] FIG. **2** is a diagram illustrating the proper outputs of the D/A converter of FIG. **1**.

[0016] FIG. **3** is a schematic diagram illustrating a conventional source driving circuit of an LCD device that includes a 3-bit D/A converter.

[0017] FIG. **4** is a schematic diagram illustrating a source driving circuit of an LCD device with a 3-bit D/A converter according to embodiments of the present invention.

[0018] FIG. **5** is a schematic diagram illustrating the source driving circuit in FIG. **4** with reference gray voltages for testing the D/A converter.

[0019] FIG. **6** is a schematic diagram illustrating a source driving circuit of an LCD device with a 3-bit D/A converter according to further embodiments of the present invention.

DETAILED DESCRIPTION

[0020] The invention is described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art.

[0021] It will be understood that when an element or layer is referred to as being "connected to" or "coupled to" another element or layer, it can be directly connected or coupled to the other element or layer or intervening elements or layers may be present. In contrast, when an element is referred to as being "directly connected to" or "directly coupled to" another element or layer, there are no intervening elements or layers present. Like numbers refer to like elements throughout. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0022] It will be understood that, although the terms first, second, etc. may be used herein to describe various elements and/or components, these elements and/or components should not be limited by these terms. These terms are only used to distinguish one element or component from another element or component. Thus, a first element or component discussed below could be termed a second element or component without departing from the teachings of the present invention.

[0023] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0024] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0025] FIG. **3** is a schematic diagram illustrating a conventional source driving circuit of an LCD device that includes a 3-bit D/A converter. As shown in FIG. **3**, the source driving circuit includes a gray voltage generator **30**, a D/A converter **40** and a buffer **50**. The gray voltage generator **30** receives reference gray voltages V**1** to V**4**, and generates 8 different gray voltage levels VG**1** to VG**8**. The D/A converter **40** has 8 conversion paths **41** to **48**, each of which selects the one of the gray voltage levels VG**1** to VG**8** that corresponds to the input data code DATA, and outputs the selected gray voltage as the output signal VDO. The output signal VDO is buffered in the buffer **50**, and then output as output signal VOUT.

[0026] The gray voltage generator **30** includes resistors R**1**, R**2** and R**3**, which are connected in series between the reference gray voltages V**1** and V**2**, resistors R**4** and R**5**, which are connected in series between the reference gray voltages V**2** and V**3**, and resistors R**6** and R**7**, which are connected in series between the reference gray voltages V**3** and V**4**.

[0027] At a normal operation, the reference gray voltages V**1** to V**4** may have sequentially decreasing values, for example, 5V, 2.8V, 1.4V, and 0V respectively, so that the gray voltage generator **30** generates the eight distinct gray voltage levels, by way of example, substantially uniformly distributed from 5V to 0V.

[0028] The source driving circuit shown in FIG. **3** operates as follows. The input data DATA comprises 3 bits of data, and the number of the conversion paths of the D/A converter is 8, that is, 2^3. The reference gray voltages V**1** to V**4** are converted by one or more of the resistors R**1** to R**7** into the gray voltages VG**1** to VG**8**. When one conversion path among the 8 conversion paths is selected according to the input data DATA, the gray voltage that corresponds to the selected conversion path is output as the output voltage VDO of the D/A converter **40**. The output voltage VDO is buffered by the buffer **50**, and then output as the output voltage VOUT to one of source lines of the LCD panel (not shown).

[0029] As shown in FIG. **3**, the first conversion path **41** of the D/A converter **40** is selected by the input data **000**. The second conversion path **42** of the D/A converter **40** is selected by the input data **001**. The third conversion path **43** of the D/A converter **40** is selected by the input data **010**. The fourth conversion path **44** of the D/A converter **40** is selected by the input data **011**. The fifth conversion path **45** of the D/A converter **40** is selected by the input data **100**. The sixth conversion path **46** of the D/A converter **40** is selected by the input data **101**. The seventh conversion path **47** of the D/A converter **40** is selected by the input data **110**. The eighth conversion path **48** of the D/A converter **40** is selected by the input data **111**.

[0030] The data **000** selects the first conversion path **41** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**1** as the output voltage VDO. The data **001** selects the second conversion path **42** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**2** as the output voltage VDO. The data **010** selects the third conversion path **43** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**3** as the output voltage VDO. The data **011** selects the fourth conversion path **44** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**4** as the output voltage VDO. The data **100** selects the fifth conversion path **45** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**5** as the output voltage VDO. The data **101** selects the sixth conversion path **46** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**6** as the output voltage VDO. The data **110** selects the seventh conversion path **47** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**7** as the output voltage VDO. The data **111** selects the eighth conversion path **48** of the D/A converter **40**, and the D/A converter outputs the gray voltage VG**8** as the output voltage VDO.

[0031] At a test operation, the reference gray voltages V**1** to V**4** have the same value. For example, all of the reference gray voltages V**1** to V**4** are 3.3V, then all of the gray voltages are also 3.3V.

[0032] In order to determine if the conversion paths **41** to **48** of the D/A converter **40** in the source driving circuit in FIG. **3** are operating properly, the reference gray voltages V**1** to V**4** with the same DC voltage levels are provided to the D/A converter **40**, and the eight possible data codes DATA are then serially input. For each of these eight tests, the output VOUT is checked to confirm that the expected output signal is received.

[0033] The D/A converter according to FIG. **3**, however, is not easily verified for interferences between the conversion paths because all of the conversion paths are provided with the reference gray voltages having the same DC voltage level.

[0034] FIG. **4** is a schematic diagram illustrating a source driving circuit of an LCD device with a 3-bit D/A converter according to embodiments of the present invention. As shown in FIG. **4**, the source driving circuit includes a gray voltage generator **60'**, a D/A converter **40'** and a buffer **50** that receives 3-bit input data DATA. The gray voltage generator **60'** receives reference gray voltages V**1** to V**4** and generates 8 different gray voltage levels VG**1** to VG**8**. The D/A converter **40'** has 8 conversion paths **41'** to **48'**, each of which selects the one of the gray voltage levels VG**1** to VG**8** that corresponds to the input data code of the conversion path. An output signal VDO that has the gray voltage level corresponding to the input data DATA is buffered by the buffer **50**, and then output as signal VOUT.

[0035] The gray voltage generator **60'** includes resistors R**8**, R**9** and R**10**, which are connected in series between the reference gray voltages V**1** and V**2**, resistors R**13** and R**14**, which are connected in series between the reference gray voltages V**2** and V**3**, and resistors R**11** and R**12**, which are connected in series between the reference gray voltages V**3** and V**4**.

[0036] At a normal operation, the reference gray voltages V**1** to V**4** may have sequentially decreasing values, for example, 5V, 2.8V, 1.4V, and 0V respectively, so that the gray voltage generator **30** generates the eight distinct gray voltage levels, by way of example, substantially uniformly distributed from 5V to 0V.

[0037] The LCD device source driving circuit shown in FIG. **4** operates as follows. The input data DATA is 3-bit data. The resistors R**8** to R**14** are used to generate the gray voltages VG**1** to VG**8** from the reference gray voltages V**1** to V**4**. One of the 8 conversion paths is selected based on the

input data DATA, and the gray voltage corresponding to the selected conversion path is output from the D/A converter **40'** as the output voltage VDO. The output voltage VDO is buffered by the buffer **50**, and then provided as output voltage VOUT to one of source lines of the LCD panel (not shown).

[**0038**] As shown in FIG. **4**, the first conversion path **41'** of the D/A converter **40'** is selected by the input data **000**. The second conversion path **42'** of the D/A converter **40'** is selected by the input data **001**. The third conversion path **43'** of the D/A converter **40'** is selected by the input data **010**. The fourth conversion path **44'** of the D/A converter **40'** is selected by the input data **011**. The fifth conversion path **45'** of the D/A converter **40'** is selected by the input data **100**. The sixth conversion path **46'** of the D/A converter **40'** is selected by the input data **101**. The seventh conversion path **47'** of the D/A converter **40'** is selected by the input data **110**. The eighth conversion path **48'** of the D/A converter **40'** is selected by the input data **111**.

[**0039**] The data **000** selects the first conversion path **41'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**1** as the output voltage VDO. The data **001** selects the second conversion path **42'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**2** as the output voltage VDO. The data **010** selects the third conversion path **43'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**3** as the output voltage VDO. The data **011** selects the fourth conversion path **44'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**4** as the output voltage VDO. The data **100** selects the fifth conversion path **45'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**5** as the output voltage VDO. The data **101** selects the sixth conversion path **46'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**6** as the output voltage VDO. The data **110** selects the seventh conversion path **47'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**7** as the output voltage VDO. The data **111** selects the eighth conversion path **48'** of the D/A converter **40'**, and the D/A converter outputs the gray voltage VG**8** as the output voltage VDO.

[**0040**] As shown in FIG. **4**, the conversion paths of the D/A converter **40'** are configured in a different order as compared to the conversion paths of the conventional D/A converter **40** of FIG. **3**. In particular, while the conversion paths of the D/A converter **40** of the conventional source driving circuit of FIG. **3** are arranged in a consecutive order increasing from **000** to **111**, the conversion paths of the D/A converter **40'** of FIG. **4** are arranged in a mixed order of the first conversion path **41'**, the fifth conversion path **45'**, the second conversion path **42'**, the sixth conversion path **46'**, the third conversion path **43'**, the seventh conversion path **47'**, the fourth conversion path **44'** and the eighth conversion path **48'**. The gray voltages associated with each of the respective conversion paths **41'** to **48'** of the D/A converter **40'** in FIG. **4** are substantially the same as the corresponding gray voltages in FIG. **3**. Thus, in the D/A converter **40'** of FIG. **4**, the gray voltage VG**1** corresponds to the input data **000**, the gray voltage VG**2** corresponds to the input data **001**, the gray voltage VG**3** corresponds to the input data **010**, the gray voltage VG**4** corresponds to the input data **011**, the gray voltage VG**5** corresponds to the input data **100**, the gray voltage VG**6** corresponds to the input data **101**, the gray voltage VG**7** corresponds to the input data **110** and the gray voltage VG**8** corresponds to the input data **111**. The D/A conversion result of the source driving circuit in FIG. **4** is substantially equal to the D/A conversion result from FIG. **3**.

[**0041**] The arrangement of the conversion paths of the D/A converter **40'** of the source driving circuit in FIG. **4** may allow for easier testing of the D/A converter **40'** than the consecutive arrangement of the conversion paths in the D/A converter **40** of FIG. **3**.

[**0042**] FIG. **5** is a schematic diagram illustrating the source driving circuit in FIG. **4** provided with reference gray voltages for testing the D/A converter. As shown in FIG. **5**, a 5V voltage is applied to the reference gray voltages V**1** and V**2**, respectively and a 0V voltage is applied to the reference gray voltages V**3** and V**4**, respectively. Because the reference gray voltages V**1** and V**2** are 5V, there is no voltage drop across the resistors R**8**, R**9** and R**10**, and the gray voltages VG**1**, VG**2**, VG**3** and VG**4** are each 5V. Similarly, because the reference gray voltages V**3** and V**4** are 0V, there are no voltage drops across the resistors R**11** and R**12**, and the gray voltages VG**6**, VG**7** and VG**8** are each 0V. The gray voltage VG**5** has a voltage level Z in a range from 0V to 5V, where the value of Z depends on the values of the resistors R**13** and R**14**.

[**0043**] Voltage differences between adjacent conversion paths of the D/A converter **40'** with the configuration of FIG. **5**, except for voltage differences with respect to the fifth conversion path **45'**, are 5V. The fifth conversion path **45'** has a voltage level Z. Z is greater than 0V but less than 5V, as determined by the values of the resistors R**13** and R**14**. The voltage level Z is sufficiently distinguishable. In this way, the fifth conversion path **45'** may be tested. The other conversion paths may be tested in a similar way. For another example, if the gray voltages V**1**, V**2** and V**3** are 5V, and the gray voltage V**4** is 0V, then the gray voltages VG**1** to VG**6** are 5V and the gray voltage V**8** is 0V, but the gray voltage VG**7** is a value between 5V and 0V which is apparently distinguishable. The seventh conversion path **47'** may be tested in such a configuration.

[**0044**] The source driving circuit in FIG. **5** can detect defects where the source driving circuit is short-circuited or open-circuited, by such a function test. The configuration in FIG. **5** may have larger voltage differences among adjacent conversion paths than the configuration in FIG. **3**, which may reduce the time necessary to perform the tests and/or increase the accuracy of the tests.

[**0045**] FIG. **6** is a schematic diagram illustrating a source driving circuit of an LCD device with a 3-bit D/A converter according to further embodiments of the present invention. In the embodiment of FIG. **6**, the D/A converter **40'** receives 5 different reference gray voltages having voltage levels V**1** to V**5**, as compared to the 4 different gray voltage levels provided in the embodiment of FIG. **5**. The reference gray voltage V**5** may be used to supply the gray voltage VG**5**. The gray voltage VG**5** in FIG. **6** has a voltage level of the reference gray voltage V**5**, while the gray voltage VG**5** in FIG. **5** has a voltage level in a range between the reference gray voltages V**1**, which is 5V, and V**3**, which is 0V, depending on the resistors R**13** and R**14**.

[**0046**] The operation of the source driving circuit illustrated in FIG. **6** is substantially identical to the operation of

the source driving circuit illustrated in FIG. **5**, and thus, a detailed description need not be repeated here.

[**0047**] A source driving circuit for an LCD device according to embodiments of the present invention may easily detect defects of the D/A conversion paths of the D/A converter by testing the conversion paths functionally. A source driving circuit for an LCD device according to the embodiments of the invention may also reduce time for testing and/or improve the accuracy of the tests.

[**0048**] The foregoing is illustrative of the present invention and is not to be construed as limiting thereof. Although a few example embodiments of this invention have been described, those skilled in the art will readily appreciate that many modifications are possible in the example embodiments without materially departing from the novel teachings and advantages of this invention. Accordingly, all such modifications are intended to be included within the scope of this invention as defined in the claims. Therefore, it is to be understood that the foregoing is illustrative of the present invention and is not to be construed as limited to the specific embodiments disclosed, and that modifications to the disclosed embodiments, as well as other embodiments, are intended to be included within the scope of the appended claims. The invention is defined by the following claims, with equivalents of the claims to be included therein.

What is claimed is:

1. A method of operating a source driving circuit of an LCD device, the source driving circuit including a D/A converter, the method comprising:

providing a first set of gray voltage levels to respective ones of a plurality of conversion paths of the D/A converter when the source driving circuit is used to drive the LCD device; and

providing a second set of gray voltage levels, that is different from the first set of gray voltage levels, to respective ones of the plurality of conversion paths of the D/A converter when testing the D/A converter,

wherein the differences between the gray voltage levels provided to at least some pairs of neighboring conversion paths, which include at least one conversion path under test during testing of the D/A converter, is greater than the differences between the gray voltage levels provided to the at least some pairs of neighboring conversion paths when the source driving circuit is used to drive the LCD device.

2. The method of claim 1, wherein the plurality of conversion paths comprises at least eight conversion paths, and wherein the second set of gray voltage levels comprises at least three different gray voltage levels that are provided to the at least eight conversion paths.

3. The method of claim 1, wherein at least two of the gray voltages in the second set of gray voltage levels have the same value.

4. The method of claim 1, wherein at least two of the gray voltages in the second set of gray voltage levels comprise the voltage level of a first reference voltage provided to the source driving circuit.

5. The method of claim 4, wherein the gray voltage level provided to all but at least one of the conversion paths under test during testing of the D/A converter are either the voltage level of the first reference voltage or the voltage level of a second reference voltage provided to the source driving circuit, and a gray voltage level provided to the at least one of the conversion paths under test during testing of the D/A converter is a voltage level between the first reference voltage and the second reference voltage.

6. A method of operating a source driving circuit of an LCD device, the source driving circuit including a D/A converter having 2^n conversion paths, the method comprising:

providing a different gray voltage level to each of the 2^n conversion paths of the D/A converter when the source driving circuit is used to drive the LCD device; and

providing a same gray voltage level to at least two of the 2^n conversion paths, wherein the at least two of the 2^n conversion paths are not under test, during testing of the D/A converter,

wherein the differences between the gray voltage levels provided to at least some pairs of neighboring conversion paths, which include at least one conversion path under test during testing of the D/A converter, is greater than the differences between the gray voltage levels provided to the at least some pairs of neighboring conversion paths when the source driving circuit is used to drive the LCD device.

7. The method of claim 6, wherein the gray voltage level provided to all but at least one of the conversion paths under test during testing of the D/A converter are approximately equal either to a highest reference voltage applied to a gray voltage generator circuit of the source driving circuit, or to a lowest reference voltage applied to the gray voltage generator circuit of the source driving circuit, and a gray voltage level provided to the at least one of the conversion paths under test during testing of the D/A converter is a voltage level between the highest reference voltage and the lowest reference voltage.

8. A source driving circuit for an LCD device, comprising:

a gray voltage generator that is configured to output at least eight distinct gray voltage levels on respective of at least eight output lines, based on at least four reference voltages when the source driving circuit is used to drive the LCD device, and configured to output at least three distinct gray voltage levels for the at least eight output lines during testing; and

a D/A converter having at least eight conversion paths that are coupled to respective of the at least eight output lines, wherein the output lines are matched to the conversion paths so that the difference between the gray voltage levels provided to any two adjacent conversion paths exceeds the smallest difference between any two of the eight gray voltage levels when the source driving circuit is used to drive the LCD device.

9. The circuit of claim 8, wherein the gray voltage level provided to all but at least one of the conversion paths under test during testing of the D/A converter are approximately equal either to a highest one of the reference voltage applied to the gray voltage generator circuit, or to a lowest reference voltage applied to the gray voltage generator circuit, and a gray voltage level provided to the at least one of the conversion paths under test during testing of the D/A converter is a voltage level between the highest reference voltage and the lowest reference voltage.

10. A source driving circuit for an LCD device comprising:

a gray voltage generator that is responsive to a plurality of reference gray voltages, the gray voltage generator configured to generate gray voltages having 2^n different voltage levels; and

a D/A converter having 2^n conversion paths, the D/A converter configured to select and output one of the 2^n gray voltages based on a received n-bit data,

wherein n is an integer, wherein a respective one of the 2^n gray voltages corresponds to each of the 2^n conversion paths, and wherein voltage differences between the gray voltages corresponding to neighboring conversion paths are adjustable for testing the D/A converter.

11. The source driving circuit of claim 10, wherein the D/A converter is functionally tested by using the voltage differences between the neighboring conversion paths.

12. The source driving circuit of claim 11, wherein the number n is 3, and wherein the gray voltage generator comprises:

a first line provided with a first of the reference gray voltages;

a second line provided with a second of the reference gray voltages;

a third line provided with a third of the reference gray voltages;

a fourth line provided with a fourth of the reference gray voltages;

a first resistor connected between the first line and a first node;

a second resistor connected between the first node and a second node;

a third resistor connected between the second node and the second line;

a fourth resistor connected between the third line and a third node;

a fifth resistor connected between the third node and the fourth line;

a sixth resistor connected between the second line and a fourth node; and

a seventh resistor connected between the fourth node and the third line, and

wherein the gray voltage generator generates first to eighth gray voltages, the first gray voltage indicating a voltage level of the first line, the second gray voltage indicating a voltage level of the first node, the third gray voltage indicating a voltage level of the second node, the fourth gray voltage indicating a voltage level of the second line, the fifth gray voltage indicating a voltage level of the fourth node, the sixth gray voltage indicating a voltage level of the third line, the seventh gray voltage indicating a voltage level of the third node, and the eighth gray voltage indicating a voltage level of the fourth line.

13. The source driving circuit of claim 12, wherein the D/A converter comprises first to eighth conversion paths configured to respectively output the first to the eighth gray voltages.

14. The source driving circuit of claim 13, wherein the first and the second reference gray voltages are about 5V, and the third and the fourth reference gray voltages are about 0V.

15. The source driving circuit of claim 11, wherein the number n is 3, and wherein the gray voltage generator comprises:

a first line provided with a first of the reference gray voltages;

a second line provided with a second of the reference gray voltages;

a third line provided with a third of the reference gray voltages;

a fourth line provided with a fourth of the reference gray voltages;

a first resistor connected between the first line and a first node;

a second resistor connected between the first node and a second node;

a third resistor connected between the second node and the second line;

a fourth resistor connected between the third line and a third node; and

a fifth resistor connected between the third node and the fourth line, and

wherein the gray voltage generator generates first to eighth gray voltages, the first gray voltage indicating a voltage level of the first line, the second gray voltage indicating a voltage level of the first node, the third gray voltage indicating a voltage level of the second node, the fourth gray voltage indicating a voltage level of the second line, the fifth gray voltage indicating a voltage level of the fifth node, the sixth gray voltage indicating a voltage level of the third line, the seventh gray voltage indicating a voltage level of the third node, and the eighth gray voltage indicating a voltage level of the fourth line.

16. The source driving circuit of claim 15, wherein the D/A converter comprises first to eighth conversion paths configured to respectively output the first to the eighth gray voltages.

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专利名称(译)	操作具有用于液晶显示器件和相关源极驱动电路的D / A转换器测试能力的源驱动电路的方法		
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[标]申请(专利权)人(译)	HER NAM JUNG		
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摘要(译)

LCD源驱动电路包括灰度电压发生器和D / A转换器。灰度电压发生器接收参考灰度电压以产生具有2n个不同电压电平的灰度电压。 D / A转换器具有2n个转换路径，并根据2n个灰度电压中接收的n位数据选择一个灰度电压，以输出所选择的灰度电压。当测试D / A转换器时，源极驱动电路可以调整相邻转换路径之间的电压差。